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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a “DS” number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is “DSXXXXXA”, where “XXXXX” is the document number and “A” is the revision level of the document.

INTRODUCTION

This chapter contains general information that will be useful to know before using the Physical+ Interface Board OS81110 / 2+0 (in the following abbreviated as Phy+ Interface Board). Topics discussed in this chapter include:

- Intended Use
- Scope of Delivery
- Document Layout
- Term Definitions
- Recommended Reading
- Customer Support
- Document Revision History

INTENDED USE

This Microchip product is intended to be used for developing, testing, or analyzing MOST® based multimedia products and systems by persons with experience in developing multimedia devices.

Note: The operation of this Microchip product is only admitted with original Microchip devices.
Do not interfere with the product's original state. Otherwise user safety, faultless operation and electromagnetic compatibility are not guaranteed.
To avoid electric shocks and short circuits use this device only in an appropriate environment.
This open device may exceed the limits of electromagnetic interference. Electromagnetic compatibility can be only achieved if the equipment is built into an appropriate housing.
SCOPE OF DELIVERY

This product is delivered with the Physical+ Interface Board OS81110 / 2+0.
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listed on the last page of this document. Providing the delivery note number eases the
handling.

DOCUMENT LAYOUT

This user’s guide describes how to use the Phy+ Interface Board. The document is
organized as follows:
• Chapter 1, Introduction – This chapter introduces the Phy+ Interface Board. It pro-
vides an overview about the product features, shows the main parts of the board
and a hardware structure example.
• Chapter 2, Board Options and Pin Configurations – The Phy+ Interface Board is
available in three different board options. Each board option provides a set of differ-
ent Pin Configurations. This chapter gives an overview of the board options and
explains how to change a Pin Configuration.
• Chapter 3, Board Details – This chapter describes the pin-outs of the board connec-
tors. In addition it explains jumper settings and LED states.
• Chapter 4, Assembly Plan – This chapter shows the top and bottom view of the
assembly plan.
• Chapter 5, Mechanical Drawing – This chapter shows the mechanical dimensions of
the board (top and bottom view), including connectors and further peripherals.
• Chapter 6, Schematics – This chapter shows the schematics for all available board
options.

TERM DEFINITIONS

This user’s guide uses the following term definitions:

<table>
<thead>
<tr>
<th>Terms</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNx</td>
<td>Connector x</td>
</tr>
<tr>
<td>FOT</td>
<td>Fiber Optic Transceiver</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>I²C™</td>
<td>Inter-Integrated Circuit</td>
</tr>
<tr>
<td>I²S™</td>
<td>Inter-IC Sound</td>
</tr>
<tr>
<td>INIC</td>
<td>Intelligent Network Interface Controller</td>
</tr>
<tr>
<td>LED</td>
<td>Light Emitting Diode</td>
</tr>
</tbody>
</table>
| MediaLB® | Media Local Bus, an open standard from Microchip for inter-chip multime-
           | dia communication |
| MOST  | Media Oriented System Transport |
| NC    | Not Connected |
| oPHY  | Optical physical layer |
RECOMMENDED READING

This user's guide describes how to use the Phy+ Interface Board. Other useful documents are listed below.

[1] OS81110 Hardware Data Sheet
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    Contact: support-ais-de@microchip.com.

    Go to: www.microchip.com.

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• Technical Support

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Technical support is available through the web site at: http://support.microchip.com

DOCUMENT REVISION HISTORY

Revision A (December 2013)

• Initial release of this document.
Chapter 1. Introduction

1.1 PRODUCT FEATURES

The product features of the Phy+ Interface Board are as follows:

• Detached interface between application hardware and MOST network
• Supports a MOST network speed grade of 150 Mbits/s
• Available for optical physical layer (oPHY) applications
• Fully encapsulated kernel hardware
• Common and standard inter-board connector
  - Connects to application hardware
  - Serves as measurement connector
• Configuration/Debug Header Connector
• Lock detection
• Offers connection capabilities to the following ports and interfaces:
  - Control port (I2C)
  - Two streaming ports (I2S): I2S A and I2S B
  - MediaLB 3-Pin port
  - MediaLB 6-Pin port
  - Two Transport Stream Interfaces (TSI): TSI 0 and TSI 1
  - Two Serial Peripheral Interfaces (SPI): SPI 0 and SPI 1

1.2 BLOCK DIAGRAM

Figure 1-1 gives an overview of the Phy+ Interface Board’s main components.

FIGURE 1-1: BLOCK DIAGRAM
As depicted in the figure below, the Phy+ Interface Board serves as an interface between the INIC Evaluation Platform OS81xxx or customer application hardware (specified as ‘Application’ in Figure 1-2) and the MOST150 network. The Phy+ Interface Board can be simply plugged on the application hardware via the inter-board connector CN7, see Section 3.1.

**FIGURE 1-2: HARDWARE STRUCTURE EXAMPLE**

![Diagram of Hardware Structure Example](image)

**Note:** Schematics and layouts are provided "as is" without any warranty as an example application, and are not guaranteed to be suitable for any particular application. Any design using this information should be tested over the full environmental stress conditions of the intended application. For application information, schematic and layout issues refer to the OS81110 hardware data sheet [1].
Chapter 2. Board Options and Pin Configurations

There are three different board options available which support a specific combination of hardware ports. Depending upon the ports required for the application and the data type(s) to be streamed, either board option 1, 2 or 3 can be chosen. Board options 1-3 provide pre-defined Pin Configurations (1-8), see Table 2-1, which can be easily accessed by using either the default Pin Configuration or selecting a Pin Configuration different to the default, see Section 2.1 “Changing the Pin Configuration”. For further reading on Pin Configurations refer to the OS81110 hardware data sheet [1] and OS81110 INIC API User’s Manual [3].

TABLE 2-1: PHY INTERFACE CONFIGURATION MODES

<table>
<thead>
<tr>
<th>OS81110 PIN</th>
<th>BOARD OPTION 1</th>
<th>PIN CONFIG. 1 (Note 1)</th>
<th>BOARD OPTION 2</th>
<th>PIN CONFIG. 3</th>
<th>BOARD OPTION 3</th>
<th>PIN CONFIG. 5 (Note 1)</th>
<th>PIN CONFIG. 6</th>
<th>PIN CONFIG. 7 (Note 1)</th>
<th>PIN CONFIG. 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>27</td>
<td>MLBSN</td>
<td>MLBSN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>MLBSP</td>
<td>MLBSP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>MLBDN</td>
<td>MLBDN</td>
<td>NC</td>
<td></td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>MLBDP</td>
<td>MLBDP</td>
<td>NC</td>
<td>SCKB</td>
<td>SCKB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>MLBCN</td>
<td>MLBCN</td>
<td>TCLK1</td>
<td>SCKLB</td>
<td>SCKLB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>MLBCP</td>
<td>MLBCP</td>
<td>TSYN1</td>
<td>TSYN1</td>
<td>TSYN1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>FSYA</td>
<td>TSYN0</td>
<td>FSYA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>SCKA</td>
<td>TCLK0</td>
<td>SCKA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>SRX0</td>
<td>TDA0</td>
<td>SRX0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>47</td>
<td>SRX1</td>
<td>TVAL0</td>
<td>SRX1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48</td>
<td>SRX2</td>
<td>NC</td>
<td>SRX2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>SRX3</td>
<td>NC</td>
<td>SRX3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>RMCK0</td>
<td>RMCK0</td>
<td>RMCK0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MEMLDAT</td>
</tr>
</tbody>
</table>

Note 1: Default Pin Configuration of board option
Note: All board options provide an I²C interface to configure and control the INIC.
Note: The default interface (MediaLB or I²C) is configurable via CN5, see Section 3.3 “Default Interface Jumper”.

Legend:
- MediaLB 3-Pin
- MediaLB 6-Pin
- TSI Port 0
- TSI Port 1
- SPI A
- SPI B
- Streaming Port A
-Streaming Port B
2.1 CHANGING THE PIN CONFIGURATION

To change the Pin Configuration of the Phy+ Interface Board, the INIC Explorer [2] is required, with its software component installed on PC and its hardware connected to both the PC (for connection information refer to the INIC Explorer Startup Guide [4]) and the Configuration/Debug Header connector [1] of the Phy+ Interface Board, see Figure 4-1. Assuming that the application setup is powered and working properly, the Pin Configuration can be changed by performing the following steps:

• Start INIC Explorer software.
• Go to the Configuration String Editor.
  (You can access the Configuration String Editor either by clicking on its entry in the context area or by opening the navigation tree.)
• Select INIC.PortConfiguration.PortVariantCfg.
• Double click on the value.
  >> A dialogue window opens.
• Open the drop down list.
• Select one of the Pin Configuration(s) valid for your board option, see Table 2-1.

| Note: | If you choose a Pin Configuration different to those supported by the board option you use, proper functionality of the Phy+ Interface Board cannot be ensured. |

• Click ‘OK’.
• Click the ‘Write’ button, which is located in the toolbar.
  >> The changes are written into the INIC’s Configuration String and a reset will be applied to the INIC in order to adapt the new setting.
Chapter 3. Board Details

3.1 MEASUREMENT CONNECTOR AND INTERFACE TO MAIN BOARD CONNECTOR

Measurement Connector CN2 (see Figure 4-1): Samtec QSH-020-01-L-D-DP-A
Interface to Main Board Connector CN7 (see Figure 4-2): Samtec QTH-020-01-L-D-DP-A

Connector CN2 is placed on the top side of the Phy+ Interface Board and can be used for measurement purposes. Connector CN7, placed on the bottom side of the Phy+ Interface Board, is used as interface to connector CN2, mounted on the customer application hardware.

CN2 and CN7 have the same pin assignment.

3.1.1 Identification Signals

Pins 4, 5, 7, 8 and 12 serve as Phy+ Interface Board identifiers in respect to the signals active on the pins. ‘GND’ means that the respective pin is tied to ground, ‘Open’ indicates the pin is not connected (NC). In the latter case, the pin needs a pull-up resistor mounted on the application board.

TABLE 3-1: IDENTIFICATION SIGNALS

<table>
<thead>
<tr>
<th>ID0</th>
<th>ID1</th>
<th>ID2</th>
<th>ID3</th>
<th>ID4</th>
<th>Phy+ Interface Board</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>GND</td>
<td>Open</td>
<td>Open</td>
<td>Open</td>
<td>Physical+ Interface Board OS81110 / 2+0 Board Option 1</td>
</tr>
<tr>
<td>GND</td>
<td>Open</td>
<td>GND</td>
<td>Open</td>
<td>Open</td>
<td>Physical+ Interface Board OS81110 / 2+0 Board Option 2</td>
</tr>
<tr>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>Open</td>
<td>Open</td>
<td>Physical+ Interface Board OS81110 / 2+0 Board Option 3</td>
</tr>
</tbody>
</table>
3.1.2 Electrical Characteristics

TABLE 3-2: ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3 V continuous</td>
<td>30</td>
<td>50</td>
<td>3.465 V</td>
<td></td>
</tr>
<tr>
<td>3.3 V</td>
<td>3.135</td>
<td>370</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

3.2 CONFIGURATION/DEBUG HEADER CONNECTOR

Configuration/Debug Header Connector CN10 (see Figure 4-1): Molex 87832-1420

TABLE 3-3: CONFIGURATION/DEBUG HEADER CONNECTOR

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 3, 13</td>
<td>NC</td>
</tr>
<tr>
<td>2, 5, 10</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>Error/Boot</td>
</tr>
<tr>
<td>6, 9</td>
<td>3.3 V</td>
</tr>
<tr>
<td>7</td>
<td>TDI/DSDA</td>
</tr>
<tr>
<td>8</td>
<td>TCK/DSCL</td>
</tr>
<tr>
<td>11</td>
<td>TDO/DINT</td>
</tr>
<tr>
<td>12</td>
<td>Reset</td>
</tr>
<tr>
<td>14</td>
<td>TMS</td>
</tr>
</tbody>
</table>

3.3 DEFAULT INTERFACE JUMPER

If the jumper CN5 (see Figure 4-1) is closed during start-up, MediaLB is set as default data interface. If the jumper is opened during start-up, I²C is set as default data interface.

3.4 ACTIVITY LED

The activity LED (see Figure 4-1) indicates different activity states.

TABLE 3-4: ACTIVITY LED

<table>
<thead>
<tr>
<th>Color</th>
<th>Activity State</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>No activity</td>
</tr>
<tr>
<td>Red</td>
<td>Activity, but no lock</td>
</tr>
<tr>
<td>Green</td>
<td>Lock</td>
</tr>
</tbody>
</table>

3.5 FOT 2+0 (oPHY)

The Phy+ Interface Board can be connected to the MOST network via a FOT unit MOST150 2+0 from Tyco (see Figure 4-1), which is a fiber optic transceiver module for the MOST connector.
Chapter 4. Assembly Plan

4.1 TOP VIEW

FIGURE 4-1: ASSEMBLY PLAN—TOP VIEW
4.2 BOTTOM VIEW

FIGURE 4-2: ASSEMBLY PLAN—BOTTOM VIEW

Interface to Main Board Connector
Chapter 5. Mechanical Drawing

5.1 TOP VIEW

FIGURE 5-1: MECHANICAL DRAWING—TOP VIEW
5.2 BOTTOM VIEW

FIGURE 5-2: MECHANICAL DRAWING—BOTTOM VIEW
Chapter 6. Schematics

The following pages show the schematics available for the different Board Options. For available Board Options and their supported Pin Configurations refer to Chapter 2.
6.1 BOARD OPTION 1

FIGURE 6-1: BOARD OPTION 1—TOP BLOCK
FIGURE 6-4: BOARD OPTION 1—OS81110
6.2 BOARD OPTION 2

FIGURE 6-5: BOARD OPTION 2—TOP BLOCK
FIGURE 6-7: BOARD OPTION 2—CONNECTORS
FIGURE 6-8: BOARD OPTION 2—OS81110
6.3 BOARD OPTION 3

FIGURE 6-9: BOARD OPTION 3—TOP BLOCK
FIGURE 6-11: BOARD OPTION 3—CONNECTORS

Application Interface

Box for Comments:

Physical Interface Board OS81110 / 2+0 User's Guide

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## Asia/Pacific

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**India - Pune**
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Fax: 81-6-6152-9310

**Japan - Tokyo**
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Fax: 81-3-6880-3771

**Korea - Daegu**
Tel: 82-53-744-4301
Fax: 82-53-744-4302

**Korea - Seoul**
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Fax: 82-2-558-5932 or 82-2-558-5934

**Malaysia - Kuala Lumpur**
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Fax: 60-3-6201-9859

**Malaysia - Penang**
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**Philippines - Manila**
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**Singapore**
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**Taiwan - Hsin Chu**
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**Taiwan - Kaohsiung**
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## Europe

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**UK - Wokingham**
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