This document includes the programming specifications for the following devices:

- PIC12F1501
- PIC12LF1501
- PIC16F1503
- PIC16LF1503
- PIC16F1507
- PIC16LF1507
- PIC16F1508
- PIC16LF1508
- PIC16F1509
- PIC16LF1509

1.0 OVERVIEW

The devices can be programmed using either the high-voltage In-Circuit Serial Programming™ (ICSP™) method or the low-voltage ICSP™ method.

1.1 Hardware Requirements

1.1.1 HIGH-VOLTAGE ICSP PROGRAMMING

In High-Voltage ICSP™ mode, these devices require two programmable power supplies: one for VDD and one for the MCLR/VPP pin.

1.1.2 LOW-VOLTAGE ICSP PROGRAMMING

In Low-Voltage ICSP™ mode, these devices can be programmed using a single VDD source in the operating range. The MCLR/VPP pin does not have to be brought to a different voltage, but can instead be left at the normal operating voltage.

1.1.2.1 Single-Supply ICSP Programming

The LVP bit in Configuration Word 2 enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a ‘1’ (enabled) from the factory. The LVP bit may only be programmed to a ‘0’ by entering the High-Voltage ICSP mode, where the MCLR/VPP pin is raised to VIHH. Once the LVP bit is programmed to a ‘0’, only the High-Voltage ICSP mode is available and only the High-Voltage ICSP mode can be used to program the device.

Note 1: The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying VIHH to the MCLR/VPP pin.

2: While in Low-Voltage ICSP mode, MCLR is always enabled, regardless of the MCLRE bit, and the port pin can no longer be used as a general purpose input.

1.2 Pin Utilization

Five pins are needed for ICSP™ programming. The pins are listed in Table 1-1.

### TABLE 1-1: PIN DESCRIPTIONS DURING PROGRAMMING

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>During Programming</th>
<th>Pin Type</th>
<th>Pin Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RA1</td>
<td>ICSPCLK</td>
<td>I</td>
<td>Clock Input – Schmitt Trigger Input</td>
</tr>
<tr>
<td>RA0</td>
<td>ICSPDAT</td>
<td>I/O</td>
<td>Data Input/Output – Schmitt Trigger Input</td>
</tr>
<tr>
<td>MCLR/VPP/RA3</td>
<td>Program/Verify mode</td>
<td>P(1)</td>
<td>Program Mode Select/Programming Power Supply</td>
</tr>
<tr>
<td>VDD</td>
<td>VDD</td>
<td>P</td>
<td>Power Supply</td>
</tr>
<tr>
<td>VSS</td>
<td>VSS</td>
<td>P</td>
<td>Ground</td>
</tr>
</tbody>
</table>

Legend:  I = Input, O = Output, P = Power

Note 1: The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to MCLR input. Since the MCLR is used for a level source, MCLR does not draw any significant current.
2.0 DEVICE PINOUTS

The pin diagrams are shown in Figure 2-1 through Figure 2-5. The pins that are required for programming are listed in Table 1-1 and shown in bold lettering in the pin diagrams.

FIGURE 2-1: 8-PIN PDIP, SOIC, MSOP, DFN DIAGRAM FOR PIC12(L)F1501

PDIP, SOIC, MSOP, DFN (2X3)

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>RA5</td>
<td>RA4</td>
<td>MCLR/Vpp/RA3</td>
<td>PIC12(L)F1501</td>
<td>RA0/ICSPDAT</td>
<td>RA1/ICSPCLK</td>
<td>Vss</td>
</tr>
</tbody>
</table>

FIGURE 2-2: 14-PIN PDIP, SOIC, TSSOP DIAGRAM FOR PIC16(L)F1503

PDIP, SOIC, TSSOP

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
<th>13</th>
<th>14</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>RA5</td>
<td>RA4</td>
<td>MCLR/Vpp/RA3</td>
<td>PIC16(L)F1503</td>
<td>RA0/ICSPDAT</td>
<td>RA1/ICSPCLK</td>
<td>RC0</td>
<td>RC1</td>
<td>RC2</td>
<td>RC3</td>
<td>RC4</td>
<td>RC5</td>
<td>VSS</td>
</tr>
</tbody>
</table>

FIGURE 2-3: 16-PIN QFN DIAGRAM FOR PIC16(L)F1503

QFN (3x3)

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
<th>13</th>
<th>14</th>
<th>15</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>NC</td>
<td>NC</td>
<td>Vss</td>
<td>RA5</td>
<td>RA4</td>
<td>MCLR/Vpp/RA3</td>
<td>RC5</td>
<td>RC4</td>
<td>RC3</td>
<td>RC2</td>
<td>RC1</td>
<td>RA0/ICSPDAT</td>
<td>RA1/ICSPCLK</td>
<td>RA2</td>
<td>RC0</td>
</tr>
</tbody>
</table>
FIGURE 2-4: 20-PIN PDIP, SOIC, SSOP DIAGRAM FOR PIC16(L)F1507/8/9

FIGURE 2-5: 20-PIN QFN DIAGRAM FOR PIC16(L)F1507/8/9
3.0 MEMORY MAP

The memory is broken into two sections: program memory and configuration memory. Only the size of the program memory changes between devices, the configuration memory remains the same.

FIGURE 3-1: PIC12(L)F1501 PROGRAM MEMORY MAPPING
FIGURE 3-2: PIC16(L)F1503/1507 PROGRAM MEMORY MAPPING

- User ID Location
- User ID Location
- User ID Location
- User ID Location
- Reserved
- Reserved
- Device ID
- Configuration Word 1
- Configuration Word 2
- Calibration Word 1
- Calibration Word 2
- Reserved

Program Memory
- 0000h
- Implemented
- 07FFh
- Maps to 0-07FFh

Configuration Memory
- 7FFFh
- Maps to 8000-81FFh
- 8200h
- 8000h
- Implemented
- FFFFh
- Maps to 8000-81FFh
FIGURE 3-3: PIC16(L)F1508 PROGRAM MEMORY MAPPING

- 0000h - Implemented
- Maps to 0-0FFFh
- 0FFFh
- 4KW
- 7FFFh
- 8000h - Implemented
- Maps to 8000-81FFh
- 8200h
- FFFFh
- 8000h
- User ID Location
- 8001h
- User ID Location
- 8002h
- User ID Location
- 8003h
- User ID Location
- 8004h
- Reserved
- 8005h
- Reserved
- 8006h
- Device ID
- 8007h
- Configuration Word 1
- 8008h
- Configuration Word 2
- 8009h
- Calibration Word 1
- 800Ah
- Calibration Word 2
- 80Bh-81FFh
- Reserved
FIGURE 3-4: PIC16(L)F1509 PROGRAM MEMORY MAPPING

The figure illustrates the program memory mapping of the PIC16(L)F1509 microcontroller. The memory is divided into several sections:

- **Program Memory**: Ranges from 0000h to 1FFFh, with specific locations used for user ID, reserved, configuration words, and calibration words.
- **Configuration Memory**: Located between 8000h and 81FFh, with sections for device ID, configuration word 1, configuration word 2, calibration word 1, and calibration word 2.

The diagram shows the implemented sections and the areas that map to specific ranges of memory.
3.1 User ID Location

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped to 8000h-8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

Note: MPLAB® IDE only displays the 7 Least Significant bits (LSb) of each user ID location, the upper bits are not read. It is recommended that only the 7 LSbs be used if MPLAB IDE is the primary tool used to read these addresses.

3.2 Device ID

The device ID word is located at 8006h. This location is read-only and cannot be erased or modified.

REGISTER 3-1: DEVICE ID: DEVICE ID REGISTER(1)

<table>
<thead>
<tr>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEV8</td>
<td>DEV7</td>
<td>DEV6</td>
<td>DEV5</td>
<td>DEV4</td>
<td>DEV3</td>
<td></td>
</tr>
<tr>
<td>bit 13</td>
<td>bit 12</td>
<td>bit 11</td>
<td>bit 10</td>
<td>bit 9</td>
<td>bit 8</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEV2</td>
<td>DEV1</td>
<td>DEV0</td>
<td>REV4</td>
<td>REV3</td>
<td>REV2</td>
<td>REV1</td>
<td>REV0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 6</td>
<td>bit 5</td>
<td>bit 4</td>
<td>bit 3</td>
<td>bit 2</td>
<td>bit 1</td>
<td>bit 0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- R = Readable bit
- P = Programmable bit
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n = Value at POR
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- x = Bit is unknown

bit 13-5 DEV<8:0>: Device ID bits
These bits are used to identify the part number.

bit 4-0 REV<4:0>: Revision ID bits
These bits are used to identify the revision.

Note 1: This location cannot be written.
TABLE 3-1: DEVICE ID VALUES

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>DEVICE ID VALUES</th>
<th>REV</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC12F1501</td>
<td>0010 1100 110</td>
<td>x xxxx</td>
</tr>
<tr>
<td>PIC12LF1501</td>
<td>0010 1101 100</td>
<td>x xxxx</td>
</tr>
<tr>
<td>PIC16F1503</td>
<td>0010 1100 111</td>
<td>x xxxx</td>
</tr>
<tr>
<td>PIC16LF1503</td>
<td>0010 1101 101</td>
<td>x xxxx</td>
</tr>
<tr>
<td>PIC16F1507</td>
<td>0010 1101 000</td>
<td>x xxxx</td>
</tr>
<tr>
<td>PIC16LF1507</td>
<td>0010 1101 110</td>
<td>x xxxx</td>
</tr>
<tr>
<td>PIC16F1508</td>
<td>0010 1101 001</td>
<td>x xxxx</td>
</tr>
<tr>
<td>PIC16LF1508</td>
<td>0010 1101 111</td>
<td>x xxxx</td>
</tr>
<tr>
<td>PIC16F1509</td>
<td>0010 1101 010</td>
<td>x xxxx</td>
</tr>
<tr>
<td>PIC16LF1509</td>
<td>0010 1110 000</td>
<td>x xxxx</td>
</tr>
</tbody>
</table>

3.3 Configuration Words

There are two Configuration Words, Configuration Word 1 (8007h) and Configuration Word 2 (8008h). The individual bits within these Configuration Words are used to enable or disable device functions such as the Brown-out Reset, code protection and Power-up Timer.

3.4 Calibration Words

The internal calibration values are factory calibrated and stored in Calibration Words 1 and 2 (8009h, 800Ah).

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.
REGISTER 3-2: CONFIGURATION WORD 1: PIC12(L)F1501 AND PIC16(L)F1503/1507 DEVICES ONLY

<table>
<thead>
<tr>
<th>Bit</th>
<th>U-1</th>
<th>U-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>U-1&lt;3&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 13</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>R/P-1</td>
<td>R/P-1</td>
<td>---</td>
</tr>
<tr>
<td>bit 8</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
</tbody>
</table>

Legend:
- W = Writable bit
- '0' = Bit is cleared
- R = Readable bit
- '1' = Bit is set
- x = Bit is unknown
- U = Unimplemented bit
- P = Programmable Bit

- Unimplemented: Read as '1'

bit 11
CLKOUTEN: Clock Out Enable bit
1 = CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin.
0 = CLKOUT function is enabled on CLKOUT pin

bit 10-9
BOREN<1:0>: Brown-out Reset Enable bits(1)
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
01 = BOR controlled by SBOREN bit of the PCON register
00 = BOR disabled

bit 8(3)
Unimplemented: Read as '1'

bit 7
CP: Code Protection bit(2)
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 6
MCLRE: MCLR/VPP Pin Function Select bit
If LVP bit = 1:
This bit is ignored.
If LVP bit = 0:
1 = MCLR/VPP pin function is MCLR; Weak pull-up enabled.
0 = MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of WPUA register.

bit 5
PWRT: Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 4-3
WDTE<1:0>: Watchdog Timer Enable bit
11 = WDT enabled
10 = WDT enabled while running and disabled in Sleep
01 = WDT controlled by the SWDTEN bit in the WDTCN register
00 = WDT disabled

bit 2
Unimplemented: Read as '1'

bit 1-0
FOSC<1:0>: Oscillator Selection bits
11 = ECH: External Clock, High-Power mode: on CLkin pin
10 = ECM: External Clock, Medium-Power mode: on CLkin pin
01 = ECL: External Clock, Low-Power mode: on CLkin pin
00 = INTOSC oscillator: I/O function on OSC1 pin

Note:
1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: The entire program memory will be erased when the code protection is turned off.
3: This bit should be maintained as ‘1’ when programmed.
REGISTER 3-3: CONFIGURATION WORD 1: PIC16(L)F1508/1509 DEVICES ONLY

<table>
<thead>
<tr>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>U-1(3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FCME</td>
<td>IESO</td>
<td>CLKOUTEN</td>
<td>BOREN1</td>
<td>BOREN0</td>
<td>—</td>
</tr>
</tbody>
</table>

bit 13 FCME: Fail-Safe Clock Monitor Enable bit
1 = Fail-Safe Clock Monitor is enabled
0 = Fail-Safe Clock Monitor is disabled

bit 12 IESO: Internal/External Switchover bit
1 = Internal/External Switchover mode is enabled
0 = Internal/External Switchover mode is disabled

bit 11 CLKOUTEN: Clock Out Enable bit
1 = CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin.
0 = CLKOUT function is enabled on CLKOUT pin

bit 10-9 BOREN<1:0>: Brown-out Reset Enable bit(1)
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
01 = BOR controlled by SBOREN bit of the PCON register
00 = BOR disabled

bit 8(3) Unimplemented: Read as ‘1’

bit 7 CP: Code Protection bit(2)
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 6 MCLRE: MCLR/VPP Pin Function Select bit
If LVP bit = 1:
This bit is ignored.
If LVP bit = 0:
1 = MCLR/VPP pin function is MCLR; Weak pull-up enabled.
0 = MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of WPUA register.

bit 5 PWRTE: Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 4-3 WDTE<1:0>: Watchdog Timer Enable bit
11 = WDT enabled
10 = WDT enabled while running and disabled in Sleep
01 = WDT controlled by the SWDTE bit in the WDTCON register
00 = WDT disabled

bit 2-0 FOSC<2:0>: Oscillator Selection bits
111 = ECH: External Clock, High-Power mode: on CLKIN pin
110 = ECM: External Clock, Medium-Power mode: on CLKIN pin
101 = ECL: External Clock, Low-Power mode: on CLKIN pin
100 = INTOSC oscillator: I/O function on OSC1 pin
011 = EXTRC oscillator: RC function on CLKin pin
010 = HS oscillator: High-speed crystal/resonator on OSC1 and OSC2 pins
001 = XT oscillator: Crystal/resonator on OSC1 and OSC2 pins
000 = LP oscillator: Low-power crystal on OSC1 and OSC2 pins

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: The entire program memory will be erased when the code protection is turned off.
3: This bit should be maintained as ‘1’ when programmed.
## REGISTER 3-4: CONFIGURATION WORD 2: PIC12(L)F1501 AND PIC16(L)F1503/1507 DEVICES ONLY

<table>
<thead>
<tr>
<th>R/P-1</th>
<th>U-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>U-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVP</td>
<td>—</td>
<td>LPBOR</td>
<td>BORV</td>
<td>STVREN</td>
</tr>
</tbody>
</table>

- **bit 13**: LVP (Low-Voltage Programming Enable bit) 
  - 1 = Low-voltage programming enabled 
  - 0 = HV on MCLR/VPP must be used for programming

- **bit 12**: Unimplemented; Read as ‘1’

- **bit 11**: LPBOR (Low-Power BOR bit) 
  - 1 = Low-Power BOR is disabled 
  - 0 = Low-Power BOR is enabled

- **bit 10**: BORV (Brown-out Reset Voltage Selection bit) 
  - 1 = Brown-out Reset Voltage (VBOR) set to 1.9V on LF devices, and 2.45V on F devices 
  - 0 = Brown-out Reset Voltage (VBOR) set to 2.7V

- **bit 9**: STVREN (Stack Overflow/Underflow Reset Enable bit) 
  - 1 = Stack Overflow or Underflow will cause a Reset 
  - 0 = Stack Overflow or Underflow will not cause a Reset

- **bit 8-2**: Unimplemented; Read as ‘1’

- **bit 1-0**: WRT<1:0>: Flash Memory Self-Write Protection bits 
  - **1 kW Flash memory (PIC12(L)F1501):** 
    - 11 = Write protection off
    - 10 = 000h to 0FFh write-protected, 100h to 3FFh may be modified by PMCON control
    - 01 = 000h to 1FFh write-protected, 200h to 3FFh may be modified by PMCON control
    - 00 = 000h to 3FFh write-protected, no addresses may be modified by PMCON control
  
  - **2 kW Flash memory (PIC16(L)F1503/1507):** 
    - 11 = Write protection off
    - 10 = 000h to 1FFh write-protected, 200h to 7FFh may be modified by PMCON control
    - 01 = 000h to 3FFh write-protected, 400h to 7FFh may be modified by PMCON control
    - 00 = 000h to 7FFh write-protected, no addresses may be modified by PMCON control

**Note 1**: The LVP bit cannot be programmed to ‘0’ when Programming mode is entered via LVP.
### REGISTER 3-5: CONFIGURATION WORD 2: PIC16(L)F1508/1509 DEVICES ONLY

<table>
<thead>
<tr>
<th>U-1</th>
<th>U-1</th>
<th>U-1</th>
<th>U-1</th>
<th>U-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>U-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 13</td>
<td>LVP</td>
<td>DEBUG</td>
<td>LPBOR</td>
<td>BORV</td>
<td>STVREN</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **W** = Writable bit
- **R** = Readable bit
- **U** = Unimplemented bit
- **P** = Programmable bit
- **’0’** = Bit is cleared
- **’1’** = Bit is set
- **x** = Bit is unknown
- **—** = Value at POR

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>bit 0</td>
</tr>
</tbody>
</table>

**bit 13**
- **LVP**: Low-Voltage Programming Enable bit\(^{(1)}\)
  - **1**: Low-voltage programming enabled
  - **0**: HV on MCLR/VPP must be used for programming

**bit 12**
- **DEBUG**: Debugger mode
  - **1**: In-Circuit Debugger disabled, ICSPCLK and ICSPDAT pins are general purpose I/O pins
  - **0**: In-Circuit Debugger enabled, ICSPCLK and ICSPDAT pins are dedicated to the debugger

**bit 11**
- **LPBOR**: Low-Power BOR bit
  - **1**: Low-Power BOR is disabled
  - **0**: Low-Power BOR is enabled

**bit 10**
- **BORV**: Brown-out Reset Voltage Selection bit
  - **1**: Brown-out Reset Voltage \((V_{BOR})\) set to 1.9V on LF devices, and 2.45V on F devices
  - **0**: Brown-out Reset Voltage \((V_{BOR})\) set to 2.7V

**bit 9**
- **STVREN**: Stack Overflow/Underflow Reset Enable bit
  - **1**: Stack Overflow or Underflow will cause a Reset
  - **0**: Stack Overflow or Underflow will not cause a Reset

**bit 8-2**
- **Unimplemented**: Read as ‘1’

**bit 1-0**
- **WRT<1:0>**: Flash Memory Self-Write Protection bits
  - **4 kW Flash memory (PIC16(L)F1508)**:
    - **11**: Write protection off
    - **10**: 000h to 1FFh write-protected, 200h to FFFh may be modified by PMCON control
    - **01**: 000h to 7FFh write-protected, 800h to FFFh may be modified by PMCON control
    - **00**: 000h to FFFh write-protected, no addresses may be modified by PMCON control
  - **8 kW Flash memory (PIC16(L)F1509)**:
    - **11**: Write protection off
    - **10**: 0000h to 01FFh write-protected, 0200h to 1FFFh may be modified by PMCON control
    - **01**: 0000h to 0FFFh write-protected, 1000h to 1FFFh may be modified by PMCON control
    - **00**: 0000h to 0FFFh write-protected, no addresses may be modified by PMCON control

**Note 1**: The LVP bit cannot be programmed to ‘0’ when Programming mode is entered via LVP.
4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and latched on the falling edge. In Program/Verify mode both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high-voltage:

- **VPP** – First entry mode
- **VDD** – First entry mode

4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on MCLR from 0V to VIHH.
3. Raise the voltage on VDD from 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, the device will execute code when Configuration Word 1 has MCLR disabled (MCLRE = 0), the Power-up Timer is disabled (PWRT = 0), the internal oscillator is selected (FOSC = 100), and ICSPCLK and ICSPDAT pins are driven by the user application. Since this may prevent entry, VPP-first entry mode is strongly recommended. See the timing diagram in Figure 8-2.

4.1.2 VDD – FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on MCLR from VDD or below to VIHH.

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 8-1.

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take MCLR to VDD or lower (VIL). See Figures 8-3 and 8-4.

4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows devices to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Word 2 register is set to ‘1’, the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to ‘0’. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify modes requires the following steps:

1. MCLR is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, '0100 0110 0100 0100 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, MCLR must be held at VIL for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see Figure 8-8 and Figure 8-9.

Exiting Program/Verify mode is done by no longer driving MCLR to VIL. See Figure 8-8 and Figure 8-9.

**Note:** To enter LVP mode, the LSB of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts.
4.3 Program/Verify Commands

The devices implement 10 programming commands; each six bits in length. The commands are summarized in Table 4-1.

Commands that have data associated with them are specified to have a minimum delay of \( T_{DLY} \) between the command and the data. After this delay 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

**TABLE 4-1: COMMAND MAPPING**

<table>
<thead>
<tr>
<th>Command</th>
<th>Mapping</th>
<th>Data/Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load Configuration</td>
<td>x 0 0 0 0 0</td>
<td>00h, 0, data (14), 0</td>
</tr>
<tr>
<td>Load Data For Program Memory</td>
<td>x 0 0 0 1 0</td>
<td>02h, 0, data (14), 0</td>
</tr>
<tr>
<td>Read Data From Program Memory</td>
<td>x 0 0 1 0 0</td>
<td>04h, 0, data (14), 0</td>
</tr>
<tr>
<td>Increment Address</td>
<td>x 0 0 1 1 0</td>
<td>06h —</td>
</tr>
<tr>
<td>Reset Address</td>
<td>x 1 0 1 1 0</td>
<td>16h —</td>
</tr>
<tr>
<td>Begin Internally Timed Programming</td>
<td>x 0 1 0 0 0</td>
<td>08h —</td>
</tr>
<tr>
<td>Begin Externally Timed Programming</td>
<td>x 1 1 0 0 0</td>
<td>18h —</td>
</tr>
<tr>
<td>End Externally Timed Programming</td>
<td>x 0 1 0 1 0</td>
<td>0Ah —</td>
</tr>
<tr>
<td>Bulk Erase Program Memory</td>
<td>x 0 1 0 0 1</td>
<td>09h, Internally Timed</td>
</tr>
<tr>
<td>Row Erase Program Memory</td>
<td>x 1 0 0 0 1</td>
<td>11h, Internally Timed</td>
</tr>
</tbody>
</table>

**Note:** Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

The only way to get back to the program memory (address 0) is to exit Program/Verify mode or issue the Reset Address command after the configuration memory has been accessed by the Load Configuration command.

4.3.1 LOAD CONFIGURATION

The Load Configuration command is used to access the configuration memory (user ID locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see Figure 4-1).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

**FIGURE 4-1: LOAD CONFIGURATION**

...
4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).

**FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY**

4.3.3 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected (CP), the data will be read as zeros (see Figure 4-3).

**FIGURE 4-3: READ DATA FROM PROGRAM MEMORY**
4.3.4 INCREMENT ADDRESS

The address is incremented when this command is received. It is not possible to decrement the address. To reset this counter, the user must use the Reset Address command or exit Program/Verify mode and re-enter it. If the address is incremented from address 7FFFFh, it will wrap-around to location 0000h. If the address is incremented from FFFFh, it will wrap-around to location 8000h.

FIGURE 4-4: INCREMENT ADDRESS

4.3.5 RESET ADDRESS

The Reset Address command will reset the address to 0000h, regardless of the current value. The address is used in program memory or the configuration memory.

FIGURE 4-5: RESET ADDRESS
4.3.6 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time, TPINT, for the programming to complete.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed.

FIGURE 4-6: BEGIN INTERNALLY TIMED PROGRAMMING

4.3.7 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming the End Externally Timed Programming command must be sent in the specified time window defined by TPEXT (see Figure 4-7).

Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

FIGURE 4-7: BEGIN EXTERNALLY TIMED PROGRAMMING
4.3.8 END EXTERNALLY TIMED PROGRAMMING

This command is required after a Begin Externally Timed Programming command is given. This command must be sent within the time window specified by TPXT after the Begin Externally Timed Programming command is sent.

After sending the End Externally Timed Programming command, an additional delay (TDIS) is required before sending the next command. This delay is longer than the delay ordinarily required between other commands (see Figure 4-8).

FIGURE 4-8: END EXTERNALLY TIMED PROGRAMMING

4.3.9 BULK ERASE PROGRAM MEMORY

The Bulk Erase Program Memory command performs two different functions dependent on the current state of the address.

Address 0000h-7FFFh:
Program Memory is erased
Configuration Words are erased

Address 8000h-8008h:
Program Memory is erased
Configuration Words are erased
User ID Locations are erased

A Bulk Erase Program Memory command should not be issued when the address is greater than 8008h.

Note: The code protection Configuration bit (CP) has no effect on the Bulk Erase Program Memory command.

FIGURE 4-9: BULK ERASE PROGRAM MEMORY
4.3.10 ROW ERASE PROGRAM MEMORY

The Row Erase Program Memory command will erase an individual row. Refer to Table 4-2 for row sizes of specific devices and the PC bits used to address them. If the program memory is code-protected, the Row Erase Program Memory command will be ignored. When the address is 8000h-8008h, the Row Erase Program Memory command will only erase the user ID locations, regardless of the setting of the Configuration bit.

After receiving the Row Erase Program Memory command, the erase will not complete until the time interval, TERAR, has expired.

**TABLE 4-2: PROGRAMMING ROW SIZE AND LATCHES**

<table>
<thead>
<tr>
<th>Devices</th>
<th>PC</th>
<th>Row Size</th>
<th>Number of Latches</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC12(L)F1501</td>
<td>&lt;15:5&gt;</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>PIC16(L)F1503/1507</td>
<td>&lt;15:4&gt;</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>PIC16(L)F1508/1509</td>
<td>&lt;15:5&gt;</td>
<td>32</td>
<td>32</td>
</tr>
</tbody>
</table>

**FIGURE 4-10: ROW ERASE PROGRAM MEMORY**

![Diagram of Row Erase Program Memory]
5.0 PROGRAMMING ALGORITHMS

The devices use internal latches to temporarily store the 14-bit words used for programming. Refer to Table 4-2 for specific latch information. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The PC’s address at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which location(s) in memory are written. Writes cannot cross the physical boundary. For example, with the PIC16F1507, attempting to write from address 0002h-0009h will result in data being written to 0008h-000Fh.

If more than the maximum number of data latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. The following figures show the recommended flowcharts for programming.
FIGURE 5-1: DEVICE PROGRAM/VERIFY FLOWCHART

Note 1: See Figure 5-2.
2: See Figure 5-5.


FIGURE 5-2: PROGRAM MEMORY FLOWCHART

Note 1: This step is optional if the device has already been erased or has not been previously programmed.
2: If the device is code-protected or must be completely erased, then Bulk Erase the device per Figure 5-6.
3: See Figure 5-3 or Figure 5-4.
Note 1: Externally timed writes are not supported for Configuration and Calibration bits.
FIGURE 5-4: MULTIPLE-WORD PROGRAM CYCLE

Program Cycle

1. Load Data for Program Memory
2. Increment Address Command
3. Load Data for Program Memory
4. Increment Address Command
5. Load Data for Program Memory

- Begin Programming Command (Internally timed)
  - Wait TPINT
- Begin Programming Command (Externally timed)
  - Wait TPEXT

End Programming Command
- Wait TDIS
FIGURE 5-5: CONFIGURATION MEMORY PROGRAM FLOWCHART

Note 1: This step is optional if the device is erased or not previously programmed.
Note 2: See Figure 5-3.
FIGURE 5-6: ERASE FLOWCHART

Start

Load Configuration

Bulk Erase Program Memory

Done

Note: This sequence does not erase the Calibration Words.
6.0 CODE PROTECTION

Code protection is controlled using the CP bit in Configuration Word 1. When code protection is enabled, all program memory locations (0000h-7FFh) read as ‘0’. Further programming is disabled for the program memory (0000h-7FFFh).

The user ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

6.1 Program Memory

Code protection is enabled by programming the CP bit in Configuration Word 1 register to ‘0’.

The only way to disable code protection is to use the Bulk Erase Program Memory command.

7.0 HEX FILE USAGE

In the hex file there are two bytes per program word stored in the Intel® INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. (Example: Configuration Word 1 is stored at 8007h on the PIC16(L)F1507. In the hex file this will be referenced as 1000Eh-1000Fh).

7.1 Configuration Word

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and user ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and user ID information should be included.

7.2 Device ID and Revision

If a device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the device ID (excluding the revision) against the value read from the part. On a mismatch condition the programmer should generate a warning message.
7.3 Checksum Computation

The checksum is calculated by two different methods dependent on the setting of the CP Configuration bit.

7.3.1 PROGRAM CODE PROTECTION DISABLED

With the program code protection disabled, the checksum is computed by reading the contents of the program memory locations and adding up the program memory data starting at address 0000h, up to the maximum user addressable location. Any Carry bit exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to ‘0’.

### TABLE 7-1: CONFIGURATION WORD MASK VALUES

<table>
<thead>
<tr>
<th>Device</th>
<th>Config. Word 1 Mask</th>
<th>Config. Word 2 Mask</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC12(L)F1501</td>
<td>0EFBh</td>
<td>2E03h</td>
</tr>
<tr>
<td>PIC16(L)F1503</td>
<td>0EFBh</td>
<td>2E03h</td>
</tr>
<tr>
<td>PIC16(L)F1507</td>
<td>0EFBh</td>
<td>2E03h</td>
</tr>
<tr>
<td>PIC16(L)F1508</td>
<td>3EFFh</td>
<td>3E03h</td>
</tr>
<tr>
<td>PIC16(L)F1509</td>
<td>3EFFh</td>
<td>3E03h</td>
</tr>
</tbody>
</table>

#### EXAMPLE 7-1: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED (CP = 1), PIC16F1507, BLANK DEVICE

<table>
<thead>
<tr>
<th>Device</th>
<th>Sum of Memory addresses 0000h-07FFh</th>
<th>F800h(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configuration Word 1</td>
<td></td>
<td>3FFFh(2)</td>
</tr>
<tr>
<td>Configuration Word 1 mask</td>
<td></td>
<td>0EFBh(3)</td>
</tr>
<tr>
<td>Configuration Word 2</td>
<td></td>
<td>3FFFh(4)</td>
</tr>
<tr>
<td>Configuration Word 2 mask</td>
<td></td>
<td>2E03h(5)</td>
</tr>
<tr>
<td>Checksum</td>
<td>= F800h + (3FFFh and 0EFBh) + (3FFFh and 2E03h)(6)</td>
<td>= 34FEh</td>
</tr>
<tr>
<td></td>
<td>= F800h + 0EFBh + 2E03h</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** This value is obtained by taking the total number of program memory locations (0x000 to 0x7FFh which is 800h) and multiplying it by the blank memory value of 0x3FFF to get the sum of 1FF F800h. Then, truncate to 16 bits, thus having a final value of F800h.

**2:** This value is obtained by making all bits of the Configuration Word 1 a ‘1’, then converting it to hex, thus having a value of 3FFFh.

**3:** This value is obtained by making all used bits of the Configuration Word 1 a ‘1’, then converting it to hex, thus having a value of 0EFBh.

**4:** This value is obtained by making all bits of the Configuration Word 2 a ‘1’, then converting it to hex, thus having a value of 3FFFh.

**5:** This value is obtained by making all used bits of the Configuration Word 2 a ‘1’, then converting it to hex, thus having a value of 2E03h.

**6:** This value is obtained by ANDing the Configuration Word value with the Configuration Word Mask Value and adding it to the sum of memory addresses: (3FFFh and 0EFBh) + (3FFFh and 2E03h) + F800h = 1 34FEh. Then, truncate to 16 bits, thus having a final value of 34FEh.
EXAMPLE 7-2: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED (CP = 1), PIC16LF1507, 00AAh AT FIRST AND LAST ADDRESS

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sum of Memory addresses 0000h-07FFh</td>
<td>7956h(1)</td>
</tr>
<tr>
<td>Configuration Word 1</td>
<td>3FFFh(2)</td>
</tr>
<tr>
<td>Configuration Word 1 mask</td>
<td>0EFBh(3)</td>
</tr>
<tr>
<td>Configuration Word 2</td>
<td>3FFFh(4)</td>
</tr>
<tr>
<td>Configuration Word 2 mask</td>
<td>2E03h(5)</td>
</tr>
<tr>
<td>Checksum = 7956h + (3FFFh and 0EFBh) + (3FFFh and 2E03h)(6)</td>
<td>B654h</td>
</tr>
</tbody>
</table>

Note 1: This value is obtained by taking the total number of program memory locations (0x000 to 0x7FFh which is 800h) subtracting 2h which yields 7FEh, then multiplying it by the blank memory value of 0x3FFF to get the sum of 1FF 7802h. Then, truncate to 16 bits the value of 7802h. Now add 00AAh (00AAh + 00AAh) to 7802h to get the final value of B654h.

2: This value is obtained by making all bits of the Configuration Word 1 a ‘1’, then converting it to hex, thus having a value of 3FFFh.

3: This value is obtained by making all used bits of the Configuration Word 1 a ‘1’, then converting it to hex, thus having a value of 0EFBh.

4: This value is obtained by making all bits of the Configuration Word 2 a ‘1’, then converting it to hex, thus having a value of 3FFFh.

5: This value is obtained by making all used bits of the Configuration Word 2 a ‘1’, then converting it to hex, thus having a value of 2E03h.

6: This value is obtained by ANDing the Configuration Word value with the Configuration Word Mask Value and adding it to the sum of memory addresses: (3FFFh and 0EFBh) + (3FFFh and 2E03h) + 7956h = B654h. Then, truncate to 16 bits, thus having a final value of B654h.
7.3.2 PROGRAM CODE PROTECTION ENABLED

With the program code protection enabled, the checksum is computed in the following manner: The Least Significant nibble of each user ID is used to create a 16-bit value. The masked value of user ID location 8000h is the Most Significant nibble. This sum of user IDs is summed with the Configuration Words (all unimplemented Configuration bits are masked to '0').

EXAMPLE 7-3: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED (CP = 0), PIC16F1507, BLANK DEVICE

<table>
<thead>
<tr>
<th>PIC16F1507</th>
<th>Configuration Word 1</th>
<th>3F7Fh(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Configuration Word 1 mask</td>
<td>0E7Bh(2)</td>
</tr>
<tr>
<td></td>
<td>Configuration Word 2</td>
<td>3FFFh(3)</td>
</tr>
<tr>
<td></td>
<td>Configuration Word 2 mask</td>
<td>2E03h(4)</td>
</tr>
<tr>
<td>User ID (8000h)</td>
<td>0006h(5)</td>
<td></td>
</tr>
<tr>
<td>User ID (8001h)</td>
<td>0007h(5)</td>
<td></td>
</tr>
<tr>
<td>User ID (8002h)</td>
<td>0001h(5)</td>
<td></td>
</tr>
<tr>
<td>User ID (8003h)</td>
<td>0002h(5)</td>
<td></td>
</tr>
</tbody>
</table>

Sum of User IDs = (0006h and 000Fh) << 12 + (0007h and 000Fh) << 8 + (0001h and 000Fh) << 4 + (0002h and 000Fh)(6) = 6000h + 0700h + 0010h + 0002h = 6712h

Checksum = (3F7Fh and 0E7Bh) + (3FFFh and 2E03h) + Sum of User IDs(7) = 0E7Bh +2E03h + 6712h = A390h

Note 1: This value is obtained by making all bits of the Configuration Word 1 a '1', but the code-protect bit is '0' (thus, enabled), then converting it to hex, thus having a value of 3F7Fh.

2: This value is obtained by making all used bits of the Configuration Word 1 a '1', but the code-protect bit is '0' (thus, enabled), then converting it to hex, thus having a value of 0E7Bh.

3: This value is obtained by making all bits of the Configuration Word 2 a '1', then converting it to hex, thus having a value of 3FFFh.

4: This value is obtained by making all used bits of the Configuration Word 2 a '1', then converting it to hex, thus having a value of 2E03h.

5: These values are picked at random for this example; they could be any 16-bit value.

6: In order to calculate the sum of user IDs, take the 16-bit value of the first user ID location (0006h), AND the address to (000Fh), thus masking the MSB. This gives you the value 0006h, then shift left 12 bits, giving you 6000h. Do the same procedure for the 16-bit value of the second user ID location (0007h), except shift left 8 bits. Also, do the same for the third user ID location (0001h), except shift left 4 bits. For the fourth user ID location do not shift. Finally, add up all four user ID values to get the final sum of user IDs of 6712h.

7: This value is obtained by ANDing the Configuration Word value with the Configuration Word Mask Value and adding it to the sum of user IDs: (3F7Fh AND 0E7Bh) + (3FFFh AND 2E03h) + 6712h = A390h.
**EXAMPLE 7-4: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED (CP = 0), PIC16LF1507, 00AAh AT FIRST AND LAST ADDRESS**

<table>
<thead>
<tr>
<th>PIC16LF1507</th>
<th>Configuration Word 1</th>
<th>3F7Fh(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Configuration Word 1 mask</td>
<td>0E7Bh(2)</td>
</tr>
<tr>
<td></td>
<td>Configuration Word 2</td>
<td>3FFFh(3)</td>
</tr>
<tr>
<td></td>
<td>Configuration Word 2 mask</td>
<td>2E03h(4)</td>
</tr>
<tr>
<td></td>
<td>User ID (8000h)</td>
<td>000Eh(5)</td>
</tr>
<tr>
<td></td>
<td>User ID (8001h)</td>
<td>0008h(5)</td>
</tr>
<tr>
<td></td>
<td>User ID (8002h)</td>
<td>0005h(5)</td>
</tr>
<tr>
<td></td>
<td>User ID (8003h)</td>
<td>0008h(5)</td>
</tr>
</tbody>
</table>

Sum of User IDs: 

\[
\text{Sum of User IDs} = (000Eh \text{ and } 000Fh) \ll 12 + (0008h \text{ and } 000Fh) \ll 8 + \]
\[
(0005h \text{ and } 000Fh) \ll 4 + (0008h \text{ and } 000Fh) \ll 0
\]
\[
= E000h + 0800h + 0050h + 0008h
\]
\[
= E858h
\]

Checksum: 

\[
\text{Checksum} = (3F7Fh \text{ and } 0E7Bh) + (3FFFh \text{ and } 2E03h) + \text{Sum of User IDs}^{(7)}
\]
\[
= 0E7Bh + 2E03h + E858h
\]
\[
= 24D6h
\]

**Note 1:**

This value is obtained by making all bits of the Configuration Word 1 a ‘1’, but the code-protect bit is ‘0’ (thus, enabled), then converting it to hex, thus having a value of 3F7Fh.

**2:** This value is obtained by making all the used bits of the Configuration Word 1 a ‘1’, but the code-protect bit is ‘0’ (thus, enabled), then converting it to hex, thus having a value of 0E7Bh.

**3:** This value is obtained by making all bits of the Configuration Word 2 a ‘1’, then converting it to hex, thus having a value of 3FFFh.

**4:** This value is obtained by making all used bits of the Configuration Word 2 a ‘1’, then converting it to hex, thus having a value of 2E03h.

**5:** These values are picked at random for this example; they could be any 16-bit value.

**6:** In order to calculate the sum of user IDs, take the 16-bit value of the first user ID location (000Eh), AND the address to (000Fh), thus masking the MSB. This gives you the value 000Eh, then shift left 12 bits, giving you E000h. Do the same procedure for the 16-bit value of the second user ID location (0008h), except shift left 8 bits. Also, do the same for the third user ID location (0005h), except shift left 4 bits. For the fourth user ID location do not shift. Finally, add up all four user ID values to get the final sum of user IDs of E858h.

**7:** This value is obtained by ANDing the Configuration Word value with the Configuration Word Mask Value and adding it to the sum of user IDs: (3F7Fh AND 0E7Bh) + (3FFFh AND 2E03h) + E858h = 24D6h.
8.0 ELECTRICAL SPECIFICATIONS

Refer to the device specific data sheet for absolute maximum ratings.

**TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE**

<table>
<thead>
<tr>
<th>AC/DC CHARACTERISTICS</th>
<th>Standard Operating Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Supply Voltages and Currents</strong></td>
<td>Production tested at 25°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD</td>
<td>Read/Write and Row Erase operations</td>
<td>VDD min. — — VDD max.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bulk Erase operations</td>
<td>— — 1.0 mA</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>IDD</td>
<td>Current on VDD, Idle</td>
<td>— — 3.0 mA</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>IDDP</td>
<td>Current on VDD, Programming</td>
<td>— — 1.0 mA</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>VPP</td>
<td>Current on MCLR/VPP</td>
<td>— — 600 μA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIHH</td>
<td>High voltage on MCLR/VPP for Program/Verify mode entry</td>
<td>8.0 — 9.0 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TVHHR</td>
<td>MCLR rise time (VIL to VIHH) for Program/Verify mode entry</td>
<td>— — 1.0 μs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>I/O pins</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>(ICSPCLK, ICSPDAT, MCLR/VPP) input high level</td>
<td>0.8 VDD — — V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>(ICSPCLK, ICSPDAT, MCLR/VPP) input low level</td>
<td>— — 0.2 VDD</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>ICSPDAT output high level</td>
<td>VDD-0.7 — — V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>ICSPDAT output low level</td>
<td>VSS+0.6</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Programming Mode Entry and Exit</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TENTS</td>
<td>Programing mode entry setup time: ICSPCLK, ICSPDAT setup time before VDD or MCLR↑</td>
<td>100 — — ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TENTH</td>
<td>Programing mode entry hold time: ICSPCLK, ICSPDAT hold time after VDD or MCLR↑</td>
<td>250 — — μs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Serial Program/Verify</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TCKL</td>
<td>Clock Low Pulse Width</td>
<td>100 — — ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TCKH</td>
<td>Clock High Pulse Width</td>
<td>100 — — ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TDS</td>
<td>Data in setup time before clock↓</td>
<td>100 — — ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TDH</td>
<td>Data in hold time after clock↓</td>
<td>100 — — ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TCO</td>
<td>Clock↑ to data out valid (during a Read Data command)</td>
<td>0 — 80 ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TLZD</td>
<td>Clock↑ to data low-impedance (during a Read Data command)</td>
<td>0 — 80 ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>THZD</td>
<td>Clock↑ to data high-impedance (during a Read Data command)</td>
<td>0 — 80 ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TDLY</td>
<td>Data input not driven to next clock input (delay required between command/data or command/command)</td>
<td>1.0 — — μs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TERAB</td>
<td>Bulk Erase cycle time</td>
<td>— — 5 ms</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TERAR</td>
<td>Row Erase cycle time</td>
<td>— — 2.5 ms</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPINT</td>
<td>Internally timed programming operation time</td>
<td>— — 2.5 ms</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPEXT</td>
<td>Externally timed programming pulse</td>
<td>1.0 — 2.1 ms</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TDIS</td>
<td>Time delay from program to compare (HV discharge time)</td>
<td>300 — — μs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TEXT</td>
<td>Time delay when exiting Program/Verify mode</td>
<td>1 — — μs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Externally timed writes are not supported for Configuration and Calibration bits.
8.1 AC Timing Diagrams

**FIGURE 8-1:** PROGRAMMING MODE ENTRY – VDD FIRST

![Programming Mode Entry - VDD First Diagram]

**FIGURE 8-2:** PROGRAMMING MODE ENTRY – VPP FIRST

![Programming Mode Entry - VPP First Diagram]

**FIGURE 8-3:** PROGRAMMING MODE EXIT – VPP LAST

![Programming Mode Exit - VPP Last Diagram]

**FIGURE 8-4:** PROGRAMMING MODE EXIT – VDD LAST

![Programming Mode Exit - VDD Last Diagram]
FIGURE 8-5: CLOCK AND DATA TIMING

ICSPCLK

ICSPDAT as input

ICSPDAT as output

ICSPDAT from input to output

ICSPDAT from output to input

FIGURE 8-6: WRITE COMMAND-PAYLOAD TIMING

ICSPCLK

ICSPDAT

Command

Payload

Next Command

FIGURE 8-7: READ COMMAND-PAYLOAD TIMING

ICSPCLK

ICSPDAT (from Programmer)

ICSPDAT (from Device)

Command

Payload

Next Command
FIGURE 8-8:  LVP ENTRY (POWERED)

FIGURE 8-9:  LVP ENTRY (POWERING UP)

Note 1: Sequence matching can start with no edge on MCLR first.
APPENDIX A:  REVISION HISTORY

Revision A (04/2011)
Original release of this document.

Revision B (05/2011)
Updated Figures 2-1 and 2-2; Added Note 3 to Register 3-2; Revised Register 3-3; Other minor corrections.

Revision C (08/2011)
Added PIC12(L)F1501 and PIC16(L)F1503/1508/1509 devices; Other minor corrections.
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