High-Performance RISC CPU:

• Only 49 Instructions to learn
• Operating Speed:
  - DC – 32 MHz clock input
  - DC – 125 ns instruction cycle
• Interrupt Capability with Automatic Context Saving
• 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
• Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

Special Microcontroller Features:

• Precision Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency range from 32 MHz to 31 kHz
• 31 kHz Low-Power Internal Oscillator
• External Oscillator Block with:
  - 4 crystal/resonator modes up to 32 MHz using 4xPLL
  - 3 external clock modes up to 32 MHz
• 4x Phase Locked Loop (PLL)
• Fail-Safe Clock Monitor
• Two-Speed Start-up
• Power-Saving Sleep mode
• Power-on Reset (POR)
• Power-up Timer (PWRT)
• Oscillator Start-Up Timer (OST)
• Brown-out Reset (BOR) with Selectable Trip Point
• Extended Watchdog Timer (WDT)
• In-Circuit Serial Programming™ (ICSP™) via two pins
• In-Circuit Debug (ICD) via Two Pins
• Enhanced Low-Voltage Programming (LVP)
• Operating Voltage Range:
  - 1.8V to 3.6V (PIC1XLF182X)
  - 1.8V to 5.5V (PIC1XF182X)
• Programmable Code Protection
• Self-Programmable under Software Control

Low-Power Features:

• Standby Current (PIC1XLF182X):
  - 30 nA @ 1.8V, typical
• Operating Current (PIC1XLF182X):
  - 75 µA @ 1 MHz, 1.8V, typical
• Low-Power Watchdog Timer Current (PIC1XLF182X):
  - 500 nA @ 1.8V, typical

Peripheral Features:

• Up to 17 I/O Pins and 1 Input-only Pin:
  - High current sink/source for LED drivers
  - Individually programmable interrupt-on-change pins
  - Individually programmable weak pull-ups
• Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
• Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Dedicated low-power 32 kHz oscillator driver
• Up to three Timer2 modules (Timer2,4,6): 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
• Up to two Enhanced Capture, Compare, PWM modules (ECCP):
  - Software selectable time-bases
  - Auto-shutdown and auto-restart
  - PWM steering
• Up to two Capture, Compare, PWM modules (CCP):
  - Software selectable time-bases
• Up to two Master Synchronous Serial Port (MSSP) with SPI and I2C™ with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
• Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, RS-485 and LIN compatible
  - Auto-Baud Detect
  - Auto-wake-up on start
• SR Latch (Integrated 555 Timer):
  - Multiple Set/Reset input options
• Analog-to-Digital Converter (ADC):
  - 10-bit resolution
  - Up to 12 channels
• Up to 2 Comparators:
  - Rail-to-rail inputs
  - Power mode control
  - Software controllable hysteresis
• Voltage Reference module:
  - Fixed voltage reference (FVR) with 1.024V, 2.048V and 4.096V output levels
  - 5-bit rail-to-rail resistive DAC with positive and negative reference selection
• Capacitive Touch oscillator module:
  - Up to 12 channels
• Data Signal Modulator:
  - Select modulator and carrier sources from various module outputs.
<table>
<thead>
<tr>
<th>Device</th>
<th>Program Memory Flash (words)</th>
<th>Data EEPROM (bytes)</th>
<th>SRAM (bytes)</th>
<th>I/Os</th>
<th>10-bit A/D (ch)</th>
<th>Timers 8/16-bit</th>
<th>EUSART</th>
<th>MSSP</th>
<th>ECCP/CCP</th>
<th>Cap Touch Channels</th>
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<tr>
<td>PIC12F1822</td>
<td>2048</td>
<td>256</td>
<td>128</td>
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<td>2/2</td>
<td>8</td>
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<td>1024</td>
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<td>2/2</td>
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<td>2/2</td>
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<td>256</td>
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<td>4/1</td>
<td>1</td>
<td>2</td>
<td>2/2</td>
<td>12</td>
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</tbody>
</table>
FIGURE 1: 8-PIN DIAGRAM FOR PIC12F1822/LF1822

Note: Pin details are subject to change.

PDIP, SOIC, DFN

VDD 1 7 AN0 DACOUT CPS0 C1IN+ — — P1B(1) TX(1) CK(1) SDO(1) SS(1) IOC MDOUT Y ICSPDAT/ICDDAT
RA1 6 AN1 VREF CPS1 C1INO- SRI — — RX(1) DT(1) SCL SCK IOC MDMIN Y ICSPCLK/ICDCLK
RA2 5 AN2 — CPS2 C1OUT SRQ T0CKI CCP1(1) P1A(1) FLT0 — SDA SDI INT/I OC MDCIN1 Y —
RA3 4 — — — — — T1G(1) — — SS(1) IOC — Y MCLR VPP ICDCLR
RA4 3 AN3 — CPS3 C1IN1- — T1G(1) T1OSO P1B(1) TX(1) CK(1) SDO(1) IOC MDCIN2 Y OSC2 CLKOUT CLKR
RA5 2 — — — — SRNO T1CKI T1OSI CCP1(1) P1A(1) RX(1) DT(1) — IOC — Y OSC1 CLKIN
VDD 1 — — — — — — — — — — — — — — — VDD
Vss 8 — — — — — — — — — — — — — — — Vss

Note 1: Pin functions can be assigned to one of two pin locations via software.
FIGURE 2: 14-PIN DIAGRAM FOR PIC16F/LF1823/1824/1825

PDIP, SOIC, TSSOP

VDD ——— 1 ——— 14 ——— VSS
RA5 ——— 2 ——— 13 ——— RA0
RA4 ——— 3 ——— 12 ——— RA1
RA3 ——— 4 ——— 11 ——— RA2
RC5 ——— 5 ——— 10 ——— RC0
RC4 ——— 6 ——— 9 ——— RC1
RC3 ——— 7 ——— 8 ——— RC2

Note: See Table 3 for location of all peripheral functions.

FIGURE 3: 16-PIN DIAGRAM FOR PIC16F/LF1823/1824/1825

QFN

VDD ——— 1 ——— 14 ——— VSS
RA5 ——— 2 ——— 13 ——— RA0
RA4 ——— 3 ——— 12 ——— RA1
RA3 ——— 4 ——— 11 ——— RA2
RC5 ——— 5 ——— 10 ——— RC0
RC4 ——— 6 ——— 9 ——— RC1
RC3 ——— 7 ——— 8 ——— RC2

Note: See Table 3 for location of all peripheral functions.
## TABLE 3: 14-PIN AND 16-PIN ALLOCATION TABLE (PIC16F/LF1823/1824/1825)

<table>
<thead>
<tr>
<th>IO</th>
<th>14-Pin PDIP/SOIC/TSSOP</th>
<th>16-Pin QFN</th>
<th>AUD</th>
<th>Reference</th>
<th>Cap Sense</th>
<th>Comparator</th>
<th>SR Latch</th>
<th>Timers</th>
<th>CCP</th>
<th>EUSART</th>
<th>MSSP</th>
<th>Interrupt</th>
<th>Modulator</th>
<th>Pull-up</th>
<th>Basic</th>
</tr>
</thead>
<tbody>
<tr>
<td>RA0</td>
<td>13 7 AN0   DACOUT       CPS0       C1IN+   —       —       —        —      TX(1) CK(1)</td>
<td>—   IOC   —       Y        ICSPDAT/ ICDDAT</td>
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<td></td>
</tr>
<tr>
<td>RA1</td>
<td>12 11 AN1  VREF         CPS1       C12IN0- SRI   —       —       —        —      RX(1) DT(1)</td>
<td>—   IOC   —       Y        ICSPCLK   ICDClk</td>
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<tr>
<td>RA2</td>
<td>11 10 AN2  —             CPS2       C1OUT   SRQ     T0CKI   CCP3(2)</td>
<td>FLT0  —       —       INT/ IOC  —       Y   —</td>
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<tr>
<td>RA3</td>
<td>4  3   —       —       —       —       —       T1G(1)</td>
<td>—       SSI(1) IOC   —       Y        MCLR   Vpp</td>
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</tr>
<tr>
<td>RA4</td>
<td>3  2 AN3   —             CPS3       —       —       —       T1G(1)</td>
<td>T1OS0  P2B(1,2) —       SDO(1) IOC   —       Y        OSC2 CLKOUT CLK</td>
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</tr>
<tr>
<td>RA5</td>
<td>2  1   —       —       —       —       —       T1CKI</td>
<td>T1OSI  CCP2(1,2)</td>
<td>P2A(1,2)  —       IOC   —       Y        OSC1 CLKR</td>
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</tr>
<tr>
<td>RC0</td>
<td>10 9 AN4   —             CPS4       C2IN+   —       —       —        —      P1D(1,2)</td>
<td>—       SCL  SCK   —       Y   —</td>
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<tr>
<td>RC1</td>
<td>9  8 AN5   —             CPS5       C12IN1- —       —       —        —      P1C(1,2) CCP4(2)</td>
<td>—       SDA  SDI   —       Y   —</td>
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<tr>
<td>RC2</td>
<td>8  7 AN6   —             CPS6       C12IN2- —       —       —        —      P1D(1) P2B(1,2)</td>
<td>—       SDO(1) —       —       MDCIN1 Y   —</td>
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<tr>
<td>RC3</td>
<td>7  6 AN7   —             CPS7       C12IN3- —       —       —        —      P1C(1) CCP2(1,2)</td>
<td>P2A(1,2) —       SSI(1) —       —       MDCIN Y   —</td>
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<tr>
<td>RC4</td>
<td>6  5   —       —       —       —       —       C2OUT</td>
<td>SRNQ  —       P1B   TX(1) CK(1)</td>
<td>—       MDOU Y   —</td>
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<tr>
<td>RC5</td>
<td>5  4   —       —       —       —       —       —       —       CCP1</td>
<td>P1A  RX(1) DT(1)</td>
<td>—       —       —       —       MDCIN2 Y   —</td>
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<td>Vcc</td>
<td>1  16  —       —       —       —       —       —       —       —       —       Vcc   —       —       —       —       Vcc</td>
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<tr>
<td>Vss</td>
<td>14 13  —       —       —       —       —       —       —       —       —       —       —       —       —       —       Vss</td>
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</tr>
</tbody>
</table>

**Note**
1. Pin functions can be assigned to one of two pin locations via software.
2. Pin function only available on PIC16F1824 and PIC16F1825.
FIGURE 4: 20-PIN DIAGRAM FOR PIC16F/LF1828/1829

PDIP, SOIC, SSOP

Vdd → 1 → 20 → Vss
RA5 → 2 → 19 → RA0
RA4 → 3 → 18 → RA1
RA3 → 4 → 17 → RA2
RC5 → 5 → 16 → RC0
RC4 → 6 → 15 → RC1
RC3 → 7 → 14 → RC2
RC6 → 8 → 13 → RB4
RC7 → 9 → 12 → RB5
RB7 → 10 → 11 → RB6

Note: See Table 4 for location of all peripheral functions.

FIGURE 5: 20-PIN DIAGRAM FOR PIC16F/LF1828/1829

QFN 4x4

Note: See Table 4 for location of all peripheral functions.
<table>
<thead>
<tr>
<th>IO</th>
<th>20-Pin PDIP/SSOP</th>
<th>A/D</th>
<th>Reference</th>
<th>Cap Sense</th>
<th>Comparator</th>
<th>SR Latch</th>
<th>Timers</th>
<th>CCP</th>
<th>EUSART</th>
<th>MSP</th>
<th>Interrupt</th>
<th>Modulator</th>
<th>Pull-up</th>
<th>Basic</th>
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<tr>
<td>RA0</td>
<td>19/16</td>
<td>AN0</td>
<td>VREF-DACOUT</td>
<td>CPS0</td>
<td>C1N+</td>
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<td>T0CKI</td>
<td>CCP3</td>
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<td>T1OSO</td>
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<td>CCP2(1)</td>
<td>P2A(1)</td>
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<td>SDO(1,2)</td>
<td>IOY</td>
<td>Y</td>
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<td>CPS10</td>
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<td>—</td>
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<td>—</td>
<td>SDA1/SO1</td>
<td>IOY</td>
<td>—</td>
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<td>SDA2(1,2)</td>
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<td>SCL(1)</td>
<td>IOY</td>
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<td>—</td>
<td>—</td>
<td>SCL1/SCK1</td>
<td>IOY</td>
<td>—</td>
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<td>T(X(1)</td>
<td>SCL2(1)</td>
<td>IOY</td>
<td>—</td>
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<tr>
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<td>AN4</td>
<td>CPS4</td>
<td>C2IN+</td>
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<td>—</td>
<td>—</td>
<td>P1D(1)</td>
<td>—</td>
<td>S5(1,2)</td>
<td>—</td>
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<tr>
<td>RC1</td>
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<td>C12IN1</td>
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<td>—</td>
<td>P1C(1)</td>
<td>—</td>
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<td>—</td>
<td>—</td>
<td>P1D(1)</td>
<td>P2B(1)</td>
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<td>P1C(1)</td>
<td>CCP2(1)</td>
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<td>RC4</td>
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<td>P1B</td>
<td>TX(1)</td>
<td>CK(1)</td>
<td>—</td>
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<tr>
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<td>CCP1</td>
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<td>—</td>
<td>Vss</td>
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**Note 1:** Pin functions can be assigned to one of two pin locations via software.
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