PIC18(L)F25/26K83

28-Pin, Low-Power, High-Performance Microcontrollers with CAN Technology

Description
The PIC18(L)FXXX83 is a full-featured CAN product family that can be used in automotive and industrial applications. The multitude of communication peripherals found on the product family, such as CAN, SPI, two I²Cs, two UARTs, LIN, DMX, and DALI can handle a wide range of wired and wireless (using external modules) communication protocols for intelligent applications. This family includes a 12-bit ADC with Computation (ADC²) extensions for automated signal analysis to reduce the complexity of the application. This, combined with the Core Independent Peripherals integration capabilities, enables functions for motor control, power supply, sensor, signal and user interface applications.

Core Features
- C Compiler Optimized RISC Architecture
- Operating Speed:
  - Up to 64 MHz clock operation
  - 62.5 ns minimum instruction cycle
- Two Direct Memory Access (DMA) Controllers:
  - Data transfers to SFR/GPR spaces from either Program Flash Memory, Data EEPROM or SFR/GPR spaces
  - User-programmable source and destination sizes
  - Hardware and software-triggered data transfers
- System Bus Arbiter with User-Configurable Priorities for Scanner and DMA1/DMA2 with respect to the main line and interrupt execution
- Vectored Interrupt Capability:
  - Selectable high/low priority
  - Fixed interrupt latency
  - Programmable vector table base address
- 31-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-Out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Variable prescaler selection
  - Variable window size selection
  - Configurable in hardware or software

Memory
- Up to 64 KB Flash Program Memory
- Up to 4 KB Data SRAM Memory
- Up to 1 KB Data EEPROM
- Memory Access Partition (MAP):
  - Configurable boot and app region sizes with individual write-protections
- Programmable Code Protection
- Device Information Area (DIA) stores:
  - Unique IDs and Device IDs
  - Temp Sensor factory-calibrated data
  - Fixed Voltage Reference calibrated data
- Device Configuration Information (DCI) stores:
  - Erase row size
  - Number of write latches per row
  - Number of user rows
  - Data EEPROM memory size
  - Pin count

Operating Characteristics
- Operating Voltage Range:
  - 1.8V to 3.6V (PIC18LF25/26K83)
  - 2.3V to 5.5V (PIC18F25/26K83)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Functionality
- DOZE mode: Ability to run CPU core slower than the system clock
- IDLE mode: Ability to halt CPU core while internal peripherals continue operating
- SLEEP mode: Lowest power consumption
- Peripheral Module Disable (PMD):
  - Ability to disable unused peripherals to minimize power consumption
eXtreme Low-Power (XLP) Features

- Sleep mode: 60 nA @ 1.8V, typical
- Windowed Watchdog Timer: 720 nA @ 1.8V, typical
- Secondary Oscillator: 580 nA @ 32 kHz
- Operating Current:
  - 4 uA @ 32 kHz, 1.8V, typical
  - 45 uA/MHz @ 1.8V, typical

Digital Peripherals

- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT):
  - Hardware monitoring and Fault detection
- Four 16-Bit Timers (TMR0/1/3/5)
- Four Configurable Logic Cell (CLC):
  - Integrated combinational and sequential logic
- Three Complementary Waveform Generators (CWGs):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
  - Programmable dead band
  - Fault-shutdown input
- Four Capture/Compare/PWM (CCP) modules
- Four 10-bit Pulse-Width Modulators (PWMs)
- Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control
  - High resolution using 20-bit accumulator and 20-bit increment values
- DSM: Data Signal Modulator:
  - Multiplex two carrier clocks, with glitch prevention feature
  - Multiple sources for each carrier
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for fail-safe operation (e.g., Class B)
  - Calculate CRC over any portion of program memory
- Two UART Modules:
  - Modules are Asynchronous, RS-232, RS-485 compatibility.
  - One of the UART modules supports LIN Master and Slave, DMX mode, DALI Gear and Device protocols
  - Automatic and user-timed BREAK period generation
  - DMA Compatible
  - Automatic checksums
  - Programmable 1, 1.5, and two Stop bits
  - Wake-up on BREAK reception

- One SPI module:
  - Configurable length bytes
  - Configurable length data packets
  - Receive-without-transmit option
  - Transmit-without-receive option
  - Transfer byte counter
  - Separate Transmit and Receive Buffers with 2-byte FIFO and DMA capabilities

- CAN module:
  - Conforms to CAN 2.0B Active Specification
  - Three operating modes: Legacy (compatible with existing PIC18CXX8/FXX8 CAN modules), Enhanced mode, and FIFO mode.
  - Message bit rates up to 1 Mbps
  - DeviceNet™ data byte filter support
  - Six programmable receive/transmit buffers
  - Three dedicated transmit buffers
  - Two dedicated receive buffers
  - 16 Full, 29-bit acceptance filters with dynamic association
  - Three full, 29-bit acceptance masks
  - Automatic remote frame handling
  - Advanced error management features.

- Two I²C modules, SMBus, PMBus™ compatible:
  - Dedicated Address, Transmit and Receive buffers
  - Bus Collision Detection with arbitration
  - Bus time-out detection and handling
  - Multi-Master mode
  - Separate Transmit and Receive Buffers with 2-byte FIFO and DMA capabilities
  - I²C, SMBus 2.0 and SMBus 3.0, and 1.8V input level selections

- Device I/O Port Features:
  - 25 I/O pins (PIC18(L)F25K83)
  - One input-only pin
  - Individually programmable I/O direction, open-drain, slew rate, weak pull-up control
  - Interrupt-on-change
  - Three External Interrupt Pins

- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

- Two Signal Measurement Timer (SMT):
  - 24-bit timer/counter with prescaler
Analog Peripherals

- Analog-to-Digital Converter with Computation (ADC):
  - 12-bit with up to 24 external channels
  - Automated post-processing
  - Automated math functions on input signals: averaging, filter calculations, oversampling and threshold comparison
  - Operates in Sleep
  - Integrated charge pump for improved low-voltage operation
- Hardware Capacitive Voltage Divider (CVD):
  - Automates touch sampling and reduces software size and CPU usage when touch or proximity sensing is required
  - Adjustable sample and hold capacitor array
  - Two guard ring output drives
- Temperature Sensor:
  - Internal connection to ADC
  - Can be calibrated for improved accuracy
- Two Comparators:
  - Low-Power/High-Speed mode
  - Fixed Voltage Reference at noninverting input(s)
  - Comparator outputs externally accessible
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Positive Reference Selection
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels

Flexible Oscillator Structure

- High-Precision Internal Oscillator:
  - Selectable frequency range up to 64 MHz
  - ±1% at calibration (nominal)
- Low-Power Internal 32 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOCS)
- External Oscillator Block with:
  - x4 PLL with external sources
  - Three crystal/resonator modes up to 20 MHz
  - Three external clock modes up to 20 MHz
- Fail-Safe Clock Monitor
- Oscillator Start-up Timer (OST):
  - Ensures stability of crystal oscillator sources
## TABLE 1: PIC18(L)FXXK83 FAMILY TYPES

<table>
<thead>
<tr>
<th>Device</th>
<th>Data Sheet Index</th>
<th>Program Flash Memory (KB)</th>
<th>Data EEPROM (B)</th>
<th>Data SRAM (bytes)</th>
<th>I/O Pins</th>
<th>12-bit ADC$^2$ (ch)</th>
<th>5-bit DAC</th>
<th>Comparator</th>
<th>8-bit (with HLT)/16-bit Timer</th>
<th>Window Watchdog Timer (WWDT)</th>
<th>Signal Measurement Timer (SMT)</th>
<th>CCP10-bit PWM</th>
<th>CWG</th>
<th>NCO</th>
<th>CLC</th>
<th>Zero-Cross Detect</th>
<th>Direct Memory Access (DMA)</th>
<th>Memory Access Partition</th>
<th>Vectored Interrupts</th>
<th>CAN</th>
<th>UART with Protocols</th>
<th>I2C/SPI</th>
<th>Peripheral Pin Select</th>
<th>Peripheral Module Disable</th>
<th>Debug$^1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC18(L)F25K83</td>
<td>(A)</td>
<td>32</td>
<td>1024</td>
<td>2048</td>
<td>25</td>
<td>24</td>
<td>2</td>
<td>3/3</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>4/4</td>
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<td>Y</td>
<td>Y</td>
<td>2</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>I</td>
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<tr>
<td>PIC18(L)F26K83</td>
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<td>64</td>
<td>1024</td>
<td>4096</td>
<td>25</td>
<td>24</td>
<td>2</td>
<td>3/3</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>4/4</td>
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<td>2</td>
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<td>Y</td>
<td>2</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>I</td>
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</tbody>
</table>

**Note 1:** I - Debugging integrated on chip.

**Data Sheet Index:**
A:DS40001943 PIC18(L)F25/26K83 Data Sheet, 28-Pin

**Note:** For other small form-factor package availability and marking information, visit [http://www.microchip.com/packaging](http://www.microchip.com/packaging) or contact your local sales office.
TABLE 2: PACKAGES

<table>
<thead>
<tr>
<th>Device</th>
<th>SPDIP</th>
<th>SOIC</th>
<th>SSOP</th>
<th>UQFN</th>
<th>QFN</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC18(L)F25K83</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>PIC18(L)F26K83</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
</tbody>
</table>

**Note 1:** Pin details are subject to change.

**Pin Diagrams**

28-pin SPDIP, SOIC, SSOP

28-pin QFN (6x6x0.9mm), UQFN (4x4x0.5mm)

**Note:** See Table 3 for location of all peripheral functions.

**Note 1:** See Table 3 for location of all peripheral functions.

2: It is recommended that the exposed bottom pad be connected to Vss, however it must not be the only Vss connection to the device.
## TABLE 3: 28-PIN ALLOCATION TABLE (PIC18(L)F25/26K83)

<table>
<thead>
<tr>
<th>V0</th>
<th>V1</th>
<th>V2</th>
<th>V3</th>
<th>V4</th>
<th>V5</th>
<th>V6</th>
<th>V7</th>
<th>V8</th>
<th>V9</th>
<th>V10</th>
<th>V11</th>
<th>V12</th>
<th>V13</th>
<th>V14</th>
</tr>
</thead>
<tbody>
<tr>
<td>28-Pin SPDIP/SOIC/SSOP</td>
<td>28-Pin (U)QFN</td>
<td>28-Pin SPDIP/SOIC/SSOP</td>
<td>28-Pin (U)QFN</td>
<td>28-Pin SPDIP/SOIC/SSOP</td>
<td>28-Pin (U)QFN</td>
<td>28-Pin SPDIP/SOIC/SSOP</td>
<td>28-Pin (U)QFN</td>
<td>28-Pin SPDIP/SOIC/SSOP</td>
<td>28-Pin (U)QFN</td>
<td>28-Pin SPDIP/SOIC/SSOP</td>
<td>28-Pin (U)QFN</td>
<td>28-Pin SPDIP/SOIC/SSOP</td>
<td>28-Pin (U)QFN</td>
<td>28-Pin SPDIP/SOIC/SSOP</td>
</tr>
<tr>
<td>ADC</td>
<td>DAC</td>
<td>Comparators</td>
<td>Zero Cross Detect</td>
<td>P/C</td>
<td>SPI</td>
<td>UART</td>
<td>DSM</td>
<td>Timer/SMT</td>
<td>CCP and PWM</td>
<td>CWG</td>
<td>QC</td>
<td>MCO</td>
<td>Clock Reference (CLKR)</td>
<td>ECAN</td>
</tr>
<tr>
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</tr>
<tr>
<td>RA0</td>
<td>2</td>
<td>27</td>
<td>ANA0</td>
<td>—</td>
<td>—</td>
<td>C1IN0-</td>
<td>C2IN0-</td>
<td>—</td>
<td>—</td>
<td>—</td>
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</tr>
<tr>
<td>RA1</td>
<td>3</td>
<td>28</td>
<td>ANA1</td>
<td>—</td>
<td>—</td>
<td>C1IN1-</td>
<td>C2IN1-</td>
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</tr>
<tr>
<td>RA2</td>
<td>4</td>
<td>1</td>
<td>ANA2</td>
<td>VIN+</td>
<td>DAC1OUT1</td>
<td>C1IN0+</td>
<td>C2IN0+</td>
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<tr>
<td>RA3</td>
<td>5</td>
<td>2</td>
<td>ANA3</td>
<td>VIN+</td>
<td>C1IN1+</td>
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<td>MD1CAR1(1)</td>
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<tr>
<td>RA4</td>
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<td>3</td>
<td>ANA4</td>
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<td>MD1CAR2(1)</td>
<td>T0CKI(1)</td>
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<tr>
<td>RA5</td>
<td>7</td>
<td>4</td>
<td>ANA5</td>
<td>—</td>
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<td>—</td>
<td>—</td>
<td>SS1(1,3)</td>
<td>MD1SRC(1)</td>
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<tr>
<td>RA6</td>
<td>10</td>
<td>7</td>
<td>ANA6</td>
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<td>RA7</td>
<td>9</td>
<td>6</td>
<td>ANA7</td>
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</tr>
<tr>
<td>RB0</td>
<td>21</td>
<td>18</td>
<td>ANB0</td>
<td>—</td>
<td>—</td>
<td>C2IN1+</td>
<td>ZCD</td>
<td>—</td>
<td>—</td>
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<td>—</td>
<td>—</td>
<td>CCP4(1)</td>
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<tr>
<td>RB1</td>
<td>22</td>
<td>19</td>
<td>ANB1</td>
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<td>—</td>
<td>C1IN3-</td>
<td>C2IN3-</td>
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<td>CWG2(1)</td>
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<td>20</td>
<td>ANB2</td>
<td>—</td>
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<td>SDA2(1,3,4)</td>
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<td>CWG3(1)</td>
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<td>RB3</td>
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<td>21</td>
<td>ANB3</td>
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<td>C1IN2-</td>
<td>C2IN2-</td>
<td>—</td>
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<tr>
<td>RB4</td>
<td>25</td>
<td>22</td>
<td>ANB4</td>
<td>ADACT(1)</td>
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<td>T5G(1)</td>
<td>SMT2WIN(1)</td>
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<td>26</td>
<td>23</td>
<td>ANB5</td>
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<td>—</td>
<td>CCP2(1)</td>
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<td>RB6</td>
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<td>24</td>
<td>ANB6</td>
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<td>RC0</td>
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<td>8</td>
<td>ANC0</td>
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</tr>
<tr>
<td>RC1</td>
<td>12</td>
<td>9</td>
<td>ANC1</td>
<td>—</td>
<td>—</td>
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<td>—</td>
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<td>RC2</td>
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<td>ANC2</td>
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</tr>
</tbody>
</table>

**Note:**
1. This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2. All output signals shown in this row are PPS remappable.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins can be configured for P/C and SMBTM 3.0/2.0 logic levels; the SCLx/SDAx signals may be assigned to any of the RB1/RB0/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected by the INLV register, instead of the P/C specific or SMBUS input buffer thresholds.
### TABLE 3: 28-PIN ALLOCATION TABLE (PIC18(L)F25/26K83) (CONTINUED)

<table>
<thead>
<tr>
<th>I/O</th>
<th>28-Pin SMDIP/SOIC/SSOP</th>
<th>28-Pin UQFN</th>
<th>ADC</th>
<th>DAC</th>
<th>Comparators</th>
<th>Zero Cross Detect</th>
<th>I2C</th>
<th>SPI</th>
<th>UART</th>
<th>DSM</th>
<th>Time of SMT</th>
<th>CCP and PWM</th>
<th>CAN</th>
<th>CLC</th>
<th>NCO</th>
<th>CLC Reference (CLKR)</th>
<th>Interrupt-on Change</th>
<th>Basic</th>
</tr>
</thead>
<tbody>
<tr>
<td>RC4</td>
<td>15</td>
<td>12</td>
<td>ANC4</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SDA1&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>SDA1&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>—</td>
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<td>—</td>
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<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>RC5</td>
<td>16</td>
<td>13</td>
<td>ANC5</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SDA1&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>SDA1&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>—</td>
<td>—</td>
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<td>—</td>
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</tr>
<tr>
<td>RC6</td>
<td>17</td>
<td>14</td>
<td>ANC6</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CTS&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>—</td>
<td>—</td>
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</tr>
<tr>
<td>RC7</td>
<td>18</td>
<td>15</td>
<td>ANC7</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>RX1&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>—</td>
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</tr>
<tr>
<td>RE3</td>
<td>1</td>
<td>26</td>
<td>—</td>
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<tr>
<td>Vcc</td>
<td>20</td>
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<td>—</td>
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<tr>
<td>Vss</td>
<td>8, 19</td>
<td>5, 16</td>
<td>—</td>
<td>—</td>
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<td>—</td>
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<td>—</td>
</tr>
<tr>
<td>OUT&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>—</td>
<td>28-Pin SPDIP/SOIC/SSOP</td>
<td>ADGRDA</td>
<td>ADGRDB</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>C1OUT</td>
<td>C2OUT</td>
<td>SDA1</td>
<td>SCL1</td>
<td>SDA2</td>
<td>SCL2</td>
<td>SS1</td>
<td>SCK1</td>
<td>SDO1</td>
<td>DTR1</td>
<td>RTS1</td>
</tr>
</tbody>
</table>

**Note:**
1. This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2. All output signals shown in this row are PPS remappable.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins can be configured for I2C and SMBTIM 3.0/2.0 logic levels; the SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I2C specific or SMBUS input buffer thresholds.
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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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1.0 DEVICE OVERVIEW

This document contains device specific information for the following devices:

- PIC18F25K83
- PIC18LF25K83
- PIC18F26K83
- PIC18LF26K83

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance Program Flash Memory, Universal Asynchronous Receiver Transmitter (UART), Serial Peripheral Interface (SPI), Inter-integrated Circuit (I²C), Direct Memory Access (DMA), Configurable Logic Cells (CLC), Signal Measurement Timer (SMT), Numerically Controlled Oscillator (NCO), and Analog-to-Digital Converter with Computation (ADC²).

1.1 New Features

- **Direct Memory Access Controller:** The Direct Memory Access (DMA) Controller is designed to service data transfers between different memory regions directly without intervention from the CPU. By eliminating the need for CPU-intensive management of handling interrupts intended for data transfers, the CPU now can spend more time on other tasks.

- **Vectored Interrupt Controller:** The Vectored Interrupt Controller module reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the CPU. It assembles all of the interrupt request signals and resolves the interrupts based on both a fixed natural order priority and a user-assigned priority, thereby eliminating scanning of interrupt sources.

- **Universal Asynchronous Receiver Transmitter:** The Universal Asynchronous Receiver Transmitter (UART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer, independent of device program execution. The UART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or one of several automated protocols. Full-Duplex mode is useful for communications with peripheral systems, with DMA/DALI/LIN support.

- **Serial Peripheral Interface:** The Serial Peripheral Interface (SPI) module is a synchronous serial data communication bus that operates in Full-Duplex mode. Devices communicate in a master/slave environment where the master device initiates the communication. A slave device is controlled through a Chip Select known as Slave Select. Example slave devices include serial EEPROMs, shift registers, display drivers, A/D converters, or another PIC.

- **I²C Module:** The I²C module provides a synchronous interface between the microcontroller and other I²C-compatible devices using the two-wire I²C serial bus. Devices communicate in a master/slave environment. The I²C bus specifies two signal connections – Serial Clock (SCL) and Serial Data (SDA). Both the SCL and SDA connections are bidirectional open-drain lines, each requiring pull-up resistors to the supply voltage.

- **12-bit A/D Converter with Computation:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduce code overhead. It has a new module called ADC² with computation features, which provides a digital filter and threshold interrupt functions.

1.2 Details on Individual Family Members

Devices in the PIC18(L)F25/26K83 family are available in 28-pin packages. The block diagram for this device is shown in Figure 3-1.

The similarities and differences among the devices are listed in the PIC18(L)F25/26K83 Family Types Table (page 4). The pinouts for all devices are listed in Table 3.
### TABLE 1-1: DEVICE FEATURES

<table>
<thead>
<tr>
<th>Features</th>
<th>PIC18(L)F25K83</th>
<th>PIC18(L)F26K83</th>
</tr>
</thead>
<tbody>
<tr>
<td>Program Memory (Bytes)</td>
<td>32768</td>
<td>65536</td>
</tr>
<tr>
<td>Program Memory (Instructions)</td>
<td>16384</td>
<td>32768</td>
</tr>
<tr>
<td>Data Memory (Bytes)</td>
<td>2048</td>
<td>4096</td>
</tr>
<tr>
<td>Data EEPROM Memory (Bytes)</td>
<td>1024</td>
<td>1024</td>
</tr>
<tr>
<td>Packages</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28-pin SPDIP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28-pin SOIC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28-pin SSOP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28-pin QFN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28-pin UQFN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I/O Ports</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A,B,C,E(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12-Bit Analog-to-Digital Conversion Module (ADC^2) with Computation Accelerator</td>
<td>5 internal</td>
<td>5 internal</td>
</tr>
<tr>
<td>Capture/Compare/PWM Modules (CCP)</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>10-Bit Pulse-Width Modulator (PWM)</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>Timers (16-/8-bit)</td>
<td>4/3</td>
<td></td>
</tr>
<tr>
<td>Serial Communications</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 UARTs with DMX/DALI/LIN, 2 I^2C, 1 SPI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Complementary Waveform Generator (CWG)</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Zero-Cross Detect (ZCD)</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Data Signal Modulator (DSM)</td>
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</tr>
<tr>
<td>Signal Measurement Timer (SMT)</td>
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<tr>
<td>5-bit Digital to Analog Converter (DAC)</td>
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<tr>
<td>Numerically Controlled Oscillator (NCO)</td>
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<td></td>
</tr>
<tr>
<td>Comparator Module</td>
<td>2</td>
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<tr>
<td>Direct Memory Access (DMA)</td>
<td>2</td>
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<tr>
<td>Configurable Logic Cell (CLC)</td>
<td>4</td>
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</tr>
<tr>
<td>Control Area Network (CAN)</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Peripheral Module Disable (PMD)</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>16-bit CRC with Scanner</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Programmable High/Low-Voltage Detect (HLVD)</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Resets (and Delays)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>POR, Programmable BOR, RESET Instruction, Stack Overflow, Stack Underflow (PWRT, OST), MCLR, WDT, MEMV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Instruction Set</td>
<td></td>
<td></td>
</tr>
<tr>
<td>81 Instructions; 87 with Extended Instruction Set enabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Operating Frequency</td>
<td>64 MHz</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** PORTE contains the single RE3 input-only pin.
1.3 Register and Bit naming conventions

1.3.1 REGISTER NAMES

When there are multiple instances of the same peripheral in a device, the peripheral control registers will be depicted as the concatenation of a peripheral identifier, peripheral instance, and control identifier. The control registers section will show just one instance of all the register names with an ‘x’ in the place of the peripheral instance number. This naming convention may also be applied to peripherals when there is only one instance of that peripheral in the device to maintain compatibility with other devices in the family that contain more than one.

1.3.2 BIT NAMES

There are two variants for bit names:
- Short name: Bit function abbreviation
- Long name: Peripheral abbreviation + short name

1.3.2.1 Short Bit Names

Short bit names are an abbreviation for the bit function. For example, some peripherals are enabled with the EN bit. The bit names shown in the registers are the short name variant.

Short bit names are useful when accessing bits in C programs. The general format for accessing bits by the short name is RegisterName.bits.ShortName. For example, the enable bit, EN, in the T0CON0 register can be set in C programs with the instruction T0CON0bits.EN = 1.

Short names are generally not useful in assembly programs because the same name may be used by different peripherals in different bit positions. When this occurs, during the include file generation, all instances of that short bit name are appended with an underscore plus the name of the register in which the bit resides to avoid naming contentions.

1.3.2.2 Long Bit Names

Long bit names are constructed by adding a peripheral abbreviation prefix to the short name. The prefix is unique to the peripheral thereby making every long bit name unique. The long bit name for the Timer0 enable bit is the Timer0 prefix, T0, appended with the enable bit short name, EN, resulting in the unique bit name T0EN.

Long bit names are useful in both C and assembly programs. For example, in C the T0CON0 enable bit can be set with the T0EN = 1 instruction. In assembly, this bit can be set with the BSF T0CON0,T0EN instruction.

1.3.3 REGISTER AND BIT NAMING EXCEPTIONS

1.3.3.1 Status, Interrupt, and Mirror Bits

Status, interrupt enables, interrupt flags, and mirror bits are contained in registers that span more than one peripheral. In these cases, the bit name shown is unique so there is no prefix or short name variant.

1.3.3.2 Bit Fields

Bit fields are two or more adjacent bits in the same register. For example, the four Least Significant bits of the T0CON0 register contain the output prescaler select bits. The short name for this field is OUTPS and the long name is T0OUTPS. Bit field access is only possible in C programs. The following example demonstrates a C program instruction for setting the Timer0 output prescaler to 1:6 Postscaler:

T0CON0bits.OUTPS = 0x5;

Individual bits in a bit field can also be accessed with long and short bit names. Each bit is the field name appended with the number of the bit position within the field. For example, the Most Significant mode bit has the short bit name OUTPS3. The following two examples demonstrate assembly program sequences for setting the Timer0 output prescaler to 1:6 Postscaler:

Example 1:

MOVLW ~((1<<OUTPS3 | 1<<OUTPS1)
ANDWF T0CON0,F
MOVLW 1<<OUTPS2 | 1<<OUTPS0
IORWF T0CON0,F

Example 2:

BCF T0CON0,OUTPS3
BSF T0CON0,OUTPS2
BCF T0CON0,OUTPS1
BSF T0CON0,OUTPS0

1.3.3 REGISTER AND BIT NAMING EXCEPTIONS

1.3.3.1 Status, Interrupt, and Mirror Bits

Status, interrupt enables, interrupt flags, and mirror bits are contained in registers that span more than one peripheral. In these cases, the bit name shown is unique so there is no prefix or short name variant.
2.0 GUIDELINES FOR GETTING STARTED WITH PIC18(L)F25/26K83 MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC18(L)F25/26K83 family of 8-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

• All VDD and VSS pins (see Section 2.2 “Power Supply Pins”)
• MCLR pin (see Section 2.3 “Master Clear (MCLR) Pin”)

These pins must also be connected if they are being used in the end application:

• ICSPCLK/ICSPDAT pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see Section 2.4 “ICSP™ Pins”)
• OSCI and OSCO pins when an external oscillator source is used (see Section 2.5 “External Oscillator Pins”)

Additionally, the following pins may be required:

• VREF+/VREF- pins are used when external voltage reference for analog modules is implemented

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS

2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins (VDD and VSS) is required.

Consider the following criteria when using decoupling capacitors:

• **Value and type of capacitor:** A 0.1 μF (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
• **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
• **Handling high-frequency noise:** If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 μF in parallel with 0.001 μF).
• **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including microcontrollers, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μF to 47 μF.
2.3 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions: Device Reset, and Device Programming and Debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application’s resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the MCLR pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the MCLR pin should be placed within 0.25 inch (6 mm) of the pin.

2.4 ICSP™ Pins

The ICSPCLK and ICSPDAT pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the ICSPCLK and ICSPDAT pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin input voltage high (Vih) and input low (Vil) requirements.

For device emulation, ensure that the “Communication Channel Select” (i.e., ICSPCLK/ICSPDAT pins), programmed into the device, matches the physical connections for the ICSP to the Microchip debugger/emulator tool.

For more information on available Microchip development tools connection requirements, refer to Section 44.0 “Development Support”.

Note 1: R1 ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin VIH and VIL specifications are met.

Note 2: R2 ≤ 470Ω will limit any current flowing into MCLR from the external capacitor, C1, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met.
2.5 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to Section 7.0 “Oscillator Module (with Fail-Safe Clock Monitor)” for details).

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 2-3. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

In planning the application’s routing and I/O assignments, ensure that adjacent port pins, and other signals in close proximity to the oscillator, are benign (i.e., free of high frequencies, short rise and fall times, and other similar noise).

For additional information and design guidance on oscillator circuits, refer to these Microchip Application Notes, available at the corporate website (www.microchip.com):
- AN826, “Crystal Oscillator Basics and Crystal Selection for rPIC™ and PICmicro® Devices”
- AN849, “Basic PICmicro® Oscillator Design”
- AN943, “Practical PICmicro® Oscillator Analysis and Design”
- AN949, “Making Your Oscillator Work”

2.6 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to Vss on unused pins and drive the output to logic low.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT
3.0 PIC18 CPU

This family of devices contains a PIC18 8-bit CPU core based on the modified Harvard architecture. The PIC18 CPU supports:

- System Arbitration which decides memory access allocation depending on user priorities
- Vectored Interrupt capability with automatic two level deep context saving
- 31-level deep hardware stack with overflow and underflow reset capabilities
- Support Direct, Indirect, and Relative Addressing modes
- 8x8 Hardware Multiplier
**FIGURE 3-1: PIC18(L)F25/26K83 FAMILY BLOCK DIAGRAM**

![Block Diagram of PIC18(L)F25/26K83 Family](image)

**Note 1:** RE3 is only available when MCLR functionality is disabled.

**Note 2:** OSC1/CLKIN and OSC2/CLKOUT are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to Section 7.0 “Oscillator Module (with Fail-Safe Clock Monitor)” for additional information.
3.1 System Arbitration

The System Arbiter resolves memory access between the System Level Selections (i.e., Main, Interrupt Service Routine) and Peripheral Selection (i.e., DMA and Scanner) based on user-assigned priorities. Each of the system level and peripheral selections has its own priority selection registers. Memory access priority is resolved using the number written to the corresponding Priority registers, 0 being the highest priority and 4 the lowest. The default priorities are listed in Table 3-1.

In case the user wants to change priorities, ensure each Priority register is written with a unique value from 0 to 4.

<table>
<thead>
<tr>
<th>Selection</th>
<th>Priority register</th>
<th>Reset value</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Level</td>
<td>ISR</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>MAIN</td>
<td>1</td>
</tr>
<tr>
<td>Peripheral</td>
<td>DMA1</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>DMA2</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>SCANNER</td>
<td>4</td>
</tr>
</tbody>
</table>
3.1.1 PRIORITY LOCK

The System arbiter grants memory access to the peripheral selections (DMAx, Scanner) when the PRLOCKED bit (PRLOCK Register) is set.

Priority selections are locked by setting the PRLOCKED bit of the PRLOCK register. Setting and clearing this bit requires a special sequence as an extra precaution against inadvertent changes. Examples of setting and clearing the PRLOCKED bit are shown in Example 3-1 and Example 3-2.

EXAMPLE 3-1: PRIORITY LOCK SEQUENCE

```assembly
; Disable interrupts
BCF INTCON0,GIE

; Bank to PRLOCK register
BANKSEL PRLOCK
MOVLW 55h

; Required sequence, next 4 instructions
MOVWF PRLOCK
MOVLW AAh
MOVWF PRLOCK
; Set PRLOCKED bit to grant memory access to peripherals
BSF PRLOCK,0

; Enable Interrupts
BSF INTCON0,GIE
```

EXAMPLE 3-2: PRIORITY UNLOCK SEQUENCE

```assembly
; Disable interrupts
BCF INTCON0,GIE

; Bank to PRLOCK register
BANKSEL PRLOCK
MOVLW 55h

; Required sequence, next 4 instructions
MOVWF PRLOCK
MOVLW AAh
MOVWF PRLOCK
; Clear PRLOCKED bit to allow changing priority settings
BCF PRLOCK,0

; Enable Interrupts
BSF INTCON0,GIE
```

3.2 Memory Access Scheme

The user can assign priorities to both system level and peripheral selections based on which the system arbiter grants memory access. Let us consider the following priority scenarios between ISR, MAIN, and Peripherals.

**Note:** It is always required that the ISR priority be higher than Main priority.

3.2.1 ISR PRIORITY > MAIN PRIORITY > PERIPHERAL PRIORITY

When the Peripheral Priority (DMAx, Scanner) is lower than ISR and MAIN Priority, and the peripheral requires:

1. Access to the Program Flash Memory, then the peripheral waits for an instruction cycle in which the CPU does not need to access the PFM (such as a branch instruction) and uses that cycle to do its own Program Flash Memory access, unless a PFM Read/Write operation is in progress.
2. Access to the SFR/GPR, then the peripheral waits for an instruction cycle in which the CPU does not need to access the SFR/GPR (such as MOVlw, CALL, NOP) and uses that cycle to do its own SFR/GPR access.
3. Access to the Data EEPROM, then the peripheral has access to Data EEPROM unless a Data EEPROM Read/Write operation is being performed.

This results in the lowest throughput for the peripheral to access the memory, and does so without any impact on execution times.

3.2.2 PERIPHERAL PRIORITY > ISR PRIORITY > MAIN PRIORITY

When the Peripheral Priority (DMAx, Scanner) is higher than ISR and MAIN Priority, the CPU operation is stalled when the peripheral requests memory.

The CPU is held in its current state until the peripheral completes its operation. Since the peripheral requests access to the bus, the peripheral cannot be disabled until it completes its operation.

This results in the highest throughput for the peripheral to access the memory, but has the cost of stalling other execution while it occurs.
3.2.3  ISR PRIORITY > PERIPHERAL
       PRIORITY > MAIN PRIORITY

In this case, interrupt routines and peripheral operation
(DMAx, Scanner) will stall the CPU. Interrupt will
preempt peripheral operation. This results in lowest
interrupt latency and highest throughput for the
peripheral to access the memory.

3.2.4  PERIPHERAL 1 PRIORITY > ISR
       PRIORITY > MAIN PRIORITY >
       PERIPHERAL 2 PRIORITY

In this case, the Peripheral 1 will stall the execution of
the CPU. However, Peripheral 2 can access the
memory in cycles unused by Peripheral 1.

The operation of the System Arbiter is controlled
through the following registers:

REGISTER 3-1:  ISRPR: INTERRUPT SERVICE ROUTINE PRIORITY REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 0</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-0/0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit
u = Bit is unchanged
1 = bit is set
0 = bit is cleared
U = Unimplemented bit, read as ‘0’
W = Writable bit
x = Bit is unknown
-n/n = Value at POR and BOR/Value at all other Resets
HS = Hardware set

bit 7-3  Unimplemented: Read as ‘0’
bit 2-0  ISRPR<2:0>: Interrupt Service Routine Priority Selection bits

REGISTER 3-2:  MAINPR: MAIN ROUTINE PRIORITY REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 0</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>R/W-0/0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>R/W-1/1</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit
u = Bit is unchanged
1 = bit is set
0 = bit is cleared
U = Unimplemented bit, read as ‘0’
W = Writable bit
x = Bit is unknown
-n/n = Value at POR and BOR/Value at all other Resets
HS = Hardware set

bit 7-3  Unimplemented: Read as ‘0’
bit 2-0  MAINPR<2:0>: Main Routine Priority Selection bits

REGISTER 3-3:  DMA1PR: DMA1 PRIORITY REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 0</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>R/W-1/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>R/W-0/0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit
u = Bit is unchanged
1 = bit is set
0 = bit is cleared
U = Unimplemented bit, read as ‘0’
W = Writable bit
x = Bit is unknown
-n/n = Value at POR and BOR/Value at all other Resets
HS = Hardware set

bit 7-3  Unimplemented: Read as ‘0’
bit 2-0  DMA1PR<2:0>: DMA1 Priority Selection bits
### REGISTER 3-4: DMA2PR: DMA2 PRIORITY REGISTER

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th>R/W-0/0</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>DMA2PR&lt;2:0&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **x** = Bit is unknown
- **1** = bit is set
- **0** = bit is cleared
- **U** = Unimplemented bit, read as ‘0’
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **HS** = Hardware set

#### bit 7-3
- **Unimplemented**: Read as ‘0’

#### bit 2-0
- **DMA2PR<2:0>**: DMA2 Priority Selection bits

### REGISTER 3-5: SCANPR: SCANNER PRIORITY REGISTER

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th>R/W-1/1</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>SCANPR&lt;2:0&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **x** = Bit is unknown
- **1** = bit is set
- **0** = bit is cleared
- **U** = Unimplemented bit, read as ‘0’
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **HS** = Hardware set

#### bit 7-3
- **Unimplemented**: Read as ‘0’

#### bit 2-0
- **SCANPR<2:0>**: Scanner Priority Selection bits

### REGISTER 3-6: PRLOCK: PRIORITY LOCK REGISTER

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>PRLOCKED</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
<td>bit 0</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **x** = Bit is unknown
- **1** = bit is set
- **0** = bit is cleared
- **U** = Unimplemented bit, read as ‘0’
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **HS** = Hardware set

#### bit 7-1
- **Unimplemented**: Read as ‘0’

#### bit 0
- **PRLOCKED**: PR Register Lock bit\(^{(1, 2)}\)
  - 0 = Priority Registers can be modified by write operations; Peripherals do not have access to the memory
  - 1 = Priority Registers are locked and cannot be written; Peripherals do not have access to the memory

**Note 1:** The PRLOCKED bit can only be set or cleared after the unlock sequence.

**2:** If PR1WAY = 1, the PRLOCKED bit cannot be cleared after it has been set. A system Reset will clear the bit and allow one more set.
### TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH CPU

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISRPR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ISPR2</td>
<td>ISPR1</td>
<td>ISPR0</td>
</tr>
<tr>
<td>MAINPR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>MAINPR2</td>
<td>MAINPR1</td>
<td>MAINPR0</td>
</tr>
<tr>
<td>DMA1PR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DMA1PR2</td>
<td>DMA1PR1</td>
<td>DMA1PR0</td>
</tr>
<tr>
<td>DMA2PR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DMA2PR2</td>
<td>DMA2PR1</td>
<td>DMA2PR0</td>
</tr>
<tr>
<td>SCANPR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SCANPR2</td>
<td>SCANPR1</td>
<td>SCANPR0</td>
</tr>
<tr>
<td>PRLOCK</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>PRLOCKED</td>
</tr>
</tbody>
</table>

Legend: — = Unimplemented location, read as '0'.
4.0 MEMORY ORGANIZATION

There are three types of memory in PIC18 enhanced microcontroller devices:

- Program Flash Memory
- Data RAM
- Data EEPROM

The Program Memory Flash and data RAM share the same bus, while data EEPROM uses a separate bus. This allows for concurrent access of the memory spaces.

Additional detailed information on the operation of the Program Flash Memory and Data EEPROM Memory is provided in Section 13.0 “Nonvolatile Memory (NVM) Control”.

4.1 Program Flash Memory Organization

PIC18 microcontrollers implement a 21-bit Program Counter, which is capable of addressing a 2 Mbyte program memory space. Accessing any unimplemented memory will return all '0's (a NOP instruction).

These devices contains the following:

- PIC18(L)F25K83: 32 Kbytes of Flash memory, up to 16,384 single-word instructions
- PIC18(L)F26K83: 64 Kbytes of Flash memory, up to 32,768 single-word instructions

The Reset vector for the device is at address 000000h. PIC18(L)F25/26K83 devices feature a vectored interrupt controller with a dedicated interrupt vector table in the program memory, see Section 9.0 “Interrupt Controller”.

Note: For memory information on this family of devices, see Table 4-1 and Table 4-3.

4.2 Memory Access Partition (MAP)

Program Flash Memory is partitioned into:

- Application Block
- Boot Block, and
- Storage Area Flash (SAF) Block

4.2.1 APPLICATION BLOCK

Application Block is where the user's program resides by default. Default settings of the Configuration bits (BBEN = 1 and SAFEN = 1) assign all memory in the Program Flash Memory area to the Application Block. The WRTAPP Configuration bit is used to protect the Application Block.

4.2.2 BOOT BLOCK

Boot Block is an area in program memory that is ideal for storing bootloader code. Code placed in this area can be executed by the CPU. The Boot Block can be write-protected, independent of the main Application Block. The Boot Block is enabled by the BBEN bit and size is based on the value of the BBSIZE bits of Configuration word (Register 5-7), see Table 5-1 for Boot Block sizes.

The WRTB Configuration bit is used to write-protect the Boot Block.

4.2.3 STORAGE AREA FLASH

Storage Area Flash (SAF) is the area in program memory that can be used as data storage. SAF is enabled by the SAFEN bit of the Configuration word in Register 5-7. If enabled, the code placed in this area cannot be executed by the CPU. The SAF block is placed at the end of memory and spans 256 bytes. The WRTSAF Configuration bit is used to write-protect the Storage Area Flash.

Note: If write-protected locations are written from NVMCON registers, memory is not changed and the WRERR bit defined in Register 13-1 is set.
### PIC18(L)F25/26K83

#### TABLE 4-1: PROGRAM AND DATA EEPROM MEMORY MAP

<table>
<thead>
<tr>
<th>Address</th>
<th>PIC18(L)F25K83</th>
<th>PIC18(L)F26K83</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 0000h</td>
<td>Reset Vector</td>
<td>Reset Vector</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>00 0008h</td>
<td>Interrupt Vector High&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>Interrupt Vector High&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>00 0018h</td>
<td>Interrupt Vector Low&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>Interrupt Vector Low&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
<tr>
<td>00 001Ah</td>
<td>Program Flash Memory (16 KW)&lt;sup&gt;(3)&lt;/sup&gt;</td>
<td>Program Flash Memory (32 KW)&lt;sup&gt;(3)&lt;/sup&gt;</td>
</tr>
<tr>
<td>00 7FFFh</td>
<td></td>
<td></td>
</tr>
<tr>
<td>00 8000h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>00 FFFFh</td>
<td>Not present&lt;sup&gt;(4)&lt;/sup&gt;</td>
<td>Not present&lt;sup&gt;(4)&lt;/sup&gt;</td>
</tr>
<tr>
<td>01 0000h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1F FFFFh</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20 0000h</td>
<td>User IDs (8 Words)&lt;sup&gt;(5)&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>20 000fh</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20 0100h</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>2F FFFFh</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30 0000h</td>
<td>Configuration Words (5 Words)&lt;sup&gt;(6)&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>30 0009h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30 000Ah</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>30 FFFFh</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31 0000h</td>
<td>Data EEPROM (1024 Bytes)</td>
<td></td>
</tr>
<tr>
<td>31 00FFh</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31 0100h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31 03FFh</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31 0400h</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>3E FFFFh</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3F 0000h</td>
<td>Device Information Area&lt;sup&gt;(5),(7)&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>3F 003Fh</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3F 0040h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3F FEFFh</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>3F F00h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3F F09h</td>
<td>Device Configuration Information (5 Words)&lt;sup&gt;(5),(6),(7)&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>3F F0Ah</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3F FFBh</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>3F FFCch</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3F FFDh</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3F FFEh</td>
<td>Device ID (1 Word)&lt;sup&gt;(5),(6),(7)&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>3F FFFFh</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** The stack is a separate SRAM panel, apart from all user memory panels.

**Note 2:** 00 0008h location is used as the reset default for the IVTBASE register, the vector table can be relocated in the memory by programming the IVTBASE register.

**Note 3:** Storage Area Flash is implemented as the last 128 Words of User Flash, if present.

**Note 4:** The addresses do not roll over. The region is read as '0'.

**Note 5:** Not code-protected.

**Note 6:** Hard-coded in silicon.

**Note 7:** This region cannot be written by the user and it is not affected by a Bulk Erase.
### TABLE 4-2: PROGRAM FLASH MEMORY PARTITION

<table>
<thead>
<tr>
<th>Region</th>
<th>Address</th>
<th>Partition(3)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>BBEN = 1 SAFEN = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BBEN = 1 SAFEN = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BBEN = 0 SAFEN = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BBEN = 0 SAFEN = 0</td>
</tr>
<tr>
<td>Program Flash Memory</td>
<td>00 0000h</td>
<td>BOOT BLOCK</td>
</tr>
<tr>
<td></td>
<td>• • •</td>
<td>APPLICATION BLOCK</td>
</tr>
<tr>
<td></td>
<td>Last Boot Block Memory Address</td>
<td>APPLICATION BLOCK</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BOOT BLOCK</td>
</tr>
<tr>
<td></td>
<td>Last Boot Block Memory Address</td>
<td>APPLICATION BLOCK</td>
</tr>
<tr>
<td></td>
<td>+ 1</td>
<td>APPLICATION BLOCK</td>
</tr>
<tr>
<td></td>
<td>• • •</td>
<td>APPLICATION BLOCK</td>
</tr>
<tr>
<td></td>
<td>Last Program Memory Address(2)</td>
<td>STORAGE AREA FLASH</td>
</tr>
<tr>
<td></td>
<td>100h</td>
<td>STORAGE AREA FLASH</td>
</tr>
<tr>
<td></td>
<td>• • •</td>
<td>STORAGE AREA FLASH</td>
</tr>
<tr>
<td></td>
<td>Last Program Memory Address(2)</td>
<td>STORAGE AREA FLASH</td>
</tr>
<tr>
<td></td>
<td>100h</td>
<td>STORAGE AREA FLASH</td>
</tr>
</tbody>
</table>

**Note 1:** Last Boot Block Memory Address is based on BBSIZE<2:0>, see Table 5-1.
**Note 2:** For Last Program Memory Address, see Table 5-1.
**Note 3:** Refer to Register 5-7: Configuration Word 4L for BBEN and SAFEN definitions.
**Note 4:** Storage Area Flash is implemented as the last 128 Words of User Flash, if present.
4.2.4 PROGRAM COUNTER

The Program Counter (PC) specifies the address of the instruction to fetch for execution. The PC is 21-bit wide and is contained in three separate 8-bit registers. The low byte, known as the PCL register, is both readable and writable. The high byte, or PCH register, contains the PC<15:8> bits; it is not directly readable or writable. Updates to the PCH register are performed through the PCLATH register. The upper byte is called PCU. This register contains the PC<20:16> bits; it is also not directly readable or writable. Updates to the PCU register are performed through the PCLATU register.

The contents of PCLATH and PCLATU are transferred to the Program Counter by any operation that writes PCL. Similarly, the upper two bytes of the Program Counter are transferred to PCLATH and PCLATU by any operation that reads PCL. This is useful for computed offsets to the PC (see Section 4.3.2.1 “Computed GOTO”).

The PC addresses bytes in the program memory. To prevent the PC from becoming misaligned with word instructions, the Least Significant bit of PCL is fixed to a value of ‘0’. The PC increments by two to address sequential instructions in the program memory.

The CALL, RCALL, GOTO and program branch instructions write to the Program Counter directly. For these instructions, the contents of PCLATH and PCLATU are not transferred to the Program Counter.

4.2.5 RETURN ADDRESS STACK

The return address stack allows any combination of up to 31 program calls and interrupts to occur. The PC is pushed onto the stack when a CALL or RCALL instruction is executed or an interrupt is acknowledged. The PC value is pulled off the stack on a RETURN, RETLW or a RETFIE instruction. PCLATU and PCLATH are not affected by any of the RETURN or CALL instructions.

The stack operates as a 31-word by 21-bit RAM and a 5-bit Stack Pointer. The stack space is not part of either program or data space. The Stack Pointer is readable and writable and the address on the top of the stack is readable and writable through the Top-of-Stack (TOS) Special File Registers. Data can also be pushed to, or popped from the stack, using these registers.

A CALL, CALLW or RCALL instruction causes a push onto the stack; the Stack Pointer is first incremented, and the location pointed to by the Stack Pointer is written with the contents of the PC (already pointing to the instruction following the CALL). A RETURN type instruction causes a pop from the stack; the contents of the location pointed to by the STKPTR are transferred to the PC and then the Stack Pointer is decremented.

The Stack Pointer is initialized to ‘00000’ after all Resets. There is no RAM associated with the location corresponding to a Stack Pointer value of ‘00000’; this is only a Reset value. Status bits in the PCON0 register indicate if the stack has overflowed or underflowed.

4.2.5.1 Top-of-Stack Access

Only the top of the return address stack (TOS) is readable and writable. A set of three registers, TOSU:TOSH:TOSL, holds the contents of the stack location pointed to by the STKPTR register (Figure 4-1). This allows users to implement a software stack, if necessary. After a CALL, RCALL or interrupt, the software can read the pushed value by reading the TOSU:TOSH:TOSL registers. These values can be placed on a user-defined software stack. At return time, the software can return these values to TOSU:TOSH:TOSL and do a return.

The user must disable the Global Interrupt Enable (GIE) bits while accessing the stack to prevent inadvertent stack corruption.
4.2.5.2 Return Stack Pointer (STKPTR)
The STKPTR register (Register 4-4) contains the Stack Pointer value. The STKOVF (Stack Overflow) Status bit and the STKUNF (Stack Underflow) Status bit can be accessed using the PCON0 register. The value of the Stack Pointer can be 0 through 31. On Reset, the Stack Pointer value will be zero. The user may read and write the Stack Pointer value. This feature can be used by a Real-Time Operating System (RTOS) for stack maintenance. After the PC is pushed onto the stack 32 times (without popping any values off the stack), the STKOVF bit is set. The STKOVF bit is cleared by software or by a POR. The action that takes place when the stack becomes full depends on the state of the STVREN (Stack Overflow Reset Enable) Configuration bit. (Refer to Section 5.1 “Configuration Words” for a description of the device Configuration bits.)

If STVREN is set (default) and the stack has been popped enough times to unload the stack, the next pop will return a value of zero to the PC, it will set the STKUNF bit and a Reset will be generated. This condition can be generated by the RETURN, RETLW and RETFIE instructions.

When STVREN = 0, STKUNF will be set but no Reset will occur.

---

**Note:** Returning a value of zero to the PC on an underflow has the effect of vectoring the program to the Reset vector, where the stack conditions can be verified and appropriate actions can be taken. This is not the same as a Reset, as the contents of the SFRs are not affected.

4.2.5.3 PUSH and POP Instructions
Since the Top-of-Stack is readable and writable, the ability to push values onto the stack and pull values off the stack without disturbing normal program execution is a desirable feature. The PIC18 instruction set includes two instructions, PUSH and POP, that permit the TOS to be manipulated under software control. TOSU, TOSH and TOSL can be modified to place data or a return address on the stack.

The PUSH instruction places the current PC value onto the stack. This increments the Stack Pointer and loads the current PC value onto the stack.

The POP instruction discards the current TOS by decrementing the Stack Pointer. The previous value pushed onto the stack then becomes the TOS value.
### 4.3 Register Definitions: Stack Pointer

#### REGISTER 4-1: TOSU: TOP-OF-STACK UPPER BYTE

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TOS&lt;20:16&gt;</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented
- **C** = Clearable only bit
- **-n** = Value at POR
  - ‘1’ = Bit is set
  - ‘0’ = Bit is cleared
  - x = Bit is unknown

- **bit 7-5** Unimplemented: Read as ‘0’
- **bit 4-0** TOS<20:16>: Top-of-Stack Location bits

#### REGISTER 4-2: TOSH: TOP-OF-STACK HIGH BYTE

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TOS&lt;15:8&gt;</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented
- **C** = Clearable only bit
- **-n** = Value at POR
  - ‘1’ = Bit is set
  - ‘0’ = Bit is cleared
  - x = Bit is unknown

- **bit 7-0** TOS<15:8>: Top-of-Stack Location bits

#### REGISTER 4-3: TOSL: TOP-OF-STACK LOW BYTE

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TOS&lt;7:0&gt;</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented
- **C** = Clearable only bit
- **-n** = Value at POR
  - ‘1’ = Bit is set
  - ‘0’ = Bit is cleared
  - x = Bit is unknown

- **bit 7-0** TOS<7:0>: Top-of-Stack Location bits
4.3.1 FAST REGISTER STACK

There are three levels of fast stack registers available - one for CALL type instructions and two for interrupts. A fast register stack is provided for the Status, WREG and BSR registers, to provide a “fast return” option for interrupts. It is loaded with the current value of the corresponding register when the processor vectors for an interrupt. All interrupt sources will push values into the stack registers. The values in the registers are then loaded back into their associated registers if the RETFIE, FAST instruction is used to return from the interrupt. Refer to Section 4.5.6 “Call Shadow Register” for interrupt call shadow registers.

Example 4-1 shows a source code example that uses the fast register stack during a subroutine call and return.

**EXAMPLE 4-1: FAST REGISTER STACK CODE EXAMPLE**

```assembly
CALL SUB1, FAST ;STATUS, WREG, BSR ;SAVED IN FAST REGISTER ;STACK

SUB1

RETURN, FAST ;RESTORE VALUES SAVED ;IN FAST REGISTER STACK
```
4.3.2 LOOK-UP TABLES IN PROGRAM MEMORY

There may be programming situations that require the creation of data structures, or look-up tables, in program memory. For PIC18 devices, look-up tables can be implemented in two ways:

• Computed GOTO
• Table Reads

4.3.2.1 Computed GOTO

A computed GOTO is accomplished by adding an offset to the Program Counter. An example is shown in Example 4-2.

A look-up table can be formed with an ADDWF PCL instruction and a group of RETLW nn instructions. The W register is loaded with an offset into the table before executing a call to that table. The first instruction of the called routine is the ADDWF PCL instruction. The next instruction executed will be one of the RETLW nn instructions that returns the value 'nn' to the calling function.

The offset value (in WREG) specifies the number of bytes that the Program Counter should advance and should be multiples of two (LSb = 0).

In this method, only one data byte may be stored in each instruction location and room on the return address stack is required.

EXAMPLE 4-2: COMPUTED GOTO USING AN OFFSET VALUE

| MOVF OFFSET, W |
| CALL TABLE |
| ORG nn00h |
| TABLE ADDWF PCL |
| RETLW nnh |
| RETLW nnh |
| RETLW nnh |

4.3.2.2 Table Reads and Table Writes

A better method of storing data in program memory allows two bytes of data to be stored in each instruction location.

Look-up table data may be stored two bytes per program word by using table reads and writes. The Table Pointer (TBLPTR) register specifies the byte address and the Table Latch (TABLAT) register contains the data that is read from or written to program memory.

Table read and table write operations are discussed further in Section 13.1.1 “Table Reads and Table Writes”.
4.4 PIC18 Instruction Cycle

4.4.1 CLOCKING SCHEME

The microcontroller clock input, whether from an internal or external source, is internally divided by four to generate four quadrature clocks (Q1, Q2, Q3 and Q4). Internally, the Program Counter is incremented on every Q1; the instruction is fetched from the program memory and latched into the instruction register during Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 4-2.

4.4.2 INSTRUCTION FLOW/PIPELINING

An “Instruction Cycle” consists of four Q cycles: Q1 through Q4. The instruction fetch and execute are pipelined in such a manner that a fetch takes one instruction cycle, while the decode and execute take another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the Program Counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 4-3).

A fetch cycle begins with the Program Counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 4-2: CLOCK/INSTRUCTION CYCLE

Example 4-3: INSTRUCTION PIPELINE FLOW

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Tcy0</th>
<th>Tcy1</th>
<th>Tcy2</th>
<th>Tcy3</th>
<th>Tcy4</th>
<th>Tcy5</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. MOVLW 55h</td>
<td>Fetch 1</td>
<td>Execute 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2. MOVWF PORTB</td>
<td>Fetch 2</td>
<td>Execute 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3. BRA SUB_1</td>
<td>Fetch 3</td>
<td>Execute 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4. BSF PORTA, BIT3 (Forced NOP)</td>
<td>Fetch 4</td>
<td>Flush (NOP)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5. Instruction @ address SUB_1</td>
<td>Fetch SUB_1</td>
<td>Execute SUB_1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: There are some instructions that take multiple cycles to execute. Refer to Section 42.0 “Instruction Set Summary” for details.
4.4.3 INSTRUCTIONS IN PROGRAM MEMORY

The program memory is addressed in bytes. Instructions are stored as either two bytes or four bytes in program memory. The Least Significant Byte of an instruction word is always stored in a program memory location with an even address (LSb = 0). To maintain alignment with instruction boundaries, the PC increments in steps of two and the LSb will always read ‘0’ (see Section 4.2.4 “Program Counter”).

Figure 4-3 shows an example of how instruction words are stored in the program memory.

The CALL and GOTO instructions have the absolute program memory address embedded into the instruction. Since instructions are always stored on word boundaries, the data contained in the instruction is a word address. The word address is written to PC<20:1>, which accesses the desired byte address in program memory. Instruction #2 in Figure 4-3 shows how the instruction GOTO 0006h is encoded in the program memory. Program branch instructions, which encode a relative address offset, operate in the same manner. The offset value stored in a branch instruction represents the number of single-word instructions that the PC will be offset by. Section 42.0 “Instruction Set Summary” provides further details of the instruction set.

FIGURE 4-3: INSTRUCTIONS IN PROGRAM MEMORY

<table>
<thead>
<tr>
<th>Program Memory Byte Locations</th>
<th>LSB = 1</th>
<th>LSB = 0</th>
<th>Word Address</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Instruction 1: MOVLW 055h</td>
<td></td>
<td></td>
<td>0000000h</td>
</tr>
<tr>
<td>Instruction 2: GOTO 0006h</td>
<td>0Fh</td>
<td>55h</td>
<td>0000008h</td>
</tr>
<tr>
<td></td>
<td>EFh</td>
<td>03h</td>
<td>000000Ah</td>
</tr>
<tr>
<td></td>
<td>F0h</td>
<td>00h</td>
<td>000000Ch</td>
</tr>
<tr>
<td>Instruction 3: MOVFF 123h, 456h</td>
<td>C1h</td>
<td>23h</td>
<td>00000Eh</td>
</tr>
<tr>
<td>Instruction 4: MOVFFL 123h, 456h</td>
<td>F4h</td>
<td>56h</td>
<td>000010h</td>
</tr>
<tr>
<td></td>
<td>00h</td>
<td>60h</td>
<td>000012h</td>
</tr>
<tr>
<td></td>
<td>F4h</td>
<td>8Ch</td>
<td>000014h</td>
</tr>
<tr>
<td></td>
<td>F4h</td>
<td>56h</td>
<td>000016h</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000018h</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00001Ah</td>
</tr>
</tbody>
</table>

4.4.4 MULTI-WORD INSTRUCTIONS

The standard PIC18 instruction set has four two-word instructions: CALL, MOVFF, GOTO and LFSR and two three-word instructions: MOVFFL and MOVSFL. In all cases, the second and the third word of the instruction always has ‘1111’ as its four Most Significant bits; the other 12 bits are literal data, usually a data memory address.

The use of ‘1111’ in the four MSbs of an instruction specifies a special form of NOP. If the instruction is executed in proper sequence – immediately after the first word – the data in the second word is accessed and used by the instruction sequence. If the first word is skipped for some reason and the second or third word is executed by itself, a NOP is executed instead. This is necessary for cases when the multi-word instruction is preceded by a conditional instruction that changes the PC. Example 4-4 shows how this works.
## EXAMPLE 4-4: TWO-WORD INSTRUCTIONS

**CASE 1:**

<table>
<thead>
<tr>
<th>Object Code</th>
<th>Source Code</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0110 0110 0000 0000</td>
<td>TSTFSZ REG1 ; is RAM location 0?</td>
<td></td>
</tr>
<tr>
<td>1100 0001 0010 0011</td>
<td>MOVFF REG1, REG2 ; Yes, skip this word</td>
<td></td>
</tr>
<tr>
<td>1111 0100 0101 0110</td>
<td>ADDWF REG3 ; continue code</td>
<td></td>
</tr>
</tbody>
</table>

**CASE 2:**

<table>
<thead>
<tr>
<th>Object Code</th>
<th>Source Code</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0110 0110 0000 0000</td>
<td>TSTFSZ REG1 ; is RAM location 0?</td>
<td></td>
</tr>
<tr>
<td>0000 0000 0110 0000</td>
<td>MOVFFL REG1, REG2 ; No, execute this word</td>
<td></td>
</tr>
<tr>
<td>1111 0100 1000 1100</td>
<td>ADDWF REG3 ; continue code</td>
<td></td>
</tr>
</tbody>
</table>

## EXAMPLE 4-5: THREE-WORD INSTRUCTIONS

**CASE 1:**

<table>
<thead>
<tr>
<th>Object Code</th>
<th>Source Code</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0110 0110 0000 0000</td>
<td>TSTFSZ REG1 ; is RAM location 0?</td>
<td></td>
</tr>
<tr>
<td>0000 0000 0110 0000</td>
<td>MOVFFL REG1, REG2 ; Yes, skip this word</td>
<td></td>
</tr>
<tr>
<td>1111 0100 1000 1100</td>
<td>ADDWF REG3 ; continue code</td>
<td></td>
</tr>
</tbody>
</table>

**CASE 2:**

<table>
<thead>
<tr>
<th>Object Code</th>
<th>Source Code</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0110 0110 0000 0000</td>
<td>TSTFSZ REG1 ; is RAM location 0?</td>
<td></td>
</tr>
<tr>
<td>0000 0000 0110 0000</td>
<td>MOVFFL REG1, REG2 ; No, execute this word</td>
<td></td>
</tr>
<tr>
<td>1111 0100 1000 1100</td>
<td>ADDWF REG3 ; continue code</td>
<td></td>
</tr>
</tbody>
</table>
4.5 Data Memory Organization

Data memory in PIC18(L)F25/26K83 devices is implemented as static RAM. Each register in the data memory has a 14-bit address, allowing up to 16384 bytes of data memory. The memory space is divided into 64 banks that contain 256 bytes each. Figure 4-5 shows the data memory organization for the PIC18(L)F25/26K83 devices in this data sheet.

The data memory contains Special Function Registers (SFRs) and General Purpose Registers (GPRs). The SFRs are used for control and status of the controller and peripheral functions, while GPRs are used for data storage and scratchpad operations in the user’s application. Any read of an unimplemented location will read as '0's.

The instruction set and architecture allow operations across all banks. The entire data memory may be accessed by Direct, Indirect or Indexed Addressing modes. Addressing modes are discussed later in this subsection.

To ensure that commonly used registers (select SFRs and GPRs) can be accessed in a single cycle, PIC18 devices implement an Access Bank. This is a 256-byte memory space that provides fast access to some SFRs and the lower portion of GPR Bank 0 without using the Bank Select Register (BSR). Section 4.5.4 “Access Bank” provides a detailed description of the Access RAM.

4.5.1 BANK SELECT REGISTER (BSR)

Large areas of data memory require an efficient addressing scheme to make rapid access to any address possible. Ideally, this means that an entire address does not need to be provided for each read or write operation. For PIC18 devices, this is accomplished with a RAM banking scheme. This divides the memory space into 64 contiguous banks of 256 bytes. Depending on the instruction, each location can be addressed directly by its full 14-bit address, or an 8-bit low-order address and a 6-bit Bank Select Register.

This SFR holds the six Most Significant bits of a location address; the instruction itself includes the eight Least Significant bits. Only the six lower bits of the BSR are implemented (BSR<5:0>). The upper two bits are unused; they will always read '0' and cannot be written to. The BSR can be loaded directly by using the MOVLB instruction.

The value of the BSR indicates the bank in data memory; the eight bits in the instruction show the location in the bank and can be thought of as an offset from the bank’s lower boundary. The relationship between the BSR’s value and the bank division in data memory is shown in Figure 4-5.

Since up to 64 registers may share the same low-order address, the user must always be careful to ensure that the proper bank is selected before performing a data read or write. For example, writing what should be program data to an 8-bit address of F9h while the BSR is 3Fh will end up corrupting the Program Counter.

While any bank can be selected, only those banks that are actually implemented can be read or written to. Writes to unimplemented banks are ignored, while reads from unimplemented banks will return '0's. Even so, the STATUS register will still be affected as if the operation was successful. The data memory maps in Figure 4-5 indicate which banks are implemented.
## FIGURE 4-4: DATA MEMORY MAP FOR PIC18(L)F25/26K83 DEVICES

<table>
<thead>
<tr>
<th>Bank</th>
<th>BSR&lt;5:0&gt;</th>
<th>addr&lt;7:0&gt;</th>
<th>PIC18(L)F25K83 Access RAM</th>
<th>PIC18(L)F26K83 Access RAM</th>
<th>Address addr&lt;13:0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bank 0</td>
<td>00 0000</td>
<td>00h FFh</td>
<td>GPR</td>
<td>GPR</td>
<td>0000h 005Fh</td>
</tr>
<tr>
<td>Bank 1</td>
<td>00 0001</td>
<td>00h FFh</td>
<td>GPR</td>
<td>GPR</td>
<td>0060h 00FFh</td>
</tr>
<tr>
<td>Bank 2</td>
<td>00 0010</td>
<td>00h FFh</td>
<td>GPR</td>
<td>GPR</td>
<td>0100h</td>
</tr>
<tr>
<td>Bank 3</td>
<td>00 0011</td>
<td>00h FFh</td>
<td>GPR</td>
<td>GPR</td>
<td></td>
</tr>
<tr>
<td>Banks 4 to 7</td>
<td>00 0100</td>
<td>00h FFh</td>
<td>GPR</td>
<td>GPR</td>
<td>0400h 07FFh</td>
</tr>
<tr>
<td></td>
<td>00 0111</td>
<td></td>
<td>Unimplemented</td>
<td>Unimplemented</td>
<td>0800h 0FFFh</td>
</tr>
<tr>
<td>Banks 8 to 15</td>
<td>00 1000</td>
<td>00h FFh</td>
<td>GPR</td>
<td>GPR</td>
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<td></td>
<td>00 1111</td>
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<td>Unimplemented</td>
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<tr>
<td>Banks 16 to 31</td>
<td>01 0000</td>
<td>00h FFh</td>
<td>CAN Test</td>
<td>CAN Test</td>
<td>3600h 36FFh</td>
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<tr>
<td></td>
<td>01 1111</td>
<td></td>
<td>CAN SFR</td>
<td>CAN SFR</td>
<td>3700h 37FFh</td>
</tr>
<tr>
<td>Banks 32 to 53</td>
<td>10 0000</td>
<td>00h FFh</td>
<td>SFR</td>
<td>SFR</td>
<td>3800h 3EFFh</td>
</tr>
<tr>
<td></td>
<td>11 0111</td>
<td></td>
<td>SFR</td>
<td>SFR</td>
<td>3F00h 3F5Fh</td>
</tr>
<tr>
<td>Bank 54</td>
<td>d54</td>
<td>00h FFh</td>
<td>CAN Test</td>
<td>CAN Test</td>
<td></td>
</tr>
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<td>Bank 55</td>
<td>d55</td>
<td>00h FFh</td>
<td>CAN SFR</td>
<td>CAN SFR</td>
<td></td>
</tr>
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<td>Banks 56 to 62</td>
<td>11 1000</td>
<td>00h FFh</td>
<td>SFR</td>
<td>SFR</td>
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</tr>
<tr>
<td></td>
<td>11 1110</td>
<td></td>
<td>SFR</td>
<td>SFR</td>
<td></td>
</tr>
<tr>
<td>Bank 63</td>
<td>11 1111</td>
<td>00h FFh</td>
<td>SFR</td>
<td>SFR</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Depends on the number of SFRs. Refer subsequent SFR tables.
FIGURE 4-5: USE OF THE BANK SELECT REGISTER (DIRECT ADDRESSING)

Note 1: The Access RAM bit of the instruction can be used to force an override of the selected bank (BSR<5:0>) to the registers of the Access Bank.
4.5.2 GENERAL PURPOSE REGISTER FILE

General Purpose RAM is available starting Bank 0 of data memory. GPRs are not initialized by a Power-on Reset and are unchanged on all other Resets.

4.5.3 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. SFRs start at the top of data memory (3FFFh) and extend downward to occupy Bank 56 through 63 (3800h to 3FFFh). A list of these registers is given in Table 4-3 to Table 4-10. A bitwise summary of these registers can be found in Section 43.0 “Register Summary”.

4.5.4 ACCESS BANK

To streamline access for the most commonly used data memory locations, the data memory is configured with an Access Bank, which allows users to access a mapped block of memory without specifying a BSR. The Access Bank consists of the first 96 bytes of memory (00h-5Fh) in Bank 0 and the last 160 bytes of memory (60h-FFh) in Bank 63. The lower half is known as the “Access RAM” and is composed of GPRs. This upper half is also where some of the SFRs of the device are mapped. These two areas are mapped contiguously in the Access Bank and can be addressed linearly by an 8-bit address (Figure 4-5).

The Access Bank is used by core PIC18 instructions that include the Access RAM bit (the ‘a’ parameter in the instruction). When ‘a’ is equal to ‘1’, the instruction uses the BSR and the 8-bit address included in the opcode for the data memory address. When ‘a’ is ‘0’, however, the instruction uses the Access Bank address map; the current value of the BSR is ignored.

Using this “forced” addressing allows the instruction to operate on a data address in a single cycle, without updating the BSR first. For 8-bit addresses of 60h and above, this means that users can evaluate and operate on SFRs more efficiently. The Access RAM below 60h is a good place for data values that the user might need to access rapidly, such as immediate computational results or common program variables. Access RAM also allows for faster and more code efficient and switching of variables.

The mapping of the Access Bank is slightly different when the extended instruction set is enabled (XINST Configuration bit = 1). This is discussed in more detail in Section 4.8.3 “Mapping the Access Bank in Indexed Literal Offset Mode”.
### TABLE 4-3: SPECIAL FUNCTION REGISTER MAP FOR PIC18(L)F25/26K83 DEVICES BANK 63

<table>
<thead>
<tr>
<th>Bank 63 Address</th>
<th>Register Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3FFFh</td>
<td>TOSU</td>
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</tr>
<tr>
<td>3FEEh</td>
<td>TOSH</td>
<td></td>
</tr>
<tr>
<td>3FDDh</td>
<td>POSTINC2</td>
<td></td>
</tr>
<tr>
<td>3FCh</td>
<td>STKPTR</td>
<td></td>
</tr>
<tr>
<td>3F8h</td>
<td>PCLATU</td>
<td></td>
</tr>
<tr>
<td>3F9h</td>
<td>PCL</td>
<td></td>
</tr>
<tr>
<td>3FAh</td>
<td>TBLPTRU</td>
<td></td>
</tr>
<tr>
<td>3FBh</td>
<td>TBLPTRL</td>
<td></td>
</tr>
<tr>
<td>3FFh</td>
<td>TABLAT</td>
<td></td>
</tr>
<tr>
<td>3F0h</td>
<td>PCON1</td>
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</tr>
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<td>PCON0</td>
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<td>PCON1</td>
<td></td>
</tr>
<tr>
<td>3F2h</td>
<td>PRECIN1</td>
<td></td>
</tr>
<tr>
<td>3F3h</td>
<td>PLUSW1</td>
<td></td>
</tr>
<tr>
<td>3F4h</td>
<td>FSROH</td>
<td></td>
</tr>
<tr>
<td>3F5h</td>
<td>WREG</td>
<td></td>
</tr>
<tr>
<td>3F6h</td>
<td>PRECIN0</td>
<td></td>
</tr>
<tr>
<td>3F7h</td>
<td>POSTDEC1</td>
<td></td>
</tr>
<tr>
<td>3F8h</td>
<td>PLUSW0</td>
<td></td>
</tr>
<tr>
<td>3F9h</td>
<td>FSROH</td>
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</tr>
<tr>
<td>3FAh</td>
<td>WREG</td>
<td></td>
</tr>
<tr>
<td>3FBh</td>
<td>PRECIN1</td>
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</tr>
<tr>
<td>3FCh</td>
<td>POSTDEC0</td>
<td></td>
</tr>
<tr>
<td>3FDh</td>
<td>PLUSW1</td>
<td></td>
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<tr>
<td>3FEh</td>
<td>FSR1H</td>
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<tr>
<td>3FFh</td>
<td>BSR</td>
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</table>

**Legend:** Unimplemented data memory locations and registers, read as '0'.

---

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Preliminary

PIC18(L)F25/26K83

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# Table 4-4: Special Function Register Map for PIC18(L)F25/26K83 Devices Bank 62

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
<th>Description</th>
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<td>3E0Fh</td>
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<td>3E8Fh</td>
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<td>---</td>
</tr>
<tr>
<td>3E4Fh</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>3E2Fh</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>3E0Fh</td>
<td>---</td>
<td>---</td>
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<td>ADCT</td>
<td>3EDFh</td>
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<td>3E5Fh</td>
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<td>3E3Fh</td>
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</tr>
<tr>
<td>3F2Ch</td>
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Legend: Unimplemented data memory locations and registers, read as '0'.
TABLE 4-5: SPECIAL FUNCTION REGISTER MAP FOR PIC18(L)F25/26K83 DEVICES BANK 61

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
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<td>U2BRGL</td>
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<td>U2BRGL</td>
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<td>U2P2H</td>
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<tr>
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</table>

Legend: Unimplemented data memory locations and registers, read as '0'.
### TABLE 4-6: SPECIAL FUNCTION REGISTER MAP FOR PIC18(L)F25/26K83 DEVICES BANK 60

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<td>3C5B0h</td>
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**Legend:** Unimplemented data memory locations and registers, read as '0'.
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Legend: Unimplemented data memory locations and registers, read as '0'.

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Legend: Unimplemented data memory locations and registers, read as '0'.
### TABLE 4-9: SPECIAL FUNCTION REGISTER MAP FOR PIC18(L)F25/26K83 DEVICES BANK 57

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<td>—</td>
<td>3981h</td>
<td>—</td>
<td>3961h</td>
<td>—</td>
</tr>
<tr>
<td>39E0h</td>
<td>—</td>
<td>39B0h</td>
<td>—</td>
<td>39A0h</td>
<td>—</td>
<td>3980h</td>
<td>—</td>
<td>3960h</td>
<td>—</td>
</tr>
</tbody>
</table>

**Legend:** Unimplemented data memory locations and registers, read as ‘0’.

**Note 1:** Unimplemented in LF devices.
### TABLE 4-10: SPECIAL FUNCTION REGISTER MAP FOR PIC18(L)F25/26K83 DEVICES BANK 56

<table>
<thead>
<tr>
<th>Address</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>38FFh</td>
<td>—</td>
</tr>
<tr>
<td>38FEh</td>
<td>—</td>
</tr>
<tr>
<td>38FDh</td>
<td>—</td>
</tr>
<tr>
<td>38FCh</td>
<td>—</td>
</tr>
<tr>
<td>38FBh</td>
<td>—</td>
</tr>
<tr>
<td>38FAh</td>
<td>—</td>
</tr>
<tr>
<td>38F9h</td>
<td>—</td>
</tr>
<tr>
<td>38F8h</td>
<td>—</td>
</tr>
<tr>
<td>38F7h</td>
<td>—</td>
</tr>
<tr>
<td>38F6h</td>
<td>—</td>
</tr>
<tr>
<td>38F5h</td>
<td>—</td>
</tr>
<tr>
<td>38F4h</td>
<td>—</td>
</tr>
<tr>
<td>38F3h</td>
<td>—</td>
</tr>
<tr>
<td>38F2h</td>
<td>—</td>
</tr>
<tr>
<td>38F1h</td>
<td>—</td>
</tr>
<tr>
<td>38F0h</td>
<td>—</td>
</tr>
<tr>
<td>38EFh</td>
<td>—</td>
</tr>
<tr>
<td>38E Eh</td>
<td>—</td>
</tr>
<tr>
<td>38EDh</td>
<td>—</td>
</tr>
<tr>
<td>38ECd</td>
<td>—</td>
</tr>
<tr>
<td>38EBh</td>
<td>—</td>
</tr>
<tr>
<td>38ECh</td>
<td>—</td>
</tr>
<tr>
<td>38E Bh</td>
<td>—</td>
</tr>
<tr>
<td>38AAAA</td>
<td>—</td>
</tr>
<tr>
<td>38Ah</td>
<td>—</td>
</tr>
<tr>
<td>38An</td>
<td>—</td>
</tr>
<tr>
<td>38A9h</td>
<td>—</td>
</tr>
<tr>
<td>38A8h</td>
<td>—</td>
</tr>
<tr>
<td>38A7h</td>
<td>—</td>
</tr>
<tr>
<td>38A6h</td>
<td>—</td>
</tr>
<tr>
<td>38A5h</td>
<td>—</td>
</tr>
<tr>
<td>38A4h</td>
<td>—</td>
</tr>
<tr>
<td>38A3h</td>
<td>—</td>
</tr>
<tr>
<td>38A2h</td>
<td>—</td>
</tr>
<tr>
<td>38A1h</td>
<td>—</td>
</tr>
<tr>
<td>38A0h</td>
<td>—</td>
</tr>
</tbody>
</table>

**Legend:** Unimplemented data memory locations and registers, read as '0'.

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### TABLE 4-11: SPECIAL FUNCTION REGISTER MAP FOR PIC18(L)F25/26K83 DEVICES BANK 55

<table>
<thead>
<tr>
<th>Address</th>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>37FFh</td>
<td>CANCON_RO0</td>
<td>CANCON_RO2</td>
</tr>
<tr>
<td>37F6h</td>
<td>CANCON_RO1</td>
<td>CANCON_RO3</td>
</tr>
<tr>
<td>37F6h</td>
<td>CANSTAT_RO1</td>
<td>CANSTAT_RO3</td>
</tr>
<tr>
<td>37F7h</td>
<td>RXB1D7</td>
<td>RXB1D5</td>
</tr>
<tr>
<td>37F8h</td>
<td>RXB1D4</td>
<td>RXB1D2</td>
</tr>
<tr>
<td>37F9h</td>
<td>RXB1D1</td>
<td>RXB1D0</td>
</tr>
<tr>
<td>37F6h</td>
<td>RXB1D1D3</td>
<td>RXB1D1D1</td>
</tr>
<tr>
<td>37F7h</td>
<td>RXB1D4</td>
<td>RXB1D2</td>
</tr>
<tr>
<td>37F8h</td>
<td>RXB1D1</td>
<td>RXB1D0</td>
</tr>
<tr>
<td>37F9h</td>
<td>RXB1D1</td>
<td>RXB1D0</td>
</tr>
<tr>
<td>37FAh</td>
<td>TXB1D7</td>
<td>TXB1D5</td>
</tr>
<tr>
<td>37FDh</td>
<td>RXB1D1</td>
<td>RXB1D0</td>
</tr>
<tr>
<td>37FFh</td>
<td>RXB1D1D3</td>
<td>RXB1D1D1</td>
</tr>
<tr>
<td>37F6h</td>
<td>RXB1D1</td>
<td>RXB1D0</td>
</tr>
<tr>
<td>37F9h</td>
<td>RXB1D1</td>
<td>RXB1D0</td>
</tr>
</tbody>
</table>

Legend: Unimplemented data memory locations and registers, read as ‘0’.
4.5.5 STATUS REGISTER

The STATUS register, shown in Register 4-2, contains the arithmetic status of the ALU. As with any other SFR, it can be the operand for any instruction.

If the STATUS register is the destination for an instruction that affects the Z, DC, C, OV or N bits, the results of the instruction are not written; instead, the STATUS register is updated according to the instruction performed. Therefore, the result of an instruction with the STATUS register as its destination may be different than intended. As an example, CLRF STATUS will set the Z bit and leave the remaining Status bits unchanged ('0uuu u1uu').

It is recommended that only BCF, BSF, SWAPF, MOVFF, MOVWF and MOVFFL instructions are used to alter the STATUS register, because these instructions do not affect the Z, C, DC, OV or N bits in the STATUS register.

For other instructions that do not affect Status bits, see the instruction set summaries in Section 42.2 “Extended Instruction Set” and Table 42-3.

Note: The C and DC bits operate as the borrow and digit borrow bits, respectively, in subtraction.

4.5.6 CALL SHADOW REGISTER

When CALL, CALLW, RCALL instructions are used, the WREG, BSR and STATUS are automatically saved in hardware and can be accessed using the WREG_C-SHAD, BSR_CSHAD and STATUS_CSHAD registers.
4.6 Register Definitions: Status Registers

**REGISTER 4-2: STATUS: STATUS REGISTER**

<table>
<thead>
<tr>
<th>bit</th>
<th>Unimplemented</th>
<th>TO: Time-Out bit</th>
<th>PD: Power-Down bit</th>
<th>N: Negative bit used for signed arithmetic (2’s complement); indicates if the result is negative, (ALU MSb = 1).</th>
<th>OV: Overflow bit used for signed arithmetic (2’s complement); indicates an overflow of the 7-bit magnitude, which causes the sign bit (bit 7) to change state.</th>
<th>Z: Zero bit</th>
<th>DC: Digit Carry/Borrow bit</th>
<th>C: Carry/Borrow bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td>1 = The result is negative</td>
<td>1 = Overflow occurred for current signed arithmetic operation</td>
<td>1 = The result of an arithmetic or logic operation is zero</td>
<td>(ADDWF, ADDLW, SUBLW, SUBWF instructions)</td>
<td>(ADDWF, ADDLW, SUBLW, SUBWF instructions)</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td>0 = The result is positive</td>
<td>0 = No overflow occurred</td>
<td>0 = The result of an arithmetic or logic operation is not zero</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td>1 = Set at power-up or by execution of CLRWDT or SLEEP instruction</td>
<td>1 = A carry-out from the 4th low-order bit of the result occurred</td>
<td>0 = A carry-out from the 4th low-order bit of the result</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td>0 = A WDT time-out occurred</td>
<td>0 = No carry-out from the 4th low-order bit of the result</td>
<td>0 = A carry-out from the Most Significant bit of the result occurred</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Unimplemented</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**Note 1:** For **Borrow**, the polarity is reversed. A subtraction is executed by adding the two’s complement of the second operand.

**Note 2:** For **Rotate (RRF, RLF) instructions**, this bit is loaded with either the high or low-order bit of the Source register.
4.7 Data Addressing Modes

**Note:** The execution of some instructions in the core PIC18 instruction set are changed when the PIC18 extended instruction set is enabled. See Section 4.8 “Data Memory and the Extended Instruction Set” for more information.

While the program memory can be addressed in only one way – through the Program Counter – information in the data memory space can be addressed in several ways. For most instructions, the addressing mode is fixed. Other instructions may use up to three modes, depending on which operands are used and whether or not the extended instruction set is enabled.

The addressing modes are:

- Inherent
- Literal
- Direct
- Indirect

An additional addressing mode, Indexed Literal Offset, is available when the extended instruction set is enabled (XINST Configuration bit = 1). Its operation is discussed in detail in Section 4.8.1 “Indexed Addressing with Literal Offset”.

4.7.1 INHERENT AND LITERAL ADDRESSING

Many PIC18 control instructions do not need any argument at all; they either perform an operation that globally affects the device or they operate implicitly on one register. This addressing mode is known as Inherent Addressing. Examples include SLEEP, RESET and DAW.

Other instructions work in a similar way but require an additional explicit argument in the opcode. This is known as Literal Addressing mode because they require some literal value as an argument. Examples include ADDLW and MOVLW, which respectively, add or move a literal value to the W register. Other examples include CALL and GOTO, which include a 20-bit program memory address.

Note: The execution of some instructions in the core PIC18 instruction set are changed when the PIC18 extended instruction set is enabled. See Section 4.8 “Data Memory and the Extended Instruction Set” for more information.
4.7.2 DIRECT ADDRESSING

Direct addressing specifies all or part of the source and/or destination address of the operation within the opcode itself. The options are specified by the arguments accompanying the instruction.

In the core PIC18 instruction set, bit-oriented and byte-oriented instructions use some version of direct addressing by default. All of these instructions include some 8-bit literal address as their Least Significant Byte. This address specifies either a register address in one of the banks of data RAM (Section 4.5.2 “General Purpose Register File”) or a location in the Access Bank (Section 4.5.4 “Access Bank”) as the data source for the instruction.

The Access RAM bit ‘a’ determines how the address is interpreted. When ‘a’ is ‘1’, the contents of the BSR (Section 4.5.1 “Bank Select Register (BSR)”) are used with the address to determine the complete 14-bit address of the register. When ‘a’ is ‘0’, the address is interpreted as being a register in the Access Bank. Addressing that uses the Access RAM is sometimes also known as Direct Forced Addressing mode.

A few instructions, such as MOVFF, include the entire 14-bit address (either source or destination) in their opcodes. In these cases, the BSR is ignored entirely.

The destination of the operation’s results is determined by the destination bit ‘d’. When ‘d’ is ‘1’, the results are stored back in the source register, overwriting its original contents. When ‘d’ is ‘0’, the results are stored in the W register. Instructions without the ‘d’ argument have a destination that is implicit in the instruction; their destination is either the target register being operated on or the W register.

4.7.3 INDIRECT ADDRESSING

Indirect addressing allows the user to access a location in data memory without giving a fixed address in the instruction. This is done by using File Select Registers (FSRs) as pointers to the locations which are to be read or written. Since the FSRs are themselves located in RAM as Special File Registers, they can also be directly manipulated under program control. This makes FSRs very useful in implementing data structures, such as tables and arrays in data memory.

The registers for indirect addressing are also implemented with Indirect File Operands (INDFs) that permit automatic manipulation of the pointer value with auto-incrementing, auto-decrementing or offsetting with another value. This allows for efficient code, using loops, such as the example of clearing an entire RAM bank in Example 4-6.

```
EXAMPLE 4-6: HOW TO CLEAR RAM (BANK 1) USING INDIRECT ADDRESSING

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
</table>
| LFSR | FSR0, 100h | SET FSR0;
| NEXT | CLR F POSTINC0 | Clear INDF;
|      | ; register then | ; inc pointer
| BTFS | FSRnH, 1 | All done with
|      | ; Bank1? | ; Bank1?
| BRA  | NEXT | NO, clear next
|      | CONTINUE | YES, continue
```

4.7.3.1 FSR Registers and the INDF Operand

At the core of indirect addressing are three sets of registers: FSR0, FSR1 and FSR2. Each represents a pair of 8-bit registers, FSRnH and FSRnL. Each FSR pair holds a 14-bit value, therefore, the two upper bits of the FSRnH register are not used. The 14-bit FSR value can address the entire range of the data memory in a linear fashion. The FSR register pairs, then, serve as pointers to data memory locations.

Indirect addressing is accomplished with a set of Indirect File Operands, INDF0 through INDF2. These can be thought of as “virtual” registers; they are mapped in the SFR space but are not physically implemented. Reading or writing to a particular INDF register actually accesses the data addressed by its corresponding FSR register pair. A read from INDF1, for example, reads the data at the address indicated by FSR1H:FSR1L. Instructions that use the INDF registers as operands actually use the contents of their corresponding FSR as a pointer to the instruction’s target. The INDF operand is just a convenient way of using the pointer.

Because indirect addressing uses a full 14-bit address, data RAM banking is not necessary. Thus, the current contents of the BSR and the Access RAM bit have no effect on determining the target address.
4.7.3.2 FSR Registers, POSTINC, POSTDEC, PREINC and PLUSW

In addition to the INDF operand, each FSR register pair also has four additional indirect operands. Like INDF, these are “virtual” registers which cannot be directly read or written. Accessing these registers actually accesses the location to which the associated FSR register pair points, and also performs a specific action on the FSR value. They are:

- **POSTDEC**: accesses the location to which the FSR points, then automatically decrements the FSR by 1 afterwards.
- **POSTINC**: accesses the location to which the FSR points, then automatically increments the FSR by 1 afterwards.
- **PREINC**: automatically increments the FSR by 1, then uses the location to which the FSR points in the operation.
- **PLUSW**: adds the signed value of the W register (range of -127 to 128) to that of the FSR and uses the location to which the result points in the operation.

In this context, accessing an INDF register uses the value in the associated FSR register without changing it. Similarly, accessing a PLUSW register gives the FSR value an offset by that in the W register; however, neither W nor the FSR is actually changed in the operation. Accessing the other virtual registers changes the value of the FSR register.

---

**FIGURE 4-6: INDIRECT ADDRESSING**

```
Using an instruction with one of the indirect addressing registers as the operand.

...uses the 14-bit address stored in the FSR pair associated with that register.

...to determine the data memory location to be used in that operation.

In this case, the FSR1 pair contains 3ECCh. This means the contents of location 3ECCh will be added to that of the W register and stored back in 3ECCh.
```
Operations on the FSRs with POSTDEC, POSTINC and PREINC affect the entire register pair; that is, roll-overs of the FSRnL register from FFh to 00h carry over to the FSRnH register. On the other hand, results of these operations do not change the value of any flags in the STATUS register (e.g., Z, N, OV, etc.).

The PLUSW register can be used to implement a form of indexed addressing in the data memory space. By manipulating the value in the W register, users can reach addresses that are fixed offsets from pointer addresses. In some applications, this can be used to implement some powerful program control structure, such as software stacks, inside of data memory.

4.7.3.3 Operations by FSRs on FSRs

Indirect addressing operations that target other FSRs or virtual registers represent special cases. For example, using an FSR to point to one of the virtual registers will not result in successful operations. As a specific case, assume that FSR0H:FSR0L contains 3FE7h, the address of INDF1. Attempts to read the value of the INDF1 using INDF0 as an operand will return 00h. Attempts to write to INDF1 using INDF0 as the operand will result in a NOP.

On the other hand, using the virtual registers to write to an FSR pair may not occur as planned. In these cases, the value will be written to the FSR pair but without any incrementing or decrementing. Thus, writing to either the INDF2 or POSTDEC2 register will write the same value to the FSR2H:FSR2L.

Since the FSRs are physical registers mapped in the SFR space, they can be manipulated through all direct operations. Users should proceed cautiously when working on these registers, particularly if their code uses indirect addressing.

Similarly, operations by indirect addressing are generally permitted on all other SFRs. Users should exercise the appropriate caution that they do not inadvertently change settings that might affect the operation of the device.

4.8 Data Memory and the Extended Instruction Set

Enabling the PIC18 extended instruction set (XINST Configuration bit = 1) significantly changes certain aspects of data memory and its addressing. Specifically, the use of the Access Bank for many of the core PIC18 instructions is different; this is due to the introduction of a new addressing mode for the data memory space.

What does not change is just as important. The size of the data memory space is unchanged, as well as its linear addressing. The SFR map remains the same. Core PIC18 instructions can still operate in both Direct and Indirect Addressing mode; inherent and literal instructions do not change at all. Indirect addressing with FSR0 and FSR1 also remain unchanged.

4.8.1 Indexed Addressing with Literal Offset

Enabling the PIC18 extended instruction set changes the behavior of indirect addressing using the FSR2 register pair within Access RAM. Under the proper conditions, instructions that use the Access Bank – that is, most bit-oriented and byte-oriented instructions – can invoke a form of indexed addressing using an offset specified in the instruction. This special addressing mode is known as Indexed Addressing with Literal Offset, or Indexed Literal Offset mode.

When using the extended instruction set, this addressing mode requires the following:

• The use of the Access Bank is forced (‘a’ = 0) and
• The file address argument is less than or equal to 5Fh.

Under these conditions, the file address of the instruction is not interpreted as the lower byte of an address (used with the BSR in direct addressing), or as an 8-bit address in the Access Bank. Instead, the value is interpreted as an offset value to an Address Pointer, specified by FSR2. The offset and the contents of FSR2 are added to obtain the target address of the operation.

4.8.2 Instructions Affected by Indexed Literal Offset Mode

Any of the core PIC18 instructions that can use direct addressing are potentially affected by the Indexed Literal Offset Addressing mode. This includes all byte-oriented and bit-oriented instructions, or almost one-half of the standard PIC18 instruction set. Instructions that only use Inherent or Literal Addressing modes are unaffected.

Additionally, byte-oriented and bit-oriented instructions are not affected if they do not use the Access Bank (Access RAM bit is ‘1’), or include a file address of 60h or above. Instructions meeting these criteria will continue to execute as before. A comparison of the different possible addressing modes when the extended instruction set is enabled is shown in Figure 4-7.

Those who desire to use byte-oriented or bit-oriented instructions in the Indexed Literal Offset mode should note the changes to assembler syntax for this mode. This is described in more detail in Section 42.2.1 “Extended Instruction Syntax”.

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FIGURE 4-7: COMPARING ADDRESSING OPTIONS FOR BIT-ORIENTED AND BYTE-ORIENTED INSTRUCTIONS (EXTENDED INSTRUCTION SET ENABLED)

EXAMPLE INSTRUCTION: ADDWF, f, d, a (Opcode: 0010 01da ffff ffff)

When ‘a’ = 0 and f ≥ 60h:
The instruction executes in Direct Forced mode. ‘f’ is interpreted as a location in the Access RAM between 060h and 0FFh. This is the same as locations 3F60h to 3FFFh (Bank 63) of data memory.
Locations below 60h are not available in this Addressing mode.

When ‘a’ = 0 and f ≤ 5Fh:
The instruction executes in Indexed Literal Offset mode. ‘f’ is interpreted as an offset to the address value in FSR2. The two are added together to obtain the address of the target register for the instruction. The address can be anywhere in the data memory space.
Note that in this mode, the correct syntax is now:
ADDWF [k], d
where ‘k’ is the same as ‘f’.

When ‘a’ = 1 (all values of f):
The instruction executes in Direct mode (also known as Direct Long mode). ‘f’ is interpreted as a location in one of the 63 banks of the data memory space. The bank is designated by the Bank Select Register (BSR). The address can be in any implemented bank in the data memory space.
4.8.3 MAPPING THE ACCESS BANK IN INDEXED LITERAL OFFSET MODE

The use of Indexed Literal Offset Addressing mode effectively changes how the first 96 locations of Access RAM (00h to 5Fh) are mapped. Rather than containing just the contents of the bottom section of Bank 0, this mode maps the contents from a user defined “window” that can be located anywhere in the data memory space. The value of FSR2 establishes the lower boundary of the addresses mapped into the window, while the upper boundary is defined by FSR2 plus 95 (5Fh). Addresses in the Access RAM above 5Fh are mapped as previously described (see Section 4.5.4 “Access Bank”). An example of Access Bank remapping in this addressing mode is shown in Figure 4-8.

Remapping of the Access Bank applies only to operations using the Indexed Literal Offset mode. Operations that use the BSR (Access RAM bit is ‘1’) will continue to use direct addressing as before.

FIGURE 4-8: REMAPPING THE ACCESS BANK WITH INDEXED LITERAL OFFSET ADDRESSING

Example Situation:

ADDWF f, d, a
FSR2H:FSR2L = 120h

Locations in the region from the FSR2 pointer (0120h) to the pointer plus 05Fh (017Fh) are mapped to the bottom of the Access RAM (000h-05Fh).

Special File Registers at 3F60h through 3FFFh are mapped to 60h through FFh, as usual.

Bank 0 addresses below 5Fh can still be addressed by using the BSR.

4.9 PIC18 Instruction Execution and the Extended Instruction Set

Enabling the extended instruction set adds eight additional commands to the existing PIC18 instruction set. These instructions are executed as described in Section 42.2 “Extended Instruction Set”.

FIGURE 4-8: REMAPPING THE ACCESS BANK WITH INDEXED LITERAL OFFSET ADDRESSING
5.0 DEVICE CONFIGURATION

Device configuration consists of the Configuration Words, User ID, Device ID, Rev ID, Device Information Area (DIA), (see Section 5.7 “Device Information Area”), and the Device Configuration Information (DCI) regions, (see Section 5.8 “Device Configuration Information”).

5.1 Configuration Words

There are six Configuration Word bits that allow the user to setup the device with several choices of oscillators, Resets and memory protection options. These are implemented as Configuration Word 1 through Configuration Word 6 at 300000h through 300008h.
5.2 Register Definitions: Configuration Words

REGISTER 5-1: CONFIGURATION WORD 1L (30 0000h)

<table>
<thead>
<tr>
<th>U-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>U-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>RSTOSC&lt;2:0&gt;</td>
<td>bit 0</td>
<td>FEXTOSC&lt;2:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit   W = Writable bit   U = Unimplemented bit, read as ‘1’
-n = Value for blank device   ‘1’ = Bit is set   ‘0’ = Bit is cleared   x = Bit is unknown

- bit 7: **Unimplemented**: Read as ‘1’
- bit 6-4: **RSTOSC<2:0>**: Power-up Default Value for COSC bits
  - 111 = EXTOSC operating per FEXTOSC<2:0> bits
  - 110 = HFINTOSC with HFFRQ = 4 MHz and CDIV = 4:1
  - 101 = LFINTOSC
  - 100 = SOSC
  - 011 = Reserved
  - 010 = EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC<2:0> bits
  - 001 = Reserved
  - 000 = HFINTOSC with HFFRQ = 64 MHz and CDIV = 1:1; resets COSC/NOSC to 3'b110

- bit 3: **Unimplemented**: Read as ‘1’

- bit 2-0: **FEXTOSC<2:0>**: FEXTOSC External Oscillator Mode Selection bits
  - 111 = EC (External Clock) above 8 MHz; PFM set to high power
  - 110 = EC (External Clock) for 500 kHz to 8 MHz; PFM set to medium power
  - 101 = EC (External Clock) below 500 kHz; PFM set to low power
  - 100 = Oscillator is not enabled
  - 011 = Reserved (do not use)
  - 010 = HS (crystal oscillator) above 8 MHz; PFM set to high power
  - 001 = XT (crystal oscillator) above 500 kHz, below 8 MHz; PFM set to medium power
  - 000 = LP (crystal oscillator) optimized for 32.768 kHz; PFM set to low power
`REGISTER 5-2: CONFIGURATION WORD 1H (30 0001h)`

<table>
<thead>
<tr>
<th>U-1</th>
<th>U-1</th>
<th>R/W-1</th>
<th>U-1</th>
<th>R/W-1</th>
<th>U-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>FCMEN</td>
<td>—</td>
<td>CSWEN</td>
<td>—</td>
<td>PR1WAY</td>
<td>CLKOUTEN</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘1’
- **-n** = Value for blank device
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

| bit 7-6 | **Unimplemented**: Read as ‘1’ |
| bit 5   | **FCMEN**: Fail-Safe Clock Monitor Enable bit |
|        | 1 = FSCM timer is enabled |
|        | 0 = FSCM timer is disabled |
| bit 4   | **Unimplemented**: Read as ‘1’ |
| bit 3   | **CSWEN**: Clock Switch Enable bit |
|        | 1 = Writing to NOSC and NDIV is allowed |
|        | 0 = The NOSC and NDIV bits cannot be changed by user software |
| bit 2   | **Unimplemented**: Read as ‘1’ |
| bit 1   | **PR1WAY**: PRLOCKED One-Way Set Enable bit |
|        | 1 = PRLOCKED bit can be cleared and set only once; Priority registers remain locked after one clear/set cycle |
|        | 0 = PRLOCKED bit can be set and cleared repeatedly (subject to the unlock sequence) |
| bit 0   | **CLKOUTEN**: Clock Out Enable bit |
|        | If FEXTOSC<2:0> = EC (high, mid or low) or Not Enabled: |
|        | 1 = CLKOUT function is disabled; I/O or oscillator function on OSC2 |
|        | 0 = CLKOUT function is enabled; Fosc/4 clock appears at OSC2 |
|        | **Otherwise**: |
|        | This bit is ignored. |
REGISTER 5-3: CONFIGURATION WORD 2L (30 0002h)

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOREN&lt;1:0&gt;</td>
<td>LPBOREN</td>
<td>IVT1WAY</td>
<td>MVECEN</td>
<td>PWRTS&lt;1:0&gt;</td>
<td>MCLRE</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘1’  
-n = Value for blank device  
‘1’ = Bit is set  
‘0’ = Bit is cleared  
x = Bit is unknown

bit 7-6  
BOREN<1:0>: Brown-out Reset Enable bits  
When enabled, Brown-out Reset Voltage (V_{BOR}) is set by the BORV bit.  
11 = Brown-out Reset is enabled, SBOREN bit is ignored  
10 = Brown-out Reset is enabled while running, disabled in Sleep; SBOREN is ignored  
01 = Brown-out Reset is enabled according to SBOREN  
00 = Brown-out Reset is disabled

bit 5  
LPBOREN: Low-Power BOR Enable bit  
1 = Low-Power BOR is disabled  
0 = Low-Power BOR is enabled

bit 4  
IVT1WAY: IVTLOCK bit One-Way Set Enable bit  
1 = IVTLOCKED bit can be cleared and set only once; IVT registers remain locked after one clear/set cycle  
0 = IVTLOCKED bit can be set and cleared repeatedly (subject to the unlock sequence)

bit 3  
MVECEN: Multi-vector Enable bit  
1 = Multi-vector enabled; Vector table used for interrupts  
0 = Legacy interrupt behavior

bit 2-1  
PWRTS<1:0>: Power-up Timer Selection bits  
11 = PWRT is disabled  
10 = PWRT set at 64 ms  
01 = PWRT set at 16 ms  
00 = PWRT set at 1 ms

bit 0  
MCLRE: Master Clear (MCLR) Enable bit  
If LVP = 1:  
RE3 pin function is MCLR  
If LVP = 0:  
1 = MCLR pin is MCLR  
0 = MCLR pin function is a port defined function
## REGISTER 5-4: CONFIGURATION WORD 2H (30 0003h)

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>XINST</th>
<th>Bit 6</th>
<th>DEBUG</th>
<th>Bit 5</th>
<th>Unimplemented</th>
<th>Bit 4</th>
<th>STVREN</th>
<th>Bit 3</th>
<th>PPS1WAY</th>
<th>Bit 2</th>
<th>ZCD</th>
<th>Bit 1-0</th>
<th>BORV&lt;1:0&gt;(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R=Read, W=Write, U=Unimplemented</td>
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<td></td>
<td>Extended Instruction Set Enable bit</td>
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<td>1 = Indexed Addressing mode and Extended instruction set are disabled (Legacy mode)</td>
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<td>0 = Indexed Addressing mode and Extended instruction set are enabled</td>
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<td>Unimplemented: Read as <code>1</code></td>
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<td>Debugger Enable bit</td>
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<td>1 = Background debugger is disabled</td>
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<td>0 = Background debugger is enabled</td>
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<td>STVREN</td>
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<td>Stack Overflow/Underflow Reset Enable bit</td>
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<td>1 = Stack Overflow or Underflow will cause a Reset</td>
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<td>0 = Stack Overflow or Underflow will not cause a Reset</td>
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<td>PPS1WAY</td>
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<td>PPSLOCKED One-Way Set Enable bit</td>
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<td>1 = PPSLOCKED bit can be cleared and set only once; PPS registers remain locked after one clear/set cycle</td>
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<td>0 = PPSLOCKED bit can be set and cleared repeatedly (subject to the unlock sequence)</td>
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<td>ZCD</td>
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<td>Zero-Cross Detect Enable bit</td>
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<td>1 = ZCD is disabled; ZCD can be enabled by setting the bit SEN of the ZCDCON register</td>
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<td>0 = ZCD is always enabled</td>
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<td>Bit 1-0</td>
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<td>BORV&lt;1:0&gt;</td>
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<td></td>
<td>Brown-out Reset Voltage Selection bits(1)</td>
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<td>PIC18F25/26K83 Devices:</td>
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<td></td>
<td>11 = Brown-out Reset Voltage (V_BOR) is set to 2.45V</td>
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<td>10 = Brown-out Reset Voltage (V_BOR) is set to 2.45V</td>
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<td>01 = Brown-out Reset Voltage (V_BOR) is set to 2.7V</td>
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<td></td>
<td>00 = Brown-out Reset Voltage (V_BOR) is set to 2.85V</td>
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<td>PIC18LF25/26K83 Device:</td>
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<td></td>
<td>11 = Brown-out Reset Voltage (V_BOR) is set to 1.90V</td>
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<td>10 = Brown-out Reset Voltage (V_BOR) is set to 2.45V</td>
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<td>01 = Brown-out Reset Voltage (V_BOR) is set to 2.7V</td>
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<td>00 = Brown-out Reset Voltage (V_BOR) is set to 2.85V</td>
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</table>

**Note 1:** The higher voltage setting is recommended for operation at or above 16 MHz.
### REGISTER 5-5: CONFIGURATION WORD 3L (300004h)

<table>
<thead>
<tr>
<th>U-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
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<tr>
<td>bit 7</td>
<td>WDTE&lt;1:0&gt;</td>
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<tr>
<td>bit 6-5</td>
<td>WDTCPS&lt;4:0&gt;</td>
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</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘1’
- **-n** = Value for blank device
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

#### bit 7
**Unimplemented:** Read as ‘1’

#### bit 6-5
**WDTE<1:0>**: WDT Operating Mode bits
- 00 = WDT is disabled, SWDTEN is ignored
- 01 = WDT is enabled/disabled by the SWDTEN bit in WDTCON0
- 10 = WDT is enabled while Sleep = 0, suspended when Sleep = 1; SWDTEN is ignored
- 11 = WDT is enabled regardless of Sleep; SWDTEN is ignored

#### bit 4-0
**WDTCPS<4:0>**: WDT Period Select bits

<table>
<thead>
<tr>
<th>WDTCPS&lt;4:0&gt;</th>
<th>WDT at POR</th>
<th>Typical Time-out (FIN = 31 kHz)</th>
<th>Software Control of WDTPS?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>Divisor Ratio</td>
<td></td>
<td></td>
</tr>
<tr>
<td>00000</td>
<td>1:32</td>
<td>2&lt;sup&gt;5&lt;/sup&gt; 1 ms</td>
<td></td>
</tr>
<tr>
<td>00001</td>
<td>1:64</td>
<td>2&lt;sup&gt;6&lt;/sup&gt; 2 ms</td>
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<tr>
<td>00010</td>
<td>1:128</td>
<td>2&lt;sup&gt;7&lt;/sup&gt; 4 ms</td>
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<tr>
<td>00011</td>
<td>1:256</td>
<td>2&lt;sup&gt;8&lt;/sup&gt; 8 ms</td>
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<tr>
<td>00100</td>
<td>1:512</td>
<td>2&lt;sup&gt;9&lt;/sup&gt; 16 ms</td>
<td></td>
</tr>
<tr>
<td>00101</td>
<td>1:1024</td>
<td>2&lt;sup&gt;10&lt;/sup&gt; 32 ms</td>
<td></td>
</tr>
<tr>
<td>00110</td>
<td>1:2048</td>
<td>2&lt;sup&gt;11&lt;/sup&gt; 64 ms</td>
<td></td>
</tr>
<tr>
<td>00111</td>
<td>1:4096</td>
<td>2&lt;sup&gt;12&lt;/sup&gt; 128 ms</td>
<td></td>
</tr>
<tr>
<td>01000</td>
<td>1:8192</td>
<td>2&lt;sup&gt;13&lt;/sup&gt; 256 ms</td>
<td></td>
</tr>
<tr>
<td>01001</td>
<td>1:16384</td>
<td>2&lt;sup&gt;14&lt;/sup&gt; 512 ms</td>
<td></td>
</tr>
<tr>
<td>01010</td>
<td>1:32768</td>
<td>2&lt;sup&gt;15&lt;/sup&gt; 1 s</td>
<td>No</td>
</tr>
<tr>
<td>01011</td>
<td>1:65536</td>
<td>2&lt;sup&gt;16&lt;/sup&gt; 2 s</td>
<td></td>
</tr>
<tr>
<td>01100</td>
<td>1:131072</td>
<td>2&lt;sup&gt;17&lt;/sup&gt; 4 s</td>
<td></td>
</tr>
<tr>
<td>01101</td>
<td>1:262144</td>
<td>2&lt;sup&gt;18&lt;/sup&gt; 8 s</td>
<td></td>
</tr>
<tr>
<td>01110</td>
<td>1:524299</td>
<td>2&lt;sup&gt;19&lt;/sup&gt; 16 s</td>
<td></td>
</tr>
<tr>
<td>01111</td>
<td>1:1048576</td>
<td>2&lt;sup&gt;20&lt;/sup&gt; 32 s</td>
<td></td>
</tr>
<tr>
<td>10000</td>
<td>1:2097152</td>
<td>2&lt;sup&gt;21&lt;/sup&gt; 64 s</td>
<td></td>
</tr>
<tr>
<td>10001</td>
<td>1:4194304</td>
<td>2&lt;sup&gt;22&lt;/sup&gt; 128 s</td>
<td></td>
</tr>
<tr>
<td>10010</td>
<td>1:8388608</td>
<td>2&lt;sup&gt;23&lt;/sup&gt; 256 s</td>
<td></td>
</tr>
<tr>
<td>10011</td>
<td>1:16777216</td>
<td>2&lt;sup&gt;24&lt;/sup&gt; 512 s</td>
<td></td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>1:32 2&lt;sup&gt;5&lt;/sup&gt; 1 ms</td>
<td>No</td>
</tr>
<tr>
<td>11110</td>
<td>11110</td>
<td>1:65536 2&lt;sup&gt;16&lt;/sup&gt; 2 s</td>
<td>Yes</td>
</tr>
<tr>
<td>11111</td>
<td>01011</td>
<td>1:65536 2&lt;sup&gt;16&lt;/sup&gt; 2 s</td>
<td>Yes</td>
</tr>
</tbody>
</table>
## REGISTER 5-6: CONFIGURATION WORD 3H (30 0005h)

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>U-1</td>
<td>U-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
</tbody>
</table>

### Legend:
- `R` = Readable bit
- `W` = Writable bit
- `U` = Unimplemented bit, read as ‘1’
- `-n` = Value for blank device
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- `x` = Bit is unknown

#### bit 7-6
Unimplemented: Read as ‘1’

#### bit 5-3
**WDTCSS<2:0>:** WDT Input Clock Selector bits

If `WDTE<1:0> Fuses = 2'b00`:
These bits are ignored.

Otherwise:
- `000` = WDT reference clock is the 31.0 kHz LFINTOSC
- `001` = WDT reference clock is the 31.25 kHz MFINTOSC
- `010` = WDT reference clock is SOSC
- `011` = Reserved (default to LFINTOSC)
- `100` = Reserved (default to LFINTOSC)
- `101` = Software control
- `110` = Software control
- `111` = Software control

#### bit 2-0
**WDTCWS<2:0>:** WDT Window Select bits

<table>
<thead>
<tr>
<th>WDTCS&lt;2:0&gt;</th>
<th>Value</th>
<th>Window Delay Percent of Time</th>
<th>Window Opening Percent of Time</th>
<th>Software Control of Window</th>
<th>Keyed Access Required?</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>000</td>
<td>87.5</td>
<td>12.5</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>001</td>
<td>001</td>
<td>75</td>
<td>25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>010</td>
<td>010</td>
<td>62.5</td>
<td>37.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>011</td>
<td>011</td>
<td>50</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>100</td>
<td>37.5</td>
<td>62.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>101</td>
<td>101</td>
<td>25</td>
<td>75</td>
<td></td>
<td></td>
</tr>
<tr>
<td>110</td>
<td>111</td>
<td>n/a</td>
<td>100</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>111</td>
<td>111</td>
<td>n/a</td>
<td>100</td>
<td></td>
<td>No</td>
</tr>
</tbody>
</table>
### REGISTER 5-7: CONFIGURATION WORD 4L (30 0006h)

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>U-1</th>
<th>U-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>WRTPP (1)</td>
<td>—</td>
<td>—</td>
<td>SAFEN (1)</td>
<td>BBEN (1)</td>
<td>BBSIZE&lt;2:0&gt; (2)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- \( R \) = Readable bit
- \( W \) = Writable bit
- \( U \) = Unimplemented bit, read as ‘1’
- \(-n\) = Value for blank device
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- \( x \) = Bit is unknown

- **bit 7**
  - **WRTPP:** Application Block Write Protection bit\(^{(1)}\)
    - 1 = Application Block is NOT write-protected
    - 0 = Application Block is write-protected

- **bit 6-5**
  - **Unimplemented:** Read as ‘1’

- **bit 4**
  - **SAFEN:** Storage Area Flash Enable bit\(^{(1)}\)
    - 1 = SAF is disabled
    - 0 = SAF is enabled

- **bit 3**
  - **BBEN:** Boot Block Enable bit\(^{(1)}\)
    - 1 = Boot Block disabled
    - 0 = Boot Block enabled

- **bit 2-0**
  - **BBSIZE<2:0>:** Boot Block Size Selection bits\(^{(2)}\)
    - Refer to Table 5-1.

**Note 1:** Bits are implemented as sticky bits. Once protection is enabled through ICSP™ or a self-write, it can only be reset through a Bulk Erase.

**Note 2:** BBSIZE<2:0> bits can only be changed when BBEN = 1. Once BBEN = 0, BBSIZE<2:0> can only be changed through a Bulk Erase.

### TABLE 5-1: BOOT BLOCK SIZE BITS

<table>
<thead>
<tr>
<th>BBEN</th>
<th>BBSIZE[2:0]</th>
<th>Boot Block Size (words)</th>
<th>END_ADDRESS_BOOT</th>
<th>Device Size(^{(1)})</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>16k</td>
</tr>
<tr>
<td>1</td>
<td>xxx</td>
<td>0</td>
<td>—</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>111</td>
<td>512</td>
<td>00 03FFh</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>110</td>
<td>1024</td>
<td>00 07FFh</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>101</td>
<td>2048</td>
<td>00 0FFFh</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>100</td>
<td>4096</td>
<td>00 1FFFh</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>011</td>
<td>8192</td>
<td>00 3FFFh</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>010</td>
<td>16384</td>
<td>00 7FFFh</td>
<td>—</td>
</tr>
<tr>
<td>0</td>
<td>001</td>
<td>32768</td>
<td>00 FFFFh</td>
<td>—</td>
</tr>
<tr>
<td>0</td>
<td>000</td>
<td>32768</td>
<td>00 FFFFh</td>
<td>—</td>
</tr>
</tbody>
</table>

**Note 1:** For each device, the quoted device size specification is listed in Table 4-1.

**Note 2:** The maximum Boot Block size is half the user program memory size. All selections higher than the maximum size default to maximum Boot Block size of half PFM. For example, all settings of BBSIZE = 000 through BBSIZE = 010, default to a Boot Block size of 16 kW on a 32 kW device.
### REGISTER 5-8: CONFIGURATION WORD 4H (30 0007h)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>U-1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>LVP&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>6</td>
<td>U-1</td>
<td>U-1</td>
<td>U-1</td>
<td>U-1</td>
<td>U-1</td>
<td>U-1</td>
<td>U-1</td>
</tr>
<tr>
<td>5</td>
<td>WRTSAF&lt;sup&gt;(1,3)&lt;/sup&gt;</td>
<td>Storage Area Flash (SAF) Write Protection bit&lt;sup&gt;(1,3)&lt;/sup&gt;</td>
<td>1 = SAF is NOT write-protected</td>
<td>0 = SAF is write-protected</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>LVP&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>Low-Voltage Programming Enable bit&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>1 = Low-voltage programming enabled. MCLR/Vpp pin function is ignored.</td>
<td>0 = HV on MCLR/Vpp must be used for programming.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>WRTD&lt;sup&gt;(1,4)&lt;/sup&gt;</td>
<td>Data EEPROM Write Protection bit&lt;sup&gt;(1,4)&lt;/sup&gt;</td>
<td>1 = Data EEPROM NOT write-protected</td>
<td>0 = Data EEPROM write-protected</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>WRTC</td>
<td>Configuration Register Write Protection bit&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>1 = Configuration Register NOT write-protected</td>
<td>0 = Configuration Register write-protected</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>WRTB</td>
<td>Boot Block Write Protection bit&lt;sup&gt;(1,5)&lt;/sup&gt;</td>
<td>1 = Boot Block NOT write-protected</td>
<td>0 = Boot Block write-protected</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘1’
- -n = Value for blank device
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**Note 1:** Bits are implemented as sticky bits. Once protection is enabled through ICSP or a self write, it can only be reset through a Bulk Brase.

2: The LVP bit cannot be written (to zero) while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the configuration state.

3: Unimplemented if SAF is not present and only applicable if SAFEN = 0.

4: Unimplemented if data EEPROM is not present.

5: Only applicable if BBEN = 0.
REGISTER 5-9: CONFIGURATION WORD 5L (30 0008h)

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>R/W-1</th>
<th>CP</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>U-1</td>
<td>—</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘1’
-n = Value for blank device  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

bit 7-1  Unimplemented: Read as ‘1’
bit 0  CP: User Program Flash Memory and Data EEPROM Code Protection bit
1 = User Program Flash Memory and Data EEPROM code protection is disabled
0 = User Program Flash Memory and Data EEPROM code protection is enabled

REGISTER 5-10: CONFIGURATION WORD 5H (30 0009h)

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>U-1</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘1’
-n = Value for blank device  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

bit 7-0  Unimplemented: Read as ‘1’

TABLE 5-2: SUMMARY OF CONFIGURATION WORDS

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Default/Unprogrammed Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>30 0000h</td>
<td>CONFIG1L</td>
<td>—</td>
<td>—</td>
<td>RSTOSC&lt;2:0&gt;</td>
<td>—</td>
<td>—</td>
<td>FEXTOSC&lt;2:0&gt;</td>
<td>1111 1111</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30 0001h</td>
<td>CONFIG1H</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>FCEN</td>
<td>—</td>
<td>CSWEN</td>
<td>PR1WAY</td>
<td>CLKOUTEN</td>
<td>1111 1111</td>
</tr>
<tr>
<td>30 0002h</td>
<td>CONFIG2L</td>
<td>—</td>
<td>LVBREN</td>
<td>—</td>
<td>IVT1WAY</td>
<td>MEVEN</td>
<td>PWRTS&lt;1:0&gt;</td>
<td>MCLRE</td>
<td>1111 1111</td>
<td></td>
</tr>
<tr>
<td>30 0003h</td>
<td>CONFIG2H</td>
<td>XINST</td>
<td>—</td>
<td>DEBUG</td>
<td>STVREN</td>
<td>PPS1WAY</td>
<td>ZCD</td>
<td>BORV&lt;1:0&gt;</td>
<td>1111 1111</td>
<td></td>
</tr>
<tr>
<td>30 0004h</td>
<td>CONFIG3L</td>
<td>—</td>
<td>—</td>
<td>WDTE&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>WDTCP&lt;4:0&gt;</td>
<td>1111 1111</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30 0005h</td>
<td>CONFIG3H</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WDTCCS&lt;2:0&gt;</td>
<td>WDTCS&lt;2:0&gt;</td>
<td>1111 1111</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30 0006h</td>
<td>CONFIG4L</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SAFEN</td>
<td>BBEN</td>
<td>BBBSIZE&lt;2:0&gt;</td>
<td>1111 1111</td>
</tr>
<tr>
<td>30 0007h</td>
<td>CONFIG4H</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>LVP</td>
<td>—</td>
<td>WRTSAF</td>
<td>WRTD</td>
</tr>
<tr>
<td>30 0008h</td>
<td>CONFIG5L</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>30 0009h</td>
<td>CONFIG5H</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>
5.3 Code Protection

Code protection allows the device to be protected from external access. Program memory protection and data memory are controlled through the CP Configuration bit. Internal access to the program memory is unaffected by code protection setting.

The entire program memory space and Data EEPROM is protected from external reads and writes by the CP bit in Configuration Words. When CP = 0, external reads and writes of memory are inhibited and a read will return all ’0’s. The CPU can continue to read program memory and data EEPROM, regardless of the protection bit settings. Self-writing the program memory or Data EEPROM is dependent upon the write protection settings.

5.4 User ID

Eight words in the memory space (200000h-200000Fh) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See Section 13.2 “Device Information Area, Device Configuration Area, User ID, Device ID and Configuration Word Access” for more information on accessing these memory locations. For more information on checksum calculation, see the “PIC18(L)F25/26K83 Memory Programming Specification” (DS40000000).
5.5 Device ID and Revision ID

The 16-bit device ID word is located at 3F FFFEh and the 16-bit revision ID is located at 3F FFFCh. These locations are read-only and cannot be erased or modified.

Development tools, such as device programmers and debuggers, may be used to read the Device ID, Revision ID and Configuration Words. Refer to 13.0 “Nonvolatile Memory (NVM) Control” for more information on accessing these locations.

5.6 Register Definitions: Device ID and Revision ID

REGISTER 5-11: DEVICE ID: DEVICE ID REGISTER

<table>
<thead>
<tr>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DEV&lt;15:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 15</td>
<td>bit 8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DEV&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit

‘1’ = Bit is set

0’ = Bit is cleared

x = Bit is unknown

bit 15-0 DEV<15:0>: Device ID bits

<table>
<thead>
<tr>
<th>Device</th>
<th>Device ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC18F25K83</td>
<td>6EE0h</td>
</tr>
<tr>
<td>PIC18F26K83</td>
<td>6EC0h</td>
</tr>
<tr>
<td>PIC18LF25K83</td>
<td>6F20h</td>
</tr>
<tr>
<td>PIC18LF26K83</td>
<td>6F00h</td>
</tr>
</tbody>
</table>
## REGISTER 5-12: REVISION ID: REVISION ID REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 15</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

*MJRREV<5:2>*

<table>
<thead>
<tr>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

*MJRREV<1:0>*

<table>
<thead>
<tr>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

*MNRREV<5:0>*

### Legend:

- **R** = Readable bit
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

#### bit 15-12

*Read as ‘1010’*

These bits are fixed with value ‘1010’ for all devices in this family.

#### bit 11-6

**MJRREV<5:0>: Major Revision ID bits**

These bits are used to identify a major revision. A major revision is indicated by revision (A0, B0, C0, etc.)

Revision A = 0b00 0000

#### bit 5-0

**MNRREV<5:0>: Minor Revision ID bits**

These bits are used to identify a minor revision.

Revision A0 = 0b00 0000
5.7 Device Information Area

The Device Information Area (DIA) is a dedicated region in the program memory space. The DIA contains the calibration data for the internal temperature indicator module, stores the Microchip Unique Identifier words and the Fixed Voltage Reference voltage readings measured in mV.

The complete DIA table is shown in Table 5-3: Device Information Area, followed by a description of each region and its functionality. The data is mapped from 3F0000h to 3F003Fh in the PIC18(L)F25/26K83 family. These locations are read-only and cannot be erased or modified by the user. The data is programmed into the device during manufacturing.

TABLE 5-3: DEVICE INFORMATION AREA

<table>
<thead>
<tr>
<th>Address Range</th>
<th>Name of Region</th>
<th>Standard Device Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>3F0000h-3F000Bh</td>
<td>MUI0</td>
<td>Microchip Unique Identifier (6 Words)</td>
</tr>
<tr>
<td></td>
<td>MUI1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MUI2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MUI3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MUI4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MUI5</td>
<td></td>
</tr>
<tr>
<td>3F000Ch-3F000Fh</td>
<td>MUI6</td>
<td>Unassigned (2 Words)</td>
</tr>
<tr>
<td></td>
<td>MUI7</td>
<td></td>
</tr>
<tr>
<td>3F0010h-3F0023h</td>
<td>EUI0</td>
<td>Optional External Unique Identifier (10 Words)</td>
</tr>
<tr>
<td></td>
<td>EUI1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EUI2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EUI3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EUI4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EUI5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EUI6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EUI7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EUI8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EUI9</td>
<td></td>
</tr>
<tr>
<td>3F0024h-3F0025h</td>
<td>TSLR1</td>
<td>Unassigned (1 Word)</td>
</tr>
<tr>
<td>3F0026h-3F0027h</td>
<td>TSLR2</td>
<td>Temperature Indicator ADC reading at @ 90°C (low range setting)</td>
</tr>
<tr>
<td>3F0028h-3F0029h</td>
<td>TSLR3</td>
<td>Unassigned (1 word)</td>
</tr>
<tr>
<td>3F002Ah-3F002Bh</td>
<td>TSHR1</td>
<td>Unassigned (1 Word)</td>
</tr>
<tr>
<td>3F002Ch-3F002Dh</td>
<td>TSHR2</td>
<td>Temperature Indicator ADC reading at @ 90°C (high range setting)</td>
</tr>
<tr>
<td>3F002Eh-3F002Fh</td>
<td>TSHR3</td>
<td>Unassigned (1 Word)</td>
</tr>
<tr>
<td>3F0030h-3F0031h</td>
<td>FVRA1X</td>
<td>ADC FVR1 Output voltage for 1x setting (in mV)</td>
</tr>
<tr>
<td>3F0032h-3F0033h</td>
<td>FVRA2X</td>
<td>ADC FVR1 Output Voltage for 2x setting (in mV)</td>
</tr>
<tr>
<td>3F0034h-3F0035h</td>
<td>FVRA4X</td>
<td>ADC FVR1 Output Voltage for 4x setting (in mV)</td>
</tr>
<tr>
<td>3F0036h-3F0037h</td>
<td>FVRC1X</td>
<td>Comparator FVR2 output voltage for 1x setting (in mV)</td>
</tr>
<tr>
<td>3F0038h-3F0039h</td>
<td>FVRC2X</td>
<td>Comparator FVR2 output voltage for 2x setting (in mV)</td>
</tr>
<tr>
<td>3F003Ah-3F003Bh</td>
<td>FVRC4X</td>
<td>Comparator FVR2 output voltage for 4x setting (in mV)</td>
</tr>
<tr>
<td>3F003Ch-3F003Fh</td>
<td></td>
<td>Unassigned (2 Words)</td>
</tr>
</tbody>
</table>
5.7.1 MICROCHIP UNIQUE IDENTIFIER (MUI)

The PIC18(L)F25/26K83 devices are individually encoded during final manufacturing with a Microchip Unique Identifier, or MUI. The MUI cannot be user-erased. This feature allows for manufacturing traceability of Microchip Technology devices in applications where this is a required. It may also be used by the application manufacturer for a number of functions that require unverified unique identification, such as:

- Tracking the device
- Unique serial number

The MUI consists of six program words. When read together, these fields form a unique identifier. The MUI is stored in nine read-only locations, located between 3F0000h to 3F000Fh in the DIA space. Table 5-3 lists the addresses of the identifier words.

| Note: | For applications that require verified unique identification, contact your Microchip Technology sales office to create a Serialized Quick Turn Programming™ option. |

5.7.2 EXTERNAL UNIQUE IDENTIFIER (EUI)

The EUI data is stored at locations 3F0010h to 3F0023h in the Program Memory region. This region is an optional space for placing application specific information. The data is coded per customer requirements during manufacturing.

| Note: | Data is stored in this address range on receiving a request from the customer. The customer may contact the local sales representative, or Field Applications Engineer, and provide them the unique identifier information that is supposed to be stored in this region. |

5.7.3 ANALOG-TO-DIGITAL CONVERSION DATA OF THE TEMPERATURE SENSOR

The purpose of the Temperature Sensor module is to provide a temperature-dependent voltage that can be measured by an analog module, see Section 36.0 “Temperature Indicator Module”.

The DIA table contains the internal ADC measurement values of the Temperature sensor for Low and High range at fixed points of reference. The values are measured during test and are unique to each device. The measurement data is stored in the DIA memory region as hexadecimal numbers corresponding to the ADC conversion result. The calibration data can be used to plot the approximate sensor output voltage, VTSENSE vs. Temperature curve without having to make calibration measurements in the application. For more information on the operation of the Temperature Sensor, refer to Section 36.0 “Temperature Indicator Module”.

- **TSLR1-TSLR3**: Address 3F0024h to 3F0029h store the measurements for the low-range setting of the Temperature Sensor at VDD = 3V.
- **TSHR1-TSHR3**: Address 3F002Ah to 3F002Fh store the measurements for the High Range setting of the Temperature Sensor at VDD = 3V.
- The stored measurements are made by the device ADC using the internal VREF = 2.048V.

**Note:** For applications that require verified unique identification, contact your Microchip Technology sales office to create a Serialized Quick Turn Programming™ option.

**Note:** Data is stored in this address range on receiving a request from the customer. The customer may contact the local sales representative, or Field Applications Engineer, and provide them the unique identifier information that is supposed to be stored in this region.
5.7.4 FIXED VOLTAGE REFERENCE DATA

The DIA stores measured FVR voltages for this device in mV for the different buffer settings of 1x, 2x or 4x at Program Memory locations 3F0030h to 3F003Bh. For more information on the FVR, refer to Section 35.0 “Fixed Voltage Reference (FVR)”.

- FVRA1X stores the value of ADC FVR1 Output voltage for 1x setting (in mV)
- FVRA2X stores the value of ADC FVR1 Output Voltage for 2x setting (in mV)
- FVRA4X stores the value of ADC FVR1 Output Voltage for 4x setting (in mV)
- FVRC1X stores the value of Comparator FVR2 output voltage for 2x setting (in mV)
- FVRC2X stores the value of Comparator FVR2 output voltage for 2x setting (in mV)
- FVRC4X stores the value of Comparator FVR2 output voltage for 4x setting (in mV)

5.8 Device Configuration Information

The Device Configuration Information (DCI) is a dedicated region in the program memory space mapped from 3FFF00h to 3FFF09h. The data stored in these locations is read-only and cannot be erased.

Refer to Table 5-4: Device Configuration Information for PIC18(L)F25/26K83 for the complete DCI table address and description. The DCI holds information about the device which is useful for programming and bootloader applications.

The erase size is the minimum erasable unit in the PFM, expressed as rows. The total device Flash memory capacity is (Row Size * Number of rows)

**TABLE 5-4: DEVICE CONFIGURATION INFORMATION FOR PIC18(L)F25/26K83**

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>Name</th>
<th>DESCRIPTION</th>
<th>VALUE</th>
<th>VALUE</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>3F FF00h-3F FF01h</td>
<td>ERSIZ</td>
<td>Erase Row Size</td>
<td>64</td>
<td>64</td>
<td>Words</td>
</tr>
<tr>
<td>3F FF02h-3F FF03h</td>
<td>WLSIZ</td>
<td>Number of write latches per row</td>
<td>128</td>
<td>128</td>
<td>Bytes</td>
</tr>
<tr>
<td>3F FF04h-3F FF05h</td>
<td>URSIZ</td>
<td>Number of User Rows</td>
<td>256</td>
<td>512</td>
<td>Rows</td>
</tr>
<tr>
<td>3F FF06h-3F FF07h</td>
<td>EESIZ</td>
<td>Data EEPROM memory size</td>
<td>1024</td>
<td>1024</td>
<td>Bytes</td>
</tr>
<tr>
<td>3F FF08h-3F FF09h</td>
<td>PCNT</td>
<td>Pin Count</td>
<td>28</td>
<td>28</td>
<td>Pins</td>
</tr>
</tbody>
</table>
6.0 RESETS

There are multiple ways to reset this device:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Low-Power Brown-Out Reset (LPBOR)
- MCLR Reset
- WDT Reset
- RESET instruction
- Stack Overflow
- Stack Underflow
- Programming mode exit
- Memory Execution Violation Reset (MEMV)

To allow VDD to stabilize, an optional Power-up Timer can be enabled to extend the Reset time after a BOR or POR event.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 6-1.
FIGURE 6-2: LPBOR, BOR, POR RELATIONSHIP
6.1 Power-on Reset (POR)

The POR circuit holds the device in Reset until VDD has reached an acceptable level for minimum operation. Slow rising VDD, fast operating speeds or analog performance may require greater than minimum VDD. The PWRT, BOR or MCLR features can be used to extend the start-up period until all device operation conditions have been met.

6.2 Brown-out Reset (BOR)

The BOR circuit holds the device in Reset when VDD reaches a selectable minimum level. Between the POR and BOR, complete voltage range coverage for execution protection can be implemented.

The Brown-out Reset module has four operating modes controlled by the BOREN<1:0> bits in Configuration Words. The four operating modes are:

- BOR is always on
- BOR is off when in Sleep
- BOR is controlled by software
- BOR is always off

Refer to Table 6-1 for more information.

The Brown-out Reset voltage level is selectable by configuring the BORV<1:0> bits in Configuration Words.

A VDD noise rejection filter prevents the BOR from triggering on small events. If VDD falls below VBOR for a duration greater than parameter TBORDC, the device will reset. See Table 45-11 for more information.

6.2.1 BOR IS ALWAYS ON

When the BOREN bits of Configuration Words are programmed to ‘11’, the BOR is always on. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is active during Sleep. The BOR does not delay wake-up from Sleep.

6.2.2 BOR IS OFF IN SLEEP

When the BOREN bits of Configuration Words are programmed to ‘10’, the BOR is on, except in Sleep. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is not active during Sleep. The device wake-up will be delayed until the BOR is ready.

6.2.3 BOR CONTROLLED BY SOFTWARE

When the BOREN bits of Configuration Words are programmed to ‘01’, the BOR is controlled by the SBOREN bit of the BORCON register. The device start-up is not delayed by the BOR ready condition or the VDD level.

BOR protection begins as soon as the BOR circuit is ready. The status of the BOR circuit is reflected in the BORRDY bit of the BORCON register.

BOR protection is unchanged by Sleep.

6.2.4 BOR AND BULK ERASE

BOR is forced ON during PFM Bulk Erase operations to make sure that a safe erase voltage is maintained for a successful erase cycle.

During Bulk Erase, the BOR is enabled at 2.45V for F and LF devices, even if it is configured to some other value. If VDD falls, the erase cycle will be aborted, but the device will not be reset.
TABLE 6-1:  BOR OPERATING MODES

<table>
<thead>
<tr>
<th>BOREN&lt;1:0&gt;</th>
<th>SBOREN</th>
<th>Device Mode</th>
<th>BOR Mode</th>
<th>Instruction Execution upon: Release of POR</th>
<th>Wake-up from Sleep</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>X</td>
<td>X</td>
<td>Active</td>
<td>Wait for release of BOR (BORRDY = 1)</td>
<td>Begins immediately</td>
</tr>
<tr>
<td>10</td>
<td>X</td>
<td>Awake</td>
<td>Active</td>
<td>Wait for release of BOR (BORRDY = 1)</td>
<td>N/A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sleep</td>
<td>Hibernate</td>
<td>Wait for release of BOR (BORRDY = 1)</td>
<td></td>
</tr>
<tr>
<td>01</td>
<td>1</td>
<td>X</td>
<td>Active</td>
<td>Wait for release of BOR (BORRDY = 1)</td>
<td>Begins immediately</td>
</tr>
<tr>
<td>00</td>
<td>X</td>
<td>X</td>
<td>Hibernate</td>
<td>Disabled</td>
<td>Begins immediately</td>
</tr>
</tbody>
</table>

Note 1:  TPWRT delay depends on PWRTS<1:0> Configuration bits.

FIGURE 6-3:  BROWN-OUT SITUATIONS
6.3 Register Definitions: BOR Control

REGISTER 6-1: BORCON: BROWN-OUT RESET CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-1/u</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R-q/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBOREN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>BORRDY</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- q = Value depends on condition
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- n/n = Value at POR and BOR/Value at all other Resets

bit 7  **SBOREN**: Software Brown-out Reset Enable bit
- If BOREN ≠ 01:
  - SBOREN is read/write, but has no effect on the BOR.
- If BOREN = 01:
  - 1 = BOR Enabled
  - 0 = BOR Disabled

bit 6-1  **Unimplemented**: Read as '0'

bit 0  **BORRDY**: Brown-out Reset Circuit Ready Status bit
- 1 = The Brown-out Reset Circuit is active and armed
- 0 = The Brown-out Reset Circuit is disabled or is warming up
6.4 Low-Power Brown-out Reset (LPBOR)

The Low-Power Brown-out Reset (LPBOR) provides an additional BOR circuit for low power operation. Refer to Figure 6-2 to see how the BOR interacts with other modules.

The LPBOR is used to monitor the external VDD pin. When too low of a voltage is detected, the device is held in Reset.

6.4.1 ENABLING LPBOR

The LPBOR is controlled by the LPBOREN bit of Configuration Word 2L. When the device is erased, the LPBOR module defaults to disabled.

6.6 Windowed Watchdog Timer (WWDT) Reset

The Windowed Watchdog Timer generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period or window set. The TO and PD bits in the STATUS register and the WD T bit in the PCON0 register are changed to indicate a WWDT Reset. The WDTWV bit in the PCON0 register indicates if the WDT Reset has occurred due to a time out or a window violation. See Section 11.0 “Windowed Watchdog Timer (WWDT)” for more information.

6.7 RESET Instruction

A RESET instruction will cause a device Reset. The RI bit in the PCON0 register will be set to '0'. See Table 6-3 for default conditions after a RESET instruction has occurred.

6.8 Stack Overflow/Underflow Reset

The device can reset when the Stack Overflows or Underflows. The STKOVF or STKUNF bits of the PCON0 register indicate the Reset condition. These Resets are enabled by setting the STVREN bit in Configuration Words. See Section 4.2.5 “Return Address Stack” for more information.

6.9 Programming Mode Exit

Upon exit of Programming mode, the device will behave as if a POR has just occurred.

6.10 Power-up Timer (PWRT)

The Power-up Timer provides a selected time-out duration on POR or Brown-out Reset.

The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the VDD to rise to an acceptable level. The Power-up Timer is selected by setting the PWRTS<1:0> Configuration bits, appropriately.

The Power-up Timer starts after the release of the POR and BOR/LPBOR if enabled, as shown in Figure 6-1.

<table>
<thead>
<tr>
<th>TABLE 6-2: MCLR CONFIGURATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCLRE</td>
</tr>
<tr>
<td>x</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

Note: An internal Reset event (RESET instruction, BOR, WWDT, POR stack), does not drive the MCLR pin low.

6.5 MCLR

The MCLR is an optional external input that can reset the device. The MCLR function is controlled by the MCLRE bit of Configuration Words and the LVP bit of Configuration Words (Table 6-2). The RMCLR bit in the PCON0 register will be set to '0' if a MCLR Reset has occurred.

6.5.1 MCLR ENABLED

When MCLR is enabled and the pin is held low, the device is held in Reset. The MCLR pin is connected to VDD through an internal weak pull-up.

The device has a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

6.5.2 MCLR DISABLED

When MCLR is disabled, the MCLR pin becomes input-only and pin functions such as internal weak pull-ups are under software control. See Section 16.2 “I/O Priorities” for more information.
6.11 Start-up Sequence

Upon the release of a POR or BOR, the following must occur before the device will begin executing:

1. Power-up Timer runs to completion (if enabled).
2. Oscillator start-up timer runs to completion (if required for selected oscillator source).
3. MCLR must be released (if enabled).

The total time out will vary based on oscillator configuration and Power-up Timer configuration. See Section 7.0 “Oscillator Module (with Fail-Safe Clock Monitor)” for more information.

The Power-up Timer and oscillator start-up timer run independently of MCLR Reset. If MCLR is kept low long enough, the Power-up Timer and oscillator Start-up Timer will expire. Upon bringing MCLR high, the device will begin execution after 10 FOSC cycles (see Figure 6-4). This is useful for testing purposes or to synchronize more than one device operating in parallel.

FIGURE 6-4: RESET START-UP SEQUENCE
6.11.1 MEMORY EXECUTION VIOLATION

If the CPU executes outside the valid execution area, a memory execution violation Reset occurs.

The invalid execution areas are:

1. Addresses outside implemented program memory (see Table 5-1).
2. Storage Area Flash (SAF) inside program memory, if it is enabled.

When a memory execution violation is generated, flag MEMV is cleared in PCON1 (Register 6-3) to signal the cause of Reset. It needs to be set in the user code after a memory execution violation Reset has occurred to detect further violation Resets.

6.12 Determining the Cause of a Reset

Upon any Reset, multiple bits in the STATUS and PCON0 registers are updated to indicate the cause of the Reset. Table 6-3 shows the Reset conditions of these registers.

<table>
<thead>
<tr>
<th>Condition</th>
<th>Program Counter</th>
<th>STATUS Register(1,2)</th>
<th>PCON0 Register</th>
<th>PCON1 Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-on Reset</td>
<td>0</td>
<td>-110 0000</td>
<td>0011 110x</td>
<td>---- --1--</td>
</tr>
<tr>
<td>Brown-out Reset</td>
<td>0</td>
<td>-110 0000</td>
<td>0011 11u0</td>
<td>---- --1--</td>
</tr>
<tr>
<td>MCLR Reset during normal operation</td>
<td>0</td>
<td>-uuu uuuu</td>
<td>uuuu 0uuu</td>
<td>---- --u--</td>
</tr>
<tr>
<td>MCLR Reset during Sleep</td>
<td>0</td>
<td>-10u uuuu</td>
<td>uuuu 0uuu</td>
<td>---- --u--</td>
</tr>
<tr>
<td>WDT Time-out Reset</td>
<td>0</td>
<td>-0uu uuuu</td>
<td>uuu0 uuuu</td>
<td>---- --u--</td>
</tr>
<tr>
<td>WWDT Window Violation Reset</td>
<td>0</td>
<td>-uuu uuuu</td>
<td>uuuu uuuu</td>
<td>---- --u--</td>
</tr>
<tr>
<td>RESET Instruction Executed</td>
<td>0</td>
<td>-uuu uuuu</td>
<td>uuuu uuuu</td>
<td>---- --u--</td>
</tr>
<tr>
<td>Stack Overflow Reset (STVREN = 1)</td>
<td>0</td>
<td>-uuu uuuu</td>
<td>1uuu uuuu</td>
<td>---- --u--</td>
</tr>
<tr>
<td>Stack Underflow Reset (STVREN = 1)</td>
<td>0</td>
<td>-uuu uuuu</td>
<td>1uuu uuuu</td>
<td>---- --u--</td>
</tr>
<tr>
<td>Memory Violation Reset</td>
<td>0</td>
<td>-uuu uuuu</td>
<td>uuuu uuuu</td>
<td>---- --0--</td>
</tr>
</tbody>
</table>

Legend:  
- unchanged,  
- unknown,  
- unimplemented bit, reads as ‘0’.

Note 1: If a Status bit is not implemented, that bit will be read as ‘0’.

2: Status bits Z, C, DC are reset by POR/BOR, but not defined by the Resets module (Register 4-2).
6.13 Power Control (PCON0/PCON1) Register

The Power Control (PCON0/PCON1) register contains flag bits to differentiate between a:

- Brown-out Reset (BOR)
- Power-on Reset (POR)
- Reset Instruction Reset (RI)
- MCLR Reset (RMCLR)
- Watchdog Timer Reset (RWDT)
- Watchdog Window Violation (WDTWV)
- Stack Underflow Reset (STKUNF)
- Stack Overflow Reset (STKOVF)
- Memory Violation Reset (MEMV)

The PCON0/1 register bits are shown in Register 6-2 and Register 6-3. Hardware will change the corresponding register bit during the Reset process; if the Reset was not caused by the condition, the bit remains unchanged (Table 6-3).

Software should reset the bit to the inactive state after restart (hardware will not reset the bit). Software may also set any PCON0 bit to the active state, so that user code may be tested, but no Reset action will be generated.
## 6.14 Register Definitions: Power Control

**REGISTER 6-2: PCON0: POWER CONTROL REGISTER 0**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value at POR and BOR/Value at all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>STKOVF: Stack Overflow Flag bit</td>
<td>Set to '0' by firmware</td>
</tr>
<tr>
<td>1</td>
<td>A Stack Overflow occurred (more CALLs than fit on the stack)</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>A Stack Overflow has not occurred or set to '0' by firmware</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>STKUNF: Stack Underflow Flag bit</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>A Stack Underflow occurred (more RETURNS than CALLs)</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>A Stack Underflow has not occurred or set to '0' by firmware</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>RWDT: WDT Window Violation bit</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>A WDT window violation has not occurred or set to '1' by firmware</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>A WDT instruction was issued when the WDT Reset window was closed (set to '0' in hardware when a WDT window violation Reset occurs)</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>RMCLR: MCLR Reset Flag bit</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>A MCLR Reset has not occurred or set to '1' by firmware</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>A MCLR Reset has occurred (set to '0' in hardware when a MCLR Reset occurs)</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>RI: RESET Instruction Flag bit</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>A RESET instruction has not been executed or set to '1' by firmware</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>A RESET instruction has been executed (set to '0' in hardware upon executing a RESET instruction)</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>POR: Power-on Reset Status bit</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>No Power-on Reset occurred or set to '1' by firmware</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>A Power-on Reset occurred (set to '0' in hardware when a Power-on Reset occurs)</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>BOR: Brown-out Reset Status bit</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>No Brown-out Reset occurred or set to '1' by firmware</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>A Brown-out Reset occurred (set to '0' in hardware when a Brown-out Reset occurs)</td>
<td></td>
</tr>
</tbody>
</table>
REGISTER 6-3:  PCON1: POWER CONTROL REGISTER 1

| Bit 7-2 | Unimplemented: Read as ‘0’ |
| bit 1   | MEMV: Memory Violation Flag bit |
| 1 =     | No memory violation Reset occurred or set to ‘1’ by firmware |
| 0 =     | A memory violation Reset occurred (set to ‘0’ in hardware when a memory violation occurs) |
| bit 0   | Unimplemented: Read as ‘0’ |

TABLE 6-4: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>BORCON</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BORRDY 75</td>
</tr>
<tr>
<td>PCON0</td>
<td>STKOVF</td>
<td>STKUNF</td>
<td>WDTWV</td>
<td>RWDT</td>
<td>RMCLR</td>
<td>RI</td>
<td>POR</td>
<td>BOR</td>
<td>80</td>
</tr>
<tr>
<td>PCON1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MEMV</td>
<td></td>
<td>81</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by Resets.
7.0 OSCILLATOR MODULE (WITH FAIL-SAFE CLOCK MONITOR)

7.1 Overview

The oscillator module has multiple clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 7-1 illustrates a block diagram of the oscillator module.

Clock sources can be supplied from external oscillators, quartz-crystal resonators and ceramic resonators. In addition, the system clock source can be supplied from one of two internal oscillators and PLL circuits, with a choice of speeds selectable via software. Additional clock features include:

- Selectable system clock source between external or internal sources via software.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, ECH, ECM, ECL) and switch automatically to the internal oscillator.
- Oscillator Start-up Timer (OST) ensures stability of crystal oscillator sources.

The RSTOSC bits of Configuration Word 1 (Register 5-1) determine the type of oscillator that will be used when the device runs after Reset, including when it is first powered up.

If an external clock source is selected, the FEXTOSC bits of Configuration Word 1 must be used in conjunction with the RSTOSC bits to select the External Clock mode.

The external oscillator module can be configured in one of the following clock modes, by setting the FEXTOSC<2:0> Configuration bits:

1. ECL – External Clock Low-Power mode (below 100 kHz)
2. ECM – External Clock Medium Power mode (100 kHz to 8 MHz)
3. ECH – External Clock High-Power mode (above 8 MHz)
4. LP – 32 kHz Low-Power Crystal mode.
5. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode (between 100 kHz and 8 MHz)
6. HS – High Gain Crystal or Ceramic Resonator mode (above 4 MHz)

The ECH, ECM, and ECL Clock modes rely on an external logic level signal as the device clock source. The LP, XT, and HS Clock modes require an external crystal or resonator to be connected to the device. Each mode is optimized for a different frequency range. The internal oscillator block produces low and high-frequency clock sources, designated LFINTOSC and HFINTOSC. (see Internal Oscillator Block, Figure 7-1). Multiple device clock frequencies may be derived from these clock sources.
FIGURE 7-1: SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM

- **CLIN/OSC1**: External Oscillator (EXTOSC)
- **CLKOUT/OSC2**: 4x PLL
- **SOSCIN/SOSCI**: Secondary Oscillator (SOSC)
- **SOSC**: 31 kHz Oscillator
- **HFINTOSC**: FRQ<3:0>
  - 1,2,4,8,12,16,32,48,64 MHz Oscillator
- **MFINTOSC**: 31.25 kHz and 500 kHz Oscillator
- **LFINTOSC**: 1.2,4,8,16,32,48,64 MHz Oscillator
- **COSC<2:0>**: LFINTOSC is used to monitor system clock
- **CDIV<4:0>**: To Peripherals
- **Post Divider**: System Clock
- **SYSCMD**: Peripheral Clock
- **FSCM**: To Peripherals
- **Sleep**: To Peripherals
- **Idle**: To Peripherals

Note: LFINTOSC is used to monitor system clock.
7.2 Clock Source Types

Clock sources can be classified as external or internal. External clock sources rely on external circuitry for the clock source to function. Examples are: oscillator modules (ECH, ECM, ECL mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes).

Internal clock sources are contained within the oscillator module. The internal oscillator block has two internal oscillators that are used to generate internal system clock sources. The High-Frequency Internal Oscillator (HFINTOSC) can produce 1, 2, 4, 8, 12, 16, 32, 48 and 64 MHz clock. The frequency can be controlled through the OSCFRQ register (Register 7-5). The Low-Frequency Internal Oscillator (LFINTOSC) generates a fixed 31 kHz frequency.

A 4x PLL is provided that can be used with an external clock. When used with the EXTOSC the 4x PLL has input frequency limitations. See Section 7.2.1.4 “4x PLL” for more details.

The system clock can be selected between external or internal clock sources via the NOSC bits in the OSCCON1 register. See Section 7.3 “Clock Switching” for additional information. The system clock can be made available on the OSC2/CLKOUT pin for any of the modes that do not use the OSC2 pin. The clock out functionality is governed by the CLKOUTEN bit in the CONFIG1H register (Register 5-2). If enabled, the clock out signal is always at a frequency of Fosc/4.

7.2.1 EXTERNAL CLOCK SOURCES

An external clock source can be used as the device system clock by performing one of the following actions:

- Program the RSTOSC<2:0> and FEXTOSC<2:0> bits in the Configuration Words to select an external clock source that will be used as the default system clock upon a device Reset.
- Write the NOSC<2:0> and NDIV<3:0> bits in the OSCCON1 register to switch the system clock source.

See Section 7.3 “Clock Switching” for more information.

7.2.1.1 EC Mode

The External Clock (EC) mode allows an externally generated logic level signal to be the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. Figure 7-2 shows the pin connections for EC mode.

EC mode has three power modes to select from through Configuration Words:
- ECH – High power, above 8 MHz
- ECM – Medium power, 100 kHz-8 MHz
- ECL – Low power, below 100 MHz

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 7-2: EXTERNAL CLOCK (EC) MODE OPERATION

7.2.1.2 LP, XT, HS Modes

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 7-3). The three modes select a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification (above 100 kHz - 8 MHz).

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting (above 8 MHz).

Figure 7-3 and Figure 7-4 show typical circuits for quartz crystal and ceramic resonators, respectively.
7.2.1.3 Oscillator Start-up Timer (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR), or a wake-up from Sleep. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

7.2.1.4 4x PLL

The oscillator module contains a 4x PLL that can be used with the external clock sources to provide a system clock source. The input frequency for the PLL must fall within specifications. See the PLL Clock Timing Specifications in Table 45-9.

The PLL can be enabled for use by one of two methods:

1. Program the RSTOSC bits in the Configuration Word 1 to 010 (enable EXTOSC with 4x PLL).
2. Write the NOSC bits in the OSCCON1 register to 010 (enable EXTOSC with 4x PLL).

---

Note 1: A series resistor (Rs) may be required for quartz crystals with low drive level.
2: The value of Rf varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

---

Note 1: A series resistor (Rs) may be required for ceramic resonators with low drive level.
2: The value of Rf varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).
3: An additional parallel feedback resistor (Rf) may be required for proper ceramic resonator operation.
7.2.1.5 Secondary Oscillator

The secondary oscillator is a separate oscillator block that can be used as an alternate system clock source. The secondary oscillator is optimized for 32.768 kHz, and can be used with an external crystal oscillator connected to the SOSCI and SOSCO device pins, or an external clock source connected to the SOSCIN pin. The secondary oscillator can be selected during runtime using clock switching. Refer to Section 7.3 “Clock Switching” for more information.

Two power modes are available for the secondary oscillator. These modes are selected with the SOSCPWR (OSCCON3<6>). Clearing this bit selects the lower Crystal Gain mode which provides lowest microcontroller power consumption. Setting this bit enables a higher Gain mode to support faster crystal start-up or crystals with higher ESR.

FIGURE 7-5: QUARTZ CRYSTAL OPERATION (SECONDARY OSCILLATOR)

Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

3: For oscillator design assistance, reference the following Microchip Application Notes:
   • AN826, “Crystal Oscillator Basics and Crystal Selection for PIC® and PIC® Devices” (DS00826)
   • AN849, “Basic PIC® Oscillator Design” (DS00849)
   • AN943, “Practical PIC® Oscillator Analysis and Design” (DS00943)
   • AN949, “Making Your Oscillator Work” (DS00949)
   • TB097, “Interfacing a Micro Crystal MS1V-T1K 32.768 kHz Tuning Fork Crystal to a PIC16F690/SS” (DS91097)
   • AN1288, “Design Practices for Low-Power External Oscillators” (DS01288)
7.2.2 INTERNAL CLOCK SOURCES

The device may be configured to use the internal oscillator block as the system clock by performing one of the following actions:

- Program the RSTOSC<2:0> bits in Configuration Words to select the INTOSC clock source, which will be used as the default system clock upon a device Reset.
- Write the NOSC<2:0> bits in the OSCCON1 register to switch the system clock source to the internal oscillator during run-time. See Section 7.3 “Clock Switching” for more information.

In INTOSC mode, OSC1/CLKIN is available for general purpose I/O, provided that FEXTOSC is configured to ‘oscillator is not enabled’. OSC2/CLKOUT is available for general purpose I/O or CLKOUT.

The function of the OSC2/CLKOUT pin is determined by the CLKOUTEN bit in Configuration Words.

The internal oscillator block has two independent oscillators that can produce two internal system clock sources.

1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory-calibrated and operates from 1 to 64 MHz. The frequency of HFINTOSC can be selected by setting the FRQ<3:0> bits of the OSCFRQ register. The NDIV<3:0> bits of the OSCCON1 register allow for division of the HFINTOSC output from a range between 1:1 and 1:512.

2. The **LFINTOSC** (Low-Frequency Internal Oscillator) is factory-calibrated and operates at 31 kHz.
7.2.2.3 Internal Oscillator Frequency Adjustment

The internal oscillator is factory-calibrated. This internal oscillator can be adjusted in software by writing to the OSCTUNE register (Register 7-3).

The default value of the OSCTUNE register is 00h. The value is a 6-bit two’s complement number. A value of 1Fh will provide an adjustment to the maximum frequency. A value of 20h will provide an adjustment to the minimum frequency.

When the OSCTUNE register is modified, the oscillator frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE **does not affect** the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), WWDT, Fail-Safe Clock Monitor (FSCM) and peripherals, are not affected by the change in frequency.

7.2.2.4 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is a factory-calibrated 31 kHz internal clock source.

The LFINTOSC is the frequency for the Power-up Timer (PWRT), Windowed Watchdog Timer (WWDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled through one of the following methods:

- Programming the RSTOSC<2:0> bits of Configuration Word 1 to enable LFINTOSC.
- Write to the NOSC<2:0> bits of the OSCCON1 register during run-time. See Section 7.3, Clock Switching for more information.

7.2.2.5 ADCRC

The ADCRC is an oscillator dedicated to the ADC² module. The ADCRC oscillator can be manually enabled using the ADOEN bit of the OSCEN register. The ADCRC runs at a fixed frequency of 600 kHz. ADCRC is automatically enabled if it is selected as the clock source for the ADC² module.
7.2.2.6 Oscillator Status and Manual Enable
The Ready status of each oscillator (including the ADCRC oscillator) is displayed in OSCSTAT (Register 7-4). The oscillators (but not the PLL) may be explicitly enabled through OSCEN (Register 7-7).

7.2.2.7 HFOR and MFOR Bits
The HFOR and MFOR bits indicate that the HFINTOSC and MFINTOSC is ready. These clocks are always valid for use at all times, but only accurate after they are ready.

When a new value is loaded into the OSCFRQ register, the HFOR and MFOR bits will clear, and set again when the oscillator is ready. During pending OSCFRQ changes the MFINTOSC clock will stall at a high or a low state, until the HFINTOSC resumes operation.

7.3 Clock Switching
The system clock source can be switched between external and internal clock sources via software using the New Oscillator Source (NOSC) bits of the OSCCON1 register. The following clock sources can be selected using the following:

- External oscillator
- Internal Oscillator Block (INTOSC)

When the new oscillator is ready, the New Oscillator Ready (NOSCR) bit of OSCCON3 and the Clock Switch Interrupt Flag (CSWIF) bit of the respective PIR register are set. If Clock Switch Interrupts are enabled (CSWIE = 1), an interrupt will be generated at that time. The Oscillator Ready (ORDY) bit of OSCCON3 can also be polled to determine when the oscillator is ready in lieu of an interrupt.

**Note:** The CSWIF interrupt will not wake the system from Sleep.

If the Clock Switch Hold (CSWHOLD) bit of OSCCON3 is clear, the oscillator switch will occur when the New Oscillator is Ready bit (NOSCR) is set, and the interrupt (if enabled) will be serviced at the new oscillator setting.

If CSWHOLD is set, the oscillator switch is suspended, while execution continues using the current (old) clock source. When the NOSCR bit is set, software should:

- Set CSWHOLD = 0 so the switch can complete, or
- Copy COSC into NOSC to abandon the switch.

If DOZE is in effect, the switch occurs on the next clock cycle, whether or not the CPU is operating during that cycle.

Changing the clock post-divider without changing the clock source (i.e., changing Fosc from 1 MHz to 2 MHz) is handled in the same manner as a clock source change, as described previously. The clock source will already be active, so the switch is relatively quick. CSWHOLD must be clear (CSWHOLD = 0) for the switch to complete.

The current COSC and CDIV are indicated in the OSCCON2 register up to the moment when the switch actually occurs, at which time OSCCON2 is updated and ORDY is set. NOSCR is cleared by hardware to indicate that the switch is complete.

7.3.1 NEW OSCILLATOR SOURCE (NOSC) AND NEW DIVIDER SELECTION REQUEST (NDIV) BITS
The New Oscillator Source (NOSC) and New Divider Selection Request (NDIV) bits of the OSCCON1 register select the system clock source and frequency that are used for the CPU and peripherals.

When new values of NOSC and NDIV are written to OSCCON1, the current oscillator selection will continue to operate while waiting for the new clock source to indicate that it is stable and ready. In some cases, the newly requested source may already be in use, and is ready immediately. In the case of a divider-only change, the new and old sources are the same, so the old source will be ready immediately. The device may enter Sleep while waiting for the switch as described in Section 7.3.2 “Clock Switch and Sleep”.

**Note:** The Clock Switch Enable bit in Configuration Word 1 can be used to enable or disable the clock switching capability. When cleared, the NOSC and NDIV bits cannot be changed by user software. When set, writing to NOSC and NDIV is allowed and would switch the clock frequency.
7.3.2 CLOCK SWITCH AND SLEEP

If OSCCON1 is written with a new value and the device is put to Sleep before the switch completes, the switch will not take place and the device will enter Sleep mode.

When the device wakes from Sleep and the CSWHOLD bit is clear, the device will wake with the 'new' clock active, and the Clock Switch Interrupt flag bit (CSWIF) will be set.

When the device wakes from Sleep and the CSWHOLD bit is set, the device will wake with the 'old' clock active and the new clock will be requested again.

**FIGURE 7-6: CLOCK SWITCH (CSWHOLD = 0)**

**FIGURE 7-7: CLOCK SWITCH (CSWHOLD = 1)**

**Note 1:** CSWIF is asserted coincident with NOSCR; interrupt is serviced at OSC#2 speed.

**Note 2:** The assertion of NOSCR is hidden from the user because it appears only for the duration of the switch.
FIGURE 7-8: CLOCK SWITCH ABANDONED

Note 1: CSWIF may be cleared before or after rewriting OSCCON1; CSWIF is not automatically cleared.

Note 2: ORDY = 0 if OSCCON1 does not match OSCCON2; a new switch will begin.
7.4 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM is enabled by setting the FCMEN bit in the Configuration Words. The FSCM is applicable to all external Oscillator modes (LP, XT, HS, ECL/M/H and Secondary Oscillator).

FIGURE 7-9: FSCM BLOCK DIAGRAM

7.4.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 7-9. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the external clock goes low.

7.4.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM overwrites the COSC bits to select HFINTOSC (3'b110). The frequency of HFINTOSC would be determined by the previous state of the FRQ bits and the NDIV/CDIV bits. The bit flag OSFIF of the respective PIR register is set. Setting this flag will generate an interrupt if the OSFIE bit of the respective PIR register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock continues to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation, by writing to the NOSC and NDIV bits of the OSCCON1 register.

7.4.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, executing a SLEEP instruction or changing the NOSC and NDIV bits of the OSCCON1 register. When switching to the external oscillator or PLL, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON1. When the OST times out, the Fail-Safe condition is cleared after successfully switching to the external clock source. The OSCFIF bit should be cleared prior to switching to the external clock source. If the Fail-Safe condition still exists, the OSCFIF flag will again become set by hardware.
7.4.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed.

FIGURE 7-10: FSCM TIMING DIAGRAM

Note: The system clock is normally at a much higher frequency than the sample clock. The relative frequencies in this example have been chosen for clarity.

TABLE 7-1: NOSC/COSC AND NDIV/CDIV BIT SETTINGS

<table>
<thead>
<tr>
<th>NOSC&lt;2:0&gt;</th>
<th>COSC&lt;2:0&gt;</th>
<th>Clock Source</th>
<th>NDIV&lt;3:0&gt;</th>
<th>CDIV&lt;3:0&gt;</th>
<th>Clock Divider</th>
</tr>
</thead>
<tbody>
<tr>
<td>111</td>
<td></td>
<td>EXTOSC(1)</td>
<td>1111-1010</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>110</td>
<td></td>
<td>HFINTOSC(2)</td>
<td>1001</td>
<td></td>
<td>512</td>
</tr>
<tr>
<td>101</td>
<td></td>
<td>LFINTOSC</td>
<td>1000</td>
<td></td>
<td>256</td>
</tr>
<tr>
<td>100</td>
<td></td>
<td>SOSC</td>
<td>0111</td>
<td></td>
<td>128</td>
</tr>
<tr>
<td>011</td>
<td></td>
<td>Reserved</td>
<td>0110</td>
<td></td>
<td>64</td>
</tr>
<tr>
<td>010</td>
<td></td>
<td>EXTOSC + 4x PLL(3)</td>
<td>0101</td>
<td></td>
<td>32</td>
</tr>
<tr>
<td>001</td>
<td></td>
<td>Reserved</td>
<td>0100</td>
<td></td>
<td>16</td>
</tr>
<tr>
<td>000</td>
<td></td>
<td>Reserved</td>
<td>0011</td>
<td></td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0010</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0001</td>
<td></td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

Note 1: EXTOSC configured by the FEXTOSC bits of Configuration Word 1 (Register 5-1).
Note 2: HFINTOSC frequency is set with the FRQ bits of the OSCFRQ register (Register 7-5).
Note 3: EXTOSC must meet the PLL specifications (Table 45-9).
### 7.5 Register Definitions: Oscillator Control

**REGISTER 7-1: OSCCON1: OSCILLATOR CONTROL REGISTER 1**

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/W-ff</th>
<th>R/W-ff</th>
<th>R/W-ff</th>
<th>R/W-q/q</th>
<th>R/W-q/q</th>
<th>R/W-q/q</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>NOSC&lt;2:0&gt;</td>
<td>NDIV&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **f** = determined by Configuration bit setting
- **q** = Reset value is determined by hardware
- **-n/n** = Value at POR and BOR/Value at all other Resets

- **bit 7 Unimplemented:** Read as '0'
- **bit 6-4 NOSC<2:0>:** New Oscillator Source Request bits\(^{1,2,3}\)
  The setting requests a source oscillator and PLL combination per Table 7-1.
  POR value = RSTOSC (Register 5-1).
- **bit 3-0 NDIV<3:0>:** New Divider Selection Request bits\(^{2,3}\)
  The setting determines the new postscaler division ratio per Table 7-1.

**Note 1:** The default value (ff/ff) is determined by the RSTOSC Configuration bits. See Table 7-2 below.

2: If NOSC is written with a reserved value (Table 7-1), the operation is ignored and neither NOSC nor NDIV is written.

3: When CSWEN = 0, this register is read-only and cannot be changed from the POR value.

#### TABLE 7-2: DEFAULT OSCILLATOR SETTINGS

<table>
<thead>
<tr>
<th>RSTOSC</th>
<th>SFR Reset Values</th>
<th>Initial Fosc Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NOCSC/COSC CDIV OSCFRQ</td>
<td></td>
</tr>
<tr>
<td>111</td>
<td>111 1:1</td>
<td>4 MHz</td>
</tr>
<tr>
<td>110</td>
<td>110 4:1</td>
<td></td>
</tr>
<tr>
<td>101</td>
<td>101 1:1</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>100 1:1</td>
<td></td>
</tr>
<tr>
<td>011</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>010</td>
<td>010 1:1</td>
<td>4 MHz</td>
</tr>
<tr>
<td>001</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>000</td>
<td>110 1:1</td>
<td>64 MHz</td>
</tr>
</tbody>
</table>

**Note 1:** EXTOSC must meet the PLL specifications (Table 45-9).
**REGISTER 7-2: OSCCON2: OSCILLATOR CONTROL REGISTER 2**

<table>
<thead>
<tr>
<th>bit 7</th>
<th>COSC&lt;2:0&gt;</th>
<th>CDIV&lt;3:0&gt;</th>
</tr>
</thead>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’ = Bit is set**
- **‘0’ = Bit is cleared**
- **-n/n = Value at POR and BOR/Value at all other Resets**

**bit 7**  
Unimplemented: Read as ‘0’

**bit 6-4**  
**COSC<2:0>:** Current Oscillator Source Select bits (read-only)<sup>1</sup>
Indicates the current source oscillator and PLL combination per Table 7-1.

**bit 3-0**  
**CDIV<3:0>:** Current Divider Select bits (read-only)<sup>1</sup>
Indicates the current postscaler division ratio per Table 7-1.

**Note 1:** The POR value is the value present when user code execution begins.

---

**REGISTER 7-3: OSCCON3: OSCILLATOR CONTROL REGISTER 3**

<table>
<thead>
<tr>
<th>bit 7</th>
<th>CSWHOLD</th>
<th>SOSCPWR</th>
<th>ORDY</th>
<th>NOSCR</th>
<th>bit 0</th>
</tr>
</thead>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’ = Bit is set**
- **‘0’ = Bit is cleared**
- **-n/n = Value at POR and BOR/Value at all other Resets**
- **HC = Bit is cleared by hardware**

**bit 7**  
**CSWHOLD:** Clock Switch Hold bit
- **1** = Clock switch will hold (with interrupt) when the oscillator selected by NOSC is ready
- **0** = Clock switch may proceed when the oscillator selected by NOSC is ready; NOSCR becomes ‘1’, the switch will occur

**bit 6**  
**SOSCPWR:** Secondary Oscillator Power Mode Select bit
- **1** = Secondary oscillator operating in High-Power mode
- **0** = Secondary oscillator operating in Low-Power mode

**bit 5**  
**Unimplemented:** Read as ‘0’

**bit 4**  
**ORDY:** Oscillator Ready bit (read-only)
- **1** = OSCCON1 = OSCCON2; the current system clock is the clock specified by NOSC
- **0** = A clock switch is in progress

**bit 3**  
**NOSCR:** New Oscillator is Ready bit (read-only)<sup>1</sup>
- **1** = A clock switch is in progress and the oscillator selected by NOSC indicates a “ready” condition
- **0** = A clock switch is not in progress, or the NOSC-selected oscillator is not yet ready

**bit 2-0**  
**Unimplemented:** Read as ‘0’

**Note 1:** If CSWHOLD = 0, the user may not see this bit set because, when the oscillator becomes ready there may be a delay of one instruction clock before this bit is set. The clock switch occurs in the next instruction cycle and this bit is cleared.
REGISTER 7-4: OSCSTAT: OSCILLATOR STATUS REGISTER 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>EXTOR</td>
<td>EXTOSC (external) Oscillator Ready bit</td>
</tr>
<tr>
<td>6</td>
<td>HFOR</td>
<td>HFINTOSC Oscillator Ready bit</td>
</tr>
<tr>
<td>5</td>
<td>MFOR</td>
<td>MFINTOSC Oscillator Ready bit</td>
</tr>
<tr>
<td>4</td>
<td>LFOR</td>
<td>LFINTOSC Oscillator Ready bit</td>
</tr>
<tr>
<td>3</td>
<td>SOR</td>
<td>Secondary (Timer1) Oscillator Ready bit</td>
</tr>
<tr>
<td>2</td>
<td>ADOR</td>
<td>ADC Oscillator Ready bit</td>
</tr>
<tr>
<td>1</td>
<td>PLLR</td>
<td>PLL is Ready bit</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets

- '1' = Bit is set
- '0' = Bit is cleared
- q = Reset value is determined by hardware

**bit 7**
EXTOR: EXTOSC (external) Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used

**bit 6**
HFOR: HFINTOSC Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used

**bit 5**
MFOR: MFINTOSC Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used

**bit 4**
LFOR: LFINTOSC Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used

**bit 3**
SOR: Secondary (Timer1) Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used

**bit 2**
ADOR: ADC Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used

**bit 1**
Unimplemented: Read as '0'

**bit 0**
PLLR: PLL is Ready bit
1 = The PLL is ready to be used
0 = The PLL is not enabled, the required input source is not ready, or the PLL is not locked.
REGISTER 7-5: OSCFRQ: HFINTOSC FREQUENCY SELECTION REGISTER

| bit 7-4 | Unimplemented: Read as '0' |
| bit 3-0 | FRQ<3:0>: HFINTOSC Frequency Selection bits[^1] |

<table>
<thead>
<tr>
<th>FRQ&lt;3:0&gt;</th>
<th>Nominal Freq (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1001</td>
<td></td>
</tr>
<tr>
<td>1010</td>
<td></td>
</tr>
<tr>
<td>1111</td>
<td></td>
</tr>
<tr>
<td>1110</td>
<td>Reserved</td>
</tr>
<tr>
<td>1101</td>
<td></td>
</tr>
<tr>
<td>1100</td>
<td></td>
</tr>
<tr>
<td>1011</td>
<td></td>
</tr>
<tr>
<td>1000</td>
<td>64</td>
</tr>
<tr>
<td>0111</td>
<td>48</td>
</tr>
<tr>
<td>0110</td>
<td>32</td>
</tr>
<tr>
<td>0101</td>
<td>16</td>
</tr>
<tr>
<td>0100</td>
<td>12</td>
</tr>
<tr>
<td>0011</td>
<td>8</td>
</tr>
<tr>
<td>0010</td>
<td>4</td>
</tr>
<tr>
<td>0001</td>
<td>2</td>
</tr>
<tr>
<td>0000</td>
<td>1</td>
</tr>
</tbody>
</table>

[^1]: FRQ<3:0> Nominal Freq (MHz) (1)

Note 1: Refer to Table 7-2 for more information.
## REGISTER 7-6: OSCTUNE: HFINTOSC TUNING REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>TUN&lt;5:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

**bit 7-6**
- **Unimplemented**: Read as ‘0’

**bit 5-0**
- **TUN<5:0>**: HFINTOSC Frequency Tuning bits
  - `01 1111` = Maximum frequency
  - `•`  
  - `•`  
  - `•`
  - `00 0000` = Center frequency. Oscillator module is running at the calibrated frequency (default value).
  - `•`  
  - `•`  
  - `•`
  - `10 0000` = Minimum frequency
## REGISTER 7-7: OSCEN: OSCILLATOR MANUAL ENABLE REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value at POR/BOB</th>
<th>Value at all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>EXTOEN: External Oscillator Manual Request Enable bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>HFOEN: HFINTOSC Oscillator Manual Request Enable bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>MFOEN: MFINTOSC (500 kHz/31.25 kHz) Oscillator Manual Request Enable bit (Derived from HFINTOSC)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>LFOEN: LFINTOSC (31 kHz) Oscillator Manual Request Enable bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>SOSCEN: Secondary Oscillator Manual Request Enable bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>ADOEN: ADC Oscillator Manual Request Enable bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1-0</td>
<td>Unimplemented</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

**bit 7**

**EXTOEN**: External Oscillator Manual Request Enable bit

- **1** = EXTOSC is explicitly enabled, operating as specified by FEXTOSC
- **0** = EXTOSC could be enabled by requesting peripheral

**bit 6**

**HFOEN**: HFINTOSC Oscillator Manual Request Enable bit

- **1** = HFINTOSC is explicitly enabled, operating as specified by OSCFRQ (Register 7-5)
- **0** = HFINTOSC could be enabled by requesting peripheral

**bit 5**

**MFOEN**: MFINTOSC (500 kHz/31.25 kHz) Oscillator Manual Request Enable bit (Derived from HFINTOSC)

- **1** = MFINTOSC is explicitly enabled
- **0** = MFINTOSC could be enabled by requesting peripheral

**bit 4**

**LFOEN**: LFINTOSC (31 kHz) Oscillator Manual Request Enable bit

- **1** = LFINTOSC is explicitly enabled
- **0** = LFINTOSC could be enabled by requesting peripheral

**bit 3**

**SOSCEN**: Secondary Oscillator Manual Request Enable bit

- **1** = Secondary Oscillator is explicitly enabled, operating as specified by SOSCPWR
- **0** = Secondary Oscillator could be enabled by requesting peripheral

**bit 2**

**ADOEN**: ADC Oscillator Manual Request Enable bit

- **1** = ADC oscillator is explicitly enabled
- **0** = ADC oscillator could be enabled by requesting peripheral

**bit 1-0**

**Unimplemented**: Read as ‘0’
## TABLE 7-3: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSCCON1</td>
<td>—</td>
<td>NOSC&lt;2:0&gt;</td>
<td></td>
<td></td>
<td>NDIV&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>94</td>
</tr>
<tr>
<td>OSCCON2</td>
<td>—</td>
<td>COSC&lt;2:0&gt;</td>
<td></td>
<td></td>
<td>CDIV&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>95</td>
</tr>
<tr>
<td>OSCCON3</td>
<td>CSWHOLD</td>
<td>SOSCPOWER</td>
<td>ORDY</td>
<td>NOSCR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>95</td>
</tr>
<tr>
<td>OSCSTAT</td>
<td>EXTOR</td>
<td>HFOR</td>
<td>MFOR</td>
<td>LFOR</td>
<td>SOR</td>
<td>ADOR</td>
<td>—</td>
<td>PLLR</td>
<td>96</td>
</tr>
<tr>
<td>OSCTUNE</td>
<td>—</td>
<td>—</td>
<td></td>
<td></td>
<td>TUN&lt;5:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>98</td>
</tr>
<tr>
<td>OSCFRQ</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>FRQ&lt;3:0&gt;</td>
<td></td>
<td></td>
<td>97</td>
</tr>
<tr>
<td>OSCEN</td>
<td>EXTOEN</td>
<td>HFOEN</td>
<td>MFOEN</td>
<td>LFOEN</td>
<td>SOSCEN</td>
<td>ADOEN</td>
<td>—</td>
<td>—</td>
<td>99</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.
8.0 REFERENCE CLOCK OUTPUT MODULE

The reference clock output module provides the ability to send a clock signal to the clock reference output pin (CLKR). The reference clock output can also be used as a signal for other peripherals, such as the Data Signal Modulator (DSM), Memory Scanner and Timer module.

The reference clock output module has the following features:

- Selectable clock source using the CLKRCLK register
- Programmable clock divider
- Selectable duty cycle

FIGURE 8-1: CLOCK REFERENCE BLOCK DIAGRAM

FIGURE 8-2: CLOCK REFERENCE TIMING
8.1 Clock Source
The input to the reference clock output can be selected using the CLKRCLK register.

8.1.1 CLOCK SYNCHRONIZATION
Once the reference clock enable (EN) is set, the module is ensured to be glitch-free at start-up.
When the reference clock output is disabled, the output signal will be disabled immediately.
Clock dividers and clock duty cycles can be changed while the module is enabled, but glitches may occur on the output. To avoid possible glitches, clock dividers and clock duty cycles should be changed only when the CLKREN is clear.

8.2 Programmable Clock Divider
The module takes the clock input and divides it based on the value of the DIV<2:0> bits of the CLKRCON register (Register 8-1).
The following configurations can be made based on the DIV<2:0> bits:
• Base FOSC value
• FOSC divided by 2
• FOSC divided by 4
• FOSC divided by 8
• FOSC divided by 16
• FOSC divided by 32
• FOSC divided by 64
• FOSC divided by 128
The clock divider values can be changed while the module is enabled; however, in order to prevent glitches on the output, the DIV<2:0> bits should only be changed when the module is disabled (EN = 0).

8.3 Selectable Duty Cycle
The DC<1:0> bits of the CLKRCON register can be used to modify the duty cycle of the output clock. A duty cycle of 25%, 50%, or 75% can be selected for all clock rates, with the exception of the undivided base FOSC value.
The duty cycle can be changed while the module is enabled; however, in order to prevent glitches on the output, the DC<1:0> bits should only be changed when the module is disabled (EN = 0).

Note: The DC1 bit is reset to ‘1’. This makes the default duty cycle 50% and not 0%.

8.4 Operation in Sleep Mode
The reference clock output module clock is based on the system clock. When the device goes to Sleep, the module outputs will remain in their current state. This will have a direct effect on peripherals using the reference clock output as an input signal. No change should occur in the module from entering or exiting from Sleep.
8.5 Register Definitions: Reference Clock

Long bit name prefixes for the Reference Clock peripherals are shown below. Refer to Section 1.3.2.2 “Long Bit Names” for more information.

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Bit Name Prefix</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKR</td>
<td>CLKR</td>
</tr>
</tbody>
</table>

REGISTER 8-1: CLKRCON: REFERENCE CLOCK CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-1/1</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>—</td>
<td>—</td>
<td>DC&lt;1:0&gt;</td>
<td></td>
<td></td>
<td>DIV&lt;2:0&gt;</td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

<table>
<thead>
<tr>
<th>bit 7</th>
<th><strong>EN</strong>: Reference Clock Module Enable bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Reference clock module enabled</td>
</tr>
<tr>
<td>0</td>
<td>Reference clock module is disabled</td>
</tr>
</tbody>
</table>

| bit 6-5 | **Unimplemented**: Read as ‘0’ |

<table>
<thead>
<tr>
<th>bit 4-3</th>
<th><strong>DC&lt;1:0&gt;</strong>: Reference Clock Duty Cycle bits(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>Clock outputs duty cycle of 75%</td>
</tr>
<tr>
<td>10</td>
<td>Clock outputs duty cycle of 50%</td>
</tr>
<tr>
<td>01</td>
<td>Clock outputs duty cycle of 25%</td>
</tr>
<tr>
<td>00</td>
<td>Clock outputs duty cycle of 0%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 2-0</th>
<th><strong>DIV&lt;2:0&gt;</strong>: Reference Clock Divider bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>111</td>
<td>Base clock value divided by 128</td>
</tr>
<tr>
<td>110</td>
<td>Base clock value divided by 64</td>
</tr>
<tr>
<td>101</td>
<td>Base clock value divided by 32</td>
</tr>
<tr>
<td>100</td>
<td>Base clock value divided by 16</td>
</tr>
<tr>
<td>011</td>
<td>Base clock value divided by 8</td>
</tr>
<tr>
<td>010</td>
<td>Base clock value divided by 4</td>
</tr>
<tr>
<td>001</td>
<td>Base clock value divided by 2</td>
</tr>
<tr>
<td>000</td>
<td>Base clock value</td>
</tr>
</tbody>
</table>

**Note 1**: Bits are valid for reference clock divider values of two or larger, the base clock cannot be further divided.
REGISTER 8-2:  CLKRCLK: CLOCK REFERENCE CLOCK SELECTION MUX

<table>
<thead>
<tr>
<th>Bit</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 0</td>
<td>CLKRCLK</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

bit 7-4      Unimplemented: Read as ‘0’
bit 3-0     **CLK<3:0>:** CLKR Clock Selection bits

- 1111 = Reserved
- 1110 = Reserved
- 1101 = Reserved
- 1100 = CLC4 Output
- 1001 = CLC3 Output
- 1000 = CLC2 Output
- 0111 = CLC1 Output
- 0110 = NCO1 Output
- 0101 = SOSC
- 0100 = MFINTOSC (31.25 kHz)
- 0011 = MFINTOSC (500 kHz)
- 0010 = LFINTOSC (31 kHz)
- 0001 = HFINTOSC
- 0000 = Fosc

TABLE 8-1:  SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK REFERENCE OUTPUT

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKRCON</td>
<td>EN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>103</td>
</tr>
<tr>
<td>CLKRCLK</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>104</td>
</tr>
</tbody>
</table>

Legend:  
- **—** = unimplemented, read as ‘0’. Shaded cells are not used by the CLKR module.
9.0 INTERRUPT CONTROLLER

The vectored interrupt controller module reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the CPU. This module includes the following major features:

- Interrupt Vector Table (IVT) with a unique vector for each interrupt source
- Fixed and ensured interrupt latency
- Programmable base address for Interrupt Vector Table (IVT) with lock
- Two user-selectable priority levels – High priority and Low priority
- Two levels of context saving
- Interrupt state Status bits to indicate the current execution status of the CPU

The interrupt controller module assembles all of the interrupt request signals and resolves the interrupts based on both a fixed natural order priority (i.e., determined by the Interrupt Vector Table), and a user-assigned priority (i.e., determined by the IPRx registers), thereby eliminating scanning of interrupt sources.

9.1 Interrupt Control and Status Registers

The devices in this family implement the following registers for the interrupt controller:

- INTCON0, INTCON1 Control Registers
- PIRx – Peripheral Interrupt Status Registers
- PIEx – Peripheral Interrupt Enable Registers
- IPRx – Peripheral Interrupt Priority Registers
- IVTBASE<20:0> Address Registers
- IVTLOCK Register

Global interrupt control functions and external interrupts are controlled from the INTCON0 register. The INTCON1 register contains the status flags for the Interrupt controller.

The PIRx registers contain all of the interrupt request flags. Each source of interrupt has a Status bit, which is set by the respective peripherals or an external signal and is cleared via software.

The PIEx registers contain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

The IPRx registers are used to set the Interrupt Priority Level for each source of interrupt. Each user interrupt source can be assigned to either a high or low priority.

The IVTBASE register is user programmable and is used to determine the start address of the Interrupt Vector Table and the IVTLOCK register is used to prevent any unintended writes to the IVTBASE register.

There are two other Configuration bits that control the way the interrupt controller can be configured.

- CONFIG2L<3>, MVECEN bit
- CONFIG2L<4>, IVT1WAY bit

The MVECEN bit in CONFIG2L determines whether the Vector table is used to determine the interrupt priorities.

- When the IVT1WAY determines the number of times the IVTLOCKED bit can be cleared and set after a device Reset. See Section 9.2.3 “Interrupt Vector Table (IVT) address calculation” for details.
9.2 Interrupt Vector Table (IVT)

The interrupt controller supports an Interrupt Vector Table (IVT) that contains the vector address location for each interrupt request source.

The Interrupt Vector Table (IVT) resides in program memory, starting at address location determined by the IVTBASE registers; refer to Registers 9-33 through 9-35 for details. The IVT contains 68 vectors, one for each source of interrupt. Each interrupt vector location contains the starting address of the associated Interrupt Service Routine (ISR).

The MVECEN bit in Configuration Word 2L controls the availability of the vector table.

9.2.1 Interrupt Vector Table Base Address (IVTBASE)

The start address of the vector table is user programmable through the IVTBASE registers. The user must ensure the start address is such that it can encompass the entire vector table inside the program memory.

Each vector address is a 16-bit word (or two address locations on PIC18 devices). So for n interrupt sources, there are 2n address locations necessary to hold the table starting from IVTBASE as the first location. So the starting address of IVTBASE should be chosen such that the address range from IVTBASE to (IVTBASE + 2n-1) can be encompassed inside the program flash memory.

For example, the K42 devices have the highest vector number: 81. So IVTBASE should be chosen such that (IVTBASE + 0xA1) is less than the last memory location in program flash memory.

A programmable vector table base address is useful in situations to switch between different sets of vector tables, depending on the application. It can also be used when the application program needs to update the existing vector table (vector address values).

Note: It is required that the user assign an even address to the IVTBASE register for correct operation.

9.2.2 Interrupt Vector Table Contents

MVECEN = 0

When MVECEN = 0, the address location pointed by the IVTBASE registers has a GOTO instruction for a high priority interrupt. Similarly, the corresponding low priority vector location also has a GOTO instruction, which is executed in case of a low priority interrupt.

MVECEN = 1

When MVECEN = 1, the value in the vector table of each interrupt, points to the address location of the first instruction of the interrupt service routine.

ISR Location = Interrupt Vector Table entry << 2.

9.2.3 Interrupt Vector Table (IVT) Address Calculation

MVECEN = 0

When the MVECEN bit in Configuration Word 2L (Register 5-3) is cleared, the address pointed by IVTBASE registers is used as the high priority interrupt vector address. The low priority interrupt vector address is offset eight instruction words from the address in IVTBASE registers.

For PIC18 devices the IVTBASE registers default to 00 0008h, the high priority interrupt vector address will be 00 0008h and the low priority interrupt vector address will be 00 0018h.

MVECEN = 1

Each interrupt has a unique vector number associated with it as defined in Table 9-2. This vector number is used for calculating the location of the interrupt vector for a particular interrupt source.

Interrupt Vector Address = IVTBASE + (2*Vector Number).

This calculated Interrupt Vector Address value is stored in the IVTAD<20:0> registers when an interrupt is received (Registers 9-36 through 9-38).

User-assigned software priority assigned using the IPRx registers does not affect address calculation and is only used to resolve concurrent interrupts.

Note: If for any reason the address of the ISR could not be fetched from the vector table, it will cause the system to reset and clear the memory execution violation flag (MEMV bit) in PCON1 register (Register 6-3). This occurs due to any one of the following:

- The entry for the interrupt in the vector table lies outside the executable PFM area (SAF area is non-executable when SAFEN = 1).
- ISR pointed by the vector table lies outside the executable PFM area (SAF area is non-executable when SAFEN = 1).
9.2.4 ACCESS CONTROL FOR IVTBASE REGISTERS

The Interrupt controller has an IVTLOCKED bit which can be set to avoid inadvertent changes to the IVTBASE registers contents. Setting and clearing this bit requires a special sequence as an extra precaution against inadvertent changes.

To allow writes to IVTBASE registers, the interrupts must be disabled (GIEH = 0) and the IVTLOCKED bit must be cleared. The user must follow the sequence shown in Example 9-1 to clear the IVTLOCKED bit.

**EXAMPLE 9-1: IVT UNLOCK SEQUENCE**

```
; Disable Interrupts:
BCF INTCON0, GIE;

; Bank to IVTLOCK register
BANKSEL IVTLOCK;
MOVLW 55h;

; Required sequence, next 4 instructions
MOVWF IVTLOCK;
MOVLW AAh;
MOVWF IVTLOCK;

; Clear IVTLOCKED bit to enable writes
BCF IVTLOCK, IVTLOCKED;

; Enable Interrupts
BSF INTCON0, GIE;
```

The user must follow the sequence shown in Example 9-2 to set the IVTLOCKED bit.

**EXAMPLE 9-2: IVT LOCK SEQUENCE**

```
; Disable Interrupts:
BCF INTCON0, GIE;

; Bank to IVTLOCK register
BANKSEL IVTLOCK;
MOVLW 55h;

; Required sequence, next 4 instructions
MOVWF IVTLOCK;
MOVLW AAh;
MOVWF IVTLOCK;

; Set IVTLOCKED bit to enable writes
BSF IVTLOCK, IVTLOCKED;

; Enable Interrupts
BSF INTCON0, GIE;
```

When the IVT1WAY Configuration bit is set, the IVTLOCKED bit can be cleared and set only once after a device Reset. The unlock operation in Example 9-1 will have no effect after the lock sequence in Example 9-2 is used to set the IVTLOCK. Unlocking is inhibited until a system Reset occurs.

<table>
<thead>
<tr>
<th>IVT Address Calculation</th>
<th>Interrupt Priority</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Vector Enable</td>
<td></td>
</tr>
<tr>
<td>CONFIG2L register</td>
<td>INTCON0 Register, IPEN bit</td>
</tr>
<tr>
<td>MVECEN bit</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>IVTBASE</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>IVTBASE + 2*(Vector Number)</td>
</tr>
</tbody>
</table>

**TABLE 9-1: IVT ADDRESS CALCULATION SUMMARY**
9.3 Interrupt Priority

The final priority level for any pending source of interrupt is determined first by the user-assigned priority of that source in the IPRx register, then by the natural order priority within the IVT. The sections below detail the operation of interrupt priorities.

9.3.1 USER (SOFTWARE) PRIORITY

User-assigned interrupt priority is enabled by setting the IPEN bit in the INTCON0 register (Register 9-1). Each peripheral interrupt source can be assigned a high or low priority level by the user. The user-assignable interrupt priority control bits for each interrupt are located in the IPRx registers (Registers 9-23 through 9-32).

The interrupts are serviced based on predefined interrupt priority scheme defined below.

1. Interrupts set by the user as high-priority interrupt have higher precedence of execution. High-priority interrupts will override a low-priority request when:
   a) A low priority interrupt has been requested or its request is already pending.
   b) A low- and high-priority interrupt are triggered concurrently, i.e., on the same instruction cycle(1).
   c) A low-priority interrupt was requested and the corresponding Interrupt Service Routine is currently executing. In this case, the lower priority interrupt routine will complete executing after the high-priority interrupt has been serviced(2).

2. Interrupts set by the user as a low priority have the lower priority of execution and are preempted by any high-priority interrupt.

3. Interrupts defined with the same software priority cannot preempt or interrupt each other. Concurrent pending interrupts with the same user priority are resolved using the natural order priority. (when MVECEN = ON) or in the order the interrupt flag bits are polled in the ISR (when MVECEN = OFF).

Note 1: When a high priority interrupt preempts a concurrent low priority interrupt, the GIEL bit may be cleared in the high priority Interrupt Service Routine. If the GIEL bit is cleared, the low priority interrupt will NOT be serviced even if it was originally requested. The corresponding interrupt flag needs to be cleared in user code.

2: When a high priority interrupt is requested while a low priority Interrupt Service Routine is executing, the GIEL bit may be cleared in the high priority Interrupt Service Routine. The pending low priority interrupt will resume even if the GIEL bit is cleared.
9.3.2 NATURAL ORDER (HARDWARE) PRIORITY

When more than one interrupt with the same user specified priority level are requested, the priority conflict is resolved by using a method called “Natural Order Priority”. Natural order priority is a fixed priority scheme that is based on the Interrupt Vector Table. Table 9-2 shows the natural order priority and the interrupt vector number assigned for each source.

The natural order priority scheme has vector interrupt 0 as the highest priority and vector interrupt 81 as the lowest priority.

For example, when two concurrently occurring interrupt sources that are both designated high priority using the IPRx register will be resolved using the natural order priority (i.e., the interrupt with a lower corresponding vector number will preempt the interrupt with the higher vector number).

The ability for the user to assign every interrupt source to high or low priority levels means that the user program can give an interrupt with a low natural order priority a higher overall priority level.

9.4 Interrupt Operation

All pending interrupts are indicated by the flag bit being equal to a '1' in the PIRx register. All pending interrupts are resolved using the priority scheme explained in Section 9.3 “Interrupt Priority”.

Once the interrupt source to be serviced is resolved, the program execution vectors to the resolved interrupt vector addresses, as explained in Section 9.2 “Interrupt Vector Table (IVT)”. The vector number is also stored in the WREG register. Most of the flag bits are required to be cleared by the application software, but in some cases, device hardware clears the interrupt automatically. Some flag bits are read-only in the PIRx registers, these flags are a summary of the source interrupts and the corresponding interrupt flags of the source must be cleared.

A valid interrupt can be either a high or low priority interrupt when in main routine or a high priority interrupt when in low priority Interrupt Service Routine. Depending on order of interrupt requests received and their relative timing, the CPU will be in the state of execution indicated by the STAT bits of the INTCON1 register (Register 9-2).

The State machine shown in Figure 9-1 and the subsequent sections detail the execution of interrupts when received in different orders.

### TABLE 9-2: INTERRUPT VECTOR PRIORITY TABLE

<table>
<thead>
<tr>
<th>Vector Number</th>
<th>Interrupt Source</th>
<th>Vector Number</th>
<th>Interrupt Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Software Interrupt</td>
<td>42</td>
<td>TXB0IF</td>
</tr>
<tr>
<td>1</td>
<td>HLVD</td>
<td>43</td>
<td>TXB1IF</td>
</tr>
<tr>
<td>2</td>
<td>OSF</td>
<td>44</td>
<td>TXB2IF/TXBnIF</td>
</tr>
<tr>
<td>3</td>
<td>CSW</td>
<td>45</td>
<td>ERRIF</td>
</tr>
<tr>
<td>4</td>
<td>NVM</td>
<td>46</td>
<td>WAKIF</td>
</tr>
<tr>
<td>5</td>
<td>SCAN</td>
<td>47</td>
<td>IRXIF</td>
</tr>
<tr>
<td>6</td>
<td>CRC</td>
<td>48</td>
<td>C2</td>
</tr>
<tr>
<td>7</td>
<td>IOC</td>
<td>49</td>
<td>SMT2</td>
</tr>
<tr>
<td>8</td>
<td>INT0</td>
<td>50</td>
<td>SMT2PRA</td>
</tr>
<tr>
<td>9</td>
<td>ZCD</td>
<td>51</td>
<td>SMT2PWA</td>
</tr>
<tr>
<td>10</td>
<td>AD</td>
<td>52</td>
<td>DMA2SCNT</td>
</tr>
<tr>
<td>11</td>
<td>ADT</td>
<td>53</td>
<td>DMA2DCNT</td>
</tr>
<tr>
<td>12</td>
<td>C1</td>
<td>54</td>
<td>DMA2OR</td>
</tr>
<tr>
<td>13</td>
<td>SMT1</td>
<td>55</td>
<td>DMA2A</td>
</tr>
<tr>
<td>14</td>
<td>SMT1PRA</td>
<td>56</td>
<td>I2C2RX</td>
</tr>
<tr>
<td>15</td>
<td>SMT1PWA</td>
<td>57</td>
<td>I2C2TX</td>
</tr>
<tr>
<td>16</td>
<td>DMA1SCNT</td>
<td>58</td>
<td>I2C2</td>
</tr>
<tr>
<td>17</td>
<td>DMA1DCNT</td>
<td>59</td>
<td>I2C2E</td>
</tr>
<tr>
<td>18</td>
<td>DMA1OR</td>
<td>60</td>
<td>U2RX</td>
</tr>
<tr>
<td>19</td>
<td>DMA1A</td>
<td>61</td>
<td>U2TX</td>
</tr>
<tr>
<td>20</td>
<td>SPI1RX</td>
<td>62</td>
<td>U2E</td>
</tr>
<tr>
<td>21</td>
<td>SPI1TX</td>
<td>63</td>
<td>SMT2</td>
</tr>
<tr>
<td>22</td>
<td>SPI1</td>
<td>64</td>
<td>TMR3</td>
</tr>
<tr>
<td>23</td>
<td>I2C1RX</td>
<td>65</td>
<td>TMR3G</td>
</tr>
<tr>
<td>24</td>
<td>I2C1TX</td>
<td>66</td>
<td>TMR4</td>
</tr>
<tr>
<td>25</td>
<td>I2C1</td>
<td>67</td>
<td>CCP2</td>
</tr>
<tr>
<td>26</td>
<td>I2C1E</td>
<td>68</td>
<td>CGW2</td>
</tr>
<tr>
<td>27</td>
<td>U1RX</td>
<td>69</td>
<td>CLC2</td>
</tr>
<tr>
<td>28</td>
<td>U1TX</td>
<td>70</td>
<td>INT2</td>
</tr>
<tr>
<td>29</td>
<td>U1E</td>
<td>71</td>
<td>TMR5</td>
</tr>
<tr>
<td>30</td>
<td>U1</td>
<td>72</td>
<td>TMR5G</td>
</tr>
<tr>
<td>31</td>
<td>TMR0</td>
<td>73</td>
<td>TMR6</td>
</tr>
<tr>
<td>32</td>
<td>TMR1</td>
<td>74</td>
<td>CCP3</td>
</tr>
<tr>
<td>33</td>
<td>TMR1G</td>
<td>75</td>
<td>CGW3</td>
</tr>
<tr>
<td>34</td>
<td>TMR2</td>
<td>76</td>
<td>CLC3</td>
</tr>
<tr>
<td>35</td>
<td>CCP1</td>
<td>77</td>
<td>CCP4</td>
</tr>
<tr>
<td>36</td>
<td>NCO</td>
<td>78</td>
<td>CLC4</td>
</tr>
<tr>
<td>37</td>
<td>CGW1</td>
<td>79</td>
<td>—</td>
</tr>
<tr>
<td>38</td>
<td>CLC1</td>
<td>80</td>
<td>—</td>
</tr>
<tr>
<td>39</td>
<td>INT1</td>
<td>81</td>
<td>—</td>
</tr>
</tbody>
</table>

Note: The state of GIEH/L is not changed by the hardware when servicing an interrupt. The internal state machine is used to keep track of execution states. These bits can be manipulated in the user code resulting in transferring execution to the main routine and ignoring existing interrupts.
FIGURE 9-1: VECTORED INTERRUPTS STATE TRANSITION DIAGRAM

- **HIGH INTSTAT = 00**
  - High Interrupt requested
  - High Interrupt addressed
  - Low Interrupt pending
- **LOW INTSTAT = 01**
  - Low Interrupt requested
  - Low Interrupt addressed
  - High Interrupt pending
- **HIGH INTSTAT = 10**
  - High Interrupt requested
  - High Interrupt addressed
  - No pending interrupts
- **LOW INTSTAT = 11**
  - Low Interrupt requested
  - High Interrupt requested
9.4.1 SERVING A HIGH OR LOW PRIORITY INTERRUPT
WHEN MAIN ROUTINE CODE IS EXECUTING

When a high or low priority interrupt is requested when the main routine code
is executing, the main routine execution is halted and the ISR is addressed, see
Figure 9-2. Upon a return from the ISR (by executing the RETFIE instruction),
the main routine resumes execution.

FIGURE 9-2: INTERRUPT EXECUTION: HIGH/LOW PRIORITY INTERRUPT WHEN EXECUTING MAIN ROUTINE

Interrupt

Main Code

ISR Code Executing

RETFIE Executed

Main Code Executing

Main Code Executing

Main Code Executing

Interrupt received

Interrupt cleared
9.4.2 SERVING A HIGH PRIORITY INTERRUPT WHILE A LOW PRIORITY INTERRUPT PENDING

A high priority interrupt request will always take precedence over any interrupt of a lower priority. The high priority interrupt is acknowledged first, then the low-priority interrupt is acknowledged. Upon a return from the high priority ISR (by executing the RETFIE instruction), the low priority interrupt is serviced, see Figure 9-3.

If any other high priority interrupts are pending and enabled, then they are serviced before servicing the pending low priority interrupt. If no other high priority interrupt requests are active, the low priority interrupt is serviced.

FIGURE 9-3: INTERRUPT EXECUTION: HIGH PRIORITY INTERRUPT WITH A LOW PRIORITY INTERRUPT PENDING
9.4.3 PREEMPTING LOW PRIORITY INTERRUPTS

Low-priority interrupts can be preempted by high priority interrupts. While in the low priority ISR, if a high-priority interrupt arrives, the high priority interrupt request is generated and the low priority ISR is suspended, while the high priority ISR is executed, see Figure 9-4.

After the high priority ISR is complete and if any other high priority interrupt requests are not active, the execution returns to the preempted low priority ISR.

Note 1: The high priority interrupt flag must be cleared to avoid recursive interrupts.

2: If a low-priority ISR was already serviced halfway before moving on to a high priority ISR, then the low priority ISR is completely serviced even if user code clears GIEL.
9.4.4 SIMULTANEOUS LOW AND HIGH PRIORITY INTERRUPTS

When both high and low interrupts are active in the same instruction cycle (i.e., simultaneous interrupt events), both the high and the low priority requests are generated. The high priority ISR is serviced first before servicing the low priority interrupt see Figure 9-5.

FIGURE 9-5: INTERRUPT EXECUTION: SIMULTANEOUS LOW AND HIGH PRIORITY INTERRUPTS
9.5  Context Saving

The Interrupt controller supports a two-level deep context saving (Main routine context and Low ISR context). Refer to state machine shown in Figure 9-6 for details.

The Program Counter (PC) is saved on the dedicated device PC stack. CPU registers saved include STATUS, WREG, BSR, FSR0/1/2, PRODL/H and PCLATH/U.

After WREG has been saved to the context registers, the resolved vector number of the interrupt source to be serviced is copied into WREG. Context save and restore operation is completed by the interrupt controller based on current state of the interrupts and the order in which they were sent to the CPU.

Context save/restore works the same way in both states of MVECEN. When IPEN = 0, there is only one level interrupt active. Hence, only the main context is saved when an interrupt is received.

9.5.1  ACCESSING SHADOW REGISTERS

The Interrupt controller automatically saves the context information in the shadow registers available in Bank 56. Both the saved context values (i.e., main routine and low ISR) can be accessed using the same set of shadow registers. By clearing the SHADLO bit in the SHADCON register (Register 9-40), the CPU register values saved for main routine context can accessed, and by setting the SHADLO bit of the CPU register, values saved for low ISR context can accessed. Low ISR context is automatically restored to the CPU registers upon exiting the high ISR. Similarly, the main context is automatically restored to the CPU registers upon exiting the low ISR.

The Shadow registers in Bank 56 are readable and writable, so if the user desires to modify the context then the corresponding shadow register should be modified and the value will be restored when exiting the ISR. Depending on the user’s application, other registers may also need to be saved.
FIGURE 9-6: CONTEXT SAVE STATE MACHINE DIAGRAM

- **MAIN**: INTSTAT = 00
  - Restore Main context
  - Save Main context

- **HIGH**: INTSTAT = 10
  - No Context Save/Restore

- **LOW**: INTSTAT = 01
  - No Context Save/Restore
  - No Context Save/Restore

- **HIGH**: INTSTAT = 11
  - No Context Save/Restore

- **MAIN**: INTSTAT = 00
  - Restore Main context
  - Save Main context
9.6 Returning from Interrupt Service Routine (ISR)

The “Return from Interrupt” instruction (RETFIE) is used to mark the end of an ISR.

When RETFIE 1 instruction is executed, the PC is loaded with the saved PC value from the top of the PC stack. Saved context is also restored with the execution of this instruction. Thus, execution returns to the previous state of operation that existed before the interrupt occurred.

When RETFIE 0 instruction is executed, the saved context is not restored back to the registers.

9.7 Interrupt Latency

By assigning each interrupt with a vector address/number (MVECEN = 1), scanning of all interrupts is not necessary to determine the source of the interrupt.

When MVECEN = 1, Vectored interrupt controller requires three clock cycles to vector to the ISR from main routine, thereby removing dependency of interrupt timing on compiled code.

There is a fixed latency of three instruction cycles between the completion of the instruction active when the interrupt occurred and the first instruction of the Interrupt Service Routine. Figure 9-7, Figure 9-8 and Figure 9-9 illustrates the sequence of events when a peripheral interrupt is asserted when the last executed instruction is one-cycle, two-cycle and three-cycle respectively, when MVECEN = 1.

After the Interrupt Flag Status bit is set, the current instruction completes executing. In the first latency cycle, the contents of the PC, STATUS, WREG, BSR, FSR0/1/2, PRODL/H and PCLATH/U registers are context saved and the IVTBASE+ Vector number is calculated. In the second latency cycle, the PC is loaded with the calculated vector table address for the interrupt source and the starting address of the ISR is fetched. In the third latency cycle, the PC is loaded with the ISR address. All the latency cycles are executed as a FNOP instruction.

When MVECEN = 0, Vectored interrupt controller requires two clock cycles to vector to the ISR from main routine. There is a latency of two instruction cycles plus the software latency between the completion of the instruction active when the interrupt occurred and the first instruction of the Interrupt Service Routine.
FIGURE 9-7: INTERRUPT TIMING DIAGRAM – ONE CYCLE INSTRUCTION

System Clock

Program Counter

Instruction Register

Interrupt

Routine

IVTBASE 0x80

Vector Number 1

Program Memory 0x82 0x86

Interrupt Location = Interrupt vector table entry << 2
= 0x86 << 2 = 0x218

Note 1: Instruction @ X is a one-cycle Instruction
FIGURE 9-8: INTERRUPT TIMING DIAGRAM – TWO WORD INSTRUCTION

System Clock

Program Counter

Instruction Register

Interrupt

Routine

Program Memory

IVTBASE

0x80

Vector Number

1

0x82

0x86

Interrupt Location = Interrupt vector table entry << 2
= 0x86 << 2 = 0x218

Note 1: Instruction @ Y is a two-cycle instruction.
FIGURE 9-9: INTERRUPT TIMING DIAGRAM – THREE CYCLE INSTRUCTION

System Clock

Program Counter

Instruction Register

Interrupt

Routine

IVTBASE

Vector Number

Program Memory

Interrupt Location = Interrupt vector table entry << 2
= 0x86 << 2 = 0x218

Note 1: Instruction @ Z is a three-cycle instruction.
9.7.1 ABORTING INTERRUPTS

If the last instruction before the interrupt controller vectors to the ISR from main routine clears the GIE, PIE or PIR bit associated with the interrupt, the controller executes one force NOP cycle before it returns to the main routine.

Figure 9-10 illustrates the sequence of events when a peripheral interrupt is asserted and then cleared on the last executed instruction cycle.

If the GIE, PIE or PIR bit associated with the interrupt is cleared prior to vectoring to the ISR, then the controller continues executing the main routine.

FIGURE 9-10: INTERRUPT TIMING DIAGRAM - ABORTING INTERRUPTS

Note 1: Inst @ X clears the interrupt flag, Example BCF INTCON0, GIE.
### 9.8 Interrupt Setup Procedure

1. When using interrupt priority levels, set the IPEN bit in INTCON0 register and then select the user-assigned priority level for the interrupt source by writing the control bits in the appropriate IPRx Control register.

   **Note:** At a device Reset, the IPRx registers are initialized, such that all user interrupt sources are assigned to high priority.

2. Clear the Interrupt Flag Status bit associated with the peripheral in the associated PIRx Status register.

3. Enable the interrupt source by setting the interrupt enable control bit associated with the source in the appropriate PIEx Control register.

4. If the vector table is used (MVECEN = 1), then setup the start address for the Interrupt Vector Table using the IVTBASE register. See Section 9.2.2 “Interrupt Vector Table Contents”.

5. Once the IVTBASE is written to, set the Interrupt enable bits in INTCON0 register.

6. An example of setting up interrupts and ISRs using assembly and C can be found in Examples 9-3 and 9-4.

### 9.9 External Interrupt Pins

The PIC18(L)F26/27/45/46/47/55/56/57K42 devices have three external interrupt sources which can be assigned to any pin on different ports based on the PPS settings. Refer Section 17.0 “Peripheral Pin Select (PPS) Module” for possible rerouting options. The external interrupt sources are edge-triggered. If the corresponding INTxEDG bit in the INTCON0 register is set (= 1), the interrupt is triggered by a rising edge. If the bit is clear, the trigger is on the falling edge.

When a valid edge appears on the INTx pin, the corresponding flag bit, INTxF in the PIRx registers, is set. This interrupt can be disabled by clearing the corresponding enable bit, INTxE. Flag bit, INTxF, must be cleared by software in the Interrupt Service Routine before re-enabling the interrupt.

All external interrupts (INT0, INT1 and INT2) can wake-up the processor from Idle or Sleep modes if bit INTxE was set prior to going into those modes. If the Global Interrupt Enable bit, GIE/GIEH, is set, the processor will branch to the interrupt vector following wake-up. Interrupt priority is determined by the value contained in the interrupt priority bits, INT0IP, INT1IP and INT2IP of the IPRx registers.

### 9.10 Wake-up from Sleep

The interrupt controller provides a wake-up request to the CPU whenever an interrupt event occurs, if the interrupt event is enabled. This occurs regardless of whether the part is in Run, Idle/Doze or Sleep modes. The status of the GIEH/GIE bits has no effect on the wake-up request. The wake-up request will be asynchronous to all clocks.

### 9.11 Interrupt Compatibility

When the MVECEN bit in Configuration Word 2L is cleared (Register 5-3), the Interrupt Vector Table feature is disabled and interrupts are compatible with previous high performance 8-bit PIC18 microcontroller devices. In this mode, the Interrupt Vector Table priority has no effect.

When the IPEN bit is also cleared, the interrupt priority feature is disabled and interrupts are compatible with PIC16 microcontroller mid-range devices. All interrupts branch to address 0008h since the interrupt priority is disabled.
EXAMPLE 9-3: SETTING UP VECTORED INTERRUPTS USING MPASM

ISR_TMR0: CODE 0x8C0 ; ISR code at 0x08C0 in PFM
BANKSEL PIR0 ; Select bank for PIR0
BCF PIR3, TMR0IF ; Clear TMR0IF
BTG LATC, 0, ACCESS ; Code to execute in ISR
RETFIE 1 ; Return from ISR

InterruptInit:
BANKSEL INTCON0 ; Select bank for INTCON0
BSF INTCON0, GIEH ; Enable high priority interrupts
BSF INTCON0, GIEL ; Enable low priority interrupts
BSF INTCON0, IPEN_INTCON0 ; Enable interrupt priority
BANKSEL PIE0 ; Select bank for PIE0
BSF PIE3, TMR0IE ; Enable TMR0 interrupt
BSF PIE4, TMR1IE ; Enable TMR1 interrupt
BCF IPR3, TMR0IP ; Make TMR0 interrupt low priority
RETURN 1

VectorTableInit:
; Set IVTBASE (optional - default is 0x000008)
MOVLW 0x00 ; This is optional
MOVWF IVTBASEU, ACCESS ; If not included, then the
MOVLW 0x40 ; hardware default value of
MOVWF IVTBASEH, ACCESS ; 0x0008 will be taken.
MOVLW 0x08
MOVWF IVTBASEL, ACCESS
; TMR0 vector at IVTBASE + 2*(TMR0 vector number i.e. 31) = 0x4046
MOVLW 0x00 ; Load TBLPTR with the
MOVWF TBLPTRU, ACCESS ; PFM memory location to be
MOVLW 0x40 ; written to.
MOVWF TBLPTRH, ACCESS
MOVLW 0x46
MOVWF TBLPTRL, ACCESS
; Write the contents of TMR0 vector location
; ISR_TMR0_ADDRESS >> 2 = 0x08C0 >> 2 = 0x0230
MOVLW 0x30 ; Low byte first
MOVWF TABLAT, ACCESS
TBLWT*+ ; Write to temp table latch
MOVLW 0x02 ; High byte next
MOVWF TABLAT, ACCESS
TBLWT*+ ; Write to temp table latch
; Write to PFM now using NVMCON
BANKSEL NVMCON1 ; Select bank for NVMCON1
MOVLL 0x84 ; Setting to write to PFM
MOVWF NVMCON1
MOVLW 0x55 ; Required unlock sequence
MOVWF NVMCON2
MOVLW 0xAA
MOVWF NVMCON2
BSF NVMCON1, WR ; Start writing to PFM
BTFSC NVMCON1, WR ; Wait for write to complete
GOTO $-2
RETURN 1
EXAMPLE 9-4: SETTING UP VECTORED INTERRUPTS USING XC8

// NOTE 1: If IVTBASE is changed from its default value of 0x000008, then the
// "base(...)" argument must be provided in the ISR. Otherwise the vector
// table will be placed at 0x0008 by default regardless of the IVTBASE value.

// NOTE 2: When MVECEN=0 and IPEN=1, a separate argument as "high_priority"
// or "low_priority" can be used to distinguish between the two ISRs.
// If the argument is not provided, the ISR is considered high priority
// by default.

// NOTE 3: Multiple interrupts can be handled by the same ISR if they are
// specified in the "irq(...)" argument. Ex: irq(IRQ_TMR0, IRQ_CCP1)

void __interrupt(irq(IRQ_TMR0), base(0x4008)) TMR0_ISR(void)
{
    PIR3bits.TMR0IF = 0; // Clear the interrupt flag
    LATCbits.LC0 ^= 1; // ISR code goes here
}

void __interrupt(irq(default), base(0x4008)) DEFAULT_ISR(void)
{
    // Unhandled interrupts go here
}

void INTERRUPT_Initialize (void)
{
    INTCON0bits.GIEH = 1; // Enable high priority interrupts
    INTCON0bits.GIEL = 1; // Enable low priority interrupts
    INTCON0bits.IPEN = 1; // Enable interrupt priority
    PIE3bits.TMR0IE = 1; // Enable TMR0 interrupt
    PIE4bits.TMR1IE = 1; // Enable TMR1 interrupt
    IPR3bits.TMR0IP = 0; // Make TMR0 interrupt low priority

    // Change IVTBASE if required
    IVTBASEU = 0x00; // Optional
    IVTBASEH = 0x40; // Default is 0x0008
    IVTBASEL = 0x08;
}
### 9.12 Register Definitions: Interrupt Control

#### REGISTER 9-1: INTCON0: INTERRUPT CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Value Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>GIE/GIEH</td>
<td>Global Interrupt Enable bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If IPEN = 0:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GIE:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Enables all unmasked interrupts</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Disables all interrupts</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If IPEN = 1:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GIEH:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Enables all unmasked high priority interrupts: bit also needs to be set for enabling low priority interrupts</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Disables all interrupts</td>
</tr>
<tr>
<td>6</td>
<td>GIEL</td>
<td>Global Low Priority Interrupt Enable bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If IPEN = 0:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reserved, read as ’0’</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If IPEN = 1:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GIEL:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Enables all unmasked low priority interrupts, GIEH also needs to be set for low priority interrupts</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Disables all low priority</td>
</tr>
<tr>
<td>5</td>
<td>IPEN</td>
<td>Interrupt Priority Enable bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Enable priority levels on interrupts</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Disable priority levels on interrupts; all interrupts are treated as high priority interrupts</td>
</tr>
<tr>
<td>4-3</td>
<td>Unimplemented</td>
<td>Read as ’0’</td>
</tr>
<tr>
<td>2</td>
<td>INT2EDG</td>
<td>External Interrupt 2 Edge Select bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Interrupt on rising edge of INT2 pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Interrupt on falling edge of INT2 pin</td>
</tr>
<tr>
<td>1</td>
<td>INT1EDG</td>
<td>External Interrupt 1 Edge Select bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Interrupt on rising edge of INT1 pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Interrupt on falling edge of INT1 pin</td>
</tr>
<tr>
<td>0</td>
<td>INT0EDG</td>
<td>External Interrupt 0 Edge Select bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Interrupt on rising edge of INT0 pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Interrupt on falling edge of INT0 pin</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ’0’
- -n = Value at POR
- ’1’ = Bit is set
- ’0’ = Bit is cleared
- x = Bit is unknown
**REGISTER 9-2: INTCON1: INTERRUPT CONTROL REGISTER 1**

<table>
<thead>
<tr>
<th>bit 7-6</th>
<th>STAT&lt;1:0&gt;: Interrupt State Status bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>High priority ISR executing, high priority interrupt was received while a low priority ISR was executing</td>
</tr>
<tr>
<td>10</td>
<td>High priority ISR executing, high priority interrupt was received in main routine</td>
</tr>
<tr>
<td>01</td>
<td>Low priority ISR executing, low priority interrupt was received in main routine</td>
</tr>
<tr>
<td>00</td>
<td>Main routine executing</td>
</tr>
</tbody>
</table>

Legend:
- **HC** = Bit is cleared by hardware
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared
- q = Value depends on condition

**bit 5-0**: Unimplemented: Read as '0'
REGISTER 9-3:  PIR0: PERIPHERAL INTERRUPT REQUEST REGISTER 0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value Explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>IOCIF: Interrupt-on-Change Interrupt Flag bit(2)</td>
<td>1 = Interrupt has occurred 0 = Interrupt event has not occurred</td>
</tr>
<tr>
<td>bit 6</td>
<td>CRCIF: CRC Interrupt Flag bit</td>
<td>1 = Interrupt has occurred (must be cleared by software) 0 = Interrupt event has not occurred</td>
</tr>
<tr>
<td>bit 5</td>
<td>SCANIF: Memory Scanner Interrupt Flag bit</td>
<td>1 = Interrupt has occurred (must be cleared by software) 0 = Interrupt event has not occurred</td>
</tr>
<tr>
<td>bit 4</td>
<td>NVMIF: NVM Interrupt Flag bit</td>
<td>1 = Interrupt has occurred (must be cleared by software) 0 = Interrupt event has not occurred</td>
</tr>
<tr>
<td>bit 3</td>
<td>CSWIF: Clock Switch Interrupt Flag bit(3)</td>
<td>1 = Interrupt has occurred (must be cleared by software) 0 = Interrupt event has not occurred</td>
</tr>
<tr>
<td>bit 2</td>
<td>OSFIF: Oscillator Fail Interrupt Flag bit</td>
<td>1 = Interrupt has occurred (must be cleared by software) 0 = Interrupt event has not occurred</td>
</tr>
<tr>
<td>bit 1</td>
<td>HLVDIF: HLVD Interrupt Flag bit</td>
<td>1 = Interrupt has occurred (must be cleared by software) 0 = Interrupt event has not occurred</td>
</tr>
<tr>
<td>bit 0</td>
<td>SWIF: Software Interrupt Flag bit</td>
<td>1 = Software Interrupt Flag Enable 0 = Software Interrupt Flag Disable</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared  HS = Bit is set in hardware

Note 1: Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

2: IOCIF is a read-only bit. To clear the interrupt condition, all bits in the IOCxF registers must be cleared.

3: The CSWIF interrupt will not wake the system from Sleep. The system will sleep until another interrupt causes the wake-up.
## REGISTER 9-4: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Readable</th>
<th>Writable</th>
<th>Unimplemented</th>
<th>Normal POR/Reset Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>SMT1PWAIF: SMT1 Pulse-Width Acquisition Interrupt Flag bit</td>
<td>1 = Interrupt has occurred (must be cleared by software)</td>
<td>0 = Interrupt event has not occurred</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>SMT1PRAIF: SMT1 Period Acquisition Interrupt Flag bit</td>
<td>1 = Interrupt has occurred (must be cleared by software)</td>
<td>0 = Interrupt event has not occurred</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>SMT1IF: SMT1 Interrupt Flag bit</td>
<td>1 = Interrupt has occurred (must be cleared by software)</td>
<td>0 = Interrupt event has not occurred</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>C1IF: CMP1 Interrupt Flag bit</td>
<td>1 = Interrupt has occurred (must be cleared by software)</td>
<td>0 = Interrupt event has not occurred</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>ADTIF: ADC Threshold Interrupt Flag bit</td>
<td>1 = Interrupt has occurred (must be cleared by software)</td>
<td>0 = Interrupt event has not occurred</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>ADIF: ADC Interrupt Flag bit</td>
<td>1 = Interrupt has occurred (must be cleared by software)</td>
<td>0 = Interrupt event has not occurred</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>ZCDIF: ZCD Interrupt Flag bit</td>
<td>1 = Interrupt has occurred (must be cleared by software)</td>
<td>0 = Interrupt event has not occurred</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>INT0IF: External Interrupt 0 Interrupt Flag bit</td>
<td>1 = Interrupt has occurred (must be cleared by software)</td>
<td>0 = Interrupt event has not occurred</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **1’** = Bit is set
- **0’** = Bit is cleared
- **HS** = Bit is set in hardware

### Notes:
1. Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.
2. The external interrupt GPIO pin is selected by the INTxPPS register.
REGISTER 9-5:  
PIR2: PERIPHERAL INTERRUPT REGISTER 2(1)

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R-0/0</td>
<td>R-0/0</td>
</tr>
<tr>
<td>R-0/0</td>
<td>R-0/0</td>
</tr>
<tr>
<td>R-0/0</td>
<td>R-0/0</td>
</tr>
<tr>
<td>R-0/0</td>
<td>R/W/HS-0/0</td>
</tr>
<tr>
<td>R-0/0</td>
<td>R/W/HS-0/0</td>
</tr>
<tr>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
</tr>
<tr>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
</tr>
<tr>
<td>I2C1RXIF(2)</td>
<td>SPI1IF(3)</td>
</tr>
<tr>
<td>SPI1TXIF(4)</td>
<td>SPI1RXIF(4)</td>
</tr>
<tr>
<td>DMA1AIF</td>
<td>DMA1ORIF</td>
</tr>
<tr>
<td>DMA1DCNTIF</td>
<td>DMA1SCNTIF</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared
- HS = Hardware set

bit 7  I2C1RXIF: I2C1 Receive Interrupt Flag bit(2)
- 1 = Interrupt has occurred
- 0 = Interrupt event has not occurred

bit 6  SPI1IF: SPI1 Interrupt Flag bit(3)
- 1 = Interrupt has occurred
- 0 = Interrupt event has not occurred

bit 5  SPI1TXIF: SPI1 Transmit Interrupt Flag bit(4)
- 1 = Interrupt has occurred
- 0 = Interrupt event has not occurred

bit 4  SPI1RXIF: SPI1 Receive Interrupt Flag bit(4)
- 1 = Interrupt has occurred
- 0 = Interrupt event has not occurred

bit 3  DMA1AIF: DMA1 Abort Interrupt Flag bit
- 1 = Interrupt has occurred (must be cleared by software)
- 0 = Interrupt event has not occurred

bit 2  DMA1ORIF: DMA1 Overrun Interrupt Flag bit
- 1 = Interrupt has occurred (must be cleared by software)
- 0 = Interrupt event has not occurred

bit 1  DMA1DCNTIF: DMA1 Destination Count Interrupt Flag bit
- 1 = Interrupt has occurred (must be cleared by software)
- 0 = Interrupt event has not occurred

bit 0  DMA1SCNTIF: DMA1 Source Count Interrupt Flag bit
- 1 = Interrupt has occurred (must be cleared by software)
- 0 = Interrupt event has not occurred

Note 1: Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

2: I2C1TXIF and I2C1RXIF are read-only bits. To clear the interrupt condition, the CLRBF bit in I2C1STAT1 register must be set.

3: SPIxIF is a read-only bit. To clear the interrupt condition, all bits in the SPIxINTF register must be cleared.

4: SPIxTXIF and SPIxRXIF are read-only bits and cannot be set/cleared by the software.
REGISTER 9-6: PIR3: PERIPHERAL INTERRUPT REGISTER 3\(^{(1)}\)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Readable</th>
<th>Writable</th>
<th>Unimplemented</th>
<th>Hardware Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>TMR0IF: TMR0 Interrupt Flag bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td>HS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td>bit 7</td>
<td>1 =</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Interrupt has occurred (must be cleared by software)</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>0 =</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Interrupt event has not occurred</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>U1IF: UART1 Interrupt Flag bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td></td>
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<tr>
<td></td>
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<td></td>
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<tr>
<td></td>
<td>bit 6</td>
<td>1 =</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Interrupt has occurred</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>0 =</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Interrupt event has not occurred</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>U1EIF: UART1 Framing Error Interrupt Flag bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td></td>
</tr>
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<td></td>
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<td></td>
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<tr>
<td></td>
<td>bit 5</td>
<td>1 =</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Interrupt has occurred</td>
<td></td>
<td></td>
<td></td>
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<tr>
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<td>0 =</td>
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<tr>
<td></td>
<td></td>
<td>Interrupt event has not occurred</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>U1TXIF: UART1 Transmit Interrupt Flag bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>bit 4</td>
<td>1 =</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Interrupt has occurred</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>0 =</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Interrupt event has not occurred</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>U1RXIF: UART1 Receive Interrupt Flag bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td></td>
</tr>
<tr>
<td></td>
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<td></td>
</tr>
<tr>
<td></td>
<td>bit 3</td>
<td>1 =</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Interrupt has occurred</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>0 =</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Interrupt event has not occurred</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>I2C1EIF: I2C1 Error Interrupt Flag bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
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<td></td>
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<td></td>
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<tr>
<td></td>
<td>bit 2</td>
<td>1 =</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Interrupt has occurred</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>0 =</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Interrupt event has not occurred</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>I2C1IF: I2C1 Interrupt Flag bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td></td>
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<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>bit 1</td>
<td>1 =</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Interrupt has occurred</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>0 =</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Interrupt event has not occurred</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>I2C1TXIF: I2C1 Transmit Interrupt Flag bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>bit 0</td>
<td>1 =</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Interrupt has occurred</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 =</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Interrupt event has not occurred</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

2: UxIF is a read-only bit. To clear the interrupt condition, all bits in the UxUIR register must be cleared.

3: UxEIF is a read-only bit. To clear the interrupt condition, all bits in the UxERRIR register must be cleared.

4: UxTXIF and UxRXIF are read-only bits and cannot be set/cleared by the software.

5: I2CxEIF is a read-only bit. To clear the interrupt condition, all bits in the I2CxERR register must be cleared.

6: I2CxIF is a read-only bit. To clear the interrupt condition, all bits in the I2CxPIR register must be cleared.

7: I2C1TXIF and I2C1RXIF are read-only bits. To clear the interrupt condition, the CLRBF bit in I2C1STAT1 register must be set.
**REGISTER 9-7: PIR4: PERIPHERAL INTERRUPT REGISTER 4(1)**

<table>
<thead>
<tr>
<th></th>
<th>INT1IF(2)</th>
<th>CLC1IF</th>
<th>CWG1IF</th>
<th>NCO1IF</th>
<th>CCP1IF</th>
<th>TMR2IF</th>
<th>TMR1GIF</th>
<th>TMR1IF</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
</tr>
<tr>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W =Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared
- HS = Bit is set in hardware

bit 7 **INT1IF:** External Interrupt 1 Interrupt Flag bit(2)
  - 1 = Interrupt has occurred (must be cleared by software)
  - 0 = Interrupt event has not occurred

bit 6 **CLC1IF:** CLC1 Interrupt Flag bit
  - 1 = Interrupt has occurred (must be cleared by software)
  - 0 = Interrupt event has not occurred

bit 5 **CWG1IF:** CWG1 Interrupt Flag bit
  - 1 = Interrupt has occurred (must be cleared by software)
  - 0 = Interrupt event has not occurred

bit 4 **NCO1IF:** NCO1 Interrupt Flag bit
  - 1 = Interrupt has occurred (must be cleared by software)
  - 0 = Interrupt event has not occurred

bit 3 **CCP1IF:** CCP1 Interrupt Flag bit
  - 1 = Interrupt has occurred (must be cleared by software)
  - 0 = Interrupt event has not occurred

bit 2 **TMR2IF:** TMR2 Interrupt Flag bit
  - 1 = Interrupt has occurred (must be cleared by software)
  - 0 = Interrupt event has not occurred

bit 1 **TMR1GIF:** TMR1 Gate Interrupt Flag bit
  - 1 = Interrupt has occurred (must be cleared by software)
  - 0 = Interrupt event has not occurred

bit 0 **TMR1IF:** TMR1 Interrupt Flag bit
  - 1 = Interrupt has occurred (must be cleared by software)
  - 0 = Interrupt event has not occurred

**Note 1:** Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

**Note 2:** The external interrupt GPIO pin is selected by the INTxPPS register.
### REGISTER 9-8:  PIR5: PERIPHERAL INTERRUPT REGISTER 5(1)

<table>
<thead>
<tr>
<th>R/W/HS-0/0</th>
<th>R/W/HS-0/0</th>
<th>R/W/HS-0/0</th>
<th>R/W/HS-0/0</th>
<th>R/W/HS-0/0</th>
<th>R/W/HS-0/0</th>
<th>R/W/HS-0/0</th>
<th>R/W/HS-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRXIF</td>
<td>WAKIF</td>
<td>ERRIF</td>
<td>TXB2IF/TXBnIF</td>
<td>TXB1IF</td>
<td>TXB0IF</td>
<td>RXB1IFn/RXBnIFn</td>
<td>RXB0IFn/FIFOFIF</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘-n/n’ = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **HS** = Bit is set in hardware

#### Bit Descriptions:

**bit 7**  
IRXIF: CAN Invalid Message Received Interrupt Flag bit  
1 = Interrupt has occurred (must be cleared by software)  
0 = Interrupt event has not occurred

**bit 6**  
WAKIF: CAN Bus Wake-Up Activity Interrupt Flag bit  
1 = Interrupt has occurred (must be cleared by software)  
0 = Interrupt event has not occurred

**bit 5**  
ERRIF: CAN Error Interrupt Flag bit (Multiple sources in the COMSTAT register)  
1 = Interrupt has occurred (must be cleared by software)  
0 = Interrupt event has not occurred

**bit 4**  
TXB2IF/TXBnIF: CAN Transmit Buffer 2/Transmit Buffer n Interrupt Flag bit  
1 = Interrupt has occurred (must be cleared by software)  
0 = Interrupt event has not occurred

**bit 3**  
TXB1IF: CAN Transmit Buffer 1 Interrupt Flag bit  
1 = Interrupt has occurred (must be cleared by software)  
0 = Interrupt event has not occurred

**bit 2**  
TXB0IF: CAN Transmit Buffer 0 Interrupt Flag bit  
1 = Interrupt has occurred (must be cleared by software)  
0 = Interrupt event has not occurred

**bit 1**  
RXB1IFn/RXBnIFn: CAN Receive Buffer 1/Receive Buffer n Interrupt Flag bit  
1 = Interrupt has occurred (must be cleared by software)  
0 = Interrupt event has not occurred

**bit 0**  
RXB0IFn/FIFOFIF: CAN Receive Buffer 0/FIFO Full 1 Interrupt Flag bit  
1 = Interrupt has occurred (must be cleared by software)  
0 = Interrupt event has not occurred

#### Note 1:  
Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.
### REGISTER 9-9: PIR6: PERIPHERAL INTERRUPT REGISTER 6(1)

<table>
<thead>
<tr>
<th>Bit</th>
<th>DMA2AIF</th>
<th>DMA2ORIF</th>
<th>DMA2DCNTIF</th>
<th>DMA2SCNTIF</th>
<th>SMT2PWAIF</th>
<th>SMT2PRAIF</th>
<th>SMT2IF</th>
<th>C2IF</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
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<td>R/W/HS-0/0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
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<td>R/W/HS-0/0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **HS** = Bit is set in hardware

**Note 1:** Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.
REGISTER 9-10: PIR7: PERIPHERAL INTERRUPT REGISTER 7(1)

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U2IF(2)</td>
<td>U2EIF(3)</td>
<td>U2TXIF(4)</td>
<td>U2RXIF(4)</td>
<td>I2C2EIF(5)</td>
<td>I2C2IF(6)</td>
<td>I2C2TXIF(7)</td>
<td>I2C2RXIF(7)</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- HS = Bit is set in hardware

bit 7
U2IF: UART2 Interrupt Flag bit(2)
1 = Interrupt has occurred
0 = Interrupt event has not occurred

bit 6
U2EIF: UART2 Framing Error Interrupt Flag bit(3)
1 = Interrupt has occurred
0 = Interrupt event has not occurred

bit 5
U2TXIF: UART2 Transmit Interrupt Flag bit(4)
1 = Interrupt has occurred
0 = Interrupt event has not occurred

bit 4
U2RXIF: UART2 Receive Interrupt Flag bit(4)
1 = Interrupt has occurred
0 = Interrupt event has not occurred

bit 3
I2C2EIF: PCl Interrupt Flag bit(5)
1 = Interrupt has occurred
0 = Interrupt event has not occurred

bit 2
I2C2IF: PCl Interrupt Flag bit(6)
1 = Interrupt has occurred
0 = Interrupt event has not occurred

bit 1
I2C2TXIF: PCl Transmit Interrupt Flag bit(7)
1 = Interrupt has occurred
0 = Interrupt event has not occurred

bit 0
I2C2RXIF: PCl Receive Interrupt Flag bit(7)
1 = Interrupt has occurred
0 = Interrupt event has not occurred

Note 1: Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

2: UxIF is a read-only bit. To clear the interrupt condition, all bits in the UxUIR register must be cleared.
3: UxEIF is a read-only bit. To clear the interrupt condition, all bits in the UxERRIR register must be cleared.
4: UxTXIF and UxRXIF are read-only bits and cannot be set/cleared by the software.
5: I2CxEIF is a read-only bit. To clear the interrupt condition, all bits in the I2CxERR register must be cleared.
6: I2CxIF is a read-only bit. To clear the interrupt condition, all bits in the I2CxPIR register must be cleared.
7: I2C2TXIF and I2C2RXIF are read-only bits. To clear the interrupt condition, the CLRBF bit in I2CxSTAT1 register must be set.
### REGISTER 9-11: PIR8: PERIPHERAL INTERRUPT REGISTER 8

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMR5IF</td>
<td>INT2IF</td>
<td>CLC2IF</td>
<td>CWG2IF</td>
<td>CCP2IF</td>
<td>TMR4IF</td>
<td>TMR3GIF</td>
<td>TMR3IF</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **HS** = Bit is set in hardware

**TMR5IF**: TMR5 Interrupt Flag bit
- 1 = Interrupt has occurred (must be cleared by software)
- 0 = Interrupt event has not occurred

**INT2IF**: External Interrupt 2 Interrupt Flag bit (2)
- 1 = Interrupt has occurred (must be cleared by software)
- 0 = Interrupt event has not occurred

**CLC2IF**: CLC2 Interrupt Flag bit
- 1 = Interrupt has occurred (must be cleared by software)
- 0 = Interrupt event has not occurred

**CWG2IF**: CWG2 Interrupt Flag bit
- 1 = Interrupt has occurred (must be cleared by software)
- 0 = Interrupt event has not occurred

**CCP2IF**: CCP2 Interrupt Flag bit
- 1 = Interrupt has occurred (must be cleared by software)
- 0 = Interrupt event has not occurred

**TMR4IF**: TMR4 Interrupt Flag bit
- 1 = Interrupt has occurred (must be cleared by software)
- 0 = Interrupt event has not occurred

**TMR3GIF**: TMR3G Gate Interrupt Flag bit
- 1 = Interrupt has occurred (must be cleared by software)
- 0 = Interrupt event has not occurred

**TMR3IF**: TMR3 Interrupt Flag bit
- 1 = Interrupt has occurred (must be cleared by software)
- 0 = Interrupt event has not occurred

**Note 1**: Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

**Note 2**: The external interrupt GPIO pin is selected by the INTxPPS register.
## REGISTER 9-12:  PIR9: PERIPHERAL INTERRUPT REGISTER 9\(^{(1)}\)

<table>
<thead>
<tr>
<th>Address</th>
<th>CLC4IF</th>
<th>CCP4IF</th>
<th>CLC3IF</th>
<th>CWG3IF</th>
<th>CCP3IF</th>
<th>TMR6IF</th>
<th>TMR5GIF</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>R/W/HS-0/0</td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

**bit 7**  
**Unimplemented**: Read as ‘0’

**bit 6**  
**CLC4IF**: CLC4 Interrupt Flag bit
- **1** = Interrupt has occurred (must be cleared by software)
- **0** = Interrupt event has not occurred

**bit 5**  
**CCP4IF**: CCP4 Interrupt Flag bit
- **1** = Interrupt has occurred (must be cleared by software)
- **0** = Interrupt event has not occurred

**bit 4**  
**CLC3IF**: CLC3 Interrupt Flag bit
- **1** = Interrupt has occurred (must be cleared by software)
- **0** = Interrupt event has not occurred

**bit 3**  
**CWG3IF**: CWG3 Interrupt Flag bit
- **1** = Interrupt has occurred (must be cleared by software)
- **0** = Interrupt event has not occurred

**bit 2**  
**CCP3IF**: CCP3 Interrupt Flag bit
- **1** = Interrupt has occurred (must be cleared by software)
- **0** = Interrupt event has not occurred

**bit 1**  
**TMR6IF**: TMR6 Interrupt Flag bit
- **1** = Interrupt has occurred (must be cleared by software)
- **0** = Interrupt event has not occurred

**bit 0**  
**TMR5GIF**: TMR5 Gate Interrupt Flag bit
- **1** = Interrupt has occurred (must be cleared by software)
- **0** = Interrupt event has not occurred

### Note 1:
Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.
REGISTER 9-13:  PIE0: PERIPHERAL INTERRUPT ENABLE REGISTER 0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Legend</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>IOCIE: Interrupt-on-Change Enable bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Enabled</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Disabled</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>CRCIE: CRC Interrupt Enable bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Enabled</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Disabled</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>SCANIE: Memory Scanner Interrupt Enable bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Enabled</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Disabled</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>NVMIE: NVM Interrupt Enable bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Enabled</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Disabled</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>CSWIE: Clock Switch Interrupt Enable bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Enabled</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Disabled</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>OSFIE: Oscillator Fail Interrupt Enable bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Enabled</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Disabled</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>HLVDIE: HLVD Interrupt Enable bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Enabled</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Disabled</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>SWIE: Software Interrupt Enable bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Enabled</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Disabled</td>
<td></td>
</tr>
</tbody>
</table>
REGISTER 9-14: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>SMT1PWAIE</td>
<td>SMT1 Pulse Width Acquisition Interrupt Enable bit</td>
</tr>
<tr>
<td>6</td>
<td>SMT1PRAIE</td>
<td>SMT1 Period Acquisition Interrupt Enable bit</td>
</tr>
<tr>
<td>5</td>
<td>SMT1IE</td>
<td>SMT1 Interrupt Enable bit</td>
</tr>
<tr>
<td>4</td>
<td>C1IE</td>
<td>C1 Interrupt Enable bit</td>
</tr>
<tr>
<td>3</td>
<td>ADTIE</td>
<td>ADC Threshold Interrupt Enable bit</td>
</tr>
<tr>
<td>2</td>
<td>ADIE</td>
<td>ADC Interrupt Enable bit</td>
</tr>
<tr>
<td>1</td>
<td>ZCDIE</td>
<td>ZCD Interrupt Enable bit</td>
</tr>
<tr>
<td>0</td>
<td>INT0IE</td>
<td>External Interrupt 0 Enable bit</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

- **1** = Enabled
- **0** = Disabled
**REGISTER 9-15: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>I2C1RXIE: I²C1 Receive Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>6</td>
<td>SPI1IE: SPI1 Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>5</td>
<td>SPI1TXIE: SPI1 Transmit Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>4</td>
<td>SPI1RXIE: SPI1 Receive Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>3</td>
<td>DMA1AIE: DMA1 Abort Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>2</td>
<td>DMA1ORIE: DMA1 Overrun Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>1</td>
<td>DMA1DCNTIE: DMA1 Destination Count Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>0</td>
<td>DMA1SCNTIE: DMA1 Source Count Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets
**REGISTER 9-16: PIE3: PERIPHERAL INTERRUPT ENABLE REGISTER 3**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>TMR0IE: TMR0 Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>6</td>
<td>U1IE: UART1 Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>5</td>
<td>U1EIE: UART1 Framing Error Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>4</td>
<td>U1TXIE: UART1 Transmit Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>3</td>
<td>U1RXIE: UART1 Receive Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>2</td>
<td>I2C1EIE: I2C1 Error Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>1</td>
<td>I2C1IE: I2C1 Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>0</td>
<td>I2C1TXIE: I2C1 Transmit Interrupt Enable bit</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets
### REGISTER 9-17: PIE4: PERIPHERAL INTERRUPT ENABLE REGISTER 4

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>INT1IE</td>
<td>CLC1IE</td>
</tr>
<tr>
<td>CWG1IE</td>
<td>NCO1IE</td>
</tr>
<tr>
<td>CCP1IE</td>
<td>TMR2IE</td>
</tr>
<tr>
<td>TMR1GIE</td>
<td>TMR1IE</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

bit 7 **INT1IE**: External Interrupt 1 Interrupt Enable bit
- 1 = Enabled
- 0 = Disabled

bit 6 **CLC1IE**: CLC1 Interrupt Enable bit
- 1 = Enabled
- 0 = Disabled

bit 5 **CWG1IE**: CWG1 Interrupt Enable bit
- 1 = Enabled
- 0 = Disabled

bit 4 **NCO1IE**: NCO1 Interrupt Enable bit
- 1 = Enabled
- 0 = Disabled

bit 3 **CCP1IE**: CCP1 Interrupt Enable bit
- 1 = Enabled
- 0 = Disabled

bit 2 **TMR2IE**: TMR2 Interrupt Enable bit
- 1 = Enabled
- 0 = Disabled

bit 1 **TMR1GIE**: TMR1 Gate Interrupt Enable bit
- 1 = Enabled
- 0 = Disabled

bit 0 **TMR1IE**: TMR1 Interrupt Enable bit
- 1 = Enabled
- 0 = Disabled
### REGISTER 9-18: PIE5: PERIPHERAL INTERRUPT ENABLE REGISTER 5

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>IRXIE</td>
<td>CAN Invalid Message Received Interrupt Enable bit</td>
</tr>
<tr>
<td>6</td>
<td>WAKIE</td>
<td>CAN Bus Wake-up Activity Interrupt Enable bit</td>
</tr>
<tr>
<td>5</td>
<td>ERRIE</td>
<td>CAN Error Interrupt Enable bit</td>
</tr>
<tr>
<td>4</td>
<td>TXB2IE/TXBnIE</td>
<td>CAN Transmit Buffer 2/Transmit Buffer n Interrupt Enable bit</td>
</tr>
<tr>
<td>3</td>
<td>TXB1IE</td>
<td>CAN Transmit Buffer 1 Interrupt Enable bit</td>
</tr>
<tr>
<td>2</td>
<td>TXB0IE</td>
<td>CAN Transmit Buffer 0 Interrupt Enable bit</td>
</tr>
<tr>
<td>1</td>
<td>RXB1IE/RXBnIE</td>
<td>CAN Receive Buffer 1/Receive Buffer n Interrupt Flag Interrupt Enable bit</td>
</tr>
<tr>
<td>0</td>
<td>RXB0IE/FIFOFIE</td>
<td>CAN Receive Buffer 0/FIFO Full Interrupt Enable bit</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

- **IRXIE**: CAN Invalid Message Received Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled

- **WAKIE**: CAN Bus Wake-up Activity Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled

- **ERRIE**: CAN Error Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled

- **TXB2IE/TXBnIE**: CAN Transmit Buffer 2/Transmit Buffer n Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled

- **TXB1IE**: CAN Transmit Buffer 1 Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled

- **TXB0IE**: CAN Transmit Buffer 0 Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled

- **RXB1IE/RXBnIE**: CAN Receive Buffer 1/Receive Buffer n Interrupt Flag Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled

- **RXB0IE/FIFOFIE**: CAN Receive Buffer 0/FIFO Full Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled
## REGISTER 9-19: PIE6: PERIPHERAL INTERRUPT ENABLE REGISTER 6

<table>
<thead>
<tr>
<th>Bit</th>
<th>DMA2AIE</th>
<th>DMA2ORIE</th>
<th>DMA2DCNTIE</th>
<th>DMA2SCNTIE</th>
<th>SMT2PWAIE</th>
<th>SMT2PRAIE</th>
<th>SMT2IE</th>
<th>C2IE</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- '1' = Bit is set
- '0' = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

- **bit 7 DMA2AIE:** DMA Abort Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled

- **bit 6 DMA2ORIE:** DMA2 Overrun Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled

- **bit 5 DMA2DCNTIE:** DMA2 Destination Count Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled

- **bit 4 DMA2SCNTIE:** DMA2 Source Count Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled

- **bit 3 SMT2PWAIE:** SMT2 Pulse-Width Acquisition Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled

- **bit 2 SMT2PRAIE:** SMT2 Period Acquisition Receive Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled

- **bit 1 SMT2IE:** SMT2 Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled

- **bit 0 C2IE:** C2 Interrupt Enable bit
  - 1 = Enabled
  - 0 = Disabled
### REGISTER 9-20: PIE7: PERIPHERAL INTERRUPT ENABLE REGISTER 7

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U2IE</td>
<td>U2EIE</td>
<td>U2TXIE</td>
<td>U2RXIE</td>
<td>I2C2EIE</td>
<td>I2C2IE</td>
<td>I2C2TXIE</td>
<td>I2C2RXIE</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘-n/n’ = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

- **bit 7**
  - **U2IE**: UART2 Interrupt Enable bit
    - 1 = Enabled
    - 0 = Disabled

- **bit 6**
  - **U2EIE**: UART2 Interrupt Enable bit
    - 1 = Enabled
    - 0 = Disabled

- **bit 5**
  - **U2TXIE**: UART2 Transmit Interrupt Enable bit
    - 1 = Enabled
    - 0 = Disabled

- **bit 4**
  - **U2RXIE**: UART2 Receive Interrupt Enable bit
    - 1 = Enabled
    - 0 = Disabled

- **bit 3**
  - **I2C2EIE**: i²C2 Error Interrupt Enable bit
    - 1 = Enabled
    - 0 = Disabled

- **bit 2**
  - **I2C2IE**: i²C2 Interrupt Enable bit
    - 1 = Enabled
    - 0 = Disabled

- **bit 1**
  - **I2C2TXIE**: i²C2 Transmit Interrupt Enable bit
    - 1 = Enabled
    - 0 = Disabled

- **bit 0**
  - **I2C2RXIE**: i²C2 Receive Interrupt Enable bit
    - 1 = Enabled
    - 0 = Disabled
## REGISTER 9-21: PIE8: PERIPHERAL INTERRUPT ENABLE REGISTER 8

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMR5IE</td>
<td>INT2IE</td>
<td>CLC2IE</td>
<td>CWG2IE</td>
<td>CCP2IE</td>
<td>TMR4IE</td>
<td>TMR3GIE</td>
<td>TMR3IE</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

- **bit 7**  
  - **TMR5IE:** TMR5 Interrupt Enable bit  
    - 1 = Enabled
    - 0 = Disabled

- **bit 6**  
  - **INT2IE:** External Interrupt 2 Interrupt Enable bit  
    - 1 = Enabled
    - 0 = Disabled

- **bit 5**  
  - **CLC2IE:** CLC2 Interrupt Enable bit  
    - 1 = Enabled
    - 0 = Disabled

- **bit 4**  
  - **CWG2IE:** CWG2 Interrupt Enable bit  
    - 1 = Enabled
    - 0 = Disabled

- **bit 3**  
  - **CCP2IE:** CCP2 Interrupt Enable bit  
    - 1 = Enabled
    - 0 = Disabled

- **bit 2**  
  - **TMR4IE:** TMR4 Interrupt Enable bit  
    - 1 = Enabled
    - 0 = Disabled

- **bit 1**  
  - **TMR3GIE:** TMR3 Gate Interrupt Enable bit  
    - 1 = Enabled
    - 0 = Disabled

- **bit 0**  
  - **TMR3IE:** TMR3 Interrupt Enable bit  
    - 1 = Enabled
    - 0 = Disabled
**REGISTER 9-22: PIE9: PERIPHERAL INTERRUPT ENABLE REGISTER 9**

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>CLC4IE</td>
<td>CCP4IE</td>
<td>CLC3IE</td>
<td>CWG3IE</td>
<td>CCP3IE</td>
<td>TMR6IE</td>
<td>TMR5GIE</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

- **bit 7**  
  Unimplemented: Read as ‘0’

- **bit 6**  
  CLC4IE: CLC4 Interrupt Enable bit
  1 = Enabled
  0 = Disabled

- **bit 5**  
  CCP4IE: CCP4 Interrupt Enable bit
  1 = Enabled
  0 = Disabled

- **bit 4**  
  CLC3IE: CLC3 Interrupt Enable bit
  1 = Enabled
  0 = Disabled

- **bit 3**  
  CWG3IE: CWG3 Interrupt Enable bit
  1 = Enabled
  0 = Disabled

- **bit 2**  
  CCP3IE: CCP3 Interrupt Enable bit
  1 = Enabled
  0 = Disabled

- **bit 1**  
  TMR6IE: TMR6 Interrupt Enable bit
  1 = Enabled
  0 = Disabled

- **bit 0**  
  TMR5GIE: TMR5 Interrupt Enable bit
  1 = Enabled
  0 = Disabled
## REGISTER 9-23: IPR0: PERIPHERAL INTERRUPT PRIORITY REGISTER 0

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>IOCIP: Interrupt-on-Change Priority bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 = High priority</td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 6</th>
<th>CRCIP: CRC Interrupt Priority bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 = High priority</td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 5</th>
<th>SCANIP: Memory Scanner Interrupt Priority bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 = High priority</td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 4</th>
<th>NVMIP: NVM Interrupt Priority bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 = High priority</td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 3</th>
<th>CSWIP: Clock Switch Interrupt Priority bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 = High priority</td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 2</th>
<th>OSFIP: Oscillator Fail Interrupt Priority bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 = High priority</td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 1</th>
<th>HLVDIP: HLVD Interrupt Priority bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 = High priority</td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 0</th>
<th>SWIP: Software Interrupt Priority bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 = High priority</td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **’1’** = Bit is set
- **’0’** = Bit is cleared
REGISTER 9-24: IPR1: PERIPHERAL INTERRUPT PRIORITY REGISTER 1

<table>
<thead>
<tr>
<th></th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMT1PWAIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMT1PRAIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMT1IP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADTIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ZCDIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT0IP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7  
SMT1PWAIP: SMT1 Pulse Width Acquisition Interrupt Priority bit
1 = High priority
0 = Low priority

bit 6  
SMT1PRAIP: SMT1 Period Acquisition Interrupt Priority bit
1 = High priority
0 = Low priority

bit 5  
SMT1IP: SMT1 Interrupt Priority bit
1 = High priority
0 = Low priority

bit 4  
C1IP: C1 Interrupt Priority bit
1 = High priority
0 = Low priority

bit 3  
ADTIP: ADC Threshold Interrupt Priority bit
1 = High priority
0 = Low priority

bit 2  
ADIP: ADC Interrupt Priority bit
1 = High priority
0 = Low priority

bit 1  
ZCDIP: ZCD Interrupt Priority bit
1 = High priority
0 = Low priority

bit 0  
INT0IP: External Interrupt 0 Interrupt Priority bit
1 = High priority
0 = Low priority

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared
REGISTER 9-25: IPR2: PERIPHERAL INTERRUPT PRIORITY REGISTER 2

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C1RXIP</td>
<td>SPI1IP</td>
<td>SPI1TXIP</td>
<td>SPI1RXIP</td>
<td>DMA1AIP</td>
<td>DMA1ORIP</td>
<td>DMA1DCNTIP</td>
<td>DMA1SCNTIP</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C1RXIP</td>
<td>I2C1 Receive Interrupt Priority bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = High priority</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
<td></td>
</tr>
<tr>
<td>Bit 6</td>
<td>SPI1IP: SPI1 Transmit Interrupt Priority bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = High priority</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
<td></td>
</tr>
<tr>
<td>Bit 5</td>
<td>SPI1TXIP: I2C1 Transmit Interrupt Priority bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = High priority</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
<td></td>
</tr>
<tr>
<td>Bit 4</td>
<td>SPI1RXIP: SPI1 Receive Interrupt Priority bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = High priority</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
<td></td>
</tr>
<tr>
<td>Bit 3</td>
<td>DMA1AIP: DMA1 Abort Transmit Interrupt Priority bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = High priority</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
<td></td>
</tr>
<tr>
<td>Bit 2</td>
<td>DMA1ORIP: DMA1 Overrun Interrupt Priority bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = High priority</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
<td></td>
</tr>
<tr>
<td>Bit 1</td>
<td>DMA1DCNTIP: DMA1 Destination Count Interrupt Priority bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = High priority</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
<td></td>
</tr>
<tr>
<td>Bit 0</td>
<td>DMA1SCNTIP: DMA1 Source Count Interrupt Priority bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = High priority</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Low priority</td>
<td></td>
</tr>
</tbody>
</table>
## REGISTER 9-26: IPR3: PERIPHERAL INTERRUPT PRIORITY REGISTER 3

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMR0IP</td>
<td>U1IP</td>
<td>U1EIP</td>
<td>U1TXIP</td>
<td>U1RXIP</td>
<td>I2C1EIP</td>
<td>I2C1IP</td>
<td>I2C1TXIP</td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **’1’** = Bit is set
- **’0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TMR0IP: TMR0 Interrupt Priority bit</td>
<td>High priority</td>
</tr>
<tr>
<td>0</td>
<td>Low priority</td>
<td></td>
</tr>
<tr>
<td>Bit 6</td>
<td>U1IP: UART1 Interrupt Priority bit</td>
<td>High priority</td>
</tr>
<tr>
<td></td>
<td>Low priority</td>
<td></td>
</tr>
<tr>
<td>Bit 5</td>
<td>U1EIP: UART1 Framing Error Interrupt Priority bit</td>
<td>High priority</td>
</tr>
<tr>
<td></td>
<td>Low priority</td>
<td></td>
</tr>
<tr>
<td>Bit 4</td>
<td>U1TXIP: UART1 Transmit Interrupt Priority bit</td>
<td>High priority</td>
</tr>
<tr>
<td></td>
<td>Low priority</td>
<td></td>
</tr>
<tr>
<td>Bit 3</td>
<td>U1RXIP: UART1 Receive Interrupt Priority bit</td>
<td>High priority</td>
</tr>
<tr>
<td></td>
<td>Low priority</td>
<td></td>
</tr>
<tr>
<td>Bit 2</td>
<td>I2C1EIP: I2C1 Error Interrupt Priority bit</td>
<td>High priority</td>
</tr>
<tr>
<td></td>
<td>Low priority</td>
<td></td>
</tr>
<tr>
<td>Bit 1</td>
<td>I2C1IP: I2C1 Interrupt Priority bit</td>
<td>High priority</td>
</tr>
<tr>
<td></td>
<td>Low priority</td>
<td></td>
</tr>
<tr>
<td>Bit 0</td>
<td>I2C1TXIP: I2C1 Transmit Interrupt Priority bit</td>
<td>High priority</td>
</tr>
<tr>
<td></td>
<td>Low priority</td>
<td></td>
</tr>
</tbody>
</table>
### REGISTER 9-27: IPR4: PERIPHERAL INTERRUPT PRIORITY REGISTER 4

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>INT1IP</td>
<td>CLC1IP</td>
<td>CWG1IP</td>
<td>NCO1IP</td>
<td>CCP1IP</td>
<td>TMR2IP</td>
<td>TMR1GIP</td>
<td>TMR1IP</td>
</tr>
</tbody>
</table>

#### Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘-n/n’** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

#### Bit Descriptions:

- **bit 7 INT1IP**: External Interrupt 1 Interrupt Priority bit
  - 1 = High priority
  - 0 = Low priority
- **bit 6 CLC1IP**: CLC1 Interrupt Priority bit
  - 1 = High priority
  - 0 = Low priority
- **bit 5 CWG1IP**: CWG1 Interrupt Priority bit
  - 1 = High priority
  - 0 = Low priority
- **bit 4 NCO1IP**: NCO1 Interrupt Priority bit
  - 1 = High priority
  - 0 = Low priority
- **bit 3 CCP1IP**: CCP1 Interrupt Priority bit
  - 1 = High priority
  - 0 = Low priority
- **bit 2 TMR2IP**: TMR2 Interrupt Priority bit
  - 1 = High priority
  - 0 = Low priority
- **bit 1 TMR1GIP**: TMR1 Gate Interrupt Priority bit
  - 1 = High priority
  - 0 = Low priority
- **bit 0 TMR1IP**: TMR1 Interrupt Priority bit
  - 1 = High priority
  - 0 = Low priority
### PIC18(L)F25/26K83

**Register 9-28: IPR5: Peripheral Interrupt Priority Register 5**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>IRXIP</td>
<td>CAN Invalid Message Received Interrupt Priority bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(1) = High priority (0) = Low priority</td>
</tr>
<tr>
<td>6</td>
<td>WAKIP</td>
<td>CAN Bus Wake-Up Activity Interrupt Priority bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(1) = High priority (0) = Low priority</td>
</tr>
<tr>
<td>5</td>
<td>ERRIP</td>
<td>CAN Error Interrupt Priority bit (Multiple Sources in the COMSTAT Register)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(1) = High priority (0) = Low priority</td>
</tr>
<tr>
<td>4</td>
<td>TXB2IP/TXBnIP</td>
<td>CAN Transmit Buffer 2/Transmit Buffer n Interrupt Priority bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(1) = High priority (0) = Low priority</td>
</tr>
<tr>
<td>3</td>
<td>TXB1IP</td>
<td>CAN Transmit Buffer 1 Interrupt Priority bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(1) = High priority (0) = Low priority</td>
</tr>
<tr>
<td>2</td>
<td>TXB0IP</td>
<td>CAN Transmit Buffer 0 Interrupt Priority bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(1) = High priority (0) = Low priority</td>
</tr>
<tr>
<td>1</td>
<td>RXB1IP/RXBnIP</td>
<td>CAN Receive Buffer 1/Receive Buffer n Interrupt Priority bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(1) = High priority (0) = Low priority</td>
</tr>
<tr>
<td>0</td>
<td>RXB0IP/FIFOFIP</td>
<td>CAN Receive Buffer 0/FIFO Full Interrupt Priority bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(1) = High priority (0) = Low priority</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- \(-n/n\) = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
## REGISTER 9-29: IPR6: PERIPHERAL INTERRUPT PRIORITY REGISTER 6

<table>
<thead>
<tr>
<th>Bit</th>
<th>DMA2AIP</th>
<th>DMA2ORIP</th>
<th>DMA2DCNTIP</th>
<th>DMA2SCNTIP</th>
<th>SMT2PWAIP</th>
<th>SMT2PRAIP</th>
<th>SMT2IP</th>
<th>C2IP</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>DMA2ORIP</td>
<td></td>
<td></td>
<td>DMA2DCNTIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>DMA2DCNTIP</td>
<td></td>
<td></td>
<td>DMA2SCNTIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>SMT2PWAIP</td>
<td></td>
<td></td>
<td>SMT2PRAIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>SMT2PRAIP</td>
<td></td>
<td></td>
<td>SMT2IP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>SMT2IP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>C2IP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

### Bit 7
**DMA2AIP**: DMA2 Abort Interrupt Priority bit
- **1** = High priority
- **0** = Low priority

### Bit 6
**DMA2ORIP**: DMA2 Overrun Interrupt Priority bit
- **1** = High priority
- **0** = Low priority

### Bit 5
**DMA2DCNTIP**: DMA2 Destination Count Interrupt Priority bit
- **1** = High priority
- **0** = Low priority

### Bit 4
**DMA2SCNTIP**: DMA2 Source Count Interrupt Priority bit
- **1** = High priority
- **0** = Low priority

### Bit 3
**SMT2PWAIP**: SMT2 Pulse-Width Acquisition Interrupt Priority bit
- **1** = High priority
- **0** = Low priority

### Bit 2
**SMT2PRAIP**: SMT2 Period Acquisition Interrupt Priority bit
- **1** = High priority
- **0** = Low priority

### Bit 1
**SMT2IP**: SMT2 Interrupt Priority bit
- **1** = High priority
- **0** = Low priority

### Bit 0
**C2IP**: C2 Interrupt Priority bit
- **1** = High priority
- **0** = Low priority
## REGISTER 9-30: IPR7: PERIPHERAL INTERRUPT PRIORITY REGISTER 7

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Readable</th>
<th>Writable</th>
<th>Unimplemented</th>
<th>Value at POR and BOR</th>
<th>Value at all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>U2IP: UART2 Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>U2EIP: UART2 Framing Error Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>U2TXIP: UART2 Transmit Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>U2RXIP: UART2 Receive Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>I2C2EIP: I2C2 Error Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>I2C2IP: I2C2 Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>I2C2TXIP: I2C2 Transmit Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>I2C2RXIP: TMR4 Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
### REGISTER 9-31: IPR8: PERIPHERAL INTERRUPT PRIORITY REGISTER 8

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
<th>Value</th>
<th>Value</th>
<th>Value</th>
<th>Value</th>
<th>Value</th>
<th>Value</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>TMR5IP: TMR5 Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>INT2IP: External Interrupt 2 Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>CLC2IP: CLC2 Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>CWG2IP: CWG2 Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>CCP2IP: CCP2 Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>TMR4IP: TMR4 Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>TMR3GIP: TMR3 Gate Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>TMR3IP: TMR3 Interrupt Priority bit</td>
<td>1 = High priority</td>
<td>0 = Low priority</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **’1’** = Bit is set
- **’0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets
## REGISTER 9-32: IPR9: PERIPHERAL INTERRUPT PRIORITY REGISTER 9

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Description</th>
<th>Value at POR/BOR</th>
<th>Value at all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>TMR5GIP</td>
<td>TMR5 Interrupt Priority bit</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>TMR6IP</td>
<td>TMR6IP Interrupt Priority bit</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>CCP3IP</td>
<td>CCP3 Interrupt Priority bit</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>CWG3IP</td>
<td>CWG3 Interrupt Priority bit</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>CLC3IP</td>
<td>CLC3 Interrupt Priority bit</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>CCP4IP</td>
<td>CCP4 Interrupt Priority bit</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>CLC4IP</td>
<td>CLC4 Interrupt Priority bit</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>Unimplemented</td>
<td>Unimplemented bit</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ’0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

### Bit Descriptions

- **bit 7**
  - **Unimplemented**: Read as '0'

- **bit 6**
  - **CLC4IP**: CLC4 Interrupt Priority bit
    - 1 = High priority
    - 0 = Low priority

- **bit 5**
  - **CCP4IP**: CCP4 Interrupt Priority bit
    - 1 = High priority
    - 0 = Low priority

- **bit 4**
  - **CLC3IP**: CLC3 Interrupt Priority bit
    - 1 = High priority
    - 0 = Low priority

- **bit 3**
  - **CWG3IP**: CWG3 Interrupt Priority bit
    - 1 = High priority
    - 0 = Low priority

- **bit 2**
  - **CCP3IP**: CCP3 Interrupt Priority bit
    - 1 = High priority
    - 0 = Low priority

- **bit 1**
  - **TMR6IP**: TMR6IP Interrupt Priority bit
    - 1 = High priority
    - 0 = Low priority

- **bit 0**
  - **TMR5GIP**: TMR5 Interrupt Priority bit
    - 1 = High priority
    - 0 = Low priority
## REGISTER 9-33: IVTBASEU: INTERRUPT VECTOR TABLE BASE ADDRESS UPPER REGISTER

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>BASE&lt;20:16&gt;</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

**bit 7-5** Unimplemented: Read as ‘0’

**bit 4-0** BASE<20:16>: Interrupt Vector Table Base Address bits

## REGISTER 9-34: IVTBASEH: INTERRUPT VECTOR TABLE BASE ADDRESS HIGH REGISTER

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>BASE&lt;15:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

**bit 7-0** BASE<15:8>: Interrupt Vector Table Base Address bits

## REGISTER 9-35: IVTBASEL: INTERRUPT VECTOR TABLE BASE ADDRESS LOW REGISTER

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-1/1</td>
</tr>
<tr>
<td>BASE&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

**bit 7-0** BASE<7:0>: Interrupt Vector Table Base Address bits
REGISTER 9-36: IVTADU: INTERRUPT VECTOR TABLE ADDRESS UPPER REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R-0/0</th>
<th>R-0/0</th>
<th>R-0/0</th>
<th>R-0/0</th>
<th>R-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

AD<20:16>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared

bit 7-5  **Unimplemented**: Read as '0'
bit 4-0  **AD<20:16>**: Interrupt Vector Table Address bits

REGISTER 9-37: IVTADH: INTERRUPT VECTOR TABLE ADDRESS HIGH REGISTER

<table>
<thead>
<tr>
<th>R-0/0</th>
<th>R-0/0</th>
<th>R-0/0</th>
<th>R-0/0</th>
<th>R-0/0</th>
<th>R-0/0</th>
<th>R-0/0</th>
<th>R-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

AD<15:8>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared

bit 7-0  **AD<15:8>**: Interrupt Vector Table Address bits

REGISTER 9-38: IVTADL: INTERRUPT VECTOR TABLE ADDRESS LOW REGISTER

<table>
<thead>
<tr>
<th>R-0/0</th>
<th>R-0/0</th>
<th>R-0/0</th>
<th>R-0/0</th>
<th>R-1/1</th>
<th>R-0/0</th>
<th>R-0/0</th>
<th>R-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

AD<7:0>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared

bit 7-0  **AD<7:0>**: Interrupt Vector Table Address bits
REGISTER 9-39:  IVTLOCK: INTERRUPT VECTOR TABLE LOCK REGISTER

| bit 7-1 | Unimplemented: Read as ‘0’ |
| bit 0   | IVTLOCKED: IVT Registers Lock bits(1,2) |
|        | 1 = IVTBASE Registers are locked and cannot be written |
|        | 0 = IVTBASE Registers can be modified by write operations |

Note 1:  The IVTLOCK bit can only be set or cleared after the unlock sequence in Example 9-1.
Note 2:  If IVT1WAY = 1, the IVTLOCK bit cannot be cleared after it has been set. See Register 5-3.

REGISTER 9-40:  SHADCON: SHADOW CONTROL REGISTER

| bit 7-1 | Unimplemented: Read as ‘0’ |
| bit 0   | SHADLO: Interrupt Shadow Register Access Switch bit |
|        | 0 = Access Main Context for Interrupt Shadow Registers |
|        | 1 = Access Low-Priority Interrupt Context for Interrupt Shadow Registers |
### TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON0</td>
<td>GIE/GIEH</td>
<td>GIEL</td>
<td>IPEN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>125</td>
</tr>
<tr>
<td>INTCON1</td>
<td>STAT&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>126</td>
</tr>
<tr>
<td>PIE0</td>
<td>IOCIE</td>
<td>CRCIE</td>
<td>SCANIE</td>
<td>NVMIE</td>
<td>CSWIE</td>
<td>OSFIE</td>
<td>HLVDIE</td>
<td>SWIE</td>
<td>137</td>
</tr>
<tr>
<td>PIE1</td>
<td>SMT1PWAIE</td>
<td>SMT1PRAIE</td>
<td>SMT1IE</td>
<td>CIE</td>
<td>ADTIE</td>
<td>ADIE</td>
<td>ZCDIE</td>
<td>INT0IE</td>
<td>138</td>
</tr>
<tr>
<td>PIE2</td>
<td>I2C1RXIE</td>
<td>SP1IE</td>
<td>SP1TXIE</td>
<td>SP1RXIE</td>
<td>DMA1AIE</td>
<td>DMA1ORIE</td>
<td>DMA1CNTIE</td>
<td>DMA1SNTIE</td>
<td>139</td>
</tr>
<tr>
<td>PIE3</td>
<td>TMR0IE</td>
<td>U1IE</td>
<td>U1EIE</td>
<td>U1TXIE</td>
<td>U1RXIE</td>
<td>I2C1IE</td>
<td>I2C2IE</td>
<td>I2C1TXIE</td>
<td>140</td>
</tr>
<tr>
<td>PIE4</td>
<td>INT1IE</td>
<td>CLC1IE</td>
<td>CGW1IE</td>
<td>NCO1IE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>TMR1FE</td>
<td>141</td>
</tr>
<tr>
<td>PIE5</td>
<td>IRXIE</td>
<td>WAKIE</td>
<td>ERRIE</td>
<td>TXB2IE/TX8nIE</td>
<td>TXB1IE</td>
<td>TXB0IE</td>
<td>RXB1IE/RXBnIE</td>
<td>RXB0IE/FIFOFIE</td>
<td>142</td>
</tr>
<tr>
<td>PIE6</td>
<td>DMA2AIE</td>
<td>DMA2ORIE</td>
<td>DMA2CNTIE</td>
<td>DMA2SNTIE</td>
<td>DMA2PWAIE</td>
<td>DMA2PRAIE</td>
<td>DMA2TIE</td>
<td>DMA2TIF</td>
<td>143</td>
</tr>
<tr>
<td>PIE7</td>
<td>U2IE</td>
<td>U2EIE</td>
<td>U2TXIE</td>
<td>U2RXIE</td>
<td>I2C2IE</td>
<td>I2C2IE</td>
<td>I2C2TXIE</td>
<td>I2C2XIE</td>
<td>144</td>
</tr>
<tr>
<td>PIE8</td>
<td>TMR5IE</td>
<td>INT2IE</td>
<td>CLC2IE</td>
<td>CGW2IE</td>
<td>CCP2IE</td>
<td>TMR4IE</td>
<td>TMR3IE</td>
<td>TMR3IE</td>
<td>145</td>
</tr>
<tr>
<td>PIE9</td>
<td>—</td>
<td>CLC4IE</td>
<td>CCP4IE</td>
<td>CLC3IE</td>
<td>CGW3IE</td>
<td>CCP3IE</td>
<td>TMR6IE</td>
<td>TMR5IE</td>
<td>146</td>
</tr>
<tr>
<td>PIR0</td>
<td>IOCIF</td>
<td>CRCIF</td>
<td>SCANIF</td>
<td>NVMIF</td>
<td>CSWIF</td>
<td>OSFIF</td>
<td>HLVDIF</td>
<td>SWIF</td>
<td>127</td>
</tr>
<tr>
<td>PIR1</td>
<td>SMT1PWAIF</td>
<td>SMT1PRAIF</td>
<td>SMT1IF</td>
<td>C1IF</td>
<td>ADTIF</td>
<td>ADIF</td>
<td>ZCDIF</td>
<td>INT0IF</td>
<td>128</td>
</tr>
<tr>
<td>PIR2</td>
<td>I2C1RXIF</td>
<td>SP1IF</td>
<td>SP1TXIF</td>
<td>SP1RXIF</td>
<td>DMA1IF</td>
<td>DMA1ORIF</td>
<td>DMA1DNTIE</td>
<td>DMA1SNTIE</td>
<td>129</td>
</tr>
<tr>
<td>PIR3</td>
<td>TMR0IF</td>
<td>U1IF</td>
<td>U1EIE</td>
<td>U1TXIF</td>
<td>U1RXIF</td>
<td>I2C1IE</td>
<td>I2C2IE</td>
<td>I2C1TXIF</td>
<td>130</td>
</tr>
<tr>
<td>PIR4</td>
<td>INT1IF</td>
<td>CLC1IF</td>
<td>CGW1IF</td>
<td>NCO1IF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>TMR1IF</td>
<td>131</td>
</tr>
<tr>
<td>PIR5</td>
<td>IRXIF</td>
<td>WAKIF</td>
<td>ERRIF</td>
<td>TXB2IF/TX8nIF</td>
<td>TXB1IF</td>
<td>TXB0IF</td>
<td>RXB1IF/RXBnIF</td>
<td>RXB0IF/FIFOFIF</td>
<td>132</td>
</tr>
<tr>
<td>PIR6</td>
<td>DMA2AIF</td>
<td>DMA2ORIF</td>
<td>DMA2DNTIE</td>
<td>DMA2SNTIE</td>
<td>DMA2PWAIF</td>
<td>DMA2PRAIF</td>
<td>DMA2TIE</td>
<td>DMA2TIF</td>
<td>133</td>
</tr>
<tr>
<td>PIR7</td>
<td>U2IF</td>
<td>U2EIE</td>
<td>U2TXIF</td>
<td>U2RXIF</td>
<td>I2C2IE</td>
<td>I2C2IF</td>
<td>I2C2TXIF</td>
<td>I2C2XIF</td>
<td>134</td>
</tr>
<tr>
<td>PIR8</td>
<td>TMR5IF</td>
<td>INT2IF</td>
<td>CLC2IF</td>
<td>CGW2IF</td>
<td>CCP2IF</td>
<td>TMR4IF</td>
<td>TMR3IF</td>
<td>TMR3IF</td>
<td>135</td>
</tr>
<tr>
<td>PIR9</td>
<td>—</td>
<td>CLC4IF</td>
<td>CCP4IF</td>
<td>CLC3IF</td>
<td>CGW3IF</td>
<td>CCP3IF</td>
<td>TMR6IF</td>
<td>TMR5IF</td>
<td>136</td>
</tr>
<tr>
<td>IPR0</td>
<td>IOCIP</td>
<td>CRCIP</td>
<td>SCANIP</td>
<td>NVMIP</td>
<td>CSWIP</td>
<td>OSFIP</td>
<td>HLVDIP</td>
<td>SWIP</td>
<td>147</td>
</tr>
<tr>
<td>IPR1</td>
<td>SMT1PWAIP</td>
<td>SMT1PRAIP</td>
<td>SMT1IP</td>
<td>C1IP</td>
<td>ADTIP</td>
<td>ADIP</td>
<td>ZCDIP</td>
<td>INT0IP</td>
<td>148</td>
</tr>
<tr>
<td>IPR2</td>
<td>I2C1RIP</td>
<td>SP1IP</td>
<td>SP1TIP</td>
<td>SP1RIP</td>
<td>DMA1IP</td>
<td>DMA1ORIP</td>
<td>DMA1DNTIE</td>
<td>DMA1SNTIE</td>
<td>149</td>
</tr>
<tr>
<td>IPR3</td>
<td>TMR0IP</td>
<td>U1IP</td>
<td>U1EIP</td>
<td>U1TXIP</td>
<td>U1RXIP</td>
<td>I2C1IE</td>
<td>I2C2IE</td>
<td>I2C1TXIP</td>
<td>150</td>
</tr>
<tr>
<td>IPR4</td>
<td>INT1IP</td>
<td>CLC1IP</td>
<td>CGW1IP</td>
<td>NCO1IP</td>
<td>CCP1IP</td>
<td>TMR2IP</td>
<td>TMR1IP</td>
<td>TMR1IP</td>
<td>151</td>
</tr>
<tr>
<td>IPR5</td>
<td>IRXIP</td>
<td>WAKIP</td>
<td>ERRIP</td>
<td>TXB2IP/TX8nIP</td>
<td>TXB1IP</td>
<td>TXB0IP</td>
<td>RXB1IP/RXBnIP</td>
<td>RXB0IP/FIFOFIP</td>
<td>152</td>
</tr>
<tr>
<td>IPR6</td>
<td>DMA2AIP</td>
<td>DMA2ORIP</td>
<td>DMA2DNTIE</td>
<td>DMA2SNTIE</td>
<td>DMA2PWAIP</td>
<td>DMA2PRAIP</td>
<td>DMA2TIP</td>
<td>DMA2TIF</td>
<td>153</td>
</tr>
<tr>
<td>IPR7</td>
<td>U2IP</td>
<td>U2EIP</td>
<td>U2TXIP</td>
<td>U2RXIP</td>
<td>I2C2IE</td>
<td>I2C2IP</td>
<td>I2C2TXIP</td>
<td>I2C2XIP</td>
<td>154</td>
</tr>
<tr>
<td>IPR8</td>
<td>TMR5IP</td>
<td>INT2IP</td>
<td>CLC2IP</td>
<td>CGW2IP</td>
<td>CCP2IP</td>
<td>TMR4IP</td>
<td>TMR3IP</td>
<td>TMR3IP</td>
<td>155</td>
</tr>
<tr>
<td>IPR9</td>
<td>—</td>
<td>CLC4IP</td>
<td>CCP4IP</td>
<td>CLC3IP</td>
<td>CGW3IP</td>
<td>CCP3IP</td>
<td>TMR6IP</td>
<td>TMR5IP</td>
<td>156</td>
</tr>
<tr>
<td>IVTBASEU</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>BASE&lt;20:16&gt;</td>
<td>157</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IVTBASEH</td>
<td>BASE&lt;15:8&gt;</td>
<td>157</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IVTBASEL</td>
<td>BASE&lt;7:0&gt;</td>
<td>157</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IVTADU</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>AD&lt;20:16&gt;</td>
<td>158</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IVTADH</td>
<td>AD&lt;15:8&gt;</td>
<td>158</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IVTADL</td>
<td>AD&lt;7:0&gt;</td>
<td>158</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IVTLOCK</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IVTLOCKED</td>
<td>159</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- "—" = unimplemented locations, read as '0'. Shaded bits are not used for interrupts.
10.0 **POWER-SAVING OPERATION MODES**

The purpose of the Power-Down modes is to reduce power consumption. There are three Power-Down modes:

- Doze mode
- Sleep mode
- Idle mode

10.1 **Doze Mode**

Doze mode allows for power saving by reducing CPU operation and program memory (PFM) access, without affecting peripheral operation. Doze mode differs from Sleep mode because the bandgap and system oscillators continue to operate, while only the CPU and PFM are affected. The reduced execution saves power by eliminating unnecessary operations within the CPU and memory.

When the Doze Enable (DOZEN) bit is set (DOZEN = 1), the CPU executes only one instruction cycle out of every N cycles as defined by the DOZE<2:0> bits of the CPUDOZE register. For example, if DOZE<2:0> = 001, the instruction cycle ratio is 1:4. The CPU and memory execute for one instruction cycle and then lay idle for three instruction cycles. During the unused cycles, the peripherals continue to operate at the system clock speed.

10.1.1 **DOZE OPERATION**

The Doze operation is illustrated in **Figure 10-1**. For this example:

- Doze enable (DOZEN) bit set (DOZEN = 1)
- **DOZE<2:0> = 001 (1:4)** ratio
- **Recover-on-Interrupt (ROI) bit set (ROI = 1)**

As with normal operation, the PFM fetches for the next instruction cycle. The Q-clocks to the peripherals continue throughout.

---

**FIGURE 10-1: DOZE MODE OPERATION EXAMPLE (DOZE<2:0> = 001, 1:4)**

- **FOSC**
- **CPU Clocks**
- **Program Counter**
- **CPU Operation**

**Note 1:** Multicycle instructions are executed to completion before fetching the interrupt vector.

**Note 2:** If the prefetched instruction clears the interrupt enable or GIEx, ISR vectoring will not occur, but DOZEN is cleared and the CPU will resume execution at full speed.
10.1.2 INTERRUPTS DURING DOZE

If an interrupt occurs and the Recover-On-Interrupt bit is clear (ROI = 0) at the time of the interrupt, the Interrupt Service Routine (ISR) continues to execute at the rate selected by DOZE<2:0>. Interrupt latency is extended by the DOZE<2:0> ratio.

If an interrupt occurs and the ROI bit is set (ROI = 1) at the time of the interrupt, the DOZEN bit is cleared and the CPU executes at full speed. The prefetched instruction is executed and then the interrupt vector sequence is executed. In Figure 10-1, the interrupt occurs during the 2nd instruction cycle of the Doze period, and immediately brings the CPU out of Doze. If the Doze-On-Exit (DOE) bit is set (DOE = 1) when the RETFIE operation is executed, DOZEN is set, and the CPU executes at the reduced rate based on the DOZE<2:0> ratio.

EXAMPLE 10-1: DOZE SOFTWARE EXAMPLE

```c
//Mainline operation
bool somethingToDo = FALSE:
void main()
{
    initializeSystem();
    // DOZE = 64:1 (for example)
    // ROI = 1;
    GIE = 1; // enable interrupts
    while (1)
    {
        // If ADC completed, process data
        if (somethingToDo)
        {
            doSomething();
            DOZEN = 1; // resume low-power
        }
    }

    // Data interrupt handler
    void interrupt()
    {
        // DOZEN = 0 because ROI = 1
        if (ADIF)
        {
            somethingToDo = TRUE;
            DOE = 0; // make main() go fast
            ADIF = 0;
        }
        // else check other interrupts...
        if (TMR0IF)
        {
            timerTick++;
            DOE = 1; // make main() go slow
            TMR0IF = 0;
        }
    }
}
```

10.2 Sleep Mode

Sleep mode is entered by executing the SLEEP instruction, while the Idle Enable (IDLEN) bit of the CPUDOZE register is clear (IDLEN = 0).

Upon entering Sleep mode, the following conditions exist:
1. WDT will be cleared but keeps running if enabled for operation during Sleep
2. The PD bit of the STATUS register is cleared (Register 4-2)
3. The TO bit of the STATUS register is set (Register 4-2)
4. The CPU clock is disabled
5. LFINTOSC, SOSC, HFINTOSC and ADCRC are unaffected and peripherals using them may continue operation in Sleep.
6. I/O ports maintain the status they had before Sleep was executed (driving high, low, or high-impedance)
7. Resets other than WDT are not affected by Sleep mode

Refer to individual chapters for more details on peripheral operation during Sleep.

To minimize current consumption, the following conditions should be considered:
- I/O pins should not be floating
- External circuitry sinking current from I/O pins
- Internal circuitry sourcing current from I/O pins
- Current draw from pins with internal weak pull-ups
- Modules using any oscillator

I/O pins that are high-impedance inputs should be pulled to VDD or VSS externally to avoid switching currents caused by floating inputs.

Examples of internal circuitry that might be sourcing current include modules such as the DAC and FVR modules. See Section 38.0 “5-Bit Digital-to-Analog Converter (DAC) Module” and Section 35.0 “Fixed Voltage Reference (FVR)” for more information on these modules.
10.2.1 WAKE-UP FROM SLEEP

The device can wake up from Sleep through one of the following events:

1. External Reset input on MCLR pin, if enabled
2. BOR Reset, if enabled
3. Low-Power Brown-Out Reset (LPBOR), if enabled
4. POR Reset
5. Windowed Watchdog Timer, if enabled
6. All interrupt sources except clock switch interrupt can wake up the part.

The first five events will cause a device Reset. The last one event is considered a continuation of program execution. To determine whether a device Reset or wake-up event occurred, refer to Section 6.13 “Power Control (PCON0/PCON1) Register”.

When the SLEEP instruction is being executed, the next instruction (PC + 2) is prefetched. For the device to wake-up through an interrupt event, the corresponding Interrupt Enable bit must be enabled. Wake-up will occur regardless of the state of the GIE bit. If the GIE bit is disabled, the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is enabled, the device executes the instruction after the SLEEP instruction, the device will then call the Interrupt Service Routine. In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

The WDT is cleared when the device wakes-up from Sleep, regardless of the source of wake-up.

Upon a wake from a Sleep event, the core will wait for a combination of three conditions before beginning execution. The conditions are:

- PFM Ready
- COSC-Selected Oscillator Ready
- BOR Ready (unless BOR is disabled)

10.2.2 WAKE-UP USING INTERRUPTS

When any interrupt source, with the exception of the clock switch interrupt, has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs before the execution of a SLEEP instruction
  - SLEEP instruction will execute as a NOP
  - WDT and WDT prescaler will not be cleared
  - TO bit of the STATUS register will not be set
  - PD bit of the STATUS register will not be cleared

- If the interrupt occurs during or after the execution of a SLEEP instruction
  - SLEEP instruction will be completely executed
  - Device will immediately wake-up from Sleep
  - WDT and WDT prescaler will be cleared
  - TO bit of the STATUS register will be set
  - PD bit of the STATUS register will be cleared

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the PD bit. If the PD bit is set, the SLEEP instruction was executed as a NOP.
10.2.3 LOW-POWER SLEEP MODE

The PIC18F25/26K83 device family contains an internal Low Dropout (LDO) voltage regulator, which allows the device I/O pins to operate at voltages up to 5.5V while the internal device logic operates at a lower voltage. The LDO and its associated reference circuitry must remain active when the device is in Sleep mode.

The PIC18F25/26K83 devices allows the user to optimize the operating current in Sleep, depending on the application requirements.

Low-Power Sleep mode can be selected by setting the VREGPM bit of the VREGCON register.

10.2.3.1 Sleep Current vs. Wake-up Time

In the default operating mode, the LDO and reference circuitry remain in the normal configuration while in Sleep. The device is able to exit Sleep mode quickly since all circuits remain active. In Low-Power Sleep mode, when waking-up from Sleep, an extra delay time is required for these circuits to return to the normal configuration and stabilize.

The Low-Power Sleep mode is beneficial for applications that stay in Sleep mode for long periods of time. The Normal mode is beneficial for applications that need to wake from Sleep quickly and frequently.
10.2.3.2 Peripheral Usage in Sleep

Some peripherals that can operate in Sleep mode will not operate properly with the Low-Power Sleep mode selected. The Low-Power Sleep mode is intended for use with these peripherals:

- Brown-out Reset (BOR)
- Windowed Watchdog Timer (WWDT)
- External interrupt pin/Interrupt-On-Change pins
- Peripherals that run off external secondary clock source

It is the responsibility of the end user to determine what is acceptable for their application when setting the VREGPM settings in order to ensure operation in Sleep.

### Note:
The PIC18LF25/26K83 devices do not have a configurable Low-Power Sleep mode. PIC18LF25/26K83 devices are unregulated and are always in the lowest power state when in Sleep, with no wake-up time penalty. These devices have a lower maximum VDD and I/O voltage than the PIC18F25/26K83 devices. See Section 45.0 “Electrical Specifications” for more information.

10.2.4 IDLE MODE

When IDLEN is set (IDLEN = 1), the SLEEP instruction will put the device into Idle mode. In Idle mode, the CPU and memory operations are halted, but the peripheral clocks continue to run. This mode is similar to Doze mode, except that in Idle both the CPU and PFM are shut off.

### Note:
If CLKOUTEN is enabled (CLKOUTEN = 0), Configuration Word 1H, the output will continue operating while in Idle.

10.2.4.1 Idle and Interrupts

IDLE mode ends when an interrupt occurs (even if GIE = 0), but IDLEN is not changed. The device can re-enter IDLE by executing the SLEEP instruction.

If Recover-On-Interrupt is enabled (ROI = 1), the interrupt that brings the device out of Idle also restores full-speed CPU execution when doze is also enabled.

10.2.4.2 Idle and WWDT

When in Idle, the WWDT Reset is blocked and will instead wake the device. The WWDT wake-up is not an interrupt, therefore ROI does not apply.

### Note:
The WDT can bring the device out of Idle, in the same way it brings the device out of Sleep. The DOZEN bit is not affected.

10.3 Peripheral Operation in Power Saving Modes

All selected clock sources and the peripherals running off them are active in both IDLE and DOZE mode. Only in Sleep mode, both the Fosc and FOSC/4 clocks are unavailable. All the other clock sources are active, if enabled manually or through peripheral clock selection before the part enters Sleep.

### Note:
If CLKOUTEN is enabled (CLKOUTEN = 0), Configuration Word 1H, the output will continue operating while in Idle.
10.4 Register Definitions: Voltage Regulator Control

REGISTER 10-1: VREGCON: VOLTAGE REGULATOR CONTROL REGISTER(1)

<table>
<thead>
<tr>
<th>bit 7-2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unimplemented: Read as ‘0’</td>
<td>VREGPM: Voltage Regulator Power Mode Selection bit</td>
<td>Reserved: Read as ‘1’. Maintain this bit set.</td>
</tr>
<tr>
<td>1 = Low-Power Sleep mode enabled in Sleep(2)</td>
<td>Draws lowest current in Sleep, slower wake-up</td>
<td>0 = Normal Power mode enabled in Sleep(2)</td>
</tr>
<tr>
<td>Draws higher current in Sleep, faster wake-up</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets

1 = Bit is set  0 = Bit is cleared

Note 1: Not present in LF parts.

2: See Section 45.0 “Electrical Specifications”.

Note 1: Not present in LF parts.

2: See Section 45.0 “Electrical Specifications”.
### REGISTER 10-2: CPU DOZE: DOZE AND IDLE REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDLEN</td>
<td>DOZEN</td>
<td>ROI</td>
<td>DOE</td>
<td>—</td>
<td>DOZE&lt;2:0&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **HC** = Bit is cleared by hardware

**bit 7**
**IDLEN:** Idle Enable bit
- **1** = A SLEEP instruction inhibits the CPU clock, but not the peripheral clock(s)
- **0** = A SLEEP instruction places the device into full Sleep mode

**bit 6**
**DOZEN:** Doze Enable bit
- **1** = The CPU executes instruction cycles according to DOZE setting
- **0** = The CPU executes all instruction cycles (fastest, highest power operation)

**bit 5**
**ROI:** Recover-On-Interrupt bit
- **1** = Entering the Interrupt Service Routine (ISR) makes DOZEN = 0 bit, bringing the CPU to full-speed operation
- **0** = Interrupt entry does not change DOZEN

**bit 4**
**DOE:** Doze-On-Exit bit
- **1** = Executing RETFIE makes DOZEN = 1, bringing the CPU to reduced speed operation
- **0** = RETFIE does not change DOZEN

**bit 3**
**Unimplemented:** Read as ‘0’

**bit 2-0**
**DOZE<2:0>:** Ratio of CPU Instruction Cycles to Peripheral Instruction Cycles
- **111** = 1:256
- **110** = 1:128
- **101** = 1:64
- **100** = 1:32
- **011** = 1:16
- **010** = 1:8
- **001** = 1:4
- **000** = 1:2

**Note 1:** When ROI = 1 or DOE = 1, DOZEN is changed by hardware interrupt entry and/or exit.
**2:** Entering ICD overrides DOZEN, returning the CPU to full execution speed; this bit is not affected.

### TABLE 10-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>VREGCON(1)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>VREGPM Reserved 166</td>
</tr>
<tr>
<td>CPUDOZE</td>
<td>IDLEN</td>
<td>DOZEN</td>
<td>ROI</td>
<td>DOE</td>
<td>—</td>
<td>DOZE&lt;2:0&gt;</td>
<td></td>
<td></td>
<td>167</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented location, read as ‘0’. Shaded cells are not used in Power-Down mode.

**Note 1:** Not present in LF parts.
11.0 WINDOWED WATCHDOG TIMER (WWDT)

The Watchdog Timer (WDT) is a system timer that generates a Reset if the firmware does not issue a \texttt{CLRWDT} instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events. The Windowed Watchdog Timer (WWDT) differs in that \texttt{CLRWDT} instructions are only accepted when they are performed within a specific window during the time-out period.

The WWDT has the following features:

- Selectable clock source
- Multiple operating modes
  - WWDT is always On
  - WWDT is off when in Sleep
  - WWDT is controlled by software
  - WWDT is always Off
- Configurable time-out period is from 1 ms to 256s (nominal)
- Configurable window size from 12.5% to 100% of the time-out period
- Multiple Reset conditions
FIGURE 11-1: WINDOWED WATCHDOG TIMER BLOCK DIAGRAM

- **CLRWD**: Clear Window
- **RESET**: Reset
- **Reserved**: Various reserved settings
- **SOSC**: System Oscillator
- **MFINTOSC**: Main Frequency Internal Oscillator (31.25 kHz)
- **LFINTOSC**: Low Frequency Internal Oscillator
- **CS**: Chip Select

**Window Sizes**
- 111
- 110
- 101
- 100
- 011
- 100

**Prescale Counter**
- 18-bit

**Comparator**
- Window Closed

**WDT Time-out**

**WDTE<1:0>**
- 01
- 11
- 10

**SEN**: Sleep
11.1 Independent Clock Source

The WWDT can derive its time base from either the 31 kHz LFINTOSC or 31.25 kHz MFINTOSC internal oscillators, depending on the value of WDTE<1:0> Configuration bits.

If WDTE = 0b1x, then the clock source will be enabled depending on the WDTCCS<2:0> Configuration bits.

If WDTE = 0b01, the SEN bit should be set by software to enable WWDT, and the clock source is enabled by the CS bits in the WDTCON1 register.

Time intervals in this chapter are based on a minimum nominal interval of 1 ms. See Section 45.0 “Electrical Specifications” for LFINTOSC and MFINTOSC tolerances.

11.2 WWDT Operating Modes

The Windowed Watchdog Timer module has four operating modes controlled by the WDTE<1:0> bits in Configuration Words. See Table 11-1.

11.2.1 WWDT IS ALWAYS ON

When the WDTE bits of Configuration Words are set to ‘11’, the WWDT is always on.

WWDT protection is active during Sleep.

11.2.2 WWDT IS OFF IN SLEEP

When the WDTE bits of Configuration Words are set to ‘10’, the WWDT is on, except in Sleep.

WWDT protection is not active during Sleep.

11.2.3 WWDT CONTROLLED BY SOFTWARE

When the WDTE bits of Configuration Words are set to ‘01’, the WWDT is controlled by the SEN bit of the WDTCON0 register.

WWDT protection is unchanged by Sleep. See Table 11-1 for more details.

11.3 Time-out Period

If the WDTCPS<4:0> Configuration bits default to 0b11111, then the PS bits of the WDTCON0 register set the time-out period from 1 ms to 256 seconds (nominal). If any value other than the default value is assigned to WDTCPS<4:0> Configuration bits, then the timer period will be based on the WDTCPS<4:0> bits in the CONFIG3L register. After a Reset, the default time-out period is 2s.

11.4 Watchdog Window

The Windowed Watchdog Timer has an optional Windowed mode that is controlled by the WDTCWS<2:0> Configuration bits and WINDOW<2:0> bits of the WDTCON1 register. In the Windowed mode, the CLRWDT instruction must occur within the allowed window of the WDT period. Any CLRWDT instruction that occurs outside of this window will trigger a window violation and will cause a WWDT Reset, similar to a WWDT time out. See Figure 11-2 for an example.

The window size is controlled by the WINDOW<2:0> Configuration bits, or the WINDOW<2:0> bits of WDTCON1, if WDTCWS<2:0> = 111.

The five Most Significant bits of the WDTTMR register are used to determine whether the window is open, as defined by the WINDOW<2:0> bits of the WDTCON1 register.

In the event of a window violation, a Reset will be generated and the WDTWV bit of the PCON0 register will be cleared. This bit is set by a POR or can be set in firmware.

11.5 Clearing the WWDT

The WWDT is cleared when any of the following conditions occur:

- Any Reset
- Valid CLRWDT instruction is executed
- Device enters Sleep
- Exit Sleep by Interrupt
- WWDT is disabled
- Oscillator Start-up Timer (OST) is running
- Any write to the WDTCON0 or WDTCON1 registers

11.5.1 CLRWDT CONSIDERATIONS (WINDOWED MODE)

When in Windowed mode, the WWDT must be armed before a CLRWDT instruction will clear the timer. This is performed by reading the WDTCON0 register. Executing a CLRWDT instruction without performing such an arming action will trigger a window violation regardless of whether the window is open or not. See Table 11-2 for more information.
11.6 Operation During Sleep

When the device enters Sleep, the WWDT is cleared. If the WWDT is enabled during Sleep, the WWDT resumes counting. When the device exits Sleep, the WWDT is cleared again.

The WWDT remains clear until the Oscillator Start-up Timer (OST) completes, if enabled. See Section 7.2.1.3 “Oscillator Start-up Timer (OST)” for more information on the OST.

When a WWDT time-out occurs while the device is in Sleep, no Reset is generated. Instead, the device wakes up and resumes operation. The TO and PD bits in the STATUS register are changed to indicate the event. The RWDT bit in the PCON0 register can also be used. See Section 4.0 “Memory Organization” for more information.

### TABLE 11-2: WWDT CLEARING CONDITIONS

<table>
<thead>
<tr>
<th>Conditions</th>
<th>WWDT</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDTE&lt;1:0&gt; = 00</td>
<td>Cleared</td>
</tr>
<tr>
<td>WDTE&lt;1:0&gt; = 01 and SEN = 0</td>
<td></td>
</tr>
<tr>
<td>WDTE&lt;1:0&gt; = 10 and enter Sleep</td>
<td></td>
</tr>
<tr>
<td>CLRWDT Command</td>
<td></td>
</tr>
<tr>
<td>Oscillator Fail Detected</td>
<td></td>
</tr>
<tr>
<td>Exit Sleep + System Clock = SOSC, EXTRC, INTOSC, EXTCLK</td>
<td></td>
</tr>
<tr>
<td>Exit Sleep + System Clock = XT, HS, LP</td>
<td>Cleared until the end of OST</td>
</tr>
<tr>
<td>Change INTOSC divider (IRCF bits)</td>
<td>Unaffected</td>
</tr>
</tbody>
</table>

### FIGURE 11-2: WINDOW PERIOD AND DELAY

![Window Period and Delay Diagram](image-url)

CLRWDT Instruction (or other WDT reset)

Window Period

Window Closed

Window Open

Window Delay (window violation can occur)

Time-out Event
11.7 Register Definitions: Windowed Watchdog Timer Control

REGISTER 11-1: WDTCON0: WATCHDOG TIMER CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W</th>
<th>[q/q]</th>
<th>R/W</th>
<th>[q/q]</th>
<th>R/W</th>
<th>[q/q]</th>
<th>R/W</th>
<th>[q/q]</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7-6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 5-1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
u = Bit is unchanged
x = Bit is unknown
-q/q = Value at POR and BOR/Value at all other Resets
1 = Bit is set
0 = Bit is cleared
q = Value depends on condition

bit 7-6 Unimplemented: Read as ‘0’
bit 5-1 PS<4:0>: Watchdog Timer Prescale Select bits(1)
  Bit Value = Prescale Rate
  11111 = Reserved. Results in minimum interval (1:32)
  10011 = 1:262144 (2^18) (Interval 8s nominal)
  10010 = 1:131072 (2^17) (Interval 4s nominal)
  10001 = 1:65536 (Interval 2s nominal) (Reset value)
  10000 = 1:32768 (Interval 1s nominal)
  01111 = Reserved. Results in minimum interval (1:32)
  10110 = 1:6388608 (2^23) (Interval 256s nominal)
  10101 = 1:3194460 (2^22) (Interval 128s nominal)
  10100 = 1:2097152 (2^21) (Interval 64s nominal)
  01111 = 1:1048576 (2^20) (Interval 32s nominal)
  01110 = 1:524288 (2^19) (Interval 16s nominal)
  01101 = 1:262144 (2^18) (Interval 8s nominal)
  01100 = 1:131072 (2^17) (Interval 4s nominal)
  01011 = 1:65536 (Interval 2s nominal) (Reset value)
  01010 = 1:32768 (Interval 1s nominal)
  01001 = 1:16384 (Interval 512 ms nominal)
  01000 = 1:8192 (Interval 256 ms nominal)
  00111 = 1:4096 (Interval 128 ms nominal)
  00110 = 1:2048 (Interval 64 ms nominal)
  00101 = 1:1024 (Interval 32 ms nominal)
  00100 = 1:512 (Interval 16 ms nominal)
  00011 = 1:256 (Interval 8 ms nominal)
  00010 = 1:128 (Interval 4 ms nominal)
  00001 = 1:64 (Interval 2 ms nominal)
  00000 = 1:32 (Interval 1 ms nominal)

bit 0 SEN: Software Enable/Disable for Watchdog Timer bit
  If WDTE<1:0> = 1x:
  This bit is ignored.
  If WDTE<1:0> = 01:
  1 = WDT is turned on
  0 = WDT is turned off
  If WDTE<1:0> = 00:
  This bit is ignored.

Note 1: Times are approximate. WDT time is based on 31 kHz LFINTOSC.
2: When WDTCPS <4:0> in CONFIG3L ≠ 11111, the Reset value of PS<4:0> is 01011. Otherwise, the Reset value of PS<4:0> is equal to WDTCPS<4:0> in CONFIG3L.
3: When WDTCPS <4:0> in CONFIG3L ≠ 11111, these bits are read-only.
4: When the WWDT is configured to run using the SOSC as a clock source and the device is allowed to undergo a Reset, as triggered by a WDT time-out, the SOSC would also undergo a Reset. That means the SOSC will execute its start-up sequence which requires 1024 SOSC clock counts before it is made available for peripherals to use. So for example, if the WDT is set for a 1 ms time-out and the device is allowed to undergo a WDT Reset, then the actual WDT Reset period will be: WDT_PERIOD = (1/(SOSC_FREQUENCY) * 1024) + 1 ms.
REGISTER 11-2:  WDTCON1: WATCHDOG TIMER CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6-4</th>
<th>bit 3</th>
<th>bit 2-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>CS&lt;2:0&gt;</td>
<td>—</td>
<td>WINDOW&lt;2:0&gt;</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared  q = Value depends on condition

bit 7  Unimplemented: Read as '0'

bit 6-4  CS<2:0>: Watchdog Timer Clock Select bits

111 = Reserved
 \cdot
 \cdot
011 = Reserved
010 = SOSC
001 = MFINTOSC 31.25 kHz
000 = LFINTOSC 31 kHz

bit 3  Unimplemented: Read as '0'

bit 2-0  WINDOW<2:0>: Watchdog Timer Window Select bits

<table>
<thead>
<tr>
<th>WINDOW&lt;2:0&gt;</th>
<th>Window delay Percent of time</th>
<th>Window opening Percent of time</th>
</tr>
</thead>
<tbody>
<tr>
<td>111</td>
<td>N/A</td>
<td>100</td>
</tr>
<tr>
<td>110</td>
<td>12.5</td>
<td>87.5</td>
</tr>
<tr>
<td>101</td>
<td>25</td>
<td>75</td>
</tr>
<tr>
<td>100</td>
<td>37.5</td>
<td>62.5</td>
</tr>
<tr>
<td>011</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>010</td>
<td>62.5</td>
<td>37.5</td>
</tr>
<tr>
<td>001</td>
<td>75</td>
<td>25</td>
</tr>
<tr>
<td>000</td>
<td>87.5</td>
<td>12.5</td>
</tr>
</tbody>
</table>

Note 1:  If WDTCCS<2:0> in CONFIG3H = 111, the Reset value of CS<2:0> is 000.

2:  The Reset value of WINDOW<2:0> is determined by the value of WDTCWS<2:0> in the CONFIG3H register.

3:  If WDTCCS<2:0> in CONFIG3H ≠ 111, these bits are read-only.

4:  If WDTCWS<2:0> in CONFIG3H ≠ 111, these bits are read-only.
REGISTER 11-3:  WDTPSL: WWDT PRESCALE SELECT LOW BYTE REGISTER (READ-ONLY)

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th>PSCNT&lt;7:0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>R-0/0</td>
<td>R-0/0</td>
</tr>
<tr>
<td>R-0/0</td>
<td>R-0/0</td>
</tr>
<tr>
<td>R-0/0</td>
<td>R-0/0</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **’1’** = Bit is set
- **’0’** = Bit is cleared

Note 1: The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should not be read during normal operation.

REGISTER 11-4:  WDTPSH: WWDT PRESCALE SELECT HIGH BYTE REGISTER (READ-ONLY)

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th>PSCNT&lt;15:8&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>R-0/0</td>
<td>R-0/0</td>
</tr>
<tr>
<td>R-0/0</td>
<td>R-0/0</td>
</tr>
<tr>
<td>R-0/0</td>
<td>R-0/0</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **’1’** = Bit is set
- **’0’** = Bit is cleared

Note 1: The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should not be read during normal operation.
REGISTER 11-5:  WDTTMR: WDT TIMER REGISTER (READ-ONLY)

<table>
<thead>
<tr>
<th>bit 7-3</th>
<th>WDTTMR&lt;4:0&gt;: Watchdog Window Value bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>WINDOW</td>
<td>WDT Window State</td>
</tr>
<tr>
<td></td>
<td>Closed</td>
</tr>
<tr>
<td>111</td>
<td>N/A</td>
</tr>
<tr>
<td>110</td>
<td>00000-00011</td>
</tr>
<tr>
<td>101</td>
<td>00000-00111</td>
</tr>
<tr>
<td>100</td>
<td>00000-01011</td>
</tr>
<tr>
<td>011</td>
<td>00000-01111</td>
</tr>
<tr>
<td>010</td>
<td>00000-10011</td>
</tr>
<tr>
<td>001</td>
<td>00000-10111</td>
</tr>
<tr>
<td>000</td>
<td>00000-11011</td>
</tr>
</tbody>
</table>

bit 2     STATE: WDT Armed Status bit
1 = WDT is armed
0 = WDT is not armed

bit 1-0   PSCNT<17:16>: Prescale Select Upper Byte bits(1)

**Note 1:** The 18-bit WDT prescale value, PSCNT<17:0> includes the WDTPSL, WDTPSH and the lower bits of the WDTTMR registers. PSCNT<17:0> is intended for debug operations and should not be read during normal operation.
### TABLE 11-3: SUMMARY OF REGISTERS ASSOCIATED WITH WINDOWED WATCHDOG TIMER

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDTCN0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>PS&lt;4:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SEN</td>
<td>172</td>
</tr>
<tr>
<td>WDTCN1</td>
<td>—</td>
<td>—</td>
<td>CS&lt;2:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WINDOW&lt;2:0&gt;</td>
<td>173</td>
<td></td>
</tr>
<tr>
<td>WDTPSL</td>
<td>—</td>
<td>—</td>
<td>PSCNT&lt;7:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>174</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WDTPSH</td>
<td>—</td>
<td>—</td>
<td>PSCNT&lt;15:8&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>174</td>
<td></td>
<td></td>
</tr>
<tr>
<td>WDTMR</td>
<td>—</td>
<td>—</td>
<td>WDTMR&lt;4:0&gt;</td>
<td>STATE</td>
<td>—</td>
<td>PSCNT&lt;17:16&gt;</td>
<td>175</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- $x$ = unknown,
- $u$ = unchanged,
- $-$ = unimplemented locations read as ‘0’. Shaded cells are not used by Windowed Watchdog Timer.
12.0 8x8 HARDWARE MULTIPLIER

12.1 Introduction

All PIC18 devices include an 8x8 hardware multiplier as part of the ALU. The multiplier performs an unsigned operation and yields a 16-bit result that is stored in the product register pair, PRODH:PRODL. The multiplier’s operation does not affect any flags in the STATUS register.

Making multiplication a hardware operation allows it to be completed in a single instruction cycle. This has the advantages of higher computational throughput and reduced code size for multiplication algorithms and allows the PIC18 devices to be used in many applications previously reserved for digital signal processors. A comparison of various hardware and software multiply operations, along with the savings in memory and execution time, is shown in Table 12-1.

12.2 Operation

Example 12-1 shows the instruction sequence for an 8x8 unsigned multiplication. Only one instruction is required when one of the arguments is already loaded in the WREG register.

Example 12-2 shows the sequence to do an 8x8 signed multiplication. To account for the sign bits of the arguments, each argument’s Most Significant bit (MSb) is tested and the appropriate subtractions are done.

TABLE 12-1: PERFORMANCE COMPARISON FOR VARIOUS MULTIPLY OPERATIONS

<table>
<thead>
<tr>
<th>Routine</th>
<th>Multiply Method</th>
<th>Program Memory (Words)</th>
<th>Cycles (Max)</th>
<th>@ 64 MHz</th>
<th>@ 40 MHz</th>
<th>@ 10 MHz</th>
<th>@ 4 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>8x8 unsigned</td>
<td>Without hardware multiply</td>
<td>13</td>
<td>69</td>
<td>4.3 µs</td>
<td>6.9 µs</td>
<td>27.6 µs</td>
<td>69 µs</td>
</tr>
<tr>
<td></td>
<td>Hardware multiply</td>
<td>1</td>
<td>1</td>
<td>62.5 ns</td>
<td>100 ns</td>
<td>400 ns</td>
<td>1 µs</td>
</tr>
<tr>
<td>8x8 signed</td>
<td>Without hardware multiply</td>
<td>33</td>
<td>91</td>
<td>5.7 µs</td>
<td>9.1 µs</td>
<td>36.4 µs</td>
<td>91 µs</td>
</tr>
<tr>
<td></td>
<td>Hardware multiply</td>
<td>6</td>
<td>6</td>
<td>375 ns</td>
<td>600 ns</td>
<td>2.4 µs</td>
<td>6 µs</td>
</tr>
<tr>
<td>16x16 unsigned</td>
<td>Without hardware multiply</td>
<td>21</td>
<td>242</td>
<td>15.1 µs</td>
<td>24.2 µs</td>
<td>96.8 µs</td>
<td>242 µs</td>
</tr>
<tr>
<td></td>
<td>Hardware multiply</td>
<td>28</td>
<td>28</td>
<td>1.8 µs</td>
<td>2.8 µs</td>
<td>11.2 µs</td>
<td>28 µs</td>
</tr>
<tr>
<td>16x16 signed</td>
<td>Without hardware multiply</td>
<td>52</td>
<td>254</td>
<td>15.9 µs</td>
<td>25.4 µs</td>
<td>102.6 µs</td>
<td>254 µs</td>
</tr>
<tr>
<td></td>
<td>Hardware multiply</td>
<td>35</td>
<td>40</td>
<td>2.5 µs</td>
<td>4.0 µs</td>
<td>16.0 µs</td>
<td>40 µs</td>
</tr>
</tbody>
</table>
Example 12-3 shows the sequence to do a 16 x 16 unsigned multiplication. **Equation 12-1** shows the algorithm that is used. The 32-bit result is stored in four registers (RES<3:0>).

**EQUATION 12-1:  16 x 16 UNSIGNED MULTIPLICATION ALGORITHM**

\[
\text{RES3:RES0} = \text{ARG1H:ARG1L} \cdot \text{ARG2H:ARG2L} \\
= (\text{ARG1H} \cdot \text{ARG2H}) \cdot 2^{16} + \\
(\text{ARG1H} \cdot \text{ARG2L}) \cdot 2^8 + \\
(\text{ARG1L} \cdot \text{ARG2H}) \cdot 2^8 + \\
(\text{ARG1L} \cdot \text{ARG2L}) \\
\]

**EXAMPLE 12-3:  16 x 16 UNSIGNED MULTIPLY ROUTINE**

```
MOVF ARG1L, W
MULWF ARG2L ; ARG1L * ARG2L -> PRODH:PRODL
MOVF ARG1H, W
MULWF ARG2H ; ARG1H * ARG2H -> PRODH:PRODL
MOVF ARG1L, W
MULWF ARG2H ; ARG1L * ARG2H -> PRODH:PRODL
MOVF ARG1L, W
MULWF ARG2L ; ARG1L * ARG2L -> PRODH:PRODL
;
MOVF PRODH, RES1 ;
MOVF PRODL, RES0 ;
;
MOVF ARG1H, W
MULWF ARG2L ; ARG1H * ARG2L -> PRODH:PRODL
MOVF PRODH, RES3 ;
MOVF PRODL, RES2 ;
;
MOVF ARG1H, W
MULWF ARG2H ; ARG1H * ARG2H -> PRODH:PRODL
MOVF PRODH, RES1 ;
MOVF PRODL, RES0 ;
;
MOVF ARG1L, W
MULWF ARG2L ; ARG1L * ARG2L -> PRODH:PRODL
;
MOVF PRODL, W ;
ADDWF RES1, F ; Add cross
MOVFF PRODH, W ; products
ADDWF RES2, F ;
CLRF WREG ;
ADDWF RES3, F ;
;
MOVF ARG1H, W
MULWF ARG2L ; ARG1H * ARG2L -> PRODH:PRODL
MOVF PRODH, W ;
ADDWF RES1, F ; Add cross
MOVFF PRODL, W ; products
ADDWF RES2, F ;
CLRF WREG ;
ADDWF RES3, F ;
```

Example 12-4 shows the sequence to do a 16 x 16 signed multiply. **Equation 12-2** shows the algorithm used. The 32-bit result is stored in four registers (RES<3:0>). To account for the sign bits of the arguments, the MSB for each argument pair is tested and the appropriate subtractions are done.

**EQUATION 12-2:  16 x 16 SIGNED MULTIPLICATION ALGORITHM**

\[
\text{RES3:RES0} = \text{ARG1H:ARG1L} \cdot \text{ARG2H:ARG2L} \\
= (\text{ARG1H} \cdot \text{ARG2H}) \cdot 2^{16} + \\
(\text{ARG1H} \cdot \text{ARG2L}) \cdot 2^8 + \\
(\text{ARG1L} \cdot \text{ARG2H}) \cdot 2^8 + \\
(\text{ARG1L} \cdot \text{ARG2L}) + \\
(-1 \cdot \text{ARG2H}<7> \cdot \text{ARG1H:ARG1L}) \cdot 2^{16} + \\
(-1 \cdot \text{ARG1H}<7> \cdot \text{ARG2H:ARG2L}) \cdot 2^8
\]

**EXAMPLE 12-4:  16 x 16 SIGNED MULTIPLY ROUTINE**

```
MOVF ARG1L, W
MULWF ARG2L ; ARG1L * ARG2L -> PRODH:PRODL
MOVF PRODH, RES1 ;
MOVF PRODL, RES0 ;
;
MOVF ARG1H, W
MULWF ARG2H ; ARG1H * ARG2H -> PRODH:PRODL
MOVF PRODH, RES3 ;
MOVF PRODL, RES2 ;
;
MOVF ARG1L, W
MULWF ARG2H ; ARG1L * ARG2H -> PRODH:PRODL
MOVF PRODH, RES1 ;
MOVF PRODL, RES0 ;
;
MOVF ARG1H, W
MULWF ARG2L ; ARG1H * ARG2L -> PRODH:PRODL
MOVFF PRODH, RES3 ;
MOVFF PRODL, RES2 ;
;
MOVF ARG1L, W
MULWF ARG2L ; ARG1L * ARG2L -> PRODH:PRODL
;
MOVF PRODL, W ;
ADDWF RES1, F ; Add cross
MOVFF PRODH, W ; products
ADDWF RES2, F ;
CLRF WREG ;
ADDWF RES3, F ;
;
MOVF ARG1H, W
MULWF ARG2L ; ARG1H * ARG2L -> PRODH:PRODL
MOVF PRODH, W ;
ADDWF RES1, F ; Add cross
MOVFF PRODL, W ; products
ADDWF RES2, F ;
CLRF WREG ;
ADDWF RES3, F ;
;
BTFSS ARG2H, 7 ; ARG2H:ARG2L neg?
BRA SIGN_ARG1 ; no, check ARG1
;
MOVF ARG1L, W
SUBWF RES2 ;
MOVF ARG1H, W
SUBWFB RES3
;
SIGN_ARG1
BTFSS ARG1H, 7 ; ARG1H:ARG1L neg?
BRA CONT_CODE ; no, done
;
MOVF ARG2L, W
SUBWF RES2 ;
MOVF ARG1H, W
SUBWFB RES3
;
CONT_CODE
```

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Preliminary

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13.0 NONVOLATILE MEMORY (NVM) CONTROL

Nonvolatile Memory (NVM) is separated into two types: Program Flash Memory (PFM) and Data EEPROM Memory.

PFM, Data EEPROM, User IDs and Configuration bits can all be accessed using the REG<1:0> bits of the NVMCON1 register.

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the operating voltage range of the device.

NVM can be protected in two ways, by either code protection or write protection. Code protection (CP and CPD bits in Configuration Word 5L) disables access, reading and writing to both PFM and Data EEPROM Memory via external device programmers. Code protection does not affect the self-write and erase functionality. Code protection can only be reset by a device programmer performing a Bulk Erase to the device, clearing all nonvolatile memory, Configuration bits and User IDs.

Write protection prohibits self-write and erase to a portion or all of the PFM, as defined by the WRT bits of Configuration Word 4H. Write protection does not affect a device programmer’s ability to read, write or erase the device.

<table>
<thead>
<tr>
<th>TABLE 13-1: NVM ORGANIZATION AND ACCESS INFORMATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory</td>
</tr>
<tr>
<td>-------------------------------------------------</td>
</tr>
<tr>
<td>Program Flash Memory (PFM)</td>
</tr>
<tr>
<td>User IDs(2)</td>
</tr>
<tr>
<td>Reserved</td>
</tr>
<tr>
<td>Configuration</td>
</tr>
<tr>
<td>User Data Memory (Data EEPROM)</td>
</tr>
<tr>
<td>Device Information Area (DIA)</td>
</tr>
<tr>
<td>Device Configuration Information (DCI)</td>
</tr>
<tr>
<td>Revision ID/Device ID</td>
</tr>
</tbody>
</table>

Note 1: Subject to Memory Write Protection settings.
2: User IDs are eight words ONLY. There is no code protection, table read protection or write protection implemented for this region.
3: Reads as '0', writes clear the WR bit and WRERR bit is set.
13.1 Program Flash Memory

The Program Flash Memory is readable, writable and erasable during normal operation over the entire VDD range.

A read from program memory is executed one byte at a time. A write to program memory or program memory erase is executed on blocks of \( n \) bytes at a time. Refer to Table 5-4 for write and erase block sizes. A Bulk Erase operation cannot be issued from user code.

Writing or erasing program memory will cease instruction fetches until the operation is complete. The program memory cannot be accessed during the write or erase, therefore, code cannot execute. An internal programming timer terminates program memory writes and erases.

A value written to program memory does not need to be a valid instruction. Executing a program memory location that forms an invalid instruction results in a \texttt{NOP}.

It is important to understand the PFM memory structure for erase and programming operations. Program memory word size is 16 bits wide. PFM is arranged in rows. A row is the minimum size that can be erased by user software. Refer to Table 5-4 for the row sizes for these devices.

After a row has been erased, all or a portion of this row can be programmed. Data to be written into the program memory row is written to 8-bit wide data write latches by means of 6 address lines. These latches are not directly accessible, but may be loaded via sequential writes to the TABLAT register.

\textbf{Note:} To modify only a portion of a previously programmed row, then the contents of the entire row must be read and saved in RAM prior to the erase. Then, the new data and retained data can be written into the write latches to reprogram the row of PFM. However, any unprogrammed locations can be written without first erasing the row. In this case, it is not necessary to save and rewrite the other previously programmed locations.

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|c|}
\hline
Device & Row Erase Size & Write Latches & Program Flash Memory & Data Memory (Bytes) \\
\hline
PIC18(L)F25K83 & 64 (Words) & 128 (Bytes) & 16384 (Words) & 1024 \\
PIC18(L)F26K83 & 64 (Words) & 128 (Bytes) & 32768 (Words) & 1024 \\
\hline
\end{tabular}
\end{table}
13.1.1 TABLE READS AND TABLE WRITES

In order to read and write program memory, there are two operations that allow the processor to move bytes between the program memory space and the data RAM:

- Table Read (TBLRD)
- Table Write (TBLWT)

The program memory space is 16 bits wide, while the data RAM space is eight bits wide. Table reads and table writes move data between these two memory spaces through an 8-bit register (TABLAT).

The table read operation retrieves one byte of data directly from program memory and places it into the TABLAT register. Figure 13-1 shows the operation of a table read.

The table write operation stores one byte of data from the TABLAT register into a write block holding register. The procedure to write the contents of the holding registers into program memory is detailed in Section 13.1.6 "Writing to Program Flash Memory". Figure 13-2 shows the operation of a table write with program memory and data RAM.

Table operations work with byte entities. Tables containing data, rather than program instructions, are not required to be word aligned. Therefore, a table can start and end at any byte address. If a table write is being used to write executable code into program memory, program instructions will need to be word aligned.

---

**FIGURE 13-1: TABLE READ OPERATION**

Instruction: TBLRD

Table Pointer\(^{(1)}\)

TBLPTRU | TBLPTRL | TBLPTRL

Table Latch (8-bit)

TABLAT

Program Memory (TBLPTR)<br>Program Memory

Note 1: Table Pointer register points to a byte in program memory.

**FIGURE 13-2: TABLE WRITE OPERATION**

Instruction: TBLWT

Table Pointer\(^{(1)}\)

TBLPTRU | TBLPTRL | TBLPTRL

Program Memory (TBLPTR<MSBs>)

Holding Registers

Note 1: During table writes the Table Pointer does not point directly to program memory. The LSBs of TBLPTRL actually point to an address within the write block holding registers. The MSBs of the Table Pointer determine where the write block will eventually be written. The process for writing the holding registers to the program memory array is discussed in Section 13.1.6 “Writing to Program Flash Memory”.

---
13.1.2 CONTROL REGISTERS

Several control registers are used in conjunction with the TBLRD and TBLWT instructions. These include the following registers:

- NVMCON1 register
- NVMCON2 register
- TABLAT register
- TBLPTR registers

13.1.2.1 NVMCON1 and NVMCON2 Registers

The NVMCON1 register (Register 13-1) is the control register for memory accesses. The NVMCON2 register is not a physical register; it is used exclusively in the memory write and erase sequences. Reading NVMCON2 will read all '0's.

The REG<1:0> control bits determine if the access will be to Data EEPROM Memory locations, PFM locations or User IDs, Configuration bits, Rev ID and Device ID. When REG<1:0> = 00, any subsequent operations will operate on the Data EEPROM Memory. When REG<1:0> = 10, any subsequent operations will operate on the program memory. When REG<1:0> = x1, any subsequent operations will operate on the Configuration bits, User IDs, Rev ID and Device ID.

The FREE bit allows the program memory erase operation. When the FREE bit is set, an erase operation is initiated on the next WR command. When FREE is clear, only writes are enabled. This bit is applicable only to the PFM and not to data EEPROM.

When set, the WREN bit will allow a program/erase operation. The WREN bit is cleared on power-up.

The WRERR bit is set by hardware when the WR bit is set and is cleared when the internal programming timer expires and the write operation is successfully complete.

The WR control bit initiates erase/write cycle operation when the REG<1:0> bits point to the Data EEPROM Memory location, and it initiates a write operation when the REG<1:0> bits point to the PFM location. The WR bit cannot be cleared by firmware; it can only be set by firmware. Then the WR bit is cleared by hardware at the completion of the write operation.

The NVMIF Interrupt Flag bit is set when the write is complete. The NVMIF flag stays set until cleared by firmware.

13.1.2.2 TABLAT – Table Latch Register

The Table Latch (TABLAT) is an 8-bit register mapped into the SFR space. The Table Latch register is used to hold 8-bit data during data transfers between program memory and data RAM.

13.1.2.3 TBLPTR – Table Pointer Register

The Table Pointer (TBLPTR) register addresses a byte within the program memory. The TBLPTR is comprised of three SFR registers: Table Pointer Upper Byte, Table Pointer High Byte and Table Pointer Low Byte (TBLPTRU:TBLPTRH:TBLPTRL). These three registers join to form a 22-bit wide pointer. The low-order 21 bits allow the device to address up to 2 Mbytes of program memory space. The 22nd bit allows access to the Device ID, the User ID and the Configuration bits.

The Table Pointer register, TBLPTR, is used by the TBLRD and TBLWT instructions. These instructions can update the TBLPTR in one of four ways based on the table operation. These operations on the TBLPTR affect only the low-order 21 bits.

13.1.2.4 Table Pointer Boundaries

TBLPTR is used in reads, writes and erases of the Program Flash Memory.

When a TBLRD is executed, all 22 bits of the TBLPTR determine which byte is read from program memory directly into the TABLAT register.

When a TBLWT is executed the byte in the TABLAT register is written, not to memory but, to a holding register in preparation for a program memory write. The holding registers constitute a write block which varies depending on the device (see Table 13-3). The 3, 4, or 5 LSbs of the TBLPTRL register determine which specific address within the holding register block is written to. The MSBs of the Table Pointer have no effect during TBLWT operations.

When a program memory write is executed the entire holding register block is written to the memory at the address determined by the MSbs of the TBLPTR. The 3, 4, or 5 LSbs are ignored during memory writes. For more detail, see Section 13.1.6 “Writing to Program Flash Memory”.

Figure 13-3 describes the relevant boundaries of TBLPTR based on Program Flash Memory operations.
TABLE 13-3: TABLE POINTER OPERATIONS WITH TBLRD AND TBLWT INSTRUCTIONS

<table>
<thead>
<tr>
<th>Example</th>
<th>Operation on Table Pointer</th>
</tr>
</thead>
<tbody>
<tr>
<td>TBLRD*</td>
<td>TBLPTR is not modified</td>
</tr>
<tr>
<td>TBLRD*+</td>
<td>TBLPTR is incremented after the read/write</td>
</tr>
<tr>
<td>TBLRD*-</td>
<td>TBLPTR is decremented after the read/write</td>
</tr>
<tr>
<td>TBLRD++</td>
<td>TBLPTR is incremented before the read/write</td>
</tr>
<tr>
<td>TBLWT*</td>
<td>TBLPTR is not modified</td>
</tr>
<tr>
<td>TBLWT*+</td>
<td>TBLPTR is incremented after the read/write</td>
</tr>
<tr>
<td>TBLWT*-</td>
<td>TBLPTR is decremented after the read/write</td>
</tr>
<tr>
<td>TBLWT++</td>
<td>TBLPTR is incremented before the read/write</td>
</tr>
</tbody>
</table>

FIGURE 13-3: TABLE POINTER BOUNDARIES BASED ON OPERATION

Note 1: Refer to Table 5-4 for the row size values.
13.1.3 READING THE PROGRAM FLASH MEMORY

The TBLRD instruction retrieves data from program memory and places it into data RAM. Table reads from program memory are performed one byte at a time. TBLPTR points to a byte address in program space. Executing TBLRD places the byte pointed to into TABLAT. In addition, TBLPTR can be modified automatically for the next table read operation.

The CPU operation is suspended during the read, and it resumes immediately after. From the user point of view, TABLAT is valid in the next instruction cycle.

The internal program memory is typically organized by words. The Least Significant bit of the address selects between the high and low bytes of the word. Figure 13-4 shows the interface between the internal program memory and the TABLAT.

**EXAMPLE 13-1: READING A PROGRAM FLASH MEMORY WORD**

```assembly
BCF NVMCON1, REG0 ; point to Program Flash Memory
BSF NVMCON1, REG1 ; access Program Flash Memory
MOVLW CODE_ADDR_UPPER ; Load TBLPTR with the base
MOVWF TBLPTRU ; address of the word
MOVLW CODE_ADDR_HIGH
MOVWF TBLPTRH
MOVLW CODE_ADDR_LOW
MOVWF TBLPTRL

READ_WORD
TBLRD*+ ; read into TABLAT and increment
MOVF TABLAT, W ; get data
MOVF WORD_EVEN
TBLRD*+ ; read into TABLAT and increment
MOVFW TABLAT, W ; get data
MOVF WORD_ODD
```

**FIGURE 13-4: READS FROM PROGRAM FLASH MEMORY**

![Program Memory Interface](image)

Instruction Register (IR) — Fetch

Program Memory

(TabLAT, Even Byte Address) — (Odd Byte Address)

TBLPTR = xxxx1

TBLPTR = xxxx0

TBLRD Read Register
FIGURE 13-5: PROGRAM FLASH MEMORY READ FLOWCHART

1. Start Read Operation
2. Select PFM (NVMREG<1:0> = 0x10)
3. Select Word Address (TBLPTR registers)
4. Initiate Read operation (TBLRD)
5. Data read now in TABLAT
6. End Read Operation
13.1.4 NVM UNLOCK SEQUENCE

The unlock sequence is a mechanism that protects the NVM from unintended self-write programming or erasing. The sequence must be executed and completed without interruption to successfully complete any of the following operations:

- PFM Row Erase
- Write of PFM write latches to PFM memory
- Write of PFM write latches to User IDs
- Write to Data EEPROM Memory
- Write to Configuration Words

The unlock sequence consists of the following steps and must be completed in order:

- Write 55h to NVMCON2
- Write AAh to NVMCON2
- Set the WR bit of NVMCON1

Once the WR bit is set, the processor will stall internal operations until the operation is complete and then resume with the next instruction.

Since the unlock sequence must not be interrupted, global interrupts should be disabled prior to the unlock sequence and re-enabled after the unlock sequence is completed.

EXAMPLE 13-2: NVM UNLOCK SEQUENCE

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCF</td>
<td>INTCON0,GIE ; Recommended so sequence is not interrupted</td>
</tr>
<tr>
<td>BANKSEL</td>
<td>NVMCON1</td>
</tr>
<tr>
<td>BSF</td>
<td>NVMCON1,WREN ; Enable write/erase</td>
</tr>
<tr>
<td>MOVLW 55h</td>
<td>; Load 55h</td>
</tr>
<tr>
<td>MOVWF</td>
<td>NVMCON2     ; Step 1: Load 55h into NVMCON2</td>
</tr>
<tr>
<td>MOVWF AAh</td>
<td>; Step 2: Load W with AAh</td>
</tr>
<tr>
<td>MOVWF NVMCON2</td>
<td>; Step 3: Load AAh into NVMCON2</td>
</tr>
<tr>
<td>BSF INTCON1,WR</td>
<td>; Step 4: Set WR bit to begin write/erase</td>
</tr>
<tr>
<td>BSF INTCON0,GIE</td>
<td>; Re-enable interrupts</td>
</tr>
</tbody>
</table>

Note 1: Sequence begins when NVMCON2 is written; steps 1-4 must occur in the cycle-accurate order shown. If the timing of the steps 1 to 4 is corrupted by an interrupt or a debugger Halt, the action will not take place.

2: Opcodes shown are illustrative; any instruction that has the indicated effect may be used.
13.1.5 ERASING PROGRAM FLASH MEMORY

The minimum erase block is 64 words (refer to Table 5-4). Only through the use of an external programmer, or through ICSP™ control, can larger blocks of program memory be bulk erased. Word erase in the program memory array is not supported.

For example, when initiating an erase sequence from a microcontroller with erase row size of 64 words, a block of 64 words (128 bytes) of program memory is erased. The Most Significant 16 bits of the TBLPTR<21:6> point to the block being erased. The TBLPTR<5:0> bits are ignored.

The NVMCON1 register commands the erase operation. The REG<1:0> bits must be set to point to the Program Flash Memory. The WREN bit must be set to enable write operations. The FREE bit is set to select an erase operation.

The NVM unlock sequence described in Section 13.1.4 “NVM Unlock Sequence” should be used to guard against accidental writes. This is sometimes referred to as a long write.

A long write is necessary for erasing program memory. Instruction execution is halted during the long write cycle. The long write is terminated by the internal programming timer.

13.1.5.1 Program Flash Memory Erase Sequence

The sequence of events for erasing a block of internal program memory is:

1. REG bits of the NVMCON1 register point to PFM
2. Set the FREE and WREN bits of the NVMCON1 register
3. Perform the unlock sequence as described in Section 13.1.4 “NVM Unlock Sequence”

If the PFM address is write-protected, the WR bit will be cleared and the erase operation will not take place, WRERR is signaled in this scenario.

The operation erases the memory row indicated by masking the LSBs of the current TBLPTR.

While erasing PFM, CPU operation is suspended and it resumes when the operation is complete. Upon completion the WR bit is cleared in hardware, the NVMIF is set and an interrupt will occur if the NVMIE bit is also set.

Write latch data is not affected by erase operations and WREN will remain unchanged.

Note 1: If a write or erase operation is terminated by an unexpected event, WRERR bit will be set which the user can check to decide whether a rewrite of the location(s) is needed.

2: WRERR is set if WR is written to ‘1’ while TBLPTR points to a write-protected address.

3: WRERR is set if WR is written to ‘1’ while TBLPTR points to an invalid address location (Table 13-1).
EXAMPLE 13-3: ERASING A PROGRAM FLASH MEMORY BLOCK

; This sample row erase routine assumes the following:
; 1. A valid address within the erase row is loaded in variables TBLPTR register

CLRF NVMCON1 ; Setup PFM Access
MOVLW CODE_ADDR_UPPER ; load TBLPTR with the base
MOVWF TBLPTRU ; address of the memory block
MOVLW CODE_ADDR_HIGH
MOVWF TBLPTRH
MOVLW CODE_ADDR_LOW
MOVWF TBLPTRL

ERASE_BLOCK

BCF NVMCON1, REG0 ; point to Program Flash Memory
BSF NVMCON1, REG1 ; access Program Flash Memory
BSF NVMCON1, WREN ; enable write to memory
BSF NVMCON1, FREE ; enable block Erase operation
BCF INTCON0, GIE ; disable interrupts

MOVLW 55h
MOVWF NVMCON2 ; write 55h

MOVLW AAh
MOVWF NVMCON2 ; write AAh

BSF NVMCON1, WR ; start erase (CPU stalls)
BSF INTCON0, GIE ; re-enable interrupts
13.1.6 WRITING TO PROGRAM FLASH MEMORY

The programming write block size is described in Table 5-4. Word or byte programming is not supported. Table writes are used internally to load the holding registers needed to program the memory. There are only as many holding registers as there are bytes in a write block. Refer to Table 5-4 for write latch size.

Since the table latch (TABLAT) is only a single byte, the TBLWT instruction needs to be executed multiple times for each programming operation. The write protection state is ignored for this operation. All of the table write operations will essentially be short writes because only the holding registers are written. NVMIF is not affected while writing to the holding registers.

After all the holding registers have been written, the programming operation of that block of memory is started by configuring the NVMCON1 register for a program memory write and performing the long write sequence.

If the PFM address in the TBLPTR is write-protected or if TBLPTR points to an invalid location, the WR bit is cleared without any effect and the WREER is signaled. The long write is necessary for programming the program memory. CPU operation is suspended during a long write cycle and resumes when the operation is complete. The long write operation completes in one instruction cycle. When complete, WR is cleared in hardware and NVMIF is set and an interrupt will occur if NVMIE is also set. The latched data is reset to all ‘1’s’. WREN is not changed.

The internal programming timer controls the write time. The write/erase voltages are generated by an on-chip charge pump, rated to operate over the voltage range of the device.

Note: The default value of the holding registers on device Resets and after write operations is FFh. A write of FFh to a holding register does not modify that byte. This means that individual bytes of program memory may be modified, provided that the change does not attempt to change any bit from a ‘0’ to a ‘1’. When modifying individual bytes, it is not necessary to load all holding registers before executing a long write operation.
13.1.6.1 Program Flash Memory Write Sequence

The sequence of events for programming an internal program memory location should be:

1. Read appropriate number of bytes into RAM. Refer to Table 13-2 for Write latch size.
2. Update data values in RAM as necessary.
3. Load Table Pointer register with address being erased.
4. Execute the block erase procedure.
5. Load Table Pointer register with address of first byte being written.
6. Write the n-byte block into the holding registers with auto-increment. Refer to Table 13-2 for Write latch size.
7. Set REG<1:0> bits to point to program memory.
10. Execute the unlock sequence (see Section 13.1.4 “NVM Unlock Sequence”).
11. WR bit is set in NVMCON1 register.
12. The CPU will stall for the duration of the write (about 2 ms using internal timer).
13. Re-enable interrupts.
14. Verify the memory (table read).

This procedure will require about 6 ms to update each write block of memory. An example of the required code is given in Example 13-4.

**Note:** Before setting the WR bit, the Table Pointer address needs to be within the intended address range of the bytes in the holding registers.
EXAMPLE 13-4:  WRITING TO PROGRAM FLASH MEMORY

```asm
MOVLW D'64' ; number of bytes in erase block
MOVF COUNTER
MOVLW BUFFER_ADDR_HIGH ; point to buffer
MOVF FSR0H
MOVLW BUFFER_ADDR_LOW
MOVF FSR0L
MOVLW CODE_ADDR_UPPER ; Load TBLPTR with the base
MOVF TBLPTRU
MOVLW CODE_ADDR_HIGH
MOVF TBLPTRH
MOVLW CODE_ADDR_LOW
MOVF TBLPTRL

READ_BLOCK
  TBLRD*+ ; read into TABLAT, and inc
  MOVF TABLAT, W ; get data
  MOVWF POSTINC0 ; store data
  DECFSZ COUNTER ; done?
  BRA READ_BLOCK ; repeat

MODIFY_WORD
  MOVLW BUFFER_ADDR_HIGH ; point to buffer
  MOVF FSR0H
  MOVLW BUFFER_ADDR_LOW
  MOVF FSR0L
  MOVLW NEW_DATA_LOW ; update buffer word
  MOVWF POSTINC0
  MOVLW NEW_DATA_HIGH
  MOVWF INDF0

ERASE_BLOCK
  MOVLW CODE_ADDR_UPPER ; load TBLPTR with the base
  MOVF TBLPTRU
  MOVLW CODE_ADDR_HIGH
  MOVF TBLPTRH
  MOVLW CODE_ADDR_LOW
  MOVF TBLPTRL
  BCF NVMCON1, REG0 ; point to Program Flash Memory
  BSF NVMCON1, REG1 ; point to Program Flash Memory
  BSF NVMCON1, WREN ; enable write to memory
  BSF NVMCON1, FREE ; enable Erase operation
  BCF INTCON0, GIE ; disable interrupts
  MOVWF 55h
  MOVF NVMCON2 ; write 55h
  MOVWF AAh
  MOVF NVMCON2 ; write 0AAh
  BSF NVMCON1, WR ; start erase (CPU stall)
  BSF INTCON0, GIE ; re-enable interrupts
  TBLRD*+ ; dummy read decrement
  MOVLW BUFFER_ADDR_HIGH ; point to buffer
  MOVF FSR0H
  MOVLW BUFFER_ADDR_LOW
  MOVF FSR0L

WRITE_BUFFER_BACK
  MOVLW BlockSize ; number of bytes in holding register
  MOVF COUNTER
  MOVLW D'64'/BlockSize ; number of write blocks in 64 bytes
  MOVF COUNTER2
```

EXAMPLE 13-4: WRITING TO PROGRAM FLASH MEMORY (CONTINUED)

WRITE_BYTE_TO_HREGS

MOVF POSTINC0, W ; get low byte of buffer data
MOVF TBLAT ; present data to table latch
TBLWT* ; write data, perform a short write
to internal TBLWT holding register.
DECFSZ COUNTER ; loop until holding registers are full
BRA WRITE_WORD_TO_HREGS

PROGRAM_MEMORY

BCF NVMCON1, REG0 ; point to Program Flash Memory
BSF NVMCON1, REG1 ; point to Program Flash Memory
BSF NVMCON1, WREN ; enable write to memory
BCF NVMCON1, FREE ; enable write to memory
BCF INTCON0, GIE ; disable interrupts

Required
MOVLW 55h
MOVWF NVMCON2 ; write 55h
Sequence
MOVLW 0AAh
MOVWF NVMCON2 ; write 0AAh
BSF NVMCON1, WR ; start program (CPU stall)
DCFSZ COUNTER2 ; repeat for remaining write blocks
BRA WRITE_BYTE_TO_HREGS
BSF INTCON0, GIE ; re-enable interrupts
BCF NVMCON1, WREN ; disable write to memory
FIGURE 13-9: PROGRAM FLASH MEMORY (PFM) WRITE FLOWCHART

Start
Write Operation

Determine number of words to be written into PFM. The number of words cannot exceed the number of words per row (word_cnt)

Select access to PFM locations using NVMREG<1:0> bits

Select Row Address TBLPTR

Select Write Operation (FREE = 0)

Load Write Latches Only

Enable Write/Erase Operation (WREN = 1)

Load the value to write TABLAT

Update the word counter (word_cnt--)

Last word to write ?

Yes

Write Latches to PFM

No

Disable Interrupts (GIE = 0)

Unlock Sequence\(^{(1)}\)

No delay when writing to PFM Latches

Write Latches to PFM

CPU stalls while Write operation completes (2 ms typical)

Unlock Sequence\(^{(1)}\)

Re-enable Interrupts (GIE = 1)

Disable Interrupts (GIE = 0)

Unlock Sequence\(^{(1)}\)

Disable Write/Erase Operation (WREN = 0)

Re-enable Interrupts (GIE = 1)

Increment Address TBLPTR++

End Write Operation
13.1.6.2 Write Verify
Depending on the application, good programming practice may dictate that the value written to the memory should be verified against the original value. This should be used in applications where excessive writes can stress bits near the specification limit. Since program memory is stored as a full page, the stored program memory contents are compared with the intended data stored in RAM after the last write is complete.

**FIGURE 13-10: PROGRAM FLASH MEMORY VERIFY FLOWCHART**

13.1.6.3 Unexpected Termination of Write Operation
If a write is terminated by an unplanned event, such as loss of power or an unexpected Reset, the memory location just programmed should be verified and reprogrammed if needed. If the write operation is interrupted by a MCLR Reset or a WDT Time-out Reset during normal operation, the WRERR bit will be set which the user can check to decide whether a rewrite of the location(s) is needed.

13.1.6.4 Protection Against Spurious Writes
A write sequence is valid only when both the following conditions are met, this prevents spurious writes which might lead to data corruption.

1. The WR bit is gated through the WREN bit. It is suggested to have the WREN bit cleared at all times except during memory writes. This prevents memory writes if the WR bit gets set accidentally.
2. The NVM unlock sequence must be performed each time before a write operation.

13.2 Device Information Area, Device Configuration Area, User ID, Device ID and Configuration Word Access

When REG<1:0> = 0x01 or 0x11 in the NVMCON1 register, the Device Information Area, the Device Configuration Area, the User ID’s, Device ID/Revision ID and Configuration Words can be accessed. Different access may exist for reads and writes (see Table 13-1).

13.2.1 Reading Access
The user can read from these blocks by setting the REG bits to 0x01 or 0x11. The user needs to load the address into the TBLPTR registers. Executing a TBLRD after that moves the byte pointed to the TABLAT register. The CPU operation is suspended during the read and resumes after. When read access is initiated on an address outside the parameters listed in Table 13-1, the TABLAT register is cleared, reading back ‘0’s.

13.2.2 Writing Access
The WREN bit in NVMCON1 must be set to enable writes. This prevents accidental writes to the CONFIG words due to errant (unexpected) code execution. The WREN bit should be kept clear at all times, except when updating the CONFIG words. The WREN bit is not cleared by hardware. The WR bit will be inhibited from being set unless the WREN bit is set.
The user needs to load the TBLPTR and TABLAT register with the address and data byte respectively before executing the Write command. An unlock sequence needs to be followed for writing to the USER IDs/DEVICE IDs/CONFIG words (Section 13.1.4, NVM Unlock Sequence). If WRTC = 0 or if TBLPTR points an invalid address location (see Table 13-1), WR bit is cleared without any effect and WRERR is set.

A single CONFIG word byte is written at once and the operation includes an implicit erase cycle for that byte (it is not necessary to set FREE). CPU execution is stalled and at the completion of the write cycle, the WR bit is cleared in hardware and the NVM Interrupt Flag bit (NVMIF) is set. The new CONFIG value takes effect when the CPU resumes operation.

**TABLE 13-4: DIA, DCI, USER ID, DEV/REV ID AND CONFIGURATION WORD ACCESS (REG<1:0> = x1)**

<table>
<thead>
<tr>
<th>Address</th>
<th>Function</th>
<th>Read Access</th>
<th>Write Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 0000h-20 000Fh</td>
<td>User IDs</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>30 0000h-30 0009h</td>
<td>Configuration Words</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>3F 0000h-3F 003Fh</td>
<td>DIA</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>3F FF00h-3F FF09h</td>
<td>DCI</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>3F FFFCh-3F FFFFh</td>
<td>Revision ID/Device ID</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>
13.3 Data EEPROM Memory

The data EEPROM is a nonvolatile memory array, separate from the data RAM and program memory, which is used for long-term storage of program data. It is not directly mapped in either the register file or program memory space but is indirectly addressed through the Special Function Registers (SFRs). The EEPROM is readable and writable during normal operation over the entire VDD range.

Four SFRs are used to read and write to the data EEPROM as well as the program memory. They are:

- NVMCON1
- NVMCON2
- NVMADAT
- NVMADRL
- NVMADRH

The data EEPROM allows byte read and write. When interfacing to the data memory block, NVMDAT holds the 8-bit data for read/write and the NVMADRH:NVMADRL register pair holds the address of the EEPROM location being accessed.

The EEPROM data memory is rated for high erase/write cycle endurance. A byte write automatically erases the location and writes the new data (erase-before-write). The write time is controlled by an internal programming timer; it will vary with voltage and temperature as well as from chip-to-chip. Refer to the Data EEPROM Memory parameters in Section 45.0 “Electrical Specifications” for limits.

13.3.1 NVMADRL AND NVMADRH REGISTERS

The NVMADRH:NVMADRL registers are used to address the data EEPROM for read and write operations.

13.3.2 NVMCON1 AND NVMCON2 REGISTERS

Access to the data EEPROM is controlled by two registers: NVMCON1 and NVMCON2. These are the same registers which control access to the program memory and are used in a similar manner for the data EEPROM.

The NVMCON1 register (Register 13-1) is the control register for data and program memory access. Control bits REG<1:0> determine if the access will be to program, Data EEPROM Memory or the User IDs, Configuration bits, Revision ID and Device ID.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear.

The WRERR bit is set by hardware when the WR bit is set and cleared when the internal programming timer expires and the write operation is complete.

The WR control bit initiates write operations. The bit can be set but not cleared by software. It is cleared only by hardware at the completion of the write operation.

The NVMIF Interrupt Flag bit of the PIR0 register is set when the write is complete. It must be cleared by software.

Control bits, RD and WR, start read and erase/write operations, respectively. These bits are set by firmware and cleared by hardware at the completion of the operation.

The RD bit cannot be set when accessing program memory (REG<1:0> = 0x10). Program memory is read using table read instructions. See Section 13.1.1 “Table Reads and Table Writes” regarding table reads.
13.3.3 READING THE DATA EEPROM MEMORY

To read a data memory location, the user must write the address to the NVMADRL and NVMADRH register pair, clear REG<1:0> control bit in NVMCON1 register to access Data EEPROM locations and then set control bit, RD. The data is available on the very next instruction cycle; therefore, the NVMDAT register can be read by the next instruction. NVMDAT will hold this value until another read operation, or until it is written to by the user (during a write operation).

The basic process is shown in Example 13-5.

FIGURE 13-11: DATA EEPROM READ FLOWCHART

13.3.4 WRITING TO THE DATA EEPROM MEMORY

To write an EEPROM data location, the address must first be written to the NVMADRL and NVMADRH register pair and the data written to the NVMDAT register. The sequence in Example 13-6 must be followed to initiate the write cycle.

The write will not begin if NVM Unlock sequence, described in Section 13.1.4 “NVM Unlock Sequence”, is not exactly followed for each byte. It is strongly recommended that interrupts be disabled during this code segment.

Additionally, the WREN bit in NVMCON1 must be set to enable writes. This mechanism prevents accidental writes to data EEPROM due to unexpected code execution (i.e., runaway programs). The WREN bit should be kept clear at all times, except when updating the EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, NVMCON1, NVMADRL, NVMADRH and NVMDAT cannot be modified. The WR bit will be inhibited from being set unless the WREN bit is set. Both WR and WREN cannot be set with the same instruction.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. A single Data EEPROM word is written and the operation includes an implicit erase cycle for that word (it is not necessary to set FREE). CPU execution continues in parallel and at the completion of the write cycle, the WR bit is cleared in hardware and the NVM Interrupt Flag bit (NVMIF) is set. The user can either enable this interrupt or poll this bit. NVMIF must be cleared by software.
13.3.5 WRITE VERIFY

Depending on the application, good programming practice may dictate that the value written to the memory should be verified against the original value. This should be used in applications where excessive writes can stress bits near the specification limit.

EXAMPLE 13-5: DATA EEPROM READ

<table>
<thead>
<tr>
<th>; Data Memory Address to read</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CLRFF            NVMCON1    ; Setup Data EEPROM Access</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVFF            EE_ADDRLL, W</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVVFF           NVMADRL     ; Setup Address</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BSF              NVMCON1, RD  ; Issue EE Read</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVFF            NVMDAT, W   ; W = EE_DATA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

EXAMPLE 13-6: DATA EEPROM WRITE

<table>
<thead>
<tr>
<th>; Data Memory Address to write</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CLRFF            NVMCON1    ; Setup Data EEPROM Access</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVFF            EE_ADDRLL, W</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVVFF           NVMADRL     ; Setup Address</td>
<td></td>
<td></td>
</tr>
<tr>
<td>; Data Memory Value to write</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVFF            EE_DATA, W</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVVFF           NVMDAT      ;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>; Enable writes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BSF              NVMCON1, WREN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>; Disable interrupts</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BCF              INTCON0, GIE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>; Required unlock sequence</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVLV            55h         ;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVVF            NVMCON2     ;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVLL            AAh         ;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOVVF            NVMCON2     ;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>; Set WR bit to begin write</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BSF              NVMCON1, WR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>; Enable INT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BSF              INTCON0, GIE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>; Wait for interrupt, write done</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SLEEP            ;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>; Disable writes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BCF              NVMCON1, WREN</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

13.3.6 OPERATION DURING CODE-PROTECT

Data EEPROM Memory has its own code-protect bits in Configuration Words. External read and write operations are disabled if code protection is enabled. If the Data EEPROM is write-protected or if NVMADR points an invalid address location, the WR bit is cleared without any effect. WRERR is signaled in this scenario.

13.3.7 PROTECTION AGAINST SPURIOUS WRITE

There are conditions when the user may not want to write to the Data EEPROM Memory. To protect against spurious EEPROM writes, various mechanisms have been implemented. On power-up, the WREN bit is cleared. In addition, writes to the EEPROM are blocked during the Power-up Timer period (TPWRT).

The unlock sequence and the WREN bit together help prevent an accidental write during brown-out, power glitch or software malfunction.
13.3.8 ERASING THE DATA EEPROM MEMORY

Data EEPROM Memory can be erased by writing 0xFF to all locations in the Data EEPROM Memory that needs to be erased.

**EXAMPLE 13-7: DATA EEPROM REFRESH ROUTINE**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLRF NVMADRL</td>
<td>Start at address 0</td>
</tr>
<tr>
<td>BCF NVMCON1, CFGS</td>
<td>Set for memory</td>
</tr>
<tr>
<td>BCF NVMCON1, EEPGD</td>
<td>Set for Data EEPROM</td>
</tr>
<tr>
<td>BCF INTCON0, GIE</td>
<td>Disable interrupts</td>
</tr>
<tr>
<td>BSF NVMCON1, WREN</td>
<td>Enable writes</td>
</tr>
<tr>
<td>Loop</td>
<td>Loop to refresh array</td>
</tr>
<tr>
<td>BSF NVMCON1, RD</td>
<td>Read current address</td>
</tr>
<tr>
<td>MOVWF NVMCON2</td>
<td>Write 55h</td>
</tr>
<tr>
<td>MOVWF NVMCON2</td>
<td>Write 0AAh</td>
</tr>
<tr>
<td>BTFSC NVMCON1, WR</td>
<td>Set WR bit to begin write</td>
</tr>
<tr>
<td>BRA  §-2</td>
<td>Wait for write to complete</td>
</tr>
<tr>
<td>INCFSZ NVMADRL, F</td>
<td>Increment address</td>
</tr>
<tr>
<td>BRA LOOP</td>
<td>Not zero, do it again</td>
</tr>
<tr>
<td>BCF NVMCON1, WREN</td>
<td>Disable writes</td>
</tr>
<tr>
<td>BSF INTCON0, GIE</td>
<td>Enable interrupts</td>
</tr>
</tbody>
</table>
### 13.4 Register Definitions: Nonvolatile Memory

**REGISTER 13-1: NVMCON1: NONVOLATILE MEMORY CONTROL 1 REGISTER**

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R/S/HC-0/0</th>
<th>R/W/HS-x/q</th>
<th>R/W-0/0</th>
<th>R/S/HC-0/0</th>
<th>R/S/HC-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>REG&lt;1:0&gt;</td>
<td>FREE</td>
<td>WRERR</td>
<td>WREN</td>
<td>WR</td>
<td>RD</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**

- R = Readable bit
- W = Writable bit
- HC = Bit is cleared by hardware
- x = Bit is unknown
- -n = Value at POR
- S = Bit can be set by software, but not cleared
- '0' = Bit is cleared
- '1' = Bit is set
- U = Unimplemented bit, read as '0'

**bit 7-6**

- **REG<1:0>: NVM Region Selection bit**
  - 10 = Access PFM Locations
  - x1 = Access User IDs, Configuration Bits, DIA, DCI, Rev ID and Device ID
  - 00 = Access Data EEPROM Memory Locations

**bit 5**

- **Unimplemented:** Read as ‘0’

**bit 4**

- **FREE: Program Flash Memory Erase Enable bit**(1)
  - 1 = Performs an erase operation on the next WR command
  - 0 = The next WR command performs a write operation

**bit 3**

- **WRERR: Write-Reset Error Flag bit**(2,3,4)
  - 1 = A write operation was interrupted by a Reset (hardware set), or WR was written to 1'b1 when an invalid address is accessed (Table 4-1, Table 13-1) or WR was written to 1'b1 when REG<1:0> and address do not point to the same region or WR was written to 1'b1 when a write-protected address is accessed (Table 4-2).
  - 0 = All write operations have completed normally

**bit 2**

- **WREN: Program/Erase Enable bit**
  - 1 = Allows program/erase and refresh cycles
  - 0 = Inhibits programming/erasing and user refresh of NVM

**bit 1**

- **WR: Write Control bit**(5,6,7)
  - When REG points to a Data EEPROM Memory location:
    - 1 = Initiates an erase/program cycle at the corresponding Data EEPROM Memory location
  - When REG points to a PFM location:
    - 1 = Initiates the PFM write operation with data from the holding registers
    - 0 = NVM program/erase operation is complete and inactive

**bit 0**

- **RD: Read Control bit**(8)
  - 1 = Initiates a read at address pointed by REG and NVMADR, and loads data into NVMDAT
  - 0 = NVM read operation is complete and inactive

**Note 1:**

- This can only be used with PFM.
- 2: This bit is set when WR = 1 and clears when the internal programming timer expires or the write is completed successfully.
- 3: Bit must be cleared by the user; hardware will not clear this bit.
- 4: Bit may be written to ‘1’ by the user in order to implement test sequences.
- 5: This bit can only be set by following the unlock sequence of Section 13.1.4 “NVM Unlock Sequence”.
- 6: Operations are self-timed and the WR bit is cleared by hardware when complete.
- 7: Once a write operation is initiated, setting this bit to zero will have no effect.
- 8: The bit can only be set in software. The bit is cleared by hardware when the operation is complete.
### REGISTER 13-2: NVMCON2: NONVOLATILE MEMORY CONTROL 2 REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>NVMCON2&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- x = Bit is unknown
- ‘0’ = Bit is cleared
- ‘1’ = Bit is set
- -n = Value at POR

**bit 7-0**  
**NVMCON2<7:0>:**
- Refer to [Section 13.1.4 “NVM Unlock Sequence”](#).

**Note 1:**  
This register always reads zeros, regardless of data written.

### Register 13-3: NVMADRL: Data EEPROM Memory Address Low

<table>
<thead>
<tr>
<th></th>
<th>R/W-x/0</th>
<th>R/W-x/0</th>
<th>R/W-x/0</th>
<th>R/W-x/0</th>
<th>R/W-x/0</th>
<th>R/W-x/0</th>
<th>R/W-x/0</th>
<th>R/W-x/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>ADR&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>R/W-x/0</th>
<th>R/W-x/0</th>
<th>R/W-x/0</th>
<th>R/W-x/0</th>
<th>R/W-x/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- x = Bit is unknown
- ‘0’ = Bit is cleared
- ‘1’ = Bit is set
- -n = Value at POR

**bit 7-0**  
**ADR<7:0>:**  
EEPROM Read Address bits

### REGISTER 13-4: NVMADRH: DATA EEPROM MEMORY ADDRESS HIGH

<table>
<thead>
<tr>
<th></th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>ADR&lt;9:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- x = Bit is unknown
- ‘0’ = Bit is cleared
- ‘1’ = Bit is set
- -n = Value at POR

**bit 7-2**  
**Unimplemented:**  
Read as ‘0’

**bit 1-0**  
**ADR<9:8>:**  
EEPROM Read Address bits
REGISTER 13-5: NVMDAT: DATA EEPROM MEMORY DATA

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAT&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **x** = Bit is unknown
- ‘0’ = Bit is cleared
- ‘1’ = Bit is set
- -n = Value at POR

bit 7-0 **DAT<7:0>**: The value of the data memory word returned from NVMADR after a Read command, or the data written by a Write command.

**TABLE 13-5:** SUMMARY OF REGISTERS ASSOCIATED WITH NONVOLATILE MEMORY CONTROL

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>NVMCON1</td>
<td>REG&lt;1:0&gt;</td>
<td>—</td>
<td>FREE</td>
<td>WRERR</td>
<td>WREN</td>
<td>WR</td>
<td>RD</td>
<td></td>
<td>200</td>
</tr>
<tr>
<td>NVMCON2</td>
<td>Unlock Pattern</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>201</td>
</tr>
<tr>
<td>NVMADRL</td>
<td></td>
<td></td>
<td>NVMADR&lt;7:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
<td>201</td>
</tr>
<tr>
<td>NVMADR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>NVMADR&lt;9:8&gt;</td>
<td>201</td>
</tr>
<tr>
<td>NVMDAT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>NVMDAT&lt;7:0&gt;</td>
<td>202</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented, read as ‘0’. Shaded bits are not used during EEPROM access.

*Page provides register information.*
14.0 CYCLIC REDUNDANCY CHECK (CRC) MODULE WITH MEMORY SCANNER

The Cyclic Redundancy Check (CRC) module provides a software-configurable hardware-implemented CRC checksum generator. This module includes the following features:

• Any standard CRC up to 16 bits can be used
• Configurable Polynomial
• Any seed value up to 16 bits can be used
• Standard and reversed bit order available
• Augmented zeros can be added automatically or by the user
• Memory scanner for fast CRC calculations on program/Data EEPROM memory user data
• Software loadable data registers for communication CRC’s

14.1 CRC Module Overview

The CRC module provides a means for calculating a check value of program/Data EEPROM memory. The CRC module is coupled with a memory scanner for faster CRC calculations. The memory scanner can automatically provide data to the CRC module. The CRC module can also be operated by directly writing data to SFRs, without using a scanner.
14.2 CRC Functional Overview

The CRC module can be used to detect bit errors in the program memory using the built-in memory scanner or through user input RAM memory. The CRC module can accept up to a 16-bit polynomial with up to a 16-bit seed value. A CRC calculated check value (or checksum) will then be generated into the CRCACC<15:0> registers for user storage. The CRC module uses an XOR shift register implementation to perform the polynomial division required for the CRC calculation.

EXAMPLE 14-1: CRC EXAMPLE

<table>
<thead>
<tr>
<th>CRC-16-ANSI</th>
<th>x^{16} + x^{15} + x^2 + 1 (17 bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard 16-bit representation = 0x8005</td>
<td></td>
</tr>
<tr>
<td>CRCXORH = 0b10000000</td>
<td></td>
</tr>
<tr>
<td>CRCXORL = 0b00000010-</td>
<td></td>
</tr>
<tr>
<td>Data Sequence:</td>
<td></td>
</tr>
<tr>
<td>0x55, 0x66, 0x77, 0x88</td>
<td></td>
</tr>
<tr>
<td>DLEN = 0b0111</td>
<td></td>
</tr>
<tr>
<td>PLEN = 0b1111</td>
<td></td>
</tr>
<tr>
<td>Data entered into the CRC:</td>
<td></td>
</tr>
<tr>
<td>SHIFTM = 0:</td>
<td></td>
</tr>
<tr>
<td>01010101 01100110 01110111 10001000</td>
<td></td>
</tr>
<tr>
<td>SHIFTM = 1:</td>
<td></td>
</tr>
<tr>
<td>10101010 01100110 11101110 00010001</td>
<td></td>
</tr>
<tr>
<td>Check Value (ACCM = 1):</td>
<td></td>
</tr>
<tr>
<td>SHIFTM = 0: 0x32D6</td>
<td></td>
</tr>
<tr>
<td>CRCACCH = 0b001100010</td>
<td></td>
</tr>
<tr>
<td>CRCACCL = 0b11010110</td>
<td></td>
</tr>
<tr>
<td>SHIFTM = 1: 0x6BA2</td>
<td></td>
</tr>
<tr>
<td>CRCACCH = 0b011010111</td>
<td></td>
</tr>
<tr>
<td>CRCACCL = 0b101000010</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Bit 0 is unimplemented. The LSb of any CRC polynomial is always ‘1’ and will always be treated as a ‘1’ by the CRC for calculating the CRC check value. This bit will be read in software as a ‘0’.
14.3 CRC Polynomial Implementation

Any polynomial can be used. The polynomial and accumulator sizes are determined by the PLEN<3:0> bits. For an n-bit accumulator, PLEN = n−1 and the corresponding polynomial is n+1 bits. Therefore the accumulator can be any size up to 16 bits with a corresponding polynomial up to 17 bits. The MSb and LSb of the polynomial are always '1' which is forced by hardware. All polynomial bits between the MSb and LSb are specified by the CRCXOR registers. For example, when using CRC-16-ANSI, the polynomial is defined as X^16+X^15+X^2+1.

\[
\text{Linear Feedback Shift Register for CRC-16-ANSI} \quad x^{16} + x^{15} + x^2 + 1
\]

Example 14-1

14.4 CRC Data Sources

Data can be input to the CRC module in two ways:

- User data using the CRCDAT registers (CRCDATH and CRCDATL)
- Program memory using the Program Memory Scanner

To set the number of bits of data, up to 16 bits, the DLEN bits of CRCCON1 must be set accordingly. Only data bits in CRCDAT registers up to DLEN will be used, other data bits in CRCDAT registers will be ignored.

Data is moved into the CRCSHIFT as an intermediate to calculate the check value located in the CRCACC registers.

The SHIFTM bit is used to determine the bit order of the data being shifted into the accumulator. If SHIFTM is not set, the data will be shifted in MSb first (Big Endian). The value of DLEN will determine the MSb. If SHIFTM bit is set, the data will be shifted into the accumulator in reversed order, LSb first (Little Endian).

The CRC module can be seeded with an initial value by setting the CRCACC<15:0> registers to the appropriate value before beginning the CRC.

14.4.1 CRC FROM USER DATA

To use the CRC module on data input from the user, the user must write the data to the CRCDAT registers. The data from the CRCDAT registers will be latched into the shift registers on any write to the CRCDATL register.

14.4.2 CRC FROM FLASH

To use the CRC module on data located in Program memory, the user can initialize the Program Memory Scanner as defined in Section 14.8, Scanner Module Overview.
14.5 CRC Check Value

The CRC check value will be located in the CRCACC registers after the CRC calculation has finished. The check value will depend on two mode settings of the CRCCON0 register: ACCM and SHIFTM. When the ACCM bit is set, the CRC module augments the data with a number of zeros equal to the length of the polynomial to align the final check value. When the ACCM bit is not set, the CRC will stop at the end of the data. A number of zeros equal to the length of the polynomial can then be entered into CRCDAT to find the same check value as augmented mode. Alternatively the expected check value can be entered at this point to make the final result equal '0'.

When the CRC check value is computed with the SHIFTM bit set, selecting LSb first, and the ACCM bit is also set then the final value in the CRCACC registers will be reversed such that the LSb will be in the MSb position and vice versa. This is the expected check value in bit reversed form. If you are creating a check value to be appended to a data stream then a bit reversal must be performed on the final value to achieve the correct checksum. You can use the CRC to do this reversal by the following method:

• Save the CRCACC value in user RAM space
• Clear the CRCACC registers
• Clear the CRCXOR registers
• Write the saved CRCACC value to the CRCDAT input.

The properly oriented check value will be in the CRCACC registers as the result.

14.6 CRC Interrupt

The CRC will generate an interrupt when the BUSY bit transitions from 1 to 0. The CRCIF Interrupt Flag is set every time the BUSY bit transitions, regardless of whether or not the CRC interrupt is enabled. The CRCIF bit can only be cleared in software.

14.7 Configuring the CRC

The following steps illustrate how to properly configure the CRC.

1. Determine if the automatic program memory scan will be used with the scanner or manual calculation through the SFR interface and perform the actions specified in Section 14.4 “CRC Data Sources”, depending on which decision was made.

2. If desired, seed a starting CRC value into the CRCACCH/L registers.

3. Program the CRCXORH/L registers with the desired generator polynomial.

4. Program the DLEN<3:0> bits of the CRCCON1 register with the length of the data word - 1 (refer to Example 14-1). This determines how many times the shifter will shift into the accumulator for each data word.

5. Program the PLEN<3:0> bits of the CRCCON1 register with the length of the polynomial - 2 (refer to Example 14-1).

6. Determine whether shifting in trailing zeros is desired and set the ACCM bit of the CRCCON0 register appropriately.

7. Likewise, determine whether the MSb or LSb should be shifted first and write the SHIFTM bit of the CRCCON0 register appropriately.

8. Write the GO bit of the CRCCON0 register to begin the shifting process.

9a. If manual SFR entry is used, monitor the FULL bit of the CRCCON0 register. When FULL = 0, another word of data can be written to the CRCDATH/L registers, keeping in mind that CRCDATH should be written first if the data has more than eight bits, as the shifter will begin upon the CRCDATL register being written.

9b. If the scanner is used, the scanner will automatically load words into the CRCDATH/L registers as needed, as long as the GO bit is set.

10a. If manual entry is used, monitor the CRCIF (and BUSY bit to determine when the completed CRC calculation can be read from CRCACCH/L registers.

10b. If using the memory scanner, monitor the SCANIF (or the GO bit) for the scanner to finish pushing information into the CRCDAT registers. After the scanner is completed, monitor the BUSY bit to determine that the CRC has been completed and the check value can be read from the CRCACC registers. If both the interrupt flags are set and the BUSY and GO bits are cleared, the completed CRC calculation can be read from the CRCACCH/L registers.
14.8 Scanner Module Overview

The Scanner allows segments of the Program Flash Memory or Data EEPROM, to be read out (scanned) to the CRC Peripheral. The Scanner module interacts with the CRC module and supplies it data one word at a time. Data is fetched from the address range defined by SCANLADR registers up to the SCANHADR registers.

The Scanner begins operation when the SGO bit is set (SCANCON0 Register) and ends when either SGO is cleared by the user or when SCANLADR increments past SCANHADR. The SGO bit is also cleared by clearing the EN bit (CRCCON0 register).

14.9 Configuring the Scanner

The scanner module may be used in conjunction with the CRC module to perform a CRC calculation over a range of program memory or Data EEPROM addresses. In order to set up the scanner to work with the CRC, perform the following steps:

1. Set up the CRC module (See Section 14.7 “Configuring the CRC”) and enable the Scanner module by setting the EN bit in the SCANCON0 register.
2. Choose which memory region the Scanner module should operate on and set the MREG bit of the SCANCON0 register appropriately.
3. If trigger is used for scanner operation, set the TRIGEN bit of the SCANCON0 register and select the trigger source using SCANTRIG register. Select the trigger source using SCANTRIG register and then set the TRIGEN bit of the SCANCON0 register. See Table 14-1 for Scanner Operation.
4. If Burst mode of operation is desired, set the BURSTMD bit (SCANCON0 register). See Table 14-1 for Scanner Operation.
5. Set the SCANLADR/L/H/U and SCANHADR/L/H/U registers with the beginning and ending locations in memory that are to be scanned.
6. Select the priority level for the Scanner module (See Section 3.1 “System Arbitration”) and lock the priorities (See Section 3.1.1 “Priority Lock”).
7. Both CRCEN and CRCGO bits must be enabled to use the scanner. Setting the SGO bit will start the scanner operation.

14.10 Scanner Interrupt

The scanner will trigger an interrupt when the SCANLADR increments past SCANHADR. The SCANIF bit can only be cleared in software.

14.11 Scanning Modes

The interaction of the scanner with the system operation is controlled by the priority selection in the System Arbiter (see Section 3.2 “Memory Access Scheme”). Additionally, BURSTMD and TRIGEN also determine the operation of the Scanner.

14.11.1 TRIGEN = 0, BURSTMD = 0

In this case, the memory access request is granted to the scanner if no other higher priority source is requesting access.

All sources with lower priority than the scanner will get the memory access cycles that are not utilized by the scanner.

14.11.2 TRIGEN = 1, BURSTMD = 0

In this case, the memory access request is generated when the CRC module is ready to accept.

The memory access request is granted to the scanner if no other higher priority source is requesting access.

All sources with lower priority than the scanner will get the memory access cycles that are not utilized by the scanner.

14.11.3 TRIGEN = x, BURSTMD = 1

In this case, the memory access is always requested by the scanner.

The memory access request is granted to the scanner if no other higher priority source is requesting access. The memory access cycles will not be granted to lower priority sources than the scanner until it completes operation i.e., SGO = 0 (SCANCON0 register)

Note: If TRIGEN = 1 and BURSTMD = 1, the user should ensure that the trigger source is active for the Scanner operation to complete.
14.12 Register Definitions: CRC and Scanner Control

Long bit name prefixes for the CRC and Scanner peripherals are shown below. Refer to Section 1.3.2.2 “Long Bit Names” for more information.

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Bit Name Prefix</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRC</td>
<td>CRC</td>
</tr>
</tbody>
</table>

**REGISTER 14-1: CRCCON0: CRC CONTROL REGISTER 0**

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R-0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>GO</td>
<td>BUSY</td>
<td>ACCM</td>
<td>—</td>
<td>—</td>
<td>SHIFTM</td>
<td>FULL</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

- **bit 7**: EN: CRC Enable bit
  - 1 = CRC module is enabled
  - 0 = CRC is disabled

- **bit 6**: GO: CRC Go bit
  - 1 = Start CRC serial shifter
  - 0 = CRC serial shifter turned off

- **bit 5**: BUSY: CRC Busy bit
  - 1 = Shifting in progress or pending
  - 0 = All valid bits in shifter have been shifted into accumulator

- **bit 4**: ACCM: Accumulator Mode bit
  - 1 = Data is concatenated with zeros
  - 0 = Data is not concatenated with zeros

- **bit 3-2**: Unimplemented: Read as ‘0’

- **bit 1**: SHIFTM: Shift Mode bit
  - 1 = Shift right (LSb)
  - 0 = Shift left (MSb)

- **bit 0**: FULL: Data Path Full Indicator bit
  - 1 = CRCDATH/L registers are full
  - 0 = CRCDATH/L registers have shifted their data into the shifter

**REGISTER 14-2: CRCCON1: CRC CONTROL REGISTER 1**

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DLEN&lt;3:0&gt;</td>
<td>PLEN&lt;3:0&gt;</td>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

- **bit 7-4**: DLEN<3:0>: Data Length bits
  Denotes the length of the data word -1 (See Example 14-1)

- **bit 3-0**: PLEN<3:0>: Polynomial Length bits
  Denotes the length of the polynomial -1 (See Example 14-1)
**REGISTER 14-3: CRCDATH: CRC DATA HIGH BYTE REGISTER**

<table>
<thead>
<tr>
<th>R/W-xx</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-0**

**DATA<15:8>: CRC Input/Output Data bits**

**REGISTER 14-4: CRCDATL: CRC DATA LOW BYTE REGISTER**

<table>
<thead>
<tr>
<th>R/W-xx</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-0**

**DATA<7:0>: CRC Input/Output Data bits**

Writing to this register fills the shifter.

**REGISTER 14-5: CRCACCH: CRC ACCUMULATOR HIGH BYTE REGISTER**

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-0**

**ACC<15:8>: CRC Accumulator Register bits**
### REGISTER 14-6: CRCACCL: CRC ACCUMULATOR LOW BYTE REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ACC&lt;7&gt;</td>
<td>CRC Accumulator Register bits</td>
</tr>
<tr>
<td>0</td>
<td>ACC&lt;0&gt;</td>
<td>CRC Accumulator Register bits</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- ‘n/n’ = Value at POR and BOR/Value at all other Resets

### REGISTER 14-7: CRCSHIFTH: CRC SHIFT HIGH BYTE REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>SHIFT&lt;15&gt;</td>
<td>CRC Shifter Register bits</td>
</tr>
<tr>
<td>0</td>
<td>SHIFT&lt;0&gt;</td>
<td>CRC Shifter Register bits</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- ‘n/n’ = Value at POR and BOR/Value at all other Resets

### REGISTER 14-8: CRCSHIFTL: CRC SHIFT LOW BYTE REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>SHIFT&lt;7&gt;</td>
<td>CRC Shifter Register bits</td>
</tr>
<tr>
<td>0</td>
<td>SHIFT&lt;0&gt;</td>
<td>CRC Shifter Register bits</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- ‘n/n’ = Value at POR and BOR/Value at all other Resets

Reading from this register reads the CRC Shifter.
### REGISTER 14-9: CRCXORH: CRC XOR HIGH BYTE REGISTER

<table>
<thead>
<tr>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
</tr>
</thead>
<tbody>
<tr>
<td>X&lt;15:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

**bit 7-0**  
X<15:8>: XOR of Polynomial Term X^n Enable bits

### REGISTER 14-10: CRCXORL: CRC XOR LOW BYTE REGISTER

<table>
<thead>
<tr>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>U-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>X&lt;7:1&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

**bit 7-1**  
X<7:1>: XOR of Polynomial Term X^n Enable bits

**bit 0**  
**Unimplemented:** Read as ‘1’
### REGISTER 14-11: SCANCON0: SCANNER ACCESS CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W/HC-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>TRIGEN</td>
<td>SGO</td>
<td></td>
<td></td>
<td>MREG</td>
<td>BURSTMD</td>
<td>BUSY</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **n/n** = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **HC** = Bit is cleared by hardware

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **n/n** = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **HC** = Bit is cleared by hardware

#### bit 7

**EN:** Scanner Enable bit\(^{(1)}\)

- 1 = Scanner is enabled
- 0 = Scanner is disabled

#### bit 6

**TRIGEN:** Scanner Trigger Enable bit\(^{(2)}\)

- 1 = Scanner trigger is enabled
- 0 = Scanner trigger is disabled

Refer [Table 14-1](#).

#### bit 5

**SGO:** Scanner GO bit\(^{(3, 4)}\)

- 1 = When the CRC is ready, the Memory region set by the MREG bit will be accessed and data is passed to the CRC peripheral.
- 0 = Scanner operations will not occur

#### bit 4-3

**Unimplemented:** Read as ‘0’

#### bit 2

**MREG:** Scanner Memory Region Select bit\(^{(2)}\)

- 1 = Scanner address points to Data EEPROM
- 0 = Scanner address points to Program Flash Memory

#### bit 1

**BURSTMD:** Scanner Burst Mode bit

- 1 = Memory access request to the CPU Arbiter is always true
- 0 = Memory access request to the CPU Arbiter is dependent on the CRC request and Trigger

Refer [Table 14-1](#).

#### bit 0

**BUSY:** Scanner Busy Indicator bit

- 1 = Scanner cycle is in process
- 0 = Scanner cycle is compete (or never started)

**Note 1:** Setting EN = 1 (SCANCON0 register) does not affect any other register content.

**Note 2:** Scanner trigger selection can be set using the SCANTRIG register.

**Note 3:** This bit can be cleared in software. It is cleared in hardware when LADR>HADR (and a data cycle is not occurring) or when CRCGO = 0 (CRCCON0 register).

**Note 4:** CRCEN and CRCGO bits (CRCCON0 register) must be set before setting the SGO bit.
TABLE 14-1: SCANNER OPERATING MODES(1)

<table>
<thead>
<tr>
<th>TRIGEN</th>
<th>BURSTMD</th>
<th>Scanner Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Memory access is requested when the CRC module is ready to accept data; the request is granted if no other higher priority source request is pending.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Memory access is requested when the CRC module is ready to accept data and trigger selection is true; the request is granted if no other higher priority source request is pending.</td>
</tr>
<tr>
<td>x</td>
<td>1</td>
<td>Memory access is always requested, the request is granted if no other higher priority source request is pending.</td>
</tr>
</tbody>
</table>

Note 1: See Section 3.1 “System Arbitration” for Priority selection and Section 3.2 “Memory Access Scheme” for Memory Access Scheme.

REGISTER 14-12: SCANLADRU: SCAN LOW ADDRESS UPPER BYTE REGISTER

| bit 7-6 | Unimplemented: Read as ‘0’ |
| bit 5-0 | LADR<21:16>: Scan Start/Current Address bits(1,2) |
|         | Upper bits of the current address to be fetched from, value increments on each fetch of memory. |

Note 1: Registers SCANLADRU/H/L form a 22-bit value, but are not guarded for atomic or asynchronous access; registers should only be read or written while SGO = 0 (SCANCON0 register).

2: While SGO = 1 (SCANCON0 register), writing to this register is ignored.

REGISTER 14-13: SCANLADRH: SCAN LOW ADDRESS HIGH BYTE REGISTER

| bit 7-0 | LADR<15:8>: Scan Start/Current Address bits(1, 2) |
|         | Most Significant bits of the current address to be fetched from, value increments on each fetch of memory. |

Note 1: Registers SCANLADRU/H/L form a 22-bit value, but are not guarded for atomic or asynchronous access; registers should only be read or written while SGO = 0 (SCANCON0 register).

2: While SGO = 1 (SCANCON0 register), writing to this register is ignored.
## REGISTER 14-14: SCANLADRL: SCAN LOW ADDRESS LOW BYTE REGISTER

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>LADR&lt;7:0&gt;</th>
<th>Scan Start/Current Address bits&lt;sup&gt;(1, 2)&lt;/sup&gt;</th>
<th>Least Significant bits of the current address to be fetched from, value increments on each fetch of memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **’1’** = Bit is set
- **’0’** = Bit is cleared

**Note 1:** Registers SCANLADRU/H/L form a 22-bit value, but are not guarded for atomic or asynchronous access; registers should only be read or written while SGO = 0 (SCANCON0 register).

**Note 2:** While SGO = 1 (SCANCON0 register), writing to this register is ignored.

## REGISTER 14-15: SCANHADRU: SCAN HIGH ADDRESS UPPER BYTE REGISTER

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>HADR&lt;21:16&gt;</th>
<th>Scan End Address bits&lt;sup&gt;(1, 2)&lt;/sup&gt;</th>
<th>Upper bits of the address at the end of the designated scan</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **’1’** = Bit is set
- **’0’** = Bit is cleared

**Unimplemented:** Read as ‘0’

**Note 1:** Registers SCANHADRU/H/L form a 22-bit value but are not guarded for atomic or asynchronous access; registers should only be read or written while SGO = 0 (SCANCON0 register).

**Note 2:** While SGO = 1 (SCANCON0 register), writing to this register is ignored.
## REGISTER 14-16: SCANHADRH: SCAN HIGH ADDRESS HIGH BYTE REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td>HADR&lt;15:8&gt;&lt;sup&gt;(1, 2)&lt;/sup&gt;</td>
<td></td>
<td>bit 0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- '1' = Bit is set
- '0' = Bit is cleared

**bit 7-0**  
**HADR<15:8>:** Scan End Address bits<sup>(1, 2)</sup>  
Most Significant bits of the address at the end of the designated scan

**Note 1:** Registers SCANHADRU/H/L form a 22-bit value, but are not guarded for atomic or asynchronous access; registers should only be read or written while SGO = 0 (SCANCON0 register).

**Note 2:** While SGO = 1 (SCANCON0 register), writing to this register is ignored.

## REGISTER 14-17: SCANHADRL: SCAN HIGH ADDRESS LOW BYTE REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td>HADR&lt;7:0&gt;&lt;sup&gt;(1, 2)&lt;/sup&gt;</td>
<td></td>
<td>bit 0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- '1' = Bit is set
- '0' = Bit is cleared

**bit 7-0**  
**HADR<7:0>:** Scan End Address bits<sup>(1, 2)</sup>  
Least Significant bits of the address at the end of the designated scan

**Note 1:** Registers SCANHADRU/H/L form a 22-bit value, but are not guarded for atomic or asynchronous access; registers should only be read or written while SGO = 0 (SCANCON0 register).

**Note 2:** While SGO = 1 (SCANCON0 register), writing to this register is ignored.
REGISTER 14-18: SCANTRIG: SCAN TRIGGER SELECTION REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

| bit 7-4 | Unimplemented: Read as ‘0’ |
| bit 3-0 | TSEL<3:0>: Scanner Data Trigger Input Selection bits |

- 1111 = Reserved
- 1010 = Reserved
- 1001 = SMT1_output
- 1000 = TMR6_postscaled
- 0111 = TMR5_output
- 0110 = TMR4_postscaled
- 0101 = TMR3_output
- 0100 = TMR2_postscaled
- 0011 = TMR1_output
- 0010 = TMR0_output
- 0001 = CLKREF_output
- 0000 = LFINTOSC

---

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## TABLE 14-2: SUMMARY OF REGISTERS ASSOCIATED WITH CRC

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRCACCH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>209</td>
</tr>
<tr>
<td>CRCACCL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>210</td>
</tr>
<tr>
<td>CRCCON0</td>
<td>EN</td>
<td>GO</td>
<td>BUSY</td>
<td>ACCM</td>
<td>—</td>
<td>—</td>
<td>SHIFTM</td>
<td>FULL</td>
<td>208</td>
</tr>
<tr>
<td>CRCCON1</td>
<td>DLEN&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>208</td>
</tr>
<tr>
<td>CRCDATH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PLEN&lt;3:0&gt;</td>
<td>209</td>
</tr>
<tr>
<td>CRCDATL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>209</td>
</tr>
<tr>
<td>CRCSHIFTH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SHIFT&lt;15:8&gt;</td>
<td>210</td>
</tr>
<tr>
<td>CRCSHIFFTL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SHIFT&lt;7:0&gt;</td>
<td>210</td>
</tr>
<tr>
<td>CRCXORH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X&lt;15:8&gt;</td>
<td>211</td>
</tr>
<tr>
<td>CRCXORL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>211</td>
</tr>
<tr>
<td>SCANCON0</td>
<td>EN</td>
<td>TRIGEN</td>
<td>SGO</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>MREG</td>
<td>BURSTMD</td>
<td>BUSY</td>
</tr>
<tr>
<td>SCANHADRU</td>
<td>—</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>HADR&lt;21:16&gt;</td>
<td>214</td>
</tr>
<tr>
<td>SCANHADRH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>HADR&lt;15:8&gt;</td>
<td>215</td>
</tr>
<tr>
<td>SCANHADRUL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>HADR&lt;7:0&gt;</td>
<td>215</td>
</tr>
<tr>
<td>SCANLADRU</td>
<td>—</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LADR&lt;21:16&gt;</td>
<td>213</td>
</tr>
<tr>
<td>SCANLADRRL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LADR&lt;15:8&gt;</td>
<td>213</td>
</tr>
<tr>
<td>SCANLADRRL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LADR&lt;7:0&gt;</td>
<td>214</td>
</tr>
<tr>
<td>SCANTRIG</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TSEL&lt;3:0&gt;</td>
<td>216</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented location, read as ‘0’. Shaded cells are not used for the CRC module.
15.0 DIRECT MEMORY ACCESS (DMA)

15.1 Introduction

The Direct Memory Access (DMA) module is designed to service data transfers between different memory regions directly without intervention from the CPU. By eliminating the need for CPU-intensive management of handling interrupts intended for data transfers, the CPU now can spend more time on other tasks.

PIC18(L)F25/26K83 family has two DMA modules which can be independently programmed to transfer data between different memory locations, move different data sizes, and use a wide range of hardware triggers to initiate transfers. The two DMA registers can even be programmed to work together, in order to carry out more complex data transfers without CPU overhead.

Key features of the DMA module include:

- Support access to the following memory regions:
  - GPR and SFR space (R/W)
  - Program Flash Memory (R only)
  - Data EEPROM Memory (R only)
- Programmable priority between the DMA and CPU Operations. Refer to Section 3.1 “System Arbitration” for details.
- Programmable Source and Destination address modes
  - Fixed address
  - Post-increment address
  - Post-decrement address
- Programmable Source and Destination sizes
- Source and destination pointer register, dynamically updated and reloadable
- Source and destination count register, dynamically updated and reloadable
- Programmable auto-stop based on Source or Destination counter
- Software triggered transfers
- Multiple user selectable sources for hardware triggered transfers
- Multiple user selectable sources for aborting DMA transfers

15.2 DMA Registers

The operation of the DMA module has the following registers:

- Control registers (DMAxCON0, DMAxCON1)
- Data buffer register (DMAxBUF)
- Source Start Address Register (DMAxSSAU:H:L)
- Source Pointer Register (DMAxSPTRU:H:L)
- Source Message Size Register (DMAxSSZH:L)
- Source Count Register (DMAxSCNTH:L)
- Destination Start Address Register (DMAxDSAH:L)
- Destination Pointer Register (DMAxDPTRH:L)
- Destination Message Size Register (DMAxDSZH:L)
- Destination Count Register (DMAxDCNTH:L)
- Start Interrupt Request Source Register (DMAxSIRQ)
- Abort Interrupt Request Source Register (DMAxAIRQ)

These registers are detailed in Section 15.13 “Register definitions: DMA”.

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15.3 DMA Organization

The DMA module on the K42 family of devices is designed to move data by using the existing Instruction Bus<16> and Data Bus<8> without the need for any dual-porting of memory or peripheral systems (Figure 15-1). The DMA accesses the required bus when it has been granted to by the System Arbiter.

FIGURE 15-1: DMA FUNCTIONAL BLOCK DIAGRAM
Depending on the priority of the DMA with respect to CPU execution (Refer to Section 3.2 “Memory Access Scheme” for more information), the DMA Controller can move data through two methods:

- Stalling the CPU execution until it has completed its transfers (DMA has higher priority over the CPU in this mode of operation)
- Utilizing unused CPU cycles for DMA transfers (CPU has higher priority over the DMA in this mode of operation). Unused CPU cycles are referred to as bubbles which are instruction cycles available for use by the DMA to perform read and write operations. In this way, the effective bandwidth for handling data is increased; at the same time, DMA operations can proceed without causing a processor stall.

15.4 DMA Interface

The DMA module transfers data from the source to the destination one byte at a time, this smallest data movement is called a DMA data transaction. A DMA Message refers to one or more DMA data transactions.

Each DMA data transaction consists of two separate actions:

- Reading the Source Address Memory and storing the value in the DMA Buffer register
- Writing the contents of the DMA Buffer register to the Destination Address Memory

**Note:** DMA data movement is a two-cycle operation.

The XIP bit (DMAxCON0 register) is a Status bit to indicate whether or not the data in the DMAxBUF register has been written to the destination address. If the bit is set then data is waiting to be written to the destination. If clear it means that either data has been written to the destination or that no source read has occurred.

The DMA has read access to PFM, Data EEPROM, and SFR/GPR space, and write access to SFR/GPR space. Based on these memory access capabilities, the DMA can support the following memory transactions:

**TABLE 15-1: DMA MEMORY ACCESS**

<table>
<thead>
<tr>
<th>Read Source</th>
<th>Write Destination</th>
</tr>
</thead>
<tbody>
<tr>
<td>Program Flash Memory</td>
<td>GPR</td>
</tr>
<tr>
<td>Program Flash Memory</td>
<td>SFR</td>
</tr>
<tr>
<td>Data EE</td>
<td>GPR</td>
</tr>
<tr>
<td>Data EE</td>
<td>SFR</td>
</tr>
<tr>
<td>GPR</td>
<td>GPR</td>
</tr>
<tr>
<td>SFR</td>
<td>SFR</td>
</tr>
<tr>
<td>GPR</td>
<td>SFR</td>
</tr>
<tr>
<td>SFR</td>
<td>SFR</td>
</tr>
</tbody>
</table>

Even though the DMA module has access to all memory and peripherals that are also available to the CPU, it is recommended that the DMA does not access any register that is part of the System arbitration. The DMA, as a system arbitration client should not be read or written by itself or by another DMA instantiation.

The following sections discuss the various control interfaces required for DMA data transfers.

15.4.1 DMA ADDRESSING

The start addresses for the source read and destination write operations are set using the DMAxSSA <21:0> and DMAxDSA <15:0> registers, respectively.

When the DMA Message transfers are in progress, the DMAxSPTR <21:0> and DMAxDPTR <15:0> registers contain the current address pointers for each source read and destination write operation, these registers are modified after each transaction based on the Address mode selection bits.

The SMODE and DMODE bits in the DMAxCON1 control register determine the address modes of operation by controlling how the DMAxSPTR <21:0> and DMAxDPTR <15:0> bits are updated after every DMA data transaction combination (Figure 15-2).

Each address can be separately configured to:

- Remain unchanged
- Increment by 1
- Decrement by 1
The DMA can initiate data transfers from the PFM, Data EEPROM or SFR/GPR Space. The SMR<1:0> bits in the DMAxCON1 register are used to select the type of memory being pointed to by the Source Address Pointer. The SMR<1,0> bits are required because the PFM and SFR/GPR spaces have overlapping addresses that do not allow the specified address to uniquely define the memory location to be accessed.

**Note 1:** For proper memory read access to occur, the combination of address and space selection must be valid.

**Note 2:** The destination does not have space selection bits because it can only write to the SFR/GPR space.

### 15.4.2 DMA MESSAGE SIZE/COUNTERS

A transaction is the transfer of one byte. A message consists of one or more transactions. A complete DMA process consists of one or more messages. The size registers determine how many transactions are in a message. The DMAxSSZ registers determine the source size and DMAxDSZ registers determine the destination size.

When a DMA transfer is initiated, the size registers are copied to corresponding counter registers that control the duration of the message. The DMAxSCNT registers count the source transactions and the DMAxDCNT registers count the destination transactions. Both are simultaneously decremented by one after each transaction.

A message is started by setting the DGO bit of the DMAxCON0 register and terminates when the smaller of the two counters reaches zero. When either counter reaches zero the DGO bit is cleared and the counter and pointer registers are immediately reloaded with the corresponding size and address data. If the other counter did not reach zero then the next message will continue with the count and address corresponding to that register.

When the source and destination size registers are not equal then the ratio of the largest to the smallest size determines how many messages are in the DMA process. For example, when the destination size is 6 and the source size is 2 then each message will consist of two transactions and the complete DMA process will consist of three messages. When the larger size is not an even integer of the smaller size then the last message in the process will terminate early when the larger count reaches zero. In that case, the larger counter will reset and the smaller counter will have a remainder skewing any subsequent messages by that amount.

**Note:** Reading the DMAxSCNT or DMAxDCNT registers will never return zero. When either register is decremented from '1' it is immediately reloaded from the corresponding size register.
Table 15-2 has a few examples of configuring DMA Message sizes.

**TABLE 15-2: EXAMPLE MESSAGE SIZE TABLE**

<table>
<thead>
<tr>
<th>Operation</th>
<th>Example</th>
<th>SCNT</th>
<th>DCNT</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read from single SFR location to RAM</td>
<td>U1RXB</td>
<td>1</td>
<td>N</td>
<td>N equals the number of bytes desired in the destination buffer. N &gt;= 1.</td>
</tr>
<tr>
<td>Write to single SFR location from RAM</td>
<td>U1TXB</td>
<td>N</td>
<td>1</td>
<td>N equals the number of bytes desired in the source buffer. N &gt;= 1.</td>
</tr>
<tr>
<td>Read from multiple SFR location</td>
<td>ADRES[H:L]</td>
<td>2</td>
<td>2*N</td>
<td>N equals the number of ADC results to be stored in memory. N&gt;= 1</td>
</tr>
<tr>
<td></td>
<td>TMR1[H:L]</td>
<td>2</td>
<td>2*N</td>
<td>N equals the number of TMR1 Acquisition results to be stored in memory. N&gt;= 1</td>
</tr>
<tr>
<td></td>
<td>SMT1CPR[U:H:L]</td>
<td>3</td>
<td>3*N</td>
<td>N equals the number of Capture Pulse Width measurements to be stored in memory. N&gt;= 1</td>
</tr>
<tr>
<td>Write to Multiple SFR registers</td>
<td>PWMDC[H:L]</td>
<td>2*N</td>
<td>2</td>
<td>N equals the number of PWM duty cycle values to be loaded from a memory table. N&gt;= 1</td>
</tr>
<tr>
<td></td>
<td>All ADC registers</td>
<td>N*31</td>
<td>31</td>
<td>Using the DMA to transfer a complete ADC context from RAM to the ADC registers. N&gt;= 1</td>
</tr>
</tbody>
</table>
15.5 DMA Message Transfers

Once the Enable bit is set to start DMA message transfers, the Source/Destination pointer and counter registers are initialized to the conditions shown in Table 15-3.

**TABLE 15-3: DMA INITIAL CONDITIONS**

<table>
<thead>
<tr>
<th>Register</th>
<th>Value loaded</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMAxSPTR&lt;21:0&gt;</td>
<td>DMAxSSA&lt;21:0&gt;</td>
</tr>
<tr>
<td>DMAxSCNT&lt;11:0&gt;</td>
<td>DMAxSSZ&lt;11:0&gt;</td>
</tr>
<tr>
<td>DMAxDPTR&lt;15:0&gt;</td>
<td>DMAxDA&lt;15:0&gt;</td>
</tr>
<tr>
<td>DMAxDCNT&lt;11:0&gt;</td>
<td>DMAxDA&lt;11:0&gt;</td>
</tr>
</tbody>
</table>

During the DMA Operation after each transaction, Table 15-4 and Table 15-5 indicate how the Source/Destination pointer and counter registers are modified.

**TABLE 15-4: DMA SOURCE POINTER/COUNTER DURING OPERATION**

<table>
<thead>
<tr>
<th>Register</th>
<th>Modified Source Counter/Pointer Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMAxSCNT&lt;11:0&gt; != 1</td>
<td>DMAxSCNT = DMAxSCNT -1</td>
</tr>
<tr>
<td></td>
<td>SMODE = 00: DMAxSPTR = DMAxSPTR</td>
</tr>
<tr>
<td></td>
<td>SMODE = 01: DMAxSPTR = DMAxSPTR + 1</td>
</tr>
<tr>
<td></td>
<td>SMODE = 10: DMAxSPTR = DMAxSPTR - 1</td>
</tr>
<tr>
<td>DMAxSCNT&lt;11:0&gt; == 1</td>
<td>DMAxSCNT = DMAxSSZ</td>
</tr>
<tr>
<td></td>
<td>DMAxSPTR = DMAxDA</td>
</tr>
</tbody>
</table>

**TABLE 15-5: DMA DESTINATION POINTER/COUNTER DURING OPERATION**

<table>
<thead>
<tr>
<th>Register</th>
<th>Modified Destination Counter/Pointer Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMAxDCNT&lt;11:0&gt; != 1</td>
<td>DMAxDCNT = DMAxDCNT -1</td>
</tr>
<tr>
<td></td>
<td>DMODE = 00: DMAxDPTR = DMAxDPTR</td>
</tr>
<tr>
<td></td>
<td>DMODE = 01: DMAxDPTR = DMAxDPTR + 1</td>
</tr>
<tr>
<td></td>
<td>DMODE = 10: DMAxDPTR = DMAxDPTR - 1</td>
</tr>
<tr>
<td>DMAxDCNT&lt;11:0&gt; == 1</td>
<td>DMAxDCNT = DMAxDA</td>
</tr>
<tr>
<td></td>
<td>DMAxDPTR = DMAxDA</td>
</tr>
</tbody>
</table>

The following sections discuss how to initiate and terminate DMA transfers.

15.5.1 STARTING DMA MESSAGE TRANSFERS

The DMA can initiate data transactions by either of the following two conditions:

1. User software control
2. Hardware trigger, SIRQ

**15.5.1.1 User Software Control**

Software starts or stops DMA transaction by setting/clearing the DGO bit. The DGO bit is also used to indicate whether a DMA hardware trigger has been received and a message is in progress.

**Note 1:** Software start can only occur if the EN bit (DMAxCON1) is set.

**Note 2:** If the CPU writes to the DGO bit while it is already set, there is no effect on the system, the DMA will continue to operate normally.
15.5.1.2 Hardware Trigger, SIRQ
A Hardware trigger is an interrupt request from another module sent to the DMA with the purpose of starting a DMA message. The DMA start trigger source is user selectable using the DMAxSIRQ register.

The SIRQEN bit (DMAxCON0 register) is used to enable sampling of external interrupt triggers by which a DMA transfer can be started. When set the DMA will sample the selected Interrupt source and when cleared, the DMA will ignore the selected Interrupt source. Clearing SIRQEN does not stop a DMA transaction currently progress, it only stops more hardware request signals from being received.

15.5.2 STOPPING DMA MESSAGE TRANSFERS
The DMA controller can stop data transactions by either of the following two conditions:
1. Clearing the DGO bit
2. Hardware trigger, AIRQ
3. Source Count reload
4. Destination Count reload
5. Clearing the Enable bit

15.5.2.1 User Software Control
If the user clears the DGO bit, the message will be stopped and the DMA will remain in the current configuration.

For example, if the user clears the DGO bit after source data has been read but before it is written to the destination, then the data in DMAxBUF will not reach its destination.

This is also referred to as a soft-stop as the operation can resume if desired by setting DGO bit again.

15.5.2.2 Hardware Trigger, AIRQ
The AIRQEN bit (DMAxCON0 register) is used to enable sampling of external interrupt triggers by which a DMA transaction can be aborted.

Once an Abort interrupt request has been received, the DMA will perform a soft-stop by clearing the DGO bit as well as clearing the SIRQEN bit so overruns do not occur. The AIRQEN bit is also cleared to prevent additional abort signals from triggering false aborts.

If desired, the DGO bit can be set again and the DMA will resume operation from where it left off after the soft-stop had occurred as none of the DMA state information is changed in the event of an abort.

15.5.2.3 Source Count Reload
A DMA message is considered to be complete when the Source count register is decremented from 1 and then reloaded (i.e., once the last byte from either the source read or destination write has occurred). When the SSTP bit is set (DMAxCON1 register) and the source count register is reloaded then further message transfer is stopped.

15.5.2.4 Destination Count Reload
A DMA message is considered to be complete when the Destination count register is decremented from 1 and then reloaded (i.e., once the last byte from either the source read or destination write has occurred). When the DSTP bit is set (DMAxCON1) and the destination count register is reloaded then further message transfer is stopped.

Note: Reading the DMAxSCNT or DMAxDCNT registers will never return zero. When either register is decremented from ‘1’ it is immediately reloaded from the corresponding size register.

15.5.2.5 Clearing the Enable bit
If the User clears the EN bit, the message will be stopped and the DMA will return to its default configuration. This is also referred to as a hard-stop as the DMA cannot resume operation from where it was stopped.

Note: After the DMA message transfer is stopped, it requires an extra instruction cycle before the Stop condition takes effect. Thus, after the Stop condition has occurred, a Source read or a Destination write can occur depending on the Source or Destination Bus availability.

15.5.3 DISABLE DMA MESSAGES TRANSFERS UPON COMPLETION
Once the DMA message is complete it may be desirable to disable the trigger source to prevent overrun or under run of data. This can be done by either of the following methods:
1. Clearing the SIRQEN bit
2. Setting the SSTP bit
3. Setting the DSTP bit
15.5.3.1 Clearing the SIRQEN bit

Clearing the SIRQEN bit (DMAxCON1 register) stops the sampling of external start interrupt triggers hence preventing further DMA Message transfers. An example would be a communications peripheral with a level-triggered interrupt. The peripheral will continue to request data (because its buffer is empty) even though there is no more data to be moved. Disabling the SIRQEN bit prevents the DMA from processing these requests.

15.5.3.2 Source/Destination Stop

The SSTP and DSTP bits (DMAxCON0 register) determine whether or not to disable the hardware triggers (SIRQEN = 0) once a DMA message has completed. When the SSTP bit is set and the DMAxSCNT = 0, then the SIRQEN bit will be cleared. Similarly, when the DSTP bit is set and the DMAxDCNT = 0, the SIRQEN bit will be cleared.

**Note:** The SSTP and DSTP bits are independent functions and do not depend on each other. It is possible for a message to be stopped by either counter at message end or both counters at message end.

15.6 Types of Hardware Triggers

The DMA has two different trigger inputs namely the Source trigger and the abort trigger. Each of these trigger sources is user configurable using the DMAxSIRQ and DMAxAIRQ registers.

Based on the source selected for each trigger, there are two types of requests that can be sent to the DMA.

- **Edge triggers**
- **Level triggers**

15.6.1 EDGE TRIGGER REQUESTS

An Edge request occurs only once when a given module interrupt requirements are true.

15.6.2 LEVEL TRIGGER REQUESTS

A level request is asserted as long as the condition that causes the interrupt is true.

15.7 Types of Data Transfers

Based on the memory access capabilities of the DMA (See Table 15-1), the following sections discuss the different types of data movement between the Source and Destination Memory regions.

- **N : 1**
  - This type of transfer is common when sending predefined data packets (such as strings) through a single interface point (such as communications modules transmit registers).

- **N : N**
  - This type of transfer is useful for moving information out of the Program Flash or Data EEPROM to SRAM for manipulation by the CPU or other peripherals.

- **1 : N**
  - This type of transfer is common when bridging two different modules data streams together (communications bridge).

- **1 : N**
  - This type of transfer is useful for moving information from a single data source into a memory buffer (communications receive registers).

15.8 DMA Interrupts

Each DMA has its own set of four interrupt flags, used to indicate a range of conditions during data transfers. The interrupt flag bits can be accessed using the corresponding PIR registers (Refer to the Interrupt Section).

15.8.1 DMA SOURCE COUNT INTERRUPT

The DMAxSCNTIF source count interrupt flag is set every time the DMAxSCNT<11:0> reaches zero and is reloaded to its starting value.

15.8.2 DMA DESTINATION COUNT INTERRUPT

The DMAxDCNTIF destination count interrupt flag is set every time the DMAxDCNT<11:0> reaches zero and is reloaded to its starting value.

The DMA Source Count zero and Destination Count zero interrupts are used in conjunction to determine when to signal the CPU when the DMA Messages are completed.

15.8.3 ABORT INTERRUPT

The DMAxAIF abort interrupt flag is used to signal that the DMA has halted activity due to an abort signal from one of the abort sources. This is used to indicate that the transaction has been halted for some reason.
15.8.4 OVERRUN INTERRUPT
When the DMA receives a trigger to start a new message before the current message is completed, then the DMAxORIF Overrun interrupt flag is set.
This condition indicates that the DMA is being requested before its current transaction is finished. This implies that the active DMA may not be able to keep up with the demands from the peripheral module being serviced, which may result in data loss.
The DMAxORIF flag being set does not cause the current DMA transfer to terminate.
The Overrun interrupt is only available for trigger sources that are edge based and not available for sources that are level-based. Therefore a level-based interrupt source does not trigger a DMA overrun error due to the potential latency issues in the system.
An example of an interrupt that could use the overrun interrupt would be a timer overflow (or period match) interrupt. This event only happens every time the timer rolls over and is not dependent on any other system conditions.
An example of an interrupt that does not allow the overrun interrupt would be the UARTTX buffer. The UART will continue to assert the interrupt until the DMA is able to process the MSG. Due to latency issues, the DMA may not be able to service an empty buffer immediately, but the UART continues to assert its transmit interrupt until it is serviced. If overrun was allowed in this case, the overrun would occur almost immediately as the module samples the interrupt sources every instruction cycle.

15.9 DMA Setup and Operation
The following steps illustrate how to configure the DMA for data transfer:
1. Program the appropriate Source and Destination addresses for the transaction into the DMAxSSA and DMAxDSA registers
2. Select the source memory region that is being addressed by DMAxSSA register, using the SMR<1:0> bits.
3. Program the SMode and DMode bits to select the addressing mode.
4. Program the Source size DMAxSSZ and Destination size DMAxDSZ registers with the number of bytes to be transferred. It is recommended for proper operation that the size registers be a multiple of each other.
5. If the user desires to disable data transfers once the message has completed, then the SSTP and DSTP bits in DMAxCON0 register need to be set.(see Section 15.5.3.2 “Source/Destination Stop”).
6. If using hardware triggers for data transfer, setup the hardware trigger interrupt sources for the starting and aborting DMA transfers (DMAxSIRQ and DMAxAIRQ), and set the corresponding interrupt request enable bits (SIRQEN and AIRQEN).
7. Select the priority level for the DMA (see Section 3.1 “System Arbitration”) and lock the priorities (see Section 3.1.1 “Priority Lock”)
8. Enable the DMA (DMAxCON1bits. EN = 1)
9. If using software control for data transfer, set the DGO bit, else this bit will be set by the hardware trigger.

Once the DMA is set up, the following flow chart describes the sequence of operation when the DMA uses hardware triggers and utilizes the unused CPU cycles (bubble) for DMA transfers.
Configure DMA Module

EN = 1

Load DMA Source/Destination Pointers & Counters

SIRQEN = 1 & Trigger?

DGO = 1

Bubble?

Source Read

DMAXBUF = &DMAXSPTR

N

 DMAxDPTR = DMABUF

Y

Update DMAxSSA, DMAxSCNT

DMAXSCNT = 0

Y

Reload DMAxSCNT & DMAxSPTR

DMAXSCNTIF = 1

DGO = 0

N

Update DMAxSSA, DMAxSCNT

DMAXDCNT = 0

Y

Reload DMAxDCNT & DMAxDPTR

DMAXDCNTIF = 1

DGO = 0

N

Update DMAxSSA, DMAxDCNT

DMAXDCNT = 0

N

DGO = 0

Y

End Process
The following sections describe with visual reference the sequence of events for different configurations of the DMA module.

15.9.1 SOURCE STOP

When the Source Stop bit is set (SSTP = 1) and the DMAxSCNT register reloads, the DMA clears the SIRQEN bit to stop receiving new start interrupt request signals and sets the DMAxSCNTIF flag.

FIGURE 15-5: GPR-GPR TRANSACTIONS WITH HARDWARE TRIGGERS, SSTP = 1

Note 1: SR – Source Read
Note 2: DW – Destination Write
15.9.2 DESTINATION STOP

When the Destination Stop bit is set (DSTP = 1) and the DMAxDCNT register reloads, the DMA clears the SIRQEN bit to stop receiving new start interrupt request signals and sets the DMAxDCNTIF flag.

**FIGURE 15-6: GPR-GPR TRANSACTIONS WITH HARDWARE TRIGGERS, DSTP = 1**

---

**Note 1:** SR – Source Read

**2:** DW – Destination Write
15.9.3 CONTINUOUS TRANSFER

When the Source or the Destination Stop bit is cleared (SSTP, DSTP = 0), the transactions continue unless cleared by the user. The DMAxSCNTIF and DMAxDCNTIF flags are set whenever the respective counter registers are reloaded.

FIGURE 15-7: GPR-GPR TRANSACTIONS WITH HARDWARE TRIGGERS, SSTP, DSTP = 0

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td></td>
</tr>
<tr>
<td>SIRQEN</td>
<td></td>
</tr>
<tr>
<td>Source</td>
<td></td>
</tr>
<tr>
<td>Hardware</td>
<td></td>
</tr>
<tr>
<td>Trigger</td>
<td></td>
</tr>
<tr>
<td>DGO</td>
<td></td>
</tr>
<tr>
<td>DMAxSPTR</td>
<td>0x100</td>
</tr>
<tr>
<td></td>
<td>0x101</td>
</tr>
<tr>
<td></td>
<td>0x100</td>
</tr>
<tr>
<td></td>
<td>0x100</td>
</tr>
<tr>
<td>DMAxDPTR</td>
<td>0x200</td>
</tr>
<tr>
<td></td>
<td>0x201</td>
</tr>
<tr>
<td></td>
<td>0x202</td>
</tr>
<tr>
<td></td>
<td>0x203</td>
</tr>
<tr>
<td>DMAxSCNT</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td>DMAxDCNT</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td>DMAxSTATE</td>
<td>IDLE</td>
</tr>
<tr>
<td></td>
<td>SR</td>
</tr>
<tr>
<td></td>
<td>DW</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>DMAxSCNTIF</td>
<td></td>
</tr>
<tr>
<td>DMAxDCNTIF</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: SR – Source Read
        2: DW – Destination Write
15.9.4 TRANSFER FROM SFR TO GPR

The following visual reference describes the sequence of events when copying ADC results to a GPR location. The ADC Interrupt Flag can be chosen as the Source Hardware trigger, the Source address can be set to point to the ADC Result registers at 3EEF, the Destination address can be set to point to any GPR location of our choice (Example 0x100).

FIGURE 15-8: SFR SPACE TO GPR SPACE TRANSFER

Note 1: SR – Source Read
2: DW – Destination Write
### 15.9.5 OVERRUN INTERRUPT

The Overrun Interrupt flag is set if the DMA receives a trigger to start a new message before the current message is completed.

#### FIGURE 15-9: OVERRUN INTERRUPT

<table>
<thead>
<tr>
<th>Instruction Clock</th>
<th>EN</th>
<th>SRQ2EN</th>
<th>Source Hardware Trigger</th>
<th>DGO</th>
<th>DMAxSPTR</th>
<th>DMAxDPTR</th>
<th>DMAxSCNT</th>
<th>DMAxDCNT</th>
<th>DMAxSTATE</th>
<th>DMAxSCNTIF</th>
<th>DMAxDCNTIF</th>
<th>DMAxORIF</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>4</td>
<td>0x100</td>
<td>0x200</td>
<td>2</td>
<td>2</td>
<td>IDLE</td>
<td>IDLE</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>3</td>
<td>0x101</td>
<td>0x201</td>
<td>1</td>
<td>1</td>
<td>SR1(1)</td>
<td>SR1(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>2</td>
<td>0x100</td>
<td>0x202</td>
<td>2</td>
<td>2</td>
<td>DW2(2)</td>
<td>DW2(2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>1</td>
<td>0x101</td>
<td>0x203</td>
<td>1</td>
<td>1</td>
<td>IDLE</td>
<td>IDLE</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>0</td>
<td>0x100</td>
<td>0x200</td>
<td>2</td>
<td>4</td>
<td>IDLE</td>
<td>IDLE</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:**
- SR – Source Read
- DW – Destination Write

**Note 2:**
- SR1(1)
- DW2(2)
15.9.6 ABORT TRIGGER, MESSAGE COMPLETE

The AIRQEN needs to be set in order for the DMA to sample Abort Interrupt sources. When an abort interrupt is received the SIRQEN bit is cleared and the AIRQEN bit is cleared to avoid receiving further abort triggers.

**FIGURE 15-10: ABORT AT THE END OF MESSAGE**

**Note 1:** SR – Source Read  
**Note 2:** DW – Destination Write
15.9.7 ABORT TRIGGER, MESSAGE IN PROGRESS

When an abort interrupt request is received in the between a DMA transaction, the DMA will perform a soft-stop by clearing the DGO (i.e., if the DMA was reading the source register, it will complete the read operation and then clear the DGO bit)

The SIRQEN bit is cleared to prevent any overrun and the AIRQEN bit is cleared to prevent any false aborts. When the DGO bit is set again the DMA will resume operation from where it left off after the soft-stop.

FIGURE 15-11: ABORT DURING MESSAGE TRANSFER

The following table contains some of the cases in which the DMA module can be configured to.

Note 1: SR – Source Read
Note 2: DW – Destination Write
<table>
<thead>
<tr>
<th>Source Module</th>
<th>Source Register(s)</th>
<th>Destination Module</th>
<th>Destination Register(s)</th>
<th>DCHxSIRQ</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal Measurement Timer (SMT)</td>
<td>SMTxCPW[U:H:L]</td>
<td>GPR</td>
<td>GPR[x,y,z]</td>
<td>SMTxPWAIF</td>
<td>Store Captured Pulse-width values</td>
</tr>
<tr>
<td></td>
<td>SMTxCPR[U:H:L]</td>
<td></td>
<td></td>
<td>SMTxPRAIF</td>
<td>Store Captured Period values</td>
</tr>
<tr>
<td>GPR/SFR/Program Flash/Data EEPROM</td>
<td>MEMORY[x,y]</td>
<td>TMR0</td>
<td>TMR0[H:L]</td>
<td>TMR0IF</td>
<td>Use as a Timer0 reload for custom 16-bit value</td>
</tr>
<tr>
<td>GPR/SFR/Program Flash/Data EEPROM</td>
<td>MEMORY[x]</td>
<td>TMR0</td>
<td>PR0</td>
<td>ANY</td>
<td>Update TMR0 frequency based on a specific trigger</td>
</tr>
<tr>
<td>GPR/SFR/Program Flash/Data EEPROM</td>
<td>MEMORY[x,y]</td>
<td>TMR1</td>
<td>TMR1[H:L]</td>
<td>TMR1IF</td>
<td>Use as a Timer1 reload for custom 16-bit value</td>
</tr>
<tr>
<td>TMR1</td>
<td>TMR1[H:L]</td>
<td>GPR</td>
<td>GPR[x,y]</td>
<td>TMR1IF</td>
<td>Use TMR1 Gate interrupt flag to read data out of TMR1 register</td>
</tr>
<tr>
<td>GPR/SFR/Program Flash/Data EEPROM</td>
<td>MEMORY[x]</td>
<td>TMR2</td>
<td>PR2</td>
<td>TMR2IF</td>
<td>Frequency generator with 50% duty cycle look up table</td>
</tr>
<tr>
<td>GPR/SFR/Program Flash/Data EEPROM</td>
<td>MEMORY[x,y,z]</td>
<td>TMR2</td>
<td>PR2</td>
<td>TMR2IF</td>
<td>Frequency generator with 50% duty cycle look up table</td>
</tr>
<tr>
<td>GPR/SFR/Program Flash/Data EEPROM</td>
<td>MEMORY[x,y,z,u,v,w]</td>
<td>CCP or PWM</td>
<td>CCPxR[H:L] or PWMDC[H:L]</td>
<td>ANY</td>
<td>Update multiple PWM values at the same time (e.g., 3-phase motor control)</td>
</tr>
<tr>
<td>GPR/SFR/Program Flash/Data EEPROM</td>
<td>MEMORY[x,y,z]</td>
<td>NCO</td>
<td>NCOxINC[U:H:L]</td>
<td>ANY</td>
<td>Frequency Generator look-up table</td>
</tr>
<tr>
<td>GPR/SFR/Program Flash/Data EEPROM</td>
<td>MEMORY[x]</td>
<td>DAC</td>
<td>DACxCON0</td>
<td>ANY</td>
<td>Update DAC values</td>
</tr>
<tr>
<td>GPR/SFR/Program Flash/Data EEPROM</td>
<td>MEMORY[x]</td>
<td>OSCTUNE</td>
<td>OSCTUNE</td>
<td>ANY</td>
<td>Automated Frequency dithering</td>
</tr>
</tbody>
</table>
15.10 Reset
The DMA registers are set to the default state on any Reset. The registers are also reset to the default state when the enable bit is cleared (DMA1CON1bits.EN=0).

15.11 Power Saving Mode Operation
The DMA utilizes system clocks and it is treated as a peripheral when it comes to power-saving operations. Like other peripherals, the DMA also uses Peripheral Module Disable bits to further tailor its operation in low-power states.

15.11.1 SLEEP MODE
When the device enters Sleep mode, the system clock to the module is shut down, therefore no DMA operation is supported in Sleep. Once the system clock is disabled, the requisite read and write clocks are also disabled without which the DMA cannot perform any of its tasks.

Any transfers that may be in progress are resumed on exiting from Sleep mode. Register contents are not affected by the device entering or leaving Sleep mode. It is recommended that DMA transactions be allowed to finish before entering Sleep mode.

15.11.2 IDLE MODE
In IDLE mode, all of the system clocks (including the read and write clocks) are still operating but the CPU is not using them to save power.

Therefore, every instruction cycle is available to the system arbiter and if the bubble is granted to the DMA, it may be utilized to move data.

15.11.3 DOZE MODE
Similar to the Idle mode, the CPU does not utilize all of the available instruction cycles slots that are available to it in order to save power. It only executes instructions based on its settings from the Doze settings.

Therefore, every instruction not used by the CPU is available for system arbitration and may be utilized by the DMA if granted by the arbiter.

15.11.4 PERIPHERAL MODULE DISABLE
The Peripheral Module Disable (PMD) registers provide a method to disable DMA by gating all clock sources supplied to it. The respective DMAXMD bit needs to be set in order to disable the DMA.

15.12 DMA Register Interfaces
The DMA can transfer data to any GPR or SFR location. For better user accessibility some of the more commonly used SFR spaces have their Mirror registers placed in Bank 64 (0x4000-0x40FF), these Mirror registers can be only accessed through the DMA Source and Destination Address registers.
EXAMPLE 15-1: SETUP DMA1 TO MOVE DATA FROM PROGRAM FLASH MEMORY TO UART1 TRANSMIT BUFFER USING HARDWARE TRIGGERS

//This code example illustrates using DMA1 to transfer 10 bytes of data from 0x1000 in PFM to U1TXB 0x3DEA

void main() {
    //System Initialize
    initializeSystem();

    //Setup UART1
    initializeUART1();

    //Setup DMA1
    //DMA1ICON1 - DPTR remains, Source Memory Region PFM, SPTR increments, SSTP
    DMA1ICON1 = 0x0B;

    //Source registers
    //Source size
    DMA1ISSZH = 0x00;
    DMA1ISSZL = 0x0A;

    //Source start address, 0x1000
    DMA1ISSAU = 0x00;
    DMA1ISSAH = 0x10;
    DMA1ISSAL = 0x00;

    //Destination registers
    //Destination size
    DMA1DSZH = 0x00;
    DMA1DSZL = 0x01;

    //Destination start address, 0x3DEA
    DMA1DSAH = 0x3D;
    DMA1DSAL = 0xEA;

    //Start trigger source U1TX
    DMA1SIRQ = 0x1C;

    //Enable & Start DMA transfer
    DMA1CON0 = 0xC0;
    
    while (1) {
        doSomething();
    }
}

15.13 Register definitions: DMA

Long bit name prefixes for the DMA peripherals are shown in Table 15-7. Refer to Section 1.3 “Register and Bit naming conventions” for more information.

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Bit Name Prefix</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMA 1</td>
<td>DMA1</td>
</tr>
<tr>
<td>DMA 2</td>
<td>DMA2</td>
</tr>
</tbody>
</table>
REGISTER 15-1: DMAxCON0: DMAx CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value at POR and BOR/Value at all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>EN: DMA Module Enable bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Enables module</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Disables module</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>SIRQEN: Start of Transfer Interrupt Request Enable bits</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Hardware triggers are allowed to start DMA transfers</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Hardware triggers are not allowed to start DMA transfers</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>DGO: DMA transaction bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = DMA transaction is in progress</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = DMA transaction is not in progress</td>
<td></td>
</tr>
<tr>
<td>4-3</td>
<td>Unimplemented: Read as ‘0’</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>AIRQEN: Abort of Transfer Interrupt Request Enable bits</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Hardware triggers are allowed to abort DMA transfers</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Hardware triggers are not allowed to abort DMA transfers</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Unimplemented: Read as ‘0’</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>XIP: Transfer in Progress Status bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = The DMAxBUF register currently holds contents from a read operation and has not transferred data to the destination.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = The DMAxBUF register is empty or has successfully transferred data to the destination address</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit       W = Writable bit       U = Unimplemented bit, read as ‘0’
-n/n = Value at POR and BOR/Value at all other Resets

0 = bit is cleared  x = bit is unknown  u = bit is unchanged
### REGISTER 15-2: DMAxCON1: DMAx CONTROL REGISTER1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Legend</th>
</tr>
</thead>
</table>
| 7-6 | DMODE<1:0> Destination Address Mode Selection    | R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'  
u = Bit is unchanged  
x = Bit is unknown  
-<n> = Value at POR and BOR/Value at all other Resets |
| 5   | DSTP Destination Counter Reload Stop bit         | 1 = SIRQEN bit is cleared when Destination Counter reloads  
0 = SIRQEN bit is not cleared when Destination Counter reloads |
| 4-3 | SMR<1:0> Source Memory Region Select bits         | 1x = DMAxSSA<21:0> points to Data EEPROM  
01 = DMAxSSA<21:0> points to Program Flash Memory  
00 = DMAxSSA<21:0> points to SFR/GPR Data Space |
| 2-1 | SMODE<1:0> Source Address Mode Selection bits     | 11 = Reserved, Do not use  
10 = DMAxSPTR<21:0> is decremented after each transfer completion  
01 = DMAxSPTR<21:0> is incremented after each transfer completion  
00 = DMAxSPTR<21:0> remains unchanged after each transfer completion |
| 0   | SSTP Source Counter Reload Stop bit              | 1 = SIRQEN bit is cleared when Source Counter reloads  
0 = SIRQEN bit is not cleared when Source Counter reloads |
**REGISTER 15-3: DMAxBUF: DMAx DATA BUFFER REGISTER**

<table>
<thead>
<tr>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BUF7</td>
<td>BUF6</td>
<td>BUF5</td>
<td>BUF4</td>
<td>BUF3</td>
<td>BUF2</td>
<td>BUF1</td>
<td>BUF0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- 
- -n/n = Value at POR
- and BOR/Value at all
- other Resets

- \(1\) = bit is set
- \(0\) = bit is cleared
- \(x\) = bit is unknown
- \(u\) = bit is unchanged

**bit 7-0 BUF<7:0>: DMA Internal Data Buffer bits**

DMABUF<7:0>

These bits reflect the content of the internal data buffer the DMA peripheral uses to hold the data being moved from the source to destination.

**REGISTER 15-4: DMAxSSAL: DMAx SOURCE START ADDRESS LOW REGISTER**

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSA&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- 
- -n/n = Value at POR
- and BOR/Value at all
- other Resets

- \(1\) = bit is set
- \(0\) = bit is cleared
- \(x\) = bit is unknown
- \(u\) = bit is unchanged

**bit 7-0 SSA<7:0>: Source Start Address bits**

**REGISTER 15-5: DMAxSSAH: DMAx SOURCE START ADDRESS HIGH REGISTER**

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSA&lt;15:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- 
- -n/n = Value at POR and
- BOR/Value at all other
- Resets

- \(1\) = bit is set
- \(0\) = bit is cleared
- \(x\) = bit is unknown
- \(u\) = bit is unchanged

**bit 7-0 SSA<15:8>: Source Start Address bits**
### REGISTER 15-6: DMAxSSAU: DMAx SOURCE START ADDRESS UPPER REGISTER

| bit 7-0 | SSA<21:16> | Source Start Address bits |

### REGISTER 15-7: DMAxSPTRL: DMAx SOURCE POINTER LOW REGISTER

| bit 7-0 | SPTR<7:0> | Current Source Address Pointer |

### REGISTER 15-8: DMAxSPTRH: DMAx SOURCE POINTER HIGH REGISTER

| bit 5-0 | SPTR<15:8> | Current Source Address Pointer |
### REGISTER 15-9: DMAxSPTRU: DMAx SOURCE POINTER UPPER REGISTER

<table>
<thead>
<tr>
<th>7-0</th>
<th>7-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td></td>
<td></td>
<td>SPTR&lt;21:16&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n/n** = Value at POR and BOR/Value at all other Resets
- 1 = bit is set
- 0 = bit is cleared
- x = bit is unknown
- u = bit is unchanged

- **bit 7-6 Unimplemented:** Read as ‘0’
- **bit 5-0 SPTR<21:16>:** Current Source Address Pointer

### REGISTER 15-10: DMAxSSZL: DMAx SOURCE SIZE LOW REGISTER

<table>
<thead>
<tr>
<th>7-0</th>
<th>7-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>SSZ&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n/n** = Value at POR and BOR/Value at all other Resets
- 1 = bit is set
- 0 = bit is cleared
- x = bit is unknown
- u = bit is unchanged

- **bit 7-0 SSZ<7:0>:** Source Message Size bits

### REGISTER 15-11: DMAxSSZH: DMAx SOURCE SIZE HIGH REGISTER

<table>
<thead>
<tr>
<th>7-0</th>
<th>7-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n/n** = Value at POR and BOR/Value at all other Resets
- 1 = bit is set
- 0 = bit is cleared
- x = bit is unknown
- u = bit is unchanged

- **bit 7-4 Unimplemented:** Read as ‘0’
- **bit 3-0 SSZ<11:8>:** Source Message Size bits
REGISTER 15-12: DMAxSCNTL: DMAx SOURCE COUNT LOW REGISTER

<table>
<thead>
<tr>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SCNT<7:0>

Legend:

R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
-n/n = Value at POR and BOR/Value at all other Resets
1 = bit is set  0 = bit is cleared  x = bit is unknown
u = bit is unchanged

bit 7-0  SCNT<7:0>: Current Source Byte Count

REGISTER 15-13: DMAxSCNTH: DMAx SOURCE COUNT HIGH REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SCNT<11:8>

Legend:

R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
-n/n = Value at POR and BOR/Value at all other Resets
1 = bit is set  0 = bit is cleared  x = bit is unknown
u = bit is unchanged

bit 7-4  Unimplemented: Read as ‘0’
bit 3-0  SCNT<11:8>: Current Source Byte Count

REGISTER 15-14: DMAxDSAL: DMAx DESTINATION START ADDRESS LOW REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

DSA<7:0>

Legend:

R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
-n/n = Value at POR and BOR/Value at all other Resets
1 = bit is set  0 = bit is cleared  x = bit is unknown
u = bit is unchanged

bit 7-0  DSA<7:0>: Destination Start Address bits
REGISTER 15-15: DMAxDSA: DMAx DESTINATION START ADDRESS HIGH REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>DSA&lt;15:8&gt;</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit       W = Writable bit       U = Unimplemented bit, read as ‘0’
-n/n = Value at POR and 1 = bit is set          0 = bit is cleared          x = bit is unknown
BOR/Value at all other    u = bit is unchanged

bit 7-0       DSA<15:8>: Destination Start Address bits

REGISTER 15-16: DMAxDPTR: DMAx DESTINATION POINTER LOW REGISTER

<table>
<thead>
<tr>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit       W = Writable bit       U = Unimplemented bit, read as ‘0’
-n/n = Value at POR and 1 = bit is set          0 = bit is cleared          x = bit is unknown
BOR/Value at all other    u = bit is unchanged

bit 7-0       DPTR<7:0>: Current Destination Address Pointer

REGISTER 15-17: DMAxDPTRH: DMAx DESTINATION POINTER HIGH REGISTER

<table>
<thead>
<tr>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit       W = Writable bit       U = Unimplemented bit, read as ‘0’
-n/n = Value at POR and 1 = bit is set          0 = bit is cleared          x = bit is unknown
BOR/Value at all other    u = bit is unchanged

bit 7-0       DPTR<15:8>: Current Destination Address Pointer
### PIC18(L)F25/26K83

**REGISTER 15-18: DMAxDSZL: DMAx DESTINATION SIZE LOW REGISTER**

<table>
<thead>
<tr>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DSZ&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **1** = bit is set
- **0** = bit is cleared
- **x** = bit is unknown
- **u** = bit is unchanged

**REGISTER 15-19: DMAxDSZH: DMAx DESTINATION SIZE HIGH REGISTER**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DSZ&lt;11:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **1** = bit is set
- **0** = bit is cleared
- **x** = bit is unknown
- **u** = bit is unchanged

**REGISTER 15-20: DMAxDCNTL: DMAx DESTINATION COUNT LOW REGISTER**

<table>
<thead>
<tr>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DCNT&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **1** = bit is set
- **0** = bit is cleared
- **x** = bit is unknown
- **u** = bit is unchanged

**bit 7-0** **DCNT<7:0>:** Current Destination Byte Count

**bit 7-0** **DSZ<7:0>:** Destination Message Size bits

**bit 3-0** **DSZ<11:8>:** Destination Message Size bits

**bit 7-0** **Unimplemented:** Read as ‘0’
### REGISTER 15-21: DMAxDCNTH: DMAx DESTINATION COUNT HIGH REGISTER

<table>
<thead>
<tr>
<th>bit 7-4</th>
<th>bit 3-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unimplemented: Read as '0'</td>
<td>DCNT&lt;11:8&gt;: Current Destination Byte Count</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **1** = bit is set
- **0** = bit is cleared
- **x** = bit is unknown
- **u** = bit is unchanged
- **-n/n** = Value at POR and BOR/Value at all other Resets

#### Bit 7-4
- **Unimplemented**: Read as '0'

#### Bit 3-0
- **DCNT<11:8>**: Current Destination Byte Count

### REGISTER 15-22: DMAxSIRQ: DMAx START INTERRUPT REQUEST SOURCE SELECTION REGISTER

<table>
<thead>
<tr>
<th>bit 7-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIRQ&lt;6:0&gt;: DMAx Start Interrupt Request Source Selection bits</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **1** = bit is set
- **0** = bit is cleared
- **x** = bit is unknown
- **u** = bit is unchanged
- **-n/n** = Value at POR and BOR/Value at all other Resets

#### Bit 7
- **Unimplemented**: Read as '0'

#### Bit 6-0
- **SIRQ<6:0>**: DMAx Start Interrupt Request Source Selection bits
  Please refer to Table 15-2 for more information.

### REGISTER 15-23: DMAxAIRQ: DMAx ABORT INTERRUPT REQUEST SOURCE SELECTION REGISTER

<table>
<thead>
<tr>
<th>bit 7-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>AIRQ&lt;6:0&gt;: DMAx Interrupt Request Source Selection bits</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **1** = bit is set
- **0** = bit is cleared
- **x** = bit is unknown
- **u** = bit is unchanged
- **-n/n** = Value at POR and BOR/Value at all other Resets

#### Bit 7
- **Unimplemented**: Read as '0'

#### Bit 6-0
- **AIRQ<6:0>**: DMAx Interrupt Request Source Selection bits
  Please refer to Table 15-2 for more information.
TABLE 15-2: DMAxSIRQ AND DMAxAIRQ INTERRUPT SOURCES

<table>
<thead>
<tr>
<th>DMAxSIRQ</th>
<th>Trigger Source</th>
<th>Level Triggered</th>
<th>DMAxSIRQ</th>
<th>Trigger Source</th>
<th>Level Triggered</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Reserved</td>
<td></td>
<td>42</td>
<td>DMA2SCNT</td>
<td>No</td>
</tr>
<tr>
<td>1</td>
<td>LVD</td>
<td>No</td>
<td>43</td>
<td>DMA2DCNT</td>
<td>No</td>
</tr>
<tr>
<td>2</td>
<td>OSF</td>
<td>No</td>
<td>44</td>
<td>DMA20R</td>
<td>No</td>
</tr>
<tr>
<td>3</td>
<td>CSW</td>
<td>No</td>
<td>45</td>
<td>DMA2A</td>
<td>No</td>
</tr>
<tr>
<td>4</td>
<td>NVM</td>
<td>No</td>
<td>46</td>
<td>I2C2RX</td>
<td>Yes</td>
</tr>
<tr>
<td>5</td>
<td>SCAN</td>
<td>No</td>
<td>47</td>
<td>I2C2TX</td>
<td>Yes</td>
</tr>
<tr>
<td>6</td>
<td>CRC</td>
<td>No</td>
<td>48</td>
<td>I2C2</td>
<td>Yes</td>
</tr>
<tr>
<td>7</td>
<td>IOC</td>
<td>Yes</td>
<td>49</td>
<td>I2C2E</td>
<td>Yes</td>
</tr>
<tr>
<td>8</td>
<td>INT0</td>
<td>No</td>
<td>50</td>
<td>U2RX</td>
<td>Yes</td>
</tr>
<tr>
<td>9</td>
<td>ZCD</td>
<td>No</td>
<td>51</td>
<td>U2TX</td>
<td>Yes</td>
</tr>
<tr>
<td>10</td>
<td>AD</td>
<td>No</td>
<td>52</td>
<td>U2E</td>
<td>Yes</td>
</tr>
<tr>
<td>11</td>
<td>ADT</td>
<td>No</td>
<td>53</td>
<td>U2</td>
<td>No</td>
</tr>
<tr>
<td>12</td>
<td>CMP1</td>
<td>No</td>
<td>54</td>
<td>TMR3</td>
<td>No</td>
</tr>
<tr>
<td>13</td>
<td>SMT1</td>
<td>No</td>
<td>55</td>
<td>TMR3G</td>
<td>No</td>
</tr>
<tr>
<td>14</td>
<td>SMT1PRA</td>
<td>No</td>
<td>56</td>
<td>TMR4</td>
<td>No</td>
</tr>
<tr>
<td>15</td>
<td>SMT1PWA</td>
<td>No</td>
<td>57</td>
<td>CCP2</td>
<td>No</td>
</tr>
<tr>
<td>16</td>
<td>DMA1SCNT</td>
<td>No</td>
<td>58</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>DMA1DCNT</td>
<td>No</td>
<td>59</td>
<td>CWG2</td>
<td>No</td>
</tr>
<tr>
<td>18</td>
<td>DMA1OR</td>
<td>No</td>
<td>60</td>
<td>CLC2</td>
<td>No</td>
</tr>
<tr>
<td>19</td>
<td>DMA1A</td>
<td>No</td>
<td>61</td>
<td>INT2</td>
<td>No</td>
</tr>
<tr>
<td>20</td>
<td>SPI1RX</td>
<td>Yes</td>
<td>62</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>SPI1TX</td>
<td>Yes</td>
<td>63</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>SPI1</td>
<td>Yes</td>
<td>64</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>I2C1RX</td>
<td>Yes</td>
<td>65</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>I2C1TX</td>
<td>Yes</td>
<td>66</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>I2C1</td>
<td>Yes</td>
<td>67</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>I2C1E</td>
<td>Yes</td>
<td>68</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>U1RX</td>
<td>Yes</td>
<td>69</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>U1TX</td>
<td>Yes</td>
<td>70</td>
<td>TMR5</td>
<td>No</td>
</tr>
<tr>
<td>29</td>
<td>U1E</td>
<td>Yes</td>
<td>71</td>
<td>TMR5G</td>
<td>No</td>
</tr>
<tr>
<td>30</td>
<td>U1</td>
<td>No</td>
<td>72</td>
<td>TMR6</td>
<td>No</td>
</tr>
<tr>
<td>31</td>
<td>TMR0</td>
<td>No</td>
<td>73</td>
<td>CCP3</td>
<td>No</td>
</tr>
<tr>
<td>32</td>
<td>TMR1</td>
<td>No</td>
<td>74</td>
<td>CWG3</td>
<td>No</td>
</tr>
<tr>
<td>33</td>
<td>TMR1G</td>
<td>No</td>
<td>75</td>
<td>CLC3</td>
<td>No</td>
</tr>
<tr>
<td>34</td>
<td>TMR2</td>
<td>No</td>
<td>76</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>CCP1</td>
<td>No</td>
<td>77</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>Reserved</td>
<td></td>
<td>78</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>NCO</td>
<td>No</td>
<td>79</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>CWG1</td>
<td>No</td>
<td>80</td>
<td>CCP4</td>
<td>No</td>
</tr>
<tr>
<td>39</td>
<td>CLC1</td>
<td>No</td>
<td>81</td>
<td>CLC4</td>
<td>No</td>
</tr>
<tr>
<td>40</td>
<td>INT1</td>
<td>No</td>
<td>82</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>CMP2</td>
<td>No</td>
<td>127</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** All trigger sources that are not Level-triggered are Edge-triggered.
### TABLE 15-3: SUMMARY OF REGISTERS ASSOCIATED WITH DMA

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMAxCON0</td>
<td>EN</td>
<td>SIRQEN</td>
<td>DGO</td>
<td>—</td>
<td>—</td>
<td>AIRQEN</td>
<td>—</td>
<td>XIP</td>
<td>238</td>
</tr>
<tr>
<td>DMAxCON1</td>
<td>DMODE&lt;1:0&gt;</td>
<td>DSTP</td>
<td>SMR&lt;1:0&gt;</td>
<td>SMODE&lt;1:0&gt;</td>
<td>SSTP</td>
<td></td>
<td></td>
<td></td>
<td>239</td>
</tr>
<tr>
<td>DMAxBUF</td>
<td>DBUF7</td>
<td>DBUF6</td>
<td>DBUF5</td>
<td>DBUF4</td>
<td>DBUF3</td>
<td>DBUF2</td>
<td>DBUF1</td>
<td>DBUF0</td>
<td>240</td>
</tr>
<tr>
<td>DMAxSSAL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SSA&lt;7:0&gt;</td>
<td></td>
<td></td>
<td>240</td>
</tr>
<tr>
<td>DMAxSSAH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SSA&lt;15:8&gt;</td>
<td></td>
<td></td>
<td>240</td>
</tr>
<tr>
<td>DMAxSSAU</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SSA&lt;21:16&gt;</td>
<td></td>
<td></td>
<td>241</td>
</tr>
<tr>
<td>DMAxSPTRL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SPTR&lt;7:0&gt;</td>
<td></td>
<td></td>
<td>241</td>
</tr>
<tr>
<td>DMAxSPTRH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SPTR&lt;15:8&gt;</td>
<td></td>
<td></td>
<td>241</td>
</tr>
<tr>
<td>DMAxSPTRU</td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SPTR&lt;21:16&gt;</td>
<td></td>
<td></td>
<td>242</td>
</tr>
<tr>
<td>DMAxSSAL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SSA&lt;7:0&gt;</td>
<td></td>
<td></td>
<td>242</td>
</tr>
<tr>
<td>DMAxSSAH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SSA&lt;15:8&gt;</td>
<td></td>
<td></td>
<td>242</td>
</tr>
<tr>
<td>DMAxSSZL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SSZ&lt;7:0&gt;</td>
<td></td>
<td></td>
<td>242</td>
</tr>
<tr>
<td>DMAxSSZH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SSZ&lt;11:8&gt;</td>
<td></td>
<td></td>
<td>242</td>
</tr>
<tr>
<td>DMAxSCNTL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SCNT&lt;7:0&gt;</td>
<td></td>
<td></td>
<td>243</td>
</tr>
<tr>
<td>DMAxSCNTH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SCNT&lt;11:8&gt;</td>
<td></td>
<td></td>
<td>243</td>
</tr>
<tr>
<td>DMAxDSAL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DSA&lt;7:0&gt;</td>
<td></td>
<td></td>
<td>243</td>
</tr>
<tr>
<td>DMAxDSAH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DSA&lt;15:8&gt;</td>
<td></td>
<td></td>
<td>244</td>
</tr>
<tr>
<td>DMAxDPTRL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DPTR&lt;7:0&gt;</td>
<td></td>
<td></td>
<td>244</td>
</tr>
<tr>
<td>DMAxDPTRH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DPTR&lt;15:8&gt;</td>
<td></td>
<td></td>
<td>244</td>
</tr>
<tr>
<td>DMAxDSZL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DSZ&lt;7:0&gt;</td>
<td></td>
<td></td>
<td>245</td>
</tr>
<tr>
<td>DMAxDSZH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DSZ&lt;11:8&gt;</td>
<td></td>
<td></td>
<td>245</td>
</tr>
<tr>
<td>DMAxDCNTL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DCNT&lt;7:0&gt;</td>
<td></td>
<td></td>
<td>245</td>
</tr>
<tr>
<td>DMAxDCNTH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DCNT&lt;11:8&gt;</td>
<td></td>
<td></td>
<td>246</td>
</tr>
<tr>
<td>DMAxSIRQ</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SIRQ&lt;6:0&gt;</td>
<td></td>
<td></td>
<td>246</td>
</tr>
<tr>
<td>DMAxAIRQ</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>AIRQ&lt;6:0&gt;</td>
<td></td>
<td></td>
<td>246</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by DMA.
16.0 I/O PORTS
The PIC18(L)F25/26K83 devices have four I/O ports, allocated as shown in Table 16-1.

<table>
<thead>
<tr>
<th>Device</th>
<th>PORTA</th>
<th>PORTB</th>
<th>PORTC</th>
<th>PORTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC18(L)F25K83</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>•(1)</td>
</tr>
<tr>
<td>PIC18(L)F26K83</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>•(1)</td>
</tr>
</tbody>
</table>

Note 1: Pin RE3 only.

Each port has ten registers to control the operation. These registers are:
- PORTx registers (reads the levels on the pins of the device)
- LATx registers (output latch)
- TRISx registers (data direction)
- ANSELx registers (analog select)
- WPUX registers (weak pull-up)
- INLVLx (input level control)
- SLRCONx registers (slew rate control)
- ODCONx registers (open-drain control)

Outside of registers to control bits of all the ports, the two following registers are also present:
- RxI2C (I2C pad control)

Most port pins share functions with device peripherals, both analog and digital. In general, when a peripheral is enabled on a port pin, that pin cannot be used as a general purpose output; however, the pin can still be read.

The Data Latch (LATx registers) is useful for read-modify-write operations on the value that the I/O pins are driving.

A write operation to the LATx register has the same effect as a write to the corresponding PORTx register. A read of the LATx register reads of the values held in the I/O PORT latches, while a read of the PORTx register reads the actual I/O pin value.

Ports that support analog inputs have an associated ANSELx register. When an ANSELx bit is set, the digital input buffer associated with that bit is disabled.

Disabling the input buffer prevents analog signal levels on the pin between a logic high and low from causing excessive current in the logic input circuitry. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 16.1.

16.1 GENERIC I/O PORT OPERATION

16.2 I/O Priorities
Each pin defaults to the PORT data latch after Reset. Other functions are selected with the peripheral pin select logic. See Section 17.0 “Peripheral Pin Select (PPS) Module” for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELx register. Digital output functions may continue to control the pin when it is in Analog mode.

Analog outputs, when enabled, take priority over digital outputs and force the digital output driver into a high-impedance state.

The pin function priorities are as follows:
1. Configuration bits
2. Analog outputs (disable the input buffers)
3. Analog inputs
4. Port inputs and outputs from PPS

16.3 PORTx Registers
In this section the generic names such as PORTx, LATx, TRISx, etc. can be associated with PORTA, PORTB, and PORTC ports. The functionality of PORTE is different compared to other ports and is explained in a separate section.
16.3.1 DATA REGISTER
PORTx is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISx (Register 16-2). Setting a TRISx bit (‘1’) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISx bit (‘0’) will make the corresponding PORTx pin an output (i.e., it enables output driver and puts the contents of the output latch on the selected pin). Example 16-1 shows how to initialize PORTx.

Example 16-1: Initializing PORTA

```assembly
BANKSEL PORTA ;
CLRF PORTA ; Init PORTA
BANKSEL LATA ; Data Latch
CLRF LATA ;
BANKSEL ANSELA ;
CLRF ANSELA ; digital I/O
BANKSEL TRISA ;
MOVLW B'11111000' ; Set RA<7:3> as inputs
MOVWF TRISA ; and set RA<2:0> as outputs
```

16.3.2 DIRECTION CONTROL
The TRISx register (Register 16-2) controls the PORTx pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISx register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

16.3.3 ANALOG CONTROL
The ANSELx register (Register 16-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELx bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELx bit has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note: The ANSELx bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

16.3.4 OPEN-DRAIN CONTROL
The ODCONx register (Register 16-6) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONx bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONx bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

Note: It is necessary to set open-drain control when using the pin for I2C.

16.3.5 SLEW RATE CONTROL
The SLRCONx register (Register 16-7) controls the slew rate option for each port pin. Slew rate for each port pin can be controlled independently. When an SLRCONx bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONx bit is cleared, the corresponding port pin drive slews at the maximum rate possible.
16.3.6 INPUT THRESHOLD CONTROL

The INLVLx register (Register 16-8) controls the input voltage threshold for each of the available PORTx input pins. A selection between the Schmitt Trigger CMOS or the TTL compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTx register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 45-4 for more information on threshold levels.

**Note:** Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

16.3.7 WEAK PULL-UP CONTROL

The WPUx register (Register 16-5) controls the individual weak pull-ups for each port pin.

16.3.8 EDGE SELECTABLE INTERRUPT-ON-CHANGE

An interrupt can be generated by detecting a signal at the port pin that has either a rising edge or a falling edge. Any individual pin can be configured to generate an interrupt. The interrupt-on-change module is present on all the pins of Ports B, C, E and on pin RG5. For further details about the IOC module refer to Section 18.0 “Interrupt-on-Change”.

16.3.9 I^2C PAD CONTROL

For the PIC18(L)F25/26K83 devices, the I^2C specific pads are available on RB1, RB2, RC3, RC4, RD0(1) and RD1(1) pins. The I^2C characteristics of each of these pins is controlled by the RxyI2C registers (see Register 16-9). These characteristics include enabling I^2C specific slew rate (over standard GPIO slew rate), selecting internal pull-ups for I^2C pins, and selecting appropriate input threshold as per SMBus specifications.

**Note 1:** RD0 and RD1 I^2C pads are not available in PIC18(L)F25K83 parts.

**Note 2:** Any peripheral using the I^2C pins read the I^2C ST inputs when enabled via RxyI2C.

16.4 PORTE Registers

16.4.1 MASTER CLEAR INPUT (MCLR)

For PIC18(L)F2xK83 devices, PORTE is only available when Master Clear functionality is disabled (MCLRE = 0). In this case, PORTE is a single bit, input-only port comprised of RE3 only. The pin operates as previously described. RE3 in PORTE register is a read-only bit and will read ‘1’ when MCLRE = 1 (i.e., Master Clear enabled).

16.4.2 RE3 WEAK PULL-UP

The port RE3 pin has an individually controlled weak internal pull-up. When set, the WPUE3 bit enables the RE3 pin pull-up. When the RE3 port pin is configured as MCLR, (CONFIG2L, MCLRE = 1 and CONFIG4H, LVP = 0), or configured for Low-Voltage Programming, (MCLRE = x and LVP = 1), the pull-up is always enabled and the WPUE3 bit has no effect.

16.4.3 INTERRUPT-ON-CHANGE

The interrupt-on-change feature is available only on the RE3 pin of PORTE for all devices. If MCLRE = 1 or LVP = 1, RE3 port functionality is disabled and interrupt-on-change on RE3 is not available. For further details refer to Section 18.0 “Interrupt-on-Change”.

Note: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

Note 1: RD0 and RD1 I^2C pads are not available in PIC18(L)F25K83 parts.

Note 2: Any peripheral using the I^2C pins read the I^2C ST inputs when enabled via RxyI2C.
16.5 Register Definitions: Port Control

REGISTER 16-1: PORTx: PORTx REGISTER(1)

<table>
<thead>
<tr>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rx7</td>
<td>Rx6</td>
<td>Rx5</td>
<td>Rx4</td>
<td>Rx3</td>
<td>Rx2</td>
<td>Rx1</td>
<td>Rx0</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown
-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0  \( Rx<7:0> \): Rx7:Rx0 Port I/O Value bits
1 = Port pin is \( \geq V_{IH} \)
0 = Port pin is \( \leq V_{IL} \)

Note 1: Writes to PORTx are actually written to the corresponding LATx register.
Reads from PORTx register return actual I/O pin values.

TABLE 16-2: PORT REGISTERS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PORTA</td>
<td>RA7</td>
<td>RA6</td>
<td>RA5</td>
<td>RA4</td>
<td>RA3</td>
<td>RA2</td>
<td>RA1</td>
<td>RA0</td>
</tr>
<tr>
<td>PORTB</td>
<td>RB7(1)</td>
<td>RB6(1)</td>
<td>RB5</td>
<td>RB4</td>
<td>RB3</td>
<td>RB2</td>
<td>RB1</td>
<td>RB0</td>
</tr>
<tr>
<td>PORTC</td>
<td>RC7</td>
<td>RC6</td>
<td>RC5</td>
<td>RC4</td>
<td>RC3</td>
<td>RC2</td>
<td>RC1</td>
<td>RC0</td>
</tr>
<tr>
<td>PORTE</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>RE3(2)</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Note 1: Bits RB6 and RB7 read ‘1’ while in Debug mode.
2: Bit PORTE3 is read-only, and will read ‘1’ when MCLRE = 1 (Master Clear enabled).
## REGISTER 16-2: TRISx: TRI-STATE CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRISx7</td>
<td>TRISx6</td>
<td>TRISx5</td>
<td>TRISx4</td>
<td>TRISx3</td>
<td>TRISx2</td>
<td>TRISx1</td>
<td>TRISx0</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- '1' = Bit is set
- '0' = Bit is cleared
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th>TRISx&lt;7:0&gt;: TRISx Port I/O Tri-state Control bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Port output driver is disabled</td>
</tr>
<tr>
<td>0</td>
<td>Port output driver is enabled</td>
</tr>
</tbody>
</table>

### TABLE 16-3: TRIS REGISTERS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRISA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
</tr>
<tr>
<td>TRISB</td>
<td>TRISB7(1)</td>
<td>TRISB6(1)</td>
<td>TRISB5</td>
<td>TRISB4</td>
<td>TRISB3</td>
<td>TRISB2</td>
<td>TRISB1</td>
<td>TRISB0</td>
</tr>
<tr>
<td>TRISC</td>
<td>TRISC7</td>
<td>TRISC6</td>
<td>TRISC5</td>
<td>TRISC4</td>
<td>TRISC3</td>
<td>TRISC2</td>
<td>TRISC1</td>
<td>TRISC0</td>
</tr>
</tbody>
</table>

**Note 1:** Bits RB6 and RB7 read '1' while in Debug mode.
REGISTER 16-3: LATx: LATx REGISTER(1)

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>LATx7</td>
<td>LATx6</td>
<td>LATx5</td>
<td>LATx4</td>
<td>LATx3</td>
<td>LATx2</td>
<td>LATx1</td>
<td>LATx0</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets

Note 1: Writes to LATx are equivalent with writes to the corresponding PORTx register. Reads from LATx register return register values, not I/O pin values.

TABLE 16-4: LAT REGISTERS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>LATA</td>
<td>LATA7</td>
<td>LATA6</td>
<td>LATA5</td>
<td>LATA4</td>
<td>LATA3</td>
<td>LATA2</td>
<td>LATA1</td>
<td>LATA0</td>
</tr>
<tr>
<td>LATB</td>
<td>LATB7</td>
<td>LATB6</td>
<td>LATB5</td>
<td>LATB4</td>
<td>LATB3</td>
<td>LATB2</td>
<td>LATB1</td>
<td>LATB0</td>
</tr>
<tr>
<td>LATC</td>
<td>LATC7</td>
<td>LATC6</td>
<td>LATC5</td>
<td>LATC4</td>
<td>LATC3</td>
<td>LATC2</td>
<td>LATC1</td>
<td>LATC0</td>
</tr>
</tbody>
</table>
REGISTER 16-4: ANSELx: ANALOG SELECT REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSELA</td>
<td>ANSELA7</td>
<td>ANSELA6</td>
<td>ANSELA5</td>
<td>ANSELA4</td>
<td>ANSELA3</td>
<td>ANSELA2</td>
<td>ANSELA1</td>
</tr>
<tr>
<td>ANSELB</td>
<td>ANSELB7</td>
<td>ANSELB6</td>
<td>ANSELB5</td>
<td>ANSELB4</td>
<td>ANSELB3</td>
<td>ANSELB2</td>
<td>ANSELB1</td>
</tr>
<tr>
<td>ANSELC</td>
<td>ANSELC7</td>
<td>ANSELC6</td>
<td>ANSELC5</td>
<td>ANSELC4</td>
<td>ANSELC3</td>
<td>ANSELC2</td>
<td>ANSELC1</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set  
‘0’ = Bit is cleared  
x = Bit is unknown
-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0  
\( \text{ANSELx}<7:0> \): Analog Select on Pins Rx<7:0>
1 = Digital Input buffers are disabled.
0 = ST and TTL input devices are enabled

TABLE 16-5: ANALOG SELECT PORT REGISTERS
REGISTER 16-5:  WPUx: WEAK PULL-UP REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>WPUx7</td>
<td>WPUx6</td>
<td>WPUx5</td>
<td>WPUx4</td>
<td>WPUx3</td>
<td>WPUx2</td>
<td>WPUx1</td>
<td>WPUx0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown
-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0  WPUx<7:0>: Weak Pull-up PORTx Control bits
1 = Weak Pull-up enabled
0 = Weak Pull-up disabled

TABLE 16-6:  WEAK PULL-UP PORT REGISTERS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>WPUA</td>
<td>WPUA7</td>
<td>WPUA6</td>
<td>WPUA5</td>
<td>WPUA4</td>
<td>WPUA3</td>
<td>WPUA2</td>
<td>WPUA1</td>
<td>WPUA0</td>
</tr>
<tr>
<td>WPUB</td>
<td>WPUB7</td>
<td>WPUB6</td>
<td>WPUB5</td>
<td>WPUB4</td>
<td>WPUB3</td>
<td>WPUB2</td>
<td>WPUB1</td>
<td>WPUB0</td>
</tr>
<tr>
<td>WPUC</td>
<td>WPUC7</td>
<td>WPUC6</td>
<td>WPUC5</td>
<td>WPUC4</td>
<td>WPUC3</td>
<td>WPUC2</td>
<td>WPUC1</td>
<td>WPUC0</td>
</tr>
<tr>
<td>WPUE</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WPUE3(1)</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Note 1:  If MCLRE = 1, the weak pull-up in RE3 is always enabled; bit WPUE3 is not affected.
REGISTER 16-6:  ODCNx: OPEN-DRAIN CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ODCx7</td>
<td>ODCx6</td>
<td>ODCx5</td>
<td>ODCx4</td>
<td>ODCx3</td>
<td>ODCx2</td>
<td>ODCx1</td>
<td>ODCx0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
1 = Bit is set  0 = Bit is cleared  x = Bit is unknown
-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0  ODCx<7:0>: Open-Drain Configuration on Pins Rx<7:0>
1 = Output drives only low-going signals (sink current only)
0 = Output drives both high-going and low-going signals (source and sink current)

TABLE 16-7: OPEN-DRAIN CONTROL REGISTERS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ODCONA</td>
<td>ODCA7</td>
<td>ODCA6</td>
<td>ODCA5</td>
<td>ODCA4</td>
<td>ODCA3</td>
<td>ODCA2</td>
<td>ODCA1</td>
<td>ODCA0</td>
</tr>
<tr>
<td>ODCONB</td>
<td>ODCB7</td>
<td>ODCB6</td>
<td>ODCB5</td>
<td>ODCB4</td>
<td>ODCB3</td>
<td>ODCB2</td>
<td>ODCB1</td>
<td>ODCB0</td>
</tr>
<tr>
<td>ODCONC</td>
<td>ODCC7</td>
<td>ODCC6</td>
<td>ODCC5</td>
<td>ODCC4</td>
<td>ODCC3</td>
<td>ODCC2</td>
<td>ODCC1</td>
<td>ODCC0</td>
</tr>
</tbody>
</table>
REGISTER 16-7:  SLRCONx: SLEW RATE CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLRCONA</td>
<td>SLRA7</td>
<td>SLRA6</td>
<td>SLRA5</td>
<td>SLRA4</td>
<td>SLRA3</td>
<td>SLRA2</td>
<td>SLRA1</td>
</tr>
<tr>
<td>SLRCONB</td>
<td>SLRB7</td>
<td>SLRB6</td>
<td>SLRB5</td>
<td>SLRB4</td>
<td>SLRB3</td>
<td>SLRB2</td>
<td>SLRB1</td>
</tr>
<tr>
<td>SLRCONC</td>
<td>SLRC7</td>
<td>SLRC6</td>
<td>SLRC5</td>
<td>SLRC4</td>
<td>SLRC3</td>
<td>SLRC2</td>
<td>SLRC1</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets

bit 7-0  \( SLR_{x<7:0>} \): Slew Rate Control on Pins \( Rx<7:0> \), respectively

\[ 1 = \text{Port pin slew rate is limited} \]
\[ 0 = \text{Port pin slews at maximum rate} \]
### REGISTER 16-8: INLVLx: INPUT LEVEL CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>INLVLx7</td>
<td>INLVLx6</td>
<td>INLVLx5</td>
<td>INLVLx4</td>
<td>INLVLx3</td>
<td>INLVLx2</td>
<td>INLVLx1</td>
<td>INLVLx0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>INLVLx&lt;7:0&gt;: Input Level Select on Pins Rx&lt;7:0&gt;, respectively</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ST input used for port reads and interrupt-on-change</td>
</tr>
<tr>
<td>0</td>
<td>TTL input used for port reads and interrupt-on-change</td>
</tr>
</tbody>
</table>

### TABLE 16-9: INPUT LEVEL PORT REGISTERS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>INLVLxA</td>
<td>INLVLx7</td>
<td>INLVLx6</td>
<td>INLVLx5</td>
<td>INLVLx4</td>
<td>INLVLx3</td>
<td>INLVLx2</td>
<td>INLVLx1</td>
<td>INLVLx0</td>
</tr>
<tr>
<td>INLVLxB</td>
<td>INLVLx7</td>
<td>INLVLx6</td>
<td>INLVLx5</td>
<td>INLVLx4</td>
<td>INLVLx3</td>
<td>INLVLx2</td>
<td>INLVLx1</td>
<td>INLVLx0</td>
</tr>
<tr>
<td>INLVLxB</td>
<td>INLVLx7</td>
<td>INLVLx6</td>
<td>INLVLx5</td>
<td>INLVLx4</td>
<td>INLVLx3</td>
<td>INLVLx2</td>
<td>INLVLx1</td>
<td>INLVLx0</td>
</tr>
<tr>
<td>INLVLxL</td>
<td>INLVLx7</td>
<td>INLVLx6</td>
<td>INLVLx5</td>
<td>INLVLx4</td>
<td>INLVLx3</td>
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<td>INLVLx0</td>
</tr>
<tr>
<td>INLVLxE</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Note 1:** Any peripheral using the I^2^C pins read the I^2^C ST inputs when enabled via Rx^I^2^C^.

**Note 2:** Unimplemented in PIC18(L)F25K83.
REGISTER 16-9: RxyI2C: I2C PAD Rxy CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>—</td>
<td>SLEW</td>
<td>PU&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TH&lt;1:0&gt;</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
u = Bit is unchanged
x = Bit is unknown
-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set
‘0’ = Bit is cleared
HS = Hardware set

bit 7 Unimplemented: Read as ‘0’

bit 6
SLEW: I2C Specific Slew Rate Limiting is Enabled
1 = I2C specific slew rate limiting is enabled. Standard pad slew limiting is disabled. The SLRxy bit is ignored.
0 = Standard GPIO Slew Rate; enabled/disabled via SLRxy bit.

bit 5-4
PU<1:0>: I2C Pull-up Selection bits
11 = Reserved
10 = 10x current of standard weak pull-up
01 = 2x current of standard weak pull-up
00 = Standard GPIO weak pull-up, enabled via WPUxy bit

bit 3-2 Unimplemented: Read as ‘0’

bit 1-0
TH<1:0>: I2C Input Threshold Selection bits
11 = SMBus 3.0 (1.35 V) input threshold
10 = SMBus 2.0 (2.1 V) input threshold
01 = I2C specific input thresholds
00 = Standard GPIO Input pull-up, enabled via INLVLxy registers

TABLE 16-10: I2C PAD CONTROL REGISTERS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RB1I2C</td>
<td>—</td>
<td>SLEW</td>
<td>PU&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TH&lt;1:0&gt;</td>
<td></td>
</tr>
<tr>
<td>RB2I2C</td>
<td>—</td>
<td>SLEW</td>
<td>PU&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TH&lt;1:0&gt;</td>
<td></td>
</tr>
<tr>
<td>RC3I2C</td>
<td>—</td>
<td>SLEW</td>
<td>PU&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TH&lt;1:0&gt;</td>
<td></td>
</tr>
<tr>
<td>RC4I2C</td>
<td>—</td>
<td>SLEW</td>
<td>PU&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TH&lt;1:0&gt;</td>
<td></td>
</tr>
</tbody>
</table>
TABLE 16-11: SUMMARY OF REGISTERS ASSOCIATED WITH I/O

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>PORTA</td>
<td>RA7</td>
<td>RA6</td>
<td>RA5</td>
<td>RA4</td>
<td>RA3</td>
<td>RA2</td>
<td>RA1</td>
<td>RA0</td>
<td>252</td>
</tr>
<tr>
<td>PORTB</td>
<td>RB7(1)</td>
<td>RB6(1)</td>
<td>RB5</td>
<td>RB4</td>
<td>RB3</td>
<td>RB2</td>
<td>RB1</td>
<td>RB0</td>
<td>252</td>
</tr>
<tr>
<td>PORTC</td>
<td>RC7</td>
<td>RC6</td>
<td>RC5</td>
<td>RC4</td>
<td>RC3</td>
<td>RC2</td>
<td>RC1</td>
<td>RC0</td>
<td>252</td>
</tr>
<tr>
<td>PORTE</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>RE3(2)</td>
<td>—</td>
<td>—</td>
<td>252</td>
</tr>
<tr>
<td>TRISA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td>253</td>
</tr>
<tr>
<td>TRISB</td>
<td>TRISB7(3)</td>
<td>TRISB6(3)</td>
<td>TRISB5</td>
<td>TRISB4</td>
<td>TRISB3</td>
<td>TRISB2</td>
<td>TRISB1</td>
<td>TRISB0</td>
<td>253</td>
</tr>
<tr>
<td>TRISC</td>
<td>TRISC7</td>
<td>TRISC6</td>
<td>TRISC5</td>
<td>TRISC4</td>
<td>TRISC3</td>
<td>TRISC2</td>
<td>TRISC1</td>
<td>TRISC0</td>
<td>253</td>
</tr>
<tr>
<td>LATA</td>
<td>LATA7</td>
<td>LATA6</td>
<td>LATA5</td>
<td>LATA4</td>
<td>LATA3</td>
<td>LATA2</td>
<td>LATA1</td>
<td>LATA0</td>
<td>254</td>
</tr>
<tr>
<td>LATB</td>
<td>LATB7</td>
<td>LATB6</td>
<td>LATB5</td>
<td>LATB4</td>
<td>LATB3</td>
<td>LATB2</td>
<td>LATB1</td>
<td>LATB0</td>
<td>254</td>
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<tr>
<td>LATC</td>
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<td>LATC6</td>
<td>LATC5</td>
<td>LATC4</td>
<td>LATC3</td>
<td>LATC2</td>
<td>LATC1</td>
<td>LATC0</td>
<td>254</td>
</tr>
<tr>
<td>ANSELA</td>
<td>ANSELA7</td>
<td>ANSELA6</td>
<td>ANSELA5</td>
<td>ANSELA4</td>
<td>ANSELA3</td>
<td>ANSELA2</td>
<td>ANSELA1</td>
<td>ANSELA0</td>
<td>255</td>
</tr>
<tr>
<td>ANSELB</td>
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<td>ANSELB6</td>
<td>ANSELB5</td>
<td>ANSELB4</td>
<td>ANSELB3</td>
<td>ANSELB2</td>
<td>ANSELB1</td>
<td>ANSELB0</td>
<td>255</td>
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<tr>
<td>ANSELC</td>
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<td>ANSELC6</td>
<td>ANSELC5</td>
<td>ANSELC4</td>
<td>ANSELC3</td>
<td>ANSELC2</td>
<td>ANSELC1</td>
<td>ANSELC0</td>
<td>255</td>
</tr>
<tr>
<td>WPUA</td>
<td>WPUA7</td>
<td>WPUA6</td>
<td>WPUA5</td>
<td>WPUA4</td>
<td>WPUA3</td>
<td>WPUA2</td>
<td>WPUA1</td>
<td>WPUA0</td>
<td>256</td>
</tr>
<tr>
<td>WPUB</td>
<td>WPUB7</td>
<td>WPUB6</td>
<td>WPUB5</td>
<td>WPUB4</td>
<td>WPUB3</td>
<td>WPUB2</td>
<td>WPUB1</td>
<td>WPUB0</td>
<td>256</td>
</tr>
<tr>
<td>WPUC</td>
<td>WPUC7</td>
<td>WPUC6</td>
<td>WPUC5</td>
<td>WPUC4</td>
<td>WPUC3</td>
<td>WPUC2</td>
<td>WPUC1</td>
<td>WPUC0</td>
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<td>WPUE</td>
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<td>—</td>
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<td>WPUE3(4)</td>
<td>—</td>
<td>—</td>
<td>256</td>
</tr>
<tr>
<td>ODCONA</td>
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<td>ODCA6</td>
<td>ODCA5</td>
<td>ODCA4</td>
<td>ODCA3</td>
<td>ODCA2</td>
<td>ODCA1</td>
<td>ODCA0</td>
<td>257</td>
</tr>
<tr>
<td>ODCONB</td>
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<td>ODCB6</td>
<td>ODCB5</td>
<td>ODCB4</td>
<td>ODCB3</td>
<td>ODCB2</td>
<td>ODCB1</td>
<td>ODCB0</td>
<td>257</td>
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<tr>
<td>ODCONC</td>
<td>ODCC7</td>
<td>ODCC6</td>
<td>ODCC5</td>
<td>ODCC4</td>
<td>ODCC3</td>
<td>ODCC2</td>
<td>ODCC1</td>
<td>ODCC0</td>
<td>257</td>
</tr>
<tr>
<td>SLRCONA</td>
<td>SLRA7</td>
<td>SLRA6</td>
<td>SLRA5</td>
<td>SLRA4</td>
<td>SLRA3</td>
<td>SLRA2</td>
<td>SLRA1</td>
<td>SLRA0</td>
<td>258</td>
</tr>
<tr>
<td>SLRCONB</td>
<td>SLRB7</td>
<td>SLRB6</td>
<td>SLRB5</td>
<td>SLRB4</td>
<td>SLRB3</td>
<td>SLRB2</td>
<td>SLRB1</td>
<td>SLRB0</td>
<td>258</td>
</tr>
<tr>
<td>SLRCONC</td>
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<td>SLRC6</td>
<td>SLRC5</td>
<td>SLRC4</td>
<td>SLRC3</td>
<td>SLRC2</td>
<td>SLRC1</td>
<td>SLRC0</td>
<td>258</td>
</tr>
<tr>
<td>INLVLA</td>
<td>INLVLA7</td>
<td>INLVLA6</td>
<td>INLVLA5</td>
<td>INLVLA4</td>
<td>INLVLA3</td>
<td>INLVLA2</td>
<td>INLVLA1</td>
<td>INLVLA0</td>
<td>259</td>
</tr>
<tr>
<td>INLVLB</td>
<td>INLVLB7</td>
<td>INLVLB6</td>
<td>INLVLB5</td>
<td>INLVLB4</td>
<td>INLVLB3</td>
<td>INLVLB2(5)</td>
<td>INLVLB1(5)</td>
<td>INLVLB0</td>
<td>259</td>
</tr>
<tr>
<td>INLVLC</td>
<td>INLVLC7</td>
<td>INLVLC6</td>
<td>INLVLC5</td>
<td>INLVLC4(5)</td>
<td>INLVLC3(5)</td>
<td>INLVLC2</td>
<td>INLVLC1</td>
<td>INLVLC0</td>
<td>259</td>
</tr>
<tr>
<td>INLVLE</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>INLVLE3</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>259</td>
</tr>
<tr>
<td>RB1I2C</td>
<td>—</td>
<td>SLEW</td>
<td>PU&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TH&lt;1:0&gt;</td>
<td>—</td>
<td>260</td>
</tr>
<tr>
<td>RB2I2C</td>
<td>—</td>
<td>SLEW</td>
<td>PU&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TH&lt;1:0&gt;</td>
<td>—</td>
<td>260</td>
</tr>
<tr>
<td>RC3I2C</td>
<td>—</td>
<td>SLEW</td>
<td>PU&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TH&lt;1:0&gt;</td>
<td>—</td>
<td>260</td>
</tr>
<tr>
<td>RC4I2C</td>
<td>—</td>
<td>SLEW</td>
<td>PU&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TH&lt;1:0&gt;</td>
<td>—</td>
<td>260</td>
</tr>
</tbody>
</table>

Legend:      — = unimplemented location, read as ‘0’. Shaded cells are not used by I/O Ports.

Note 1: Bits RB6 and RB7 read ‘1’ while in Debug mode.
2: Bit PORTE3 is read-only, and will read ‘1’ when MCLRE = 1 (Master Clear enabled).
3: Bits RB6 and RB7 read ‘1’ while in Debug mode.
4: If MCLRE = 1, the weak pull-up in RE3 is always enabled; bit WPUE3 is not affected.
5: Any peripheral using the I2C pins read the I2C ST inputs when enabled via RxyI2C.
17.0 PERIPHERAL PIN SELECT (PPS) MODULE

The Peripheral Pin Select (PPS) module connects peripheral inputs and outputs to the device I/O pins. Only digital signals are included in the selections. All analog inputs and outputs remain fixed to their assigned pins. Input and output selections are independent as shown in the simplified block diagram Figure 17-1.

The peripheral input is selected with the peripheral xxxPPS register (Register 17-1), and the peripheral output is selected with the PORT RxyPPS register (Register 17-2). For example, to select PORTC<7> as the UART1 RX input, set U1RXPPS to 0b1 0111, and to select PORTC<6> as the UART1 TX output set RC6PPS to 0b01 0011.

17.1 PPS Inputs

Each peripheral has a PPS register with which the inputs to the peripheral are selected. Inputs include the device pins.

Multiple peripherals can operate from the same source simultaneously. Port reads always return the pin level regardless of peripheral PPS selection. If a pin also has analog functions associated, the ANSEL bit for that pin must be cleared to enable the digital input buffer.

Although every peripheral has its own PPS input selection register, the selections are identical for every peripheral as shown in Register 17-1.

**Note:** The notation “xxx” in the register name is a place holder for the peripheral identifier. For example, INTOPPS.

17.2 PPS Outputs

Each I/O pin has a PPS register with which the pin output source is selected. With few exceptions, the port TRIS control associated with that pin retains control over the pin output driver. Peripherals that control the pin output driver as part of the peripheral operation will override the TRIS control as needed. These peripherals include:

- UART

Although every pin has its own PPS peripheral selection register, the selections are identical for every pin as shown in Register 17-2.

**Note:** The notation “Rxy” is a place holder for the pin identifier. For example, RA0PPS.
17.3 Bidirectional Pins

PPS selections for peripherals with bidirectional signals on a single pin must be made so that the PPS input and PPS output select the same pin. Peripherals that have bidirectional signals include:

- I²C

Note: Refer to Table 17-1 for pins that are I²C compatible. Clock and data signals can be routed to any pin, however pins without I²C compatibility will operate at standard TTL/ST logic levels as selected by the INVLV register.

17.4 PPS Lock

The PPS includes a mode in which all input and output selections can be locked to prevent inadvertent changes. PPS selections are locked by setting the PPSLOCKED bit of the PPSLOCK register. Setting and clearing this bit requires a special sequence as an extra precaution against inadvertent changes. Examples of setting and clearing the PPSLOCKED bit are shown in Example 17-1.

EXAMPLE 17-1: PPS LOCK SEQUENCE

```
; Disable interrupts:
BCF INTCON0,GIE

; Bank to PPSLOCK register
BANKSEL PPSLOCK
MOVLB PPSLOCK
MOVLW 55h

; Required sequence, next 4 instructions
MOVF PPSLOCK
MOVLW AAh
MOVF PPSLOCK

; Set PPSLOCKED bit to disable writes
; Only a BSF instruction will work
BSF PPSLOCK,0

; Enable Interrupts
BSF INTCON0,GIE
```

17.5 PPS One-way Lock

When this bit is set, the PPSLOCKED bit can only be cleared and set one time after a device Reset. This allows for clearing the PPSLOCKED bit so that the input and output selections can be made during initialization. When the PPSLOCKED bit is set after all selections have been made, it will remain set and cannot be cleared until after the next device Reset event.

17.6 Operation During Sleep

PPS input and output selections are unaffected by Sleep.

17.7 Effects of a Reset

A device Power-on-Reset (POR) clears all PPS input and output selections to their default values. All other Resets leave the selections unchanged. Default input selections are shown in pin allocation Table 3. The PPS one-way lock is also removed.
17.8 Register Definitions: PPS Input Selection

**REGISTER 17-1: xxxPPS: PERIPHERAL xxx INPUT SELECTION**

| bit 7-6 | Unimplemented: Read as ‘0’ |
| bit 5-3 | xxxPPS<5:3>: Peripheral xxx Input PORTx Pin Selection bits |
| See Table 17-1 for the list of available ports and default pin locations. |
| 111 = Peripheral input is from PORTx Pin 7 (Rx7) |
| 110 = Peripheral input is from PORTx Pin 6 (Rx6) |
| 101 = Peripheral input is from PORTx Pin 5 (Rx5) |
| 100 = Peripheral input is from PORTx Pin 4 (Rx4) |
| 011 = Peripheral input is from PORTx Pin 3 (Rx3) |
| 010 = Peripheral input is from PORTx Pin 2 (Rx2) |
| 001 = Peripheral input is from PORTx Pin 1 (Rx1) |
| 000 = Peripheral input is from PORTx Pin 0 (Rx0) |

| bit 2-0 | xxxPPS<2:0>: Peripheral xxx Input PORTx Pin Selection bits |
| 111 = Peripheral input is from PORTx Pin 7 (Rx7) |
| 110 = Peripheral input is from PORTx Pin 6 (Rx6) |
| 101 = Peripheral input is from PORTx Pin 5 (Rx5) |
| 100 = Peripheral input is from PORTx Pin 4 (Rx4) |
| 011 = Peripheral input is from PORTx Pin 3 (Rx3) |
| 010 = Peripheral input is from PORTx Pin 2 (Rx2) |
| 001 = Peripheral input is from PORTx Pin 1 (Rx1) |
| 000 = Peripheral input is from PORTx Pin 0 (Rx0) |

**Note 1:** The Reset value ‘m’ of this register is determined by device default locations for that input.

---

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **u** = Bit is unchanged
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets
- **x** = Bit is unknown
- **U** = Unimplemented bit, read as ‘0’
- **q** = value depends on peripheral
- **m** = value depends on default location for that input

---

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>xxxPPS&lt;5:0&gt;</td>
<td>xxxPPS&lt;5:0&gt;</td>
</tr>
</tbody>
</table>
### TABLE 17-1: PPS INPUT REGISTER DETAILS

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>PPS Input Register</th>
<th>Default Pin Selection at POR</th>
<th>Register Reset Value at POR</th>
<th>Input Available from Selected PORTx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupt 0</td>
<td>INT0PPS</td>
<td>RB0</td>
<td>0b0 1000</td>
<td>A B —</td>
</tr>
<tr>
<td>Interrupt 1</td>
<td>INT1PPS</td>
<td>RB1</td>
<td>0b0 1001</td>
<td>A B —</td>
</tr>
<tr>
<td>Interrupt 2</td>
<td>INT2PPS</td>
<td>RB2</td>
<td>0b0 1010</td>
<td>A B —</td>
</tr>
<tr>
<td>Timer0 Clock</td>
<td>T0CKIPPS</td>
<td>RA4</td>
<td>0b0 0100</td>
<td>A B —</td>
</tr>
<tr>
<td>Timer1 Clock</td>
<td>T1CKIPPS</td>
<td>RC0</td>
<td>0b1 0000</td>
<td>A — C</td>
</tr>
<tr>
<td>Timer1 Gate</td>
<td>T1GPPS</td>
<td>RB5</td>
<td>0b0 1101</td>
<td>— B C</td>
</tr>
<tr>
<td>Timer3 Clock</td>
<td>T3CKIPPS</td>
<td>RC0</td>
<td>0b1 0000</td>
<td>— B C</td>
</tr>
<tr>
<td>Timer3 Gate</td>
<td>T3GPPS</td>
<td>RC0</td>
<td>0b1 0000</td>
<td>A — C</td>
</tr>
<tr>
<td>Timer5 Clock</td>
<td>T5CKIPPS</td>
<td>RC2</td>
<td>0b1 0010</td>
<td>A — C</td>
</tr>
<tr>
<td>Timer5 Gate</td>
<td>T5GPPS</td>
<td>RB4</td>
<td>0b0 1100</td>
<td>— B C</td>
</tr>
<tr>
<td>Timer2 Clock</td>
<td>T2INPPS</td>
<td>RC3</td>
<td>0b1 0011</td>
<td>A — C</td>
</tr>
<tr>
<td>Timer4 Clock</td>
<td>T4INPPS</td>
<td>RC5</td>
<td>0b1 0101</td>
<td>— B C</td>
</tr>
<tr>
<td>Timer6 Clock</td>
<td>T6INPPS</td>
<td>RB7</td>
<td>0b0 1111</td>
<td>— B C</td>
</tr>
<tr>
<td>CCP1</td>
<td>CCP1PPS</td>
<td>RC2</td>
<td>0b1 0010</td>
<td>— B C</td>
</tr>
<tr>
<td>CCP2</td>
<td>CCP2PPS</td>
<td>RC1</td>
<td>0b1 0001</td>
<td>— B C</td>
</tr>
<tr>
<td>CCP3</td>
<td>CCP3PPS</td>
<td>RB5</td>
<td>0b0 1101</td>
<td>— B C</td>
</tr>
<tr>
<td>CCP4</td>
<td>CCP4PPS</td>
<td>RB0</td>
<td>0b0 1000</td>
<td>— B C</td>
</tr>
<tr>
<td>SMT1 Window</td>
<td>SMT1WINPPS</td>
<td>RC0</td>
<td>0b1 0000</td>
<td>— B C</td>
</tr>
<tr>
<td>SMT1 Signal</td>
<td>SMT1SIGPPS</td>
<td>RB4</td>
<td>0b0 1100</td>
<td>— B C</td>
</tr>
<tr>
<td>SMT2 Window</td>
<td>SMT2WINPPS</td>
<td>RB5</td>
<td>0b0 1101</td>
<td>— B C</td>
</tr>
<tr>
<td>SMT2 Signal</td>
<td>SMT2SIGPPS</td>
<td>RC1</td>
<td>0b1 0001</td>
<td>— B C</td>
</tr>
<tr>
<td>CWG1</td>
<td>CWG1PPS</td>
<td>RB0</td>
<td>0b0 1000</td>
<td>— B C</td>
</tr>
<tr>
<td>CWG2</td>
<td>CWG2PPS</td>
<td>RB1</td>
<td>0b0 1001</td>
<td>— B C</td>
</tr>
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<td>CWG3PPS</td>
<td>RB2</td>
<td>0b0 1010</td>
<td>— B C</td>
</tr>
<tr>
<td>DSM1 Carrier Low</td>
<td>MD1CARLPPS</td>
<td>RA3</td>
<td>0b0 0011</td>
<td>A — C</td>
</tr>
<tr>
<td>DSM1 Carrier High</td>
<td>MD1CARHPPS</td>
<td>RA4</td>
<td>0b0 0100</td>
<td>A — C</td>
</tr>
<tr>
<td>DSM1 Source</td>
<td>MD1SRCPPS</td>
<td>RA5</td>
<td>0b0 0101</td>
<td>A — C</td>
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<td>CLCx Input 1</td>
<td>CLCIN0PPS</td>
<td>RA0</td>
<td>0b0 0000</td>
<td>A — C</td>
</tr>
<tr>
<td>CLCx Input 2</td>
<td>CLCIN1PPS</td>
<td>RA1</td>
<td>0b0 0001</td>
<td>A — C</td>
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<tr>
<td>CLCx Input 3</td>
<td>CLCIN2PPS</td>
<td>RB6</td>
<td>0b0 1110</td>
<td>— B C</td>
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<tr>
<td>ADC Input 4</td>
<td>CLCIN3PPS</td>
<td>RB7</td>
<td>0b0 1111</td>
<td>— B C</td>
</tr>
<tr>
<td>SPI1 Clock</td>
<td>SPI1SCKPPS</td>
<td>RC3</td>
<td>0b1 0011</td>
<td>— B C</td>
</tr>
<tr>
<td>SPI1 Data</td>
<td>SPI1DIPPS</td>
<td>RC4</td>
<td>0b1 0100</td>
<td>— B C</td>
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<tr>
<td>SPI1 Slave Select</td>
<td>SPI1SSPPS</td>
<td>RA5</td>
<td>0b0 0101</td>
<td>A — C</td>
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<tr>
<td>I²C1 Clock</td>
<td>I2C1SLCLPPS</td>
<td>RC3</td>
<td>0b1 0011</td>
<td>— B C</td>
</tr>
<tr>
<td>I²C1 Data</td>
<td>I2C1SDAPP</td>
<td>RC4</td>
<td>0b1 0100</td>
<td>— B C</td>
</tr>
<tr>
<td>I²C2 Clock</td>
<td>I2C2SLCLPPS</td>
<td>RB1</td>
<td>0b0 1001</td>
<td>— B C</td>
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<td>I²C2 Data</td>
<td>I2C2SDAPP</td>
<td>RB2</td>
<td>0b0 1010</td>
<td>— B C</td>
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<tr>
<td>UART1 Receive</td>
<td>U1RXPPS</td>
<td>RC7</td>
<td>0b1 0111</td>
<td>— B C</td>
</tr>
<tr>
<td>UART1 Clear To Send</td>
<td>U1CTSPPS</td>
<td>RC6</td>
<td>0b1 0110</td>
<td>— B C</td>
</tr>
<tr>
<td>UART2 Receive</td>
<td>U2RXPPS</td>
<td>RB7</td>
<td>0b0 1111</td>
<td>— B C</td>
</tr>
<tr>
<td>UART2 Clear To Send</td>
<td>U2CTSPPS</td>
<td>RB6</td>
<td>0b0 1110</td>
<td>— B C</td>
</tr>
<tr>
<td>CAN Receive</td>
<td>CANRXPPS</td>
<td>RB3</td>
<td>0b0 1011</td>
<td>— B C</td>
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REGISTER 17-2:  RxyPPS: PIN Rxy OUTPUT SOURCE SELECTION REGISTER

<table>
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<tr>
<th>bit 7-6</th>
<th>bit 5-0</th>
<th>Legend</th>
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<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>Unimplemented: Read as '0'</td>
</tr>
<tr>
<td>R/W-0/u</td>
<td>R/W-0/u</td>
<td>bit 5-0  RxyPPS&lt;5:0&gt;: Pin Rxy Output Source Selection bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Table 17-2 for the list of available ports.</td>
</tr>
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</table>
### TABLE 17-2: PPS OUTPUT REGISTER DETAILS

<table>
<thead>
<tr>
<th>RxyPPS&lt;5:0&gt;</th>
<th>Pin Rxy Output Source</th>
<th>Device Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11 1111 - 0b11 0101</td>
<td>Reserved</td>
<td>PIC18(L)F2xK83</td>
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<tr>
<td>0b11 0100</td>
<td>CANTX1</td>
<td>—</td>
</tr>
<tr>
<td>0b11 0011</td>
<td>CANTX0</td>
<td>—</td>
</tr>
<tr>
<td>0b10 1111</td>
<td>ADGRDB</td>
<td>A</td>
</tr>
<tr>
<td>0b10 0011</td>
<td>ADGROA</td>
<td>A</td>
</tr>
<tr>
<td>0b10 0000</td>
<td>CWG3D</td>
<td>A</td>
</tr>
<tr>
<td>0b10 1110</td>
<td>CWG3B</td>
<td>A</td>
</tr>
<tr>
<td>0b10 1100</td>
<td>CWG2D</td>
<td>—</td>
</tr>
<tr>
<td>0b10 1011</td>
<td>CWG2C</td>
<td>—</td>
</tr>
<tr>
<td>0b10 1010</td>
<td>CWG2B</td>
<td>—</td>
</tr>
<tr>
<td>0b10 1001</td>
<td>CWG2A</td>
<td>—</td>
</tr>
<tr>
<td>0b10 1000</td>
<td>DSM1</td>
<td>A</td>
</tr>
<tr>
<td>0b10 0111</td>
<td>CLKR</td>
<td>—</td>
</tr>
<tr>
<td>0b10 0110</td>
<td>NCO1</td>
<td>A</td>
</tr>
<tr>
<td>0b10 0101</td>
<td>TMR0</td>
<td>—</td>
</tr>
<tr>
<td>0b10 0100</td>
<td>PC2 (SDA)</td>
<td>—</td>
</tr>
<tr>
<td>0b10 0011</td>
<td>PC2 (SCL)</td>
<td>—</td>
</tr>
<tr>
<td>0b10 0010</td>
<td>PC1 (SDA)</td>
<td>—</td>
</tr>
<tr>
<td>0b10 0001</td>
<td>PC1 (SCL)</td>
<td>—</td>
</tr>
<tr>
<td>0b10 0000</td>
<td>SPI1 (SS)</td>
<td>A</td>
</tr>
<tr>
<td>0b01 1111</td>
<td>SPI1 (SDO)</td>
<td>—</td>
</tr>
<tr>
<td>0b01 1110</td>
<td>SPI1 (SCK)</td>
<td>—</td>
</tr>
<tr>
<td>0b01 1101</td>
<td>C2OUT</td>
<td>A</td>
</tr>
<tr>
<td>0b01 1100</td>
<td>C1OUT</td>
<td>A</td>
</tr>
<tr>
<td>0b01 1011 - 0b01 1001</td>
<td>Reserved</td>
<td>PIC18(L)F2xK83</td>
</tr>
<tr>
<td>0b01 1000</td>
<td>UART2 (RTS)</td>
<td>—</td>
</tr>
<tr>
<td>0b01 0111</td>
<td>UART2 (TXDE)</td>
<td>—</td>
</tr>
<tr>
<td>0b01 0110</td>
<td>UART2 (TX)</td>
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<td>UART1 (RTS)</td>
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<tr>
<td>0b01 0100</td>
<td>UART1 (TXDE)</td>
<td>—</td>
</tr>
<tr>
<td>0b01 0101</td>
<td>UART1 (TX)</td>
<td>—</td>
</tr>
<tr>
<td>0b01 0010 - 0b01 0001</td>
<td>Reserved</td>
<td>PIC18(L)F2xK83</td>
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<tr>
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<td>PWM7</td>
<td>A</td>
</tr>
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<td>0b00 1110</td>
<td>PWM6</td>
<td>A</td>
</tr>
<tr>
<td>0b00 1101</td>
<td>PWM5</td>
<td>A</td>
</tr>
<tr>
<td>0b00 1100</td>
<td>CCP4</td>
<td>—</td>
</tr>
<tr>
<td>0b00 1011</td>
<td>CCP3</td>
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<td>0b00 1010</td>
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<td>0b00 0111</td>
<td>CWG1C</td>
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</tr>
<tr>
<td>0b00 0110</td>
<td>CWG1B</td>
<td>—</td>
</tr>
</tbody>
</table>
## REGISTER 17-3: PPSLOCK: PPS LOCK REGISTER

<table>
<thead>
<tr>
<th>bit 7-1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Unimplemented</strong>: Read as '0'</td>
<td><strong>PPSLOCKED</strong>: PPS Locked bit</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = PPS is locked.</td>
</tr>
<tr>
<td></td>
<td>0 = PPS is not locked. PPS selections can be changed.</td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

<table>
<thead>
<tr>
<th></th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>PPSLOCKED</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit 0</td>
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</table>

---

**Note:**
- All registers in the PIC18(L)F25/26K83 series are 32 bits wide, regardless of the actual number of bits used. This is done to maintain consistency across different devices.
## TABLE 17-3: SUMMARY OF REGISTERS ASSOCIATED WITH THE PPS MODULE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPSLOCK</td>
<td>—</td>
<td>—</td>
<td>—</td>
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<td>—</td>
<td>PPSLOCKED 268</td>
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<td>INT0PPS</td>
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<td>INT0PPS&lt;4:0&gt; 264</td>
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<tr>
<td>INT1PPS</td>
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<td>—</td>
<td>—</td>
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<td>INT1PPS&lt;4:0&gt; 264</td>
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<td>INT2PPS</td>
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<td>INT2PPS&lt;4:0&gt; 264</td>
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<td>T0CKIPPS</td>
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<td>T0CKIPPS&lt;4:0&gt; 264</td>
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<td>T1CKIPPS&lt;4:0&gt; 264</td>
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<tr>
<td>T1GPPS</td>
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<td>T1GPPS&lt;4:0&gt; 264</td>
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<tr>
<td>T3CKIPPS</td>
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<td>T3CKIPPS&lt;4:0&gt; 264</td>
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<td>T3GPPS&lt;4:0&gt; 264</td>
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<td>T5CKIPPS</td>
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<td>T5CKIPPS&lt;4:0&gt; 264</td>
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<td>T2INPPS&lt;4:0&gt; 264</td>
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<td>T6INPPS&lt;4:0&gt; 264</td>
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<td>CCP1PPS&lt;4:0&gt; 264</td>
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<td>CCP2PPS</td>
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<td>CCP2PPS&lt;4:0&gt; 264</td>
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<td>CCP3PPS</td>
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<td>CCP3PPS&lt;4:0&gt; 264</td>
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<td>CCP4PPS&lt;4:0&gt; 264</td>
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<td>SMT1WINPPS&lt;4:0&gt; 264</td>
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<tr>
<td>SMT1SIGPPS</td>
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<td>SPI1CKPPS</td>
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<td>SPI1DIAPP&lt;4:0&gt; 264</td>
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<td>SPI1SSPPS&lt;4:0&gt; 264</td>
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<td>I2C1CLPPS</td>
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<td>I2C1CLPPS&lt;4:0&gt; 264</td>
</tr>
<tr>
<td>I2C1SADPPL</td>
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<td>I2C2CLPPS</td>
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<td>I2C2CLPPS&lt;4:0&gt; 264</td>
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<tr>
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<td>I2C2SADPPL&lt;4:0&gt; 264</td>
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<td>U1RXPPS</td>
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<td>U1RXPPS&lt;4:0&gt; 264</td>
</tr>
<tr>
<td>U1CTSPPS</td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>U1CTSPPS&lt;4:0&gt; 264</td>
</tr>
<tr>
<td>U2RXPPS</td>
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<td>—</td>
<td>—</td>
<td>—</td>
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<td>—</td>
<td>—</td>
<td>U2RXPPS&lt;4:0&gt; 264</td>
</tr>
<tr>
<td>U2CTSPPS</td>
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<td>—</td>
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<td>—</td>
<td>—</td>
<td>U2CTSPPS&lt;4:0&gt; 264</td>
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<tr>
<td>RxyPPS</td>
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<td>—</td>
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<td>RxyPPS&lt;4:0&gt; 264</td>
</tr>
<tr>
<td>CANRXPPS</td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CANRXPPS&lt;4:0&gt; 264</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the PPS module.
18.0 INTERRUPT-ON-CHANGE

PORTA, PORTB, PORTC and pin RE3 of PORTE can be configured to operate as Interrupt-on-Change (IOC) pins on PIC18(L)F25/26K83 family devices. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual port pin, or combination of port pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

• Interrupt-on-Change enable (Master Switch)
• Individual pin configuration
• Rising and falling edge detection
• Individual pin interrupt flags

Figure 18-1 is a block diagram of the IOC module.

18.1 Enabling the Module

To allow individual port pins to generate an interrupt, the IOCIE bit of the PIE0 register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

18.2 Individual Pin Configuration

For each port pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCxP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCxN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting both associated bits of the IOCxP and IOCxN registers, respectively.

18.3 Interrupt Flags

The IOCAFx, IOCBFx, IOCCFx and IOCEF3 bits located in the IOCAF, IOCBF, IOCCF and IOCEF registers respectively, are status flags that correspond to the interrupt-on-change pins of the associated port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the PIR0 register reflects the status of all IOCAFx, IOCBFx, IOCCFx and IOCEF3 bits.

18.4 Clearing Interrupt Flags

The individual status flags, (IOCAFx, IOCBFx, IOCCFx and IOCEF3 bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

EXAMPLE 18-1: CLEARING INTERRUPT FLAGS

(PORTA EXAMPLE)

```
MOVLW 0xff
XORWF IOCAF, W
ANDWF IOCAF, F
```

18.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set. If an edge is detected while in Sleep mode, the IOCxF register will be updated prior to the first instruction executed out of Sleep.
FIGURE 18-1: INTERRUPT-ON-CHANGE BLOCK DIAGRAM (PORTA EXAMPLE)

- IOCANx
- IOCAPx
- Q2
- RAx
- edge detect
- data bus = 0 or 1
- write IOCAFx
- to data bus IOCAFx
- from all other IOCnFx individual pin detectors
- IOC interrupt to CPU core
18.6 Register Definitions: Interrupt-on-Change Control

REGISTER 18-1: IOCxP: INTERRUPT-ON-CHANGE POSITIVE EDGE REGISTER EXAMPLE

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOCxP7</td>
<td>IOCxP6</td>
</tr>
<tr>
<td>IOCxP5</td>
<td>IOCxP4</td>
</tr>
<tr>
<td>IOCxP3</td>
<td>IOCxP2</td>
</tr>
<tr>
<td>IOCxP1</td>
<td>IOCxP0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared

bit 7-0  IOCxP<7:0>: Interrupt-on-Change Positive Edge Enable bits
1 = Interrupt-on-Change enabled on the IOCx pin for a positive-going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 18-2: IOCxN: INTERRUPT-ON-CHANGE NEGATIVE EDGE REGISTER EXAMPLE

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOCxN7</td>
<td>IOCxN6</td>
</tr>
<tr>
<td>IOCxN5</td>
<td>IOCxN4</td>
</tr>
<tr>
<td>IOCxN3</td>
<td>IOCxN2</td>
</tr>
<tr>
<td>IOCxN1</td>
<td>IOCxN0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared

bit 7-0  IOCxN<7:0>: Interrupt-on-Change Negative Edge Enable bits
1 = Interrupt-on-Change enabled on the IOCx pin for a negative-going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 18-3: IOCxF: INTERRUPT-ON-CHANGE FLAG REGISTER EXAMPLE

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOCxF7</td>
<td>IOCxF6</td>
</tr>
<tr>
<td>IOCxF5</td>
<td>IOCxF4</td>
</tr>
<tr>
<td>IOCxF3</td>
<td>IOCxF2</td>
</tr>
<tr>
<td>IOCxF1</td>
<td>IOCxF0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared
HS - Bit is set in hardware

bit 7-0  IOCxF<7:0>: Interrupt-on-Change Flag bits
1 = A enabled change was detected on the associated pin. Set when IOCP[n] = 1 and a positive edge was detected on the IOCx pin, or when IOCN[n] = 1 and a negative edge was detected on the IOCx pin
0 = No change was detected, or the user cleared the detected change
### TABLE 18-1: IOC REGISTERS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOCAP</td>
<td>IOCAP7</td>
<td>IOCAP6</td>
<td>IOCAP5</td>
<td>IOCAP4</td>
<td>IOCAP3</td>
<td>IOCAP2</td>
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<td>IOCAN0</td>
</tr>
<tr>
<td>IOCAF</td>
<td>IOCAF7</td>
<td>IOCAF6</td>
<td>IOCAF5</td>
<td>IOCAF4</td>
<td>IOCAF3</td>
<td>IOCAF2</td>
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<td>IOCAF0</td>
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<td>IOCBP</td>
<td>IOCBP7</td>
<td>IOCBP6</td>
<td>IOCBP5</td>
<td>IOCBP4</td>
<td>IOCBP3</td>
<td>IOCBP2</td>
<td>IOCBP1</td>
<td>IOCBP0</td>
</tr>
<tr>
<td>IOCBN</td>
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<td>IOCBN5</td>
<td>IOCBN4</td>
<td>IOCBN3</td>
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<td>IOCBF4</td>
<td>IOCBF3</td>
<td>IOCBF2</td>
<td>IOCBF1</td>
<td>IOCBF0</td>
</tr>
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<td>IOCCP</td>
<td>IOCCP7</td>
<td>IOCCP6</td>
<td>IOCCP5</td>
<td>IOCCP4</td>
<td>IOCCP3</td>
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<td>IOCCF5</td>
<td>IOCCF4</td>
<td>IOCCF3</td>
<td>IOCCF2</td>
<td>IOCCF1</td>
<td>IOCCF0</td>
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<td>—</td>
</tr>
</tbody>
</table>

Note 1: If MCLRE = 1 or LVP = 1, RE3 port functionality is disabled and IOC on RE3 is not available.

### TABLE 18-2: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPT-ON-CHANGE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOCxF</td>
<td>IOCxF7</td>
<td>IOCxF6</td>
<td>IOCxF5</td>
<td>IOCxF4</td>
<td>IOCxF3</td>
<td>IOCxF2</td>
<td>IOCxF1</td>
<td>IOCxF0</td>
<td>272</td>
</tr>
<tr>
<td>IOCxN</td>
<td>IOCxN7</td>
<td>IOCxN6</td>
<td>IOCxN5</td>
<td>IOCxN4</td>
<td>IOCxN3</td>
<td>IOCxN2</td>
<td>IOCxN1</td>
<td>IOCxN0</td>
<td>272</td>
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<tr>
<td>IOCxP</td>
<td>IOCxP7</td>
<td>IOCxP6</td>
<td>IOCxP5</td>
<td>IOCxP4</td>
<td>IOCxP3</td>
<td>IOCxP2</td>
<td>IOCxP1</td>
<td>IOCxP0</td>
<td>272</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by interrupt-on-change.
19.0 PERIPHERAL MODULE DISABLE (PMD)

Sleep, Idle and Doze modes allow users to substantially reduce power consumption by slowing or stopping the CPU clock. Even so, peripheral modules still remain clocked, and thus, consume some amount of power. There may be cases where the application needs what these modes do not provide: the ability to allocate limited power resources to the CPU while eliminating power consumption from the peripherals.

The PIC18(L)F25/26K83 family addresses this requirement by allowing peripheral modules to be selectively enabled or disabled, placing them into the lowest possible power mode.

All modules are ON by default following any Reset.

19.1 Disabling a Module

Disabling a module has the following effects:

- All clock and control inputs to the module are suspended; there are no logic transitions, and the module will not function.
- The module is held in Reset.
- Any SFR becomes "unimplemented"
  - Writing is disabled
  - Reading returns 00h
- I/O functionality is prioritized as per Section 16.2, I/O Priorities
- All associated Input Selection registers are also disabled

19.2 Enabling a Module

When the PMD register bit is cleared, the module is re-enabled and will be in its Reset state (Power-on Reset). SFR data will reflect the POR Reset values.

Depending on the module, it may take up to one full instruction cycle for the module to become active. There should be no interaction with the module (e.g., writing to registers) for at least one instruction after it has been re-enabled.

19.3 Effects of a Reset

Following any Reset, each control bit is set to ‘0’, enabling all modules.

19.4 System Clock Disable

Setting SYSCMD (PMD0, Register 19-1) disables the system clock (Fosc) distribution network to the peripherals. Not all peripherals make use of SYSCLK, so not all peripherals are affected. Refer to the specific peripheral description to see if it will be affected by this bit.
19.5 Register Definitions: Peripheral Module Disable

REGISTER 19-1: PMD0: PMD CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>SYSCMD</th>
<th>FVRMD</th>
<th>HLVDMD</th>
<th>CRCMD</th>
<th>SCANMD</th>
<th>NVMDM</th>
<th>CLKRMD</th>
<th>IOCMD</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared  q = Value depends on condition

bit 7 SYSCMD: Disable Peripheral System Clock Network bit(1)
See description in Section 19.4 “System Clock Disable”.
1 = System clock network disabled (FOSC)
0 = System clock network enabled

bit 6 FVRMD: Disable Fixed Voltage Reference bit
1 = FVR module disabled
0 = FVR module enabled

bit 5 HLVDMD: Disable Low-Voltage Detect bit
1 = HLVD module disabled
0 = HLVD module enabled

bit 4 CRCMD: Disable CRC Engine bit
1 = CRC module disabled
0 = CRC module enabled

bit 3 SCANMD: Disable NVM Memory Scanner bit(2)
1 = NVM Memory Scan module disabled
0 = NVM Memory Scan module enabled

bit 2 NVMMD: NVM Module Disable bit(3)
1 = All Memory reading and writing is disabled; NVMCON registers cannot be written
0 = NVM module enabled

bit 1 CLKRMD: Disable Clock Reference bit
1 = CLKR module disabled
0 = CLKR module enabled

bit 0 IOCMD: Disable Interrupt-on-Change bit, All Ports
1 = IOC module(s) disabled
0 = IOC module(s) enabled

Note 1: Clearing the SYSCMD bit disables the system clock (Fosc) to peripherals, however peripherals clocked by Fosc/4 are not affected.
2: Subject to SCANE bit in CONFIG4H.
3: When enabling NVM, a delay of up to 1 µs may be required before accessing data.
## REGISTER 19-2: PMD1: PMD CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value 1</th>
<th>Value 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>NCO1MD: Disable NCO1 Module bit</td>
<td>1 = NCO1 module disabled</td>
<td>0 = NCO1 module enabled</td>
</tr>
<tr>
<td>6</td>
<td>TMR6MD: Disable Timer TMR6 bit</td>
<td>1 = TMR6 module disabled</td>
<td>0 = TMR6 module enabled</td>
</tr>
<tr>
<td>5</td>
<td>TMR5MD: Disable Timer TMR5 bit</td>
<td>1 = TMR5 module disabled</td>
<td>0 = TMR5 module enabled</td>
</tr>
<tr>
<td>4</td>
<td>TMR4MD: Disable Timer TMR4 bit</td>
<td>1 = TMR4 module disabled</td>
<td>0 = TMR4 module enabled</td>
</tr>
<tr>
<td>3</td>
<td>TMR3MD: Disable Timer TMR3 bit</td>
<td>1 = TMR3 module disabled</td>
<td>0 = TMR3 module enabled</td>
</tr>
<tr>
<td>2</td>
<td>TMR2MD: Disable Timer TMR2 bit</td>
<td>1 = TMR2 module disabled</td>
<td>0 = TMR2 module enabled</td>
</tr>
<tr>
<td>1</td>
<td>TMR1MD: Disable Timer TMR1 bit</td>
<td>1 = TMR1 module disabled</td>
<td>0 = TMR1 module enabled</td>
</tr>
<tr>
<td>0</td>
<td>TMR0MD: Disable Timer TMR0 bit</td>
<td>1 = TMR0 module disabled</td>
<td>0 = TMR0 module enabled</td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **q** = Value depends on condition
# REGISTER 19-3: PMD2: PMD CONTROL REGISTER 2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Value 1</th>
<th>Value 0</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>DACMD</td>
<td>Disable DAC bit</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>ADCMD</td>
<td>Disable ADCC bit</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>CMP2MD</td>
<td>Disable Comparator CMP2 bit</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>4-3</td>
<td>Unimplemented: Read as '0'</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>CMP1MD</td>
<td>Disable Comparator CMP1 bit</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>ZCDMD(1)</td>
<td>Disable Zero-Cross Detect module bit(1)</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **q** = Value depends on condition

### Notes:
1. Subject to ZCD bit in CONFIG2H.
### REGISTER 19-4: PMD3: PMD CONTROL REGISTER 3

<table>
<thead>
<tr>
<th>bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PWM8MD: Disable Pulse-Width Modulator PWM8 bit</td>
<td>1 = PWM8 module disabled, 0 = PWM8 module enabled</td>
</tr>
<tr>
<td>6</td>
<td>PWM7MD: Disable Pulse-Width Modulator PWM7 bit</td>
<td>1 = PWM7 module disabled, 0 = PWM7 module enabled</td>
</tr>
<tr>
<td>5</td>
<td>PWM6MD: Disable Pulse-Width Modulator PWM6 bit</td>
<td>1 = PWM6 module disabled, 0 = PWM6 module enabled</td>
</tr>
<tr>
<td>4</td>
<td>PWM5MD: Disable Pulse-Width Modulator PWM5 bit</td>
<td>1 = PWM5 module disabled, 0 = PWM5 module enabled</td>
</tr>
<tr>
<td>3</td>
<td>CCP4MD: Disable Capture/Compare/PWM CCP4 bit</td>
<td>1 = CCP4 module disabled, 0 = CCP4 module enabled</td>
</tr>
<tr>
<td>2</td>
<td>CCP3MD: Disable Capture/Compare/PWM CCP3 bit</td>
<td>1 = CCP3 module disabled, 0 = CCP3 module enabled</td>
</tr>
<tr>
<td>1</td>
<td>CCP2MD: Disable Capture/Compare/PWM CCP2 bit</td>
<td>1 = CCP2 module disabled, 0 = CCP2 module enabled</td>
</tr>
<tr>
<td>0</td>
<td>CCP1MD: Disable Capture/Compare/PWM CCP1 bit</td>
<td>1 = CCP1 module disabled, 0 = CCP1 module enabled</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- q = Value depends on condition
## REGISTER 19-5: PMD4: PMD CONTROL REGISTER 4

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CWG3MD</td>
<td>Disable CWG3 Module bit</td>
</tr>
<tr>
<td>1 = CWG3 module disabled</td>
<td></td>
</tr>
<tr>
<td>0 = CWG3 module enabled</td>
<td></td>
</tr>
<tr>
<td>CWG2MD</td>
<td>Disable CWG2 Module bit</td>
</tr>
<tr>
<td>1 = CWG2 module disabled</td>
<td></td>
</tr>
<tr>
<td>0 = CWG2 module enabled</td>
<td></td>
</tr>
<tr>
<td>CWG1MD</td>
<td>Disable CWG1 Module bit</td>
</tr>
<tr>
<td>1 = CWG1 module disabled</td>
<td></td>
</tr>
<tr>
<td>0 = CWG1 module enabled</td>
<td></td>
</tr>
<tr>
<td>Unimplemented</td>
<td>Read as '0'</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **1** = Bit is set
- **0** = Bit is cleared
- **q** = Value depends on condition
- **-n/n** = Value at POR and BOR/Value at all other Resets
### REGISTER 19-6: PMD5: PMD CONTROL REGISTER 5

<table>
<thead>
<tr>
<th>bit 7-6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>U2MD</td>
<td>U1MD</td>
<td>SPI1MD</td>
<td>I2C2MD</td>
<td>I2C1MD</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7-6</th>
<th>Unimplemented: Read as '0'</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 5</td>
<td>U2MD: Disable UART2 bit</td>
</tr>
<tr>
<td></td>
<td>1 = UART2 module disabled</td>
</tr>
<tr>
<td></td>
<td>0 = UART2 module enabled</td>
</tr>
<tr>
<td>bit 4</td>
<td>U1MD: Disable UART1 bit</td>
</tr>
<tr>
<td></td>
<td>1 = UART1 module disabled</td>
</tr>
<tr>
<td></td>
<td>0 = UART1 module enabled</td>
</tr>
<tr>
<td>bit 3</td>
<td>Unimplemented: Read as '0'</td>
</tr>
<tr>
<td>bit 2</td>
<td>SPI1MD: Disable SPI1 Module bit</td>
</tr>
<tr>
<td></td>
<td>1 = SPI1 module disabled</td>
</tr>
<tr>
<td></td>
<td>0 = SPI1 module enabled</td>
</tr>
<tr>
<td>bit 1</td>
<td>I2C2MD: Disable I2C2 Module bit</td>
</tr>
<tr>
<td></td>
<td>1 = I2C2 module disabled</td>
</tr>
<tr>
<td></td>
<td>0 = I2C2 module enabled</td>
</tr>
<tr>
<td>bit 0</td>
<td>I2C1MD: Disable I2C1 Module bit</td>
</tr>
<tr>
<td></td>
<td>1 = I2C1 module disabled</td>
</tr>
<tr>
<td></td>
<td>0 = I2C1 module enabled</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **q** = Value depends on condition
- **n/n** = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared
## REGISTER 19-7: PMD6: PMD CONTROL REGISTER 6

<table>
<thead>
<tr>
<th>bit</th>
<th>Unimplemented: Read as '0'</th>
<th>SMT2MD: Disable SMT2 Module bit</th>
<th>SMT1MD: Disable SMT1 Module bit</th>
<th>CLC1MD: Disable CLC1 Module bit</th>
<th>CLC2MD: Disable CLC2 Module bit</th>
<th>CLC3MD: Disable CLC3 Module bit</th>
<th>CLC4MD: Disable CLC4 Module bit</th>
<th>DSMMD: Disable Data Signal Modulator bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **q** = Value depends on condition

- **SMT2MD**: Disable SMT2 Module bit
  - 1 = SMT2 module disabled
  - 0 = SMT2 module enabled

- **SMT1MD**: Disable SMT1 Module bit
  - 1 = SMT1 module disabled
  - 0 = SMT1 module enabled

- **CLC1MD**: Disable CLC1 Module bit
  - 1 = CLC1 module disabled
  - 0 = CLC1 module enabled

- **CLC2MD**: Disable CLC2 Module bit
  - 1 = CLC2 module disabled
  - 0 = CLC2 module enabled

- **CLC3MD**: Disable CLC3 Module bit
  - 1 = CLC3 module disabled
  - 0 = CLC3 module enabled

- **CLC4MD**: Disable CLC4 Module bit
  - 1 = CLC4 module disabled
  - 0 = CLC4 module enabled

- **DSMMD**: Disable Data Signal Modulator bit
  - 1 = DSM module disabled
  - 0 = DSM module enabled
REGISTER 19-8: PMD7: PMD CONTROL REGISTER 7

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CANMD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>DMA2MD</td>
<td>DMA1MD</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- q = Value depends on condition

bit 7     CANMD: Disable CAN Module bit
1 = CAN module disabled
0 = CAN module enabled

bit 6-2   Unimplemented: Read as ‘0’

bit 1     DMA2MD: Disable DMA2 Module bit
1 = DMA2 module disabled
0 = DMA2 module enabled

bit 0     DMA1MD: Disable DMA1 Module bit
1 = DMA1 module disabled
0 = DMA1 module enabled

TABLE 19-1: SUMMARY OF REGISTERS ASSOCIATED WITH PERIPHERAL MODULE DISABLE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMD0</td>
<td>SYSCMD</td>
<td>FVRMD</td>
<td>HLVDMD</td>
<td>CRCMD</td>
<td>SCANMD</td>
<td>NVMMC</td>
<td>CLKRMD</td>
<td>IOCMD</td>
<td>275</td>
</tr>
<tr>
<td>PMD1</td>
<td>NCO1MD</td>
<td>TMR6MD</td>
<td>TMR5MD</td>
<td>TMR4MD</td>
<td>TMR3MD</td>
<td>TMR2MD</td>
<td>TMR1MD</td>
<td>TMR0MD</td>
<td>276</td>
</tr>
<tr>
<td>PMD2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMD3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMD4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMD5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMD6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMD7</td>
<td>CANMD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by peripheral module disable.
20.0 TIMER0 MODULE

Timer0 module is an 8/16-bit timer/counter with the following features:

- 16-bit timer/counter
- 8-bit timer/counter with programmable period
- Synchronous or asynchronous operation
- Selectable clock sources
- Programmable prescaler
- Programmable postscaler
- Operation during Sleep mode
- Interrupt on match or overflow
- Output on I/O pin (via PPS) or to other peripherals

FIGURE 20-1: BLOCK DIAGRAM OF TIMER0
20.1 Timer0 Operation

Timer0 can operate as either an 8-bit timer/counter or a 16-bit timer/counter. The mode is selected with the MD16 bit of the T0CON register.

20.1.1 16-BIT MODE

The register pair TMR0H:TMR0L increments on the rising edge of the clock source. A 15-bit prescaler on the clock input gives several prescale options (see prescaler control bits, CKPS<3:0> in the T0CON1 register).

20.1.1.1 Timer0 Reads and Writes in 16-Bit Mode

In 16-bit mode, in order to avoid rollover between reading high and low registers, the TMR0H register is a buffered copy of the actual high byte of Timer0, which is neither directly readable, nor writable (see Figure 20-1). TMR0H is updated with the contents of the high byte of Timer0 during a read of TMR0L. This provides the ability to read all 16 bits of Timer0 without having to verify that the read of the high and low byte was valid, due to a rollover between successive reads of the high and low byte.

Similarly, a write to the high byte of Timer0 must also take place through the TMR0H Buffer register. The high byte is updated with the contents of TMR0H when a write occurs to TMR0L. This allows all 16 bits of Timer0 to be updated at once.

20.1.2 8-BIT MODE

In 8-bit mode, the value of TMR0L is compared to that of the Period buffer, a copy of TMR0H, on each clock cycle. When the two values match, the following events happen:

- TMR0_out goes high for one prescaled clock period
- TMR0L is reset
- The contents of TMR0H are copied to the period buffer

In 8-bit mode, the TMR0L and TMR0H registers are both directly readable and writable. The TMR0L register is cleared on any device Reset, while the TMR0H register initializes at FFh.

Both the prescaler and postscaler counters are cleared on the following events:

- A write to the TMR0L register
- A write to either the T0CON0 or T0CON1 registers
- Any device Reset – Power-on Reset (POR), MCLR Reset, Watchdog Timer Reset (WDTR) or Brown-out Reset (BOR)

20.1.3 COUNTER MODE

In Counter mode, the prescaler is normally disabled by setting the CKPS bits of the T0CON1 register to '0000'. Each rising edge of the clock input (or the output of the prescaler if the prescaler is used) increments the counter by 1.

20.1.4 TIMER MODE

In Timer mode, the Timer0 module will increment every instruction cycle as long as there is a valid clock signal and the CKPS bits of the T0CON1 register (Register 20-2) are set to '0000'. When a prescaler is added, the timer will increment at the rate based on the prescaler value.

20.1.5 ASYNCHRONOUS MODE

When the ASYNC bit of the T0CON1 register is set (ASYNC = '1'), the counter increments with each rising edge of the input source (or output of the prescaler, if used). Asynchronous mode allows the counter to continue operation during Sleep mode provided that the clock also continues to operate during Sleep.

20.1.6 SYNCHRONOUS MODE

When the ASYNC bit of the T0CON1 register is clear (ASYNC = '0'), the counter clock is synchronized to the system clock (Fosc/4). When operating in Synchronous mode, the counter clock frequency cannot exceed Fosc/4.

20.2 Clock Source Selection

The CS<2:0> bits of the T0CON1 register are used to select the clock source for Timer0. Register 20-2 displays the clock source selections.

20.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, Timer0 operates as a timer and will increment on multiples of the clock source, as determined by the Timer0 prescaler.

20.2.2 EXTERNAL CLOCK SOURCE

When an external clock source is selected, Timer0 can operate as either a timer or a counter. Timer0 will increment on multiples of the rising edge of the external clock source, as determined by the Timer0 prescaler.
20.3 Programmable Prescaler

A software programmable prescaler is available for exclusive use with Timer0. There are 16 prescaler options for Timer0 ranging in powers of two from 1:1 to 1:32768. The prescaler values are selected using the CKPS<3:0> bits of the T0CON1 register.

The prescaler is not directly readable or writable. Clearing the prescaler register can be done by writing to the TMR0L register or to the T0CON0/T0CON1 register or by any Reset.

20.4 Programmable Postscaler

A software programmable postscaler (output divider) is available for exclusive use with Timer0. There are 16 postscaler options for Timer0 ranging from 1:1 to 1:16. The postscaler values are selected using the OUTPS bits of the T0CON0 register.

The postscaler is not directly readable or writable. Clearing the postscaler register can be done by writing to the TMR0L register or to the T0CON0/T0CON1 register or by any Reset.

20.5 Operation During Sleep

When operating synchronously, Timer0 will halt. When operating asynchronously, Timer0 will continue to increment and wake the device from Sleep (if Timer0 interrupts are enabled) provided that the input clock source is active.

20.6 Timer0 Interrupts

The Timer0 interrupt flag bit (TMR0IF) is set when either of the following conditions occur:
- 8-bit TMR0L matches the TMR0H value
- 16-bit TMR0 rolls over from 'FFFFh'

When the postscaler bits (OUTPS) are set to 1:1 operation (no division), the TOIF flag bit will be set with every TMR0 match or rollover. In general, the TMR0IF flag bit will be set every OUTPS +1 matches or rollovers.

If Timer0 interrupts are enabled (TMR0IE bit of the PIE3 register = ‘1’), the CPU will be interrupted and the device may wake from Sleep (see Section 20.2 “Clock Source Selection” for more details).

20.7 Timer0 Output

The Timer0 output can be routed to any I/O pin via the RxPPS output selection register (see Section 17.0 “Peripheral Pin Select (PPS) Module” for additional information). The Timer0 output can also be used by other peripherals, such as the auto-conversion trigger of the Analog-to-Digital Converter. Finally, the Timer0 output can be monitored through software via the Timer0 output bit (OUT) of the T0CON0 register (Register 20-1).

TMR0_out will be a pulse of one postscaled clock period when a match occurs between TMR0L and PR0 (Period register for TMR0) in 8-bit mode, or when TMR0 rolls over in 16-bit mode. The Timer0 output is a 50% duty cycle that toggles on each TMR0_out rising clock edge.
## 20.8 Register Definitions: Timer0 Control

### REGISTER 20-1: T0CON0: TIMER0 CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>Field</th>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>7</td>
<td>TMR0 Enable bit</td>
<td>1: Module is enabled and operating, 0: Module is disabled and in the lowest power mode</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>Unimplemented: Read as ‘0’</td>
<td></td>
</tr>
<tr>
<td>OUT</td>
<td>5</td>
<td>TMR0 Output bit (read-only)</td>
<td></td>
</tr>
<tr>
<td>MD16</td>
<td>4</td>
<td>TMR0 Operating as 16-Bit Timer Select bit</td>
<td>1: TMR0 is a 16-bit timer, 0: TMR0 is an 8-bit timer</td>
</tr>
</tbody>
</table>

**Legend:**
- `R` = Readable bit
- `W` = Writable bit
- `U` = Unimplemented bit, read as ‘0’
- `u` = Bit is unchanged
- `x` = Bit is unknown
- `-n/n` = Value at POR and BOR/Value at all other Resets
- `'1'` = Bit is set
- `'0'` = Bit is cleared
REGISTER 20-2: T0CON1: TIMER0 CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS&lt;2:0&gt;</td>
<td>ASYNC</td>
<td>CKPS&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

**bit 7-5**  
CS<2:0>: Timer0 Clock Source Select bits
- 111 = CLC1
- 110 = SOSC
- 101 = MFINTOSC (500 kHz)
- 100 = LFINTOSC
- 011 = HFINTOSC
- 010 = Fosc/4
- 001 = Pin selected by T0CKIPPS (Inverted)
- 000 = Pin selected by T0CKIPPS (Non-inverted)

**bit 4**  
ASYNC: TMR0 Input Asynchronization Enable bit
- 1 = The input to the TMR0 counter is not synchronized to system clocks
- 0 = The input to the TMR0 counter is synchronized to Fosc/4

**bit 3-0**  
CKPS<3:0>: Prescaler Rate Select bit
- 1111 = 1:32768
- 1110 = 1:16384
- 1101 = 1:8192
- 1100 = 1:4096
- 1011 = 1:2048
- 1010 = 1:1024
- 1001 = 1:512
- 1000 = 1:256
- 0111 = 1:128
- 0110 = 1:64
- 0101 = 1:32
- 0100 = 1:16
- 0011 = 1:8
- 0010 = 1:4
- 0001 = 1:2
- 0000 = 1:1
REGISTER 20-3:  TMR0L: TIMER0 COUNT REGISTER

| Bit 0 | Bit 7 | Bit 8 | Bit 9 | Bit 10 | Bit 11 | Bit 12 | Bit 13 | Bit 14 | Bit 15 | Bit 16 | Bit 17 | Bit 18 | Bit 19 | Bit 20 | Bit 21 | Bit 22 | Bit 23 | Bit 24 | Bit 25 | Bit 26 | Bit 27 | Bit 28 | Bit 29 | Bit 30 | Bit 31 |
|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
|       |       |       |       |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       | TMR0L<7:0> |       |       |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set  '0' = Bit is cleared

bit 7-0  TMR0L<7:0>: TMR0 Count register <7:0>

REGISTER 20-4:  TMR0H: TIMER0 PERIOD REGISTER

| Bit 0 | Bit 7 | Bit 8 | Bit 9 | Bit 10 | Bit 11 | Bit 12 | Bit 13 | Bit 14 | Bit 15 | Bit 16 | Bit 17 | Bit 18 | Bit 19 | Bit 20 | Bit 21 | Bit 22 | Bit 23 | Bit 24 | Bit 25 | Bit 26 | Bit 27 | Bit 28 | Bit 29 | Bit 30 | Bit 31 |
|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
|       |       |       |       |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|       | TMR0H<15:8> |       |       |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set  '0' = Bit is cleared

bit 7-0  TMR0H<15:8>: TMR0 Counter bits <15:8>

When MD16 = 0
PR0<7:0>: TMR0 Period Register Bits <7:0>
When MD16 = 1
TMR0H<15:8>: TMR0 Counter bits <15:8>

TABLE 20-1:  SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>T0CON0</td>
<td>EN</td>
<td>—</td>
<td>OUT</td>
<td>MD16</td>
<td>OUTPS&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>286</td>
</tr>
<tr>
<td>T0CON1</td>
<td>CS&lt;2:0&gt;</td>
<td></td>
<td>ASYNC</td>
<td>CKPS&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>287</td>
</tr>
<tr>
<td>TMR0L</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TMR0L&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>288</td>
</tr>
<tr>
<td>TMR0H</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TMR0H&lt;15:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td>288</td>
</tr>
</tbody>
</table>

Legend:  — = unimplemented location, read as '0'. Shaded cells are not used by Timer0.
21.0 TIMER1/3/5 MODULE WITH GATE CONTROL

Timer1/3/5 module is a 16-bit timer/counter with the following features:
• 16-bit timer/counter register pair (TMRxH:TMRxL)
• Programmable internal or external clock source
• 2-bit prescaler
• Dedicated Secondary 32 kHz oscillator circuit
• Optionally synchronized comparator out
• Multiple Timer1/3/5 gate (count enable) sources
• Interrupt-on-overflow
• Wake-up on overflow (external clock, asynchronous mode only)

Asynchronous mode only)
• 16-Bit Read/Write Operation
• Time base for the Capture/Compare function with the CCP modules
• Special Event Trigger (with CCP)
• Selectable Gate Source Polarity
• Gate Toggle mode
• Gate Single-pulse mode
• Gate Value Status
• Gate Event Interrupt

Figure 21-1 is a block diagram of the Timer1/3/5 module.

FIGURE 21-1: TIMER1/3/5 BLOCK DIAGRAM
21.1 Timer1/3/5 Operation

The Timer1/3/5 module is a 16-bit incrementing counter which is accessed through the TMRxH:TMRxL register pair. Writes to TMRxH or TMRxL directly update the counter.

When used with an internal clock source, the module is a timer and increments on every instruction cycle. When used with an external clock source, the module can be used as either a timer or counter and increments on every selected edge of the external source.

Timer1/3/5 is enabled by configuring the ON and GE bits in the TxCON and TxGCON registers, respectively. Table 21-1 displays the Timer1/3/5 enable selections.

<table>
<thead>
<tr>
<th>ON</th>
<th>GE</th>
<th>Timer1/3/5 Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>Count Enabled</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Always On</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Off</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Off</td>
</tr>
</tbody>
</table>

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after any one or more of the following conditions:
- Timer1/3/5 enabled after POR
- Write to TMRxH or TMRxL
- Timer1/3/5 is disabled
- Timer1/3/5 is disabled (TMRxON = 0) when TxCKI is high then Timer1/3/5 is enabled (TMRxON = 1) when TxCKI is low.

21.2 Clock Source Selection

The CS<4:0> bits of the TMRxCLK register (Register 21-3) are used to select the clock source for Timer1/3/5. The five TMRxCLK bits allow the selection of several possible synchronous and asynchronous clock sources. Register 21-3 displays the clock source selections.

21.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected the TMRxH:TMRxL register pair will increment on multiples of Fosc as determined by the Timer1/3/5 prescaler.

When the Fosc internal clock source is selected, the Timer1/3/5 register value will increment by four counts every instruction clock cycle. Due to this condition, a 2 LSB error in resolution will occur when reading the Timer1/3/5 value. To utilize the full resolution of Timer1/3/5, an asynchronous input signal must be used to gate the Timer1/3/5 clock input.

The following asynchronous sources may be used at the Timer1/3/5 gate:
- Asynchronous event on the TxGPPS pin
- TMR0OUT
- TMR1/3/5OUT (excluding the TMR for which it is being used)
- TMR 2/4/6OUT (post-scaled)
- CMP1/2OUT
- SMT1_match
- NCO1OUT
- PWM3/4 OUT
- CCP1/2/3/4 OUT
- CLC1/2/3/4 OUT
- ZCDOUT

21.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1/3/5 module may work as a timer or a counter.

When enabled to count, Timer1/3/5 is incremented on the rising edge of the external clock input of the TxCKIIPPS pin. This external clock source can be synchronized to the microcontroller system clock or it can run asynchronously.

When used as a timer with a clock oscillator, an external 32,768 kHz crystal can be used in conjunction with the dedicated secondary internal oscillator circuit.
21.3 Timer1/3/5 Prescaler

Timer1/3/5 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The CKPS bits of the TxCON register control the prescaler counter. The prescaler counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMRxH or TMRxL.

21.4 Timer1/3/5 Operation in Asynchronous Counter Mode

If control bit SYN of the TxCON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake up the processor. However, special precautions in software are needed to read/write the timer (see Section 21.4.1 “Reading and Writing Timer1/3/5 in Asynchronous Counter Mode”).

Note: When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

21.4.1 READING AND WRITING TIMER1/3/5 IN ASYNCHRONOUS COUNTER MODE

Reading TMRxH or TMRxL while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads. For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMRxH:TMRxL register pair.

21.5 Timer1/3/5 16-Bit Read/Write Mode

Timer1/3/5 can be configured to read and write all 16 bits of data, to and from, the 8-bit TMRxL and TMRxH registers, simultaneously. The 16-bit read and write operations are enabled by setting the RD16 bit of the TxCON register.

To accomplish this function, the TMRxH register value is mapped to a buffer register called the TMRxH buffer register. While in 16-Bit mode, the TMRxH register is not directly readable or writable and all read and write operations take place through the use of this TMRxH buffer register.

When a read from the TMRxL register is requested, the value of the TMRxH register is simultaneously loaded into the TMRxH buffer register. When a read from the TMRxH register is requested, the value is provided from the TMRxH buffer register instead. This provides the user with the ability to accurately read all 16 bits of the Timer1/3/5 value from a single instance in time. Reference the block diagram in Figure 21-2 for more details.

In contrast, when not in 16-Bit mode, the user must read each register separately and determine if the values have become invalid due to a rollover that may have occurred between the read operations.

When a write request of the TMRxL register is requested, the TMRxH buffer register is simultaneously updated with the contents of the TMRxH register. The value of TMRxH must be preloaded into the TMRxH buffer register prior to the write request for the TMRxL register. This provides the user with the ability to write all 16 bits to the TMRxL:TMRxH register pair at the same time.

Any requests to write to the TMRxH directly does not clear the Timer1/3/5 prescaler value. The prescaler value is only cleared through write requests to the TMRxL register.
21.6 Timer1/3/5 Gate

Timer1/3/5 can be configured to count freely or the count can be enabled and disabled using Timer1/3/5 gate circuitry. This is also referred to as Timer1/3/5 gate enable.

Timer1/3/5 gate can also be driven by multiple selectable sources.

21.6.1 TIMER1/3/5 GATE ENABLE

The Timer1/3/5 Gate Enable mode is enabled by setting the TMRxGE bit of the TxGCON register. The polarity of the Timer1/3/5 Gate Enable mode is configured using the TxGPOL bit of the TxGCON register.

When Timer1/3/5 Gate Enable mode is enabled, Timer1/3/5 will increment on the rising edge of the Timer1/3/5 clock source. When Timer1/3/5 Gate signal is inactive, the timer will not increment and hold the current count. See Figure 21-4 for timing details.

### TABLE 21-2: TIMER1/3/5 GATE ENABLE SELECTIONS

<table>
<thead>
<tr>
<th>TMRxCLK</th>
<th>TxGPOL</th>
<th>TxG</th>
<th>Timer1/3/5 Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>↑</td>
<td>1</td>
<td>1</td>
<td>Counts</td>
</tr>
<tr>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>Holds Count</td>
</tr>
<tr>
<td>↑</td>
<td>0</td>
<td>1</td>
<td>Holds Count</td>
</tr>
<tr>
<td>↑</td>
<td>0</td>
<td>0</td>
<td>Counts</td>
</tr>
</tbody>
</table>
21.6.2 TIMER1/3/5 GATE SOURCE SELECTION
The gate source for Timer1/3/5 can be selected using the GSS<4:0> bits of the TMRxGATE register (Register 21-4). The polarity selection for the gate source is controlled by the TxGPOL bit of the TxGCON register (Register 21-2).

Any of the above mentioned signals can be used to trigger the gate. The output of the CMPx can be synchronized to the Timer1/3/5 clock or left asynchronous. For more information see Section 39.3.1 “Comparator Output Synchronization”.

21.6.3 TIMER1/3/5 GATE TOGGLE MODE
When Timer1/3/5 Gate Toggle mode is enabled, it is possible to measure the duration between every rising and falling edge of the gate signal.

The Timer1/3/5 gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. See Figure 21-5 for timing details.

Timer1/3/5 Gate Toggle mode is enabled by setting the GTM bit of the TxGCON register. When the GTM bit is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

Note: Enabling Toggle mode at the same time as changing the gate polarity may result in indeterminate operation.

21.6.4 TIMER1/3/5 GATE SINGLE-PULSE MODE
When Timer1/3/5 Gate Single-Pulse mode is enabled, it is possible to capture a single-pulse gate event. Timer1/3/5 Gate Single-Pulse mode is first enabled by setting the GSPM bit in the TxGCON register. Next, the GGO/DONE bit in the TxGCON register must be set. The Timer1/3/5 will be fully enabled on the next incrementing edge of the gate signal. On the next trailing edge of the pulse, the GGO/DONE bit will automatically be cleared. No other gate events will be allowed to increment Timer1/3/5 until the GGO/DONE bit is once again set in software.

Clearing the TxGSPM bit of the TxGCON register will also clear the GGO/DONE bit. See Figure 21-6 for timing details.

Enabling the Toggle mode and the Single-Pulse mode simultaneously will permit both sections to work together. This allows the period on the Timer1/3/5 gate source to be measured. See Figure 21-7 for timing details.

21.6.5 TIMER1/3/5 GATE VALUE STATUS
When Timer1/3/5 Gate Value Status is utilized, it is possible to read the most current level of the gate signal. The value is stored in the GVAL bit in the TxGCON register. The GVAL bit is valid even when the Timer1/3/5 gate is not enabled (GE bit is cleared).

21.6.6 TIMER1/3/5 GATE EVENT INTERRUPT
When Timer1/3/5 Gate Event Interrupt is enabled, it is possible to generate an interrupt upon the completion of a gate event. When the falling edge of GVAL occurs, the TMRxGIF flag bit in the respective PIR register will be set. If the TMRxGIE bit in the respective PIE register is set, then an interrupt will be recognized.

The TMRxGIF flag bit operates even when the Timer1/3/5 gate is not enabled (GE bit is cleared).

For more information on selecting high or low priority status for the Timer1/3/5 Gate Event Interrupt see Section 9.0 “Interrupt Controller”.

Note: Enabling Toggle mode at the same time as changing the gate polarity may result in indeterminate operation.
21.7 Timer1/3/5 Interrupt

The Timer1/3/5 register pair (TMRxH:TMRxL) increments to FFFFh and rolls over to 0000h. When Timer1/3/5 rolls over, the Timer1/3/5 interrupt flag bit of the respective PIR register is set. To enable the interrupt-on-rollover, you must set these bits:

- ON bit of the TxCON register
- TMRxIE bits of the respective PIE register
- GIE/GIEH bit of the INTCON0 register

The interrupt is cleared by clearing the TMRxIF bit in the Interrupt Service Routine.

For more information on selecting high or low priority status for the Timer1/3/5 Overflow Interrupt, see Section 9.0 “Interrupt Controller”.

21.8 Timer1/3/5 Operation During Sleep

Timer1/3/5 can only operate during Sleep when set up in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- ON bit of the TxCON register must be set
- TMRxIE bit of the respective PIE register must be set
- SYNC bit of the TxCON register must be set
- Configure the TMRxCLK register for using secondary oscillator as the clock source
- Enable the SOSCEN bit of the OSCEN register (Register 7-7)

The device will wake-up on an overflow and execute the next instruction. If the GIE/GIEH bit of the INTCON0 register is set, the device will call the Interrupt Service Routine.

The secondary oscillator will continue to operate in Sleep regardless of the SYNC bit setting.

21.9 CCP Capture/Compare Time Base

The CCP modules use the TMRxH:TMRxL register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMRxH:TMRxL register pair is copied into the CCPRxH:CCPRxL register pair on a configured event.

In Compare mode, an event is triggered when the value in the CCPRxH:CCPRxL register pair matches the value in the TMRxH:TMRxL register pair. This event can be a Special Event Trigger.

For more information, see Section 23.0 “Capture/Compare/PWM Module”.

21.10 CCP Special Event Trigger

When any of the CCP’s are configured to trigger a special event, the trigger will clear the TMRxH:TMRxL register pair. This special event does not cause a Timer1/3/5 interrupt. The CCP module may still be configured to generate a CCP interrupt.

In this mode of operation, the CCPRxH:CCPRxL register pair becomes the period register for Timer1/3/5.

Timer1/3/5 should be synchronized and FOSC/4 should be selected as the clock source in order to utilize the Special Event Trigger. Asynchronous operation of Timer1/3/5 can cause a Special Event Trigger to be missed.

In the event that a write to TMRxH or TMRxL coincides with a Special Event Trigger from the CCP, the write will take precedence.

Note: The TMRxH:TMRxL register pair and the TMRxIF bit should be cleared before enabling interrupts.
FIGURE 21-3: TIMER1/3/5 INCREMENTING EDGE

<table>
<thead>
<tr>
<th>TxCKI</th>
<th>When TxTMR Enabled</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Arrows indicate counter increments.
2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

FIGURE 21-4: TIMER1/3/5 GATE ENABLE MODE
FIGURE 21-5: TIMER1/3/5 GATE TOGGLE MODE

TMRxGE
TxGPOL
TxGTM
TxTxG_IN
TxCKI
TxGVAL

TIMER1/3/5

N
N + 1
N + 2
N + 3
N + 4
N + 5
N + 6
N + 7
N + 8

FIGURE 21-6: TIMER1/3/5 GATE SINGLE-PULSE MODE

TMRxGE
TxGPOL
TxGSPM
TxGGO/
DONE
TxG_IN
TxCKI
TxGVAL

TIMER1/3/5

N
N + 1
N + 2

TMRxGIF

Cleared by software
Set by hardware on falling edge of TxGVAL
Cleared by software
Set by hardware on falling edge of TxGVAL
Set by software
Cleared by hardware on falling edge of TxGVAL
Counting enabled on rising edge of TxG
21.11 Peripheral Module Disable

When a peripheral module is not used or inactive, the module can be disabled by setting the Module Disable bit in the PMD registers. This will reduce power consumption to an absolute minimum. Setting the PMD bits holds the module in Reset and disconnects the module’s clock source. The Module Disable bits for Timer1 (TMR1MD), Timer3 (TMR3MD) and Timer5 (TMR5MD) are in the respective PMD registers. See Section 19.0 “Peripheral Module Disable (PMD)” for more information.
21.12 Register Definitions: Timer1/3/5

Long bit name prefixes for the Timer1/3/5 are shown below. Refer to Section 1.3.2.2 “Long Bit Names” for more information.

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Bit Name Prefix</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer1</td>
<td>T1</td>
</tr>
<tr>
<td>Timer3</td>
<td>T3</td>
</tr>
<tr>
<td>Timer5</td>
<td>T5</td>
</tr>
</tbody>
</table>

REGISTER 21-1: TXCON: TIMERx CONTROL REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/u</th>
<th>R/W-0/u</th>
<th>U-0</th>
<th>R/W-0/u</th>
<th>R/W-0/0</th>
<th>R/W-0/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>CKPS&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>SYNC</td>
<td>RD16</td>
<td>ON</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  u = unchanged

bit 7-6 Unimplemented: Read as ‘0’

bit 5-4 CKPS<1:0>: Timerx Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 Unimplemented: Read as ‘0’

bit 2 SYNC: Timerx External Clock Input Synchronization Control bit
TMRxCLK = FOSC/4 or FOSC:
This bit is ignored. Timer1 uses the incoming clock as is.
Else:
1 = Do not synchronize external clock input
0 = Synchronize external clock input with system clock

bit 1 RD16: 16-Bit Read/Write Mode Enable bit
1 = Enables register read/write of Timerx in one 16-bit operation
0 = Enables register read/write of Timerx in two 8-bit operation

bit 0 ON: Timerx On bit
1 = Enables Timerx
0 = Disables Timerx
### REGISTER 21-2: TxGCON: TIMERx GATE CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>GE</td>
<td>GPOL</td>
<td>GTM</td>
<td>GSPM</td>
<td>GGO/DONE</td>
<td>GVAL</td>
<td>—</td>
</tr>
<tr>
<td>R/W-0/u</td>
<td>R/W-0/u</td>
<td>R/W-0/u</td>
<td>R/W-0/u</td>
<td>R-x</td>
<td>U-0</td>
<td>U-0</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

#### Bit 7: GE
- **Timerx Gate Enable bit**
  - **If TMRxON = 1:**
    - 1 = Timerx counting is controlled by the Timerx gate function
    - 0 = Timerx is always counting
  - **If TMRxON = 0:**
    - This bit is ignored

#### Bit 6: GPOL
- **Timerx Gate Polarity bit**
  - 1 = Timerx gate is active-high (Timerx counts when gate is high)
  - 0 = Timerx gate is active-low (Timerx counts when gate is low)

#### Bit 5: GTM
- **Timerx Gate Toggle Mode bit**
  - 1 = Timerx Gate Toggle mode is enabled
  - 0 = Timerx Gate Toggle mode is disabled and Toggle flip-flop is cleared
  - Timerx Gate Flip Flop Toggles on every rising edge

#### Bit 4: GSPM
- **Timerx Gate Single Pulse Mode bit**
  - 1 = Timerx Gate Single Pulse mode is enabled and is controlling Timerx gate
  - 0 = Timerx Gate Single Pulse mode is disabled

#### Bit 3: GGO/DONE
- **Timerx Gate Single Pulse Acquisition Status bit**
  - 1 = Timerx Gate Single Pulse Acquisition is ready, waiting for an edge
  - 0 = Timerx Gate Single Pulse Acquisition has completed or has not been started.
  - This bit is automatically cleared when TxGSPM is cleared.

#### Bit 2: GVAL
- **Timerx Gate Current State bit**
  - Indicates the current state of the Timerx gate that could be provided to TMRxH:TMRxL
  - Unaffected by Timerx Gate Enable (TMRxGE)

#### Bit 1-0: Unimplemented
- Read as ‘0’
**REGISTER 21-3: TxCLK: TIMERx CLOCK REGISTER**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/u</th>
<th>R/W-0/u</th>
<th>R/W-0/u</th>
<th>R/W-0/u</th>
<th>R/W-0/u</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>CS&lt;4:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **-n** = Value at POR
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **u** = unchanged

**bit 7-5**  
**Unimplemented:** Read as ‘0’

**bit 4-0**  
**CS<4:0>: Timerx Clock Source Selection bits**

<table>
<thead>
<tr>
<th>CS</th>
<th>Timer1 Clock Source</th>
<th>Timer3 Clock Source</th>
<th>Timer5 Clock Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>11111=10001</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>10000</td>
<td>CLC4</td>
<td>CLC4</td>
<td>CLC4</td>
</tr>
<tr>
<td>01111</td>
<td>CLC3</td>
<td>CLC3</td>
<td>CLC3</td>
</tr>
<tr>
<td>01110</td>
<td>CLC2</td>
<td>CLC2</td>
<td>CLC2</td>
</tr>
<tr>
<td>01101</td>
<td>CLC1</td>
<td>CLC1</td>
<td>CLC1</td>
</tr>
<tr>
<td>01100</td>
<td>TMR5 overflow</td>
<td>TMR5 overflow</td>
<td>Reserved</td>
</tr>
<tr>
<td>01101</td>
<td>TMR3 overflow</td>
<td>Reserved</td>
<td>TMR3 overflow</td>
</tr>
<tr>
<td>01011</td>
<td>Reserved</td>
<td>TMR1 overflow</td>
<td>TMR1 overflow</td>
</tr>
<tr>
<td>01010</td>
<td>TMR0 overflow</td>
<td>TMR0 overflow</td>
<td>TMR0 overflow</td>
</tr>
<tr>
<td>01000</td>
<td>CLKREF</td>
<td>CLKREF</td>
<td>CLKREF</td>
</tr>
<tr>
<td>00111</td>
<td>SOSC</td>
<td>SOSC</td>
<td>SOSC</td>
</tr>
<tr>
<td>00110</td>
<td>MFINTOSC (32 kHz)</td>
<td>MFINTOSC (32 kHz)</td>
<td>MFINTOSC (32 kHz)</td>
</tr>
<tr>
<td>00101</td>
<td>MFINTOSC (500 kHz)</td>
<td>MFINTOSC (500 kHz)</td>
<td>MFINTOSC (500 kHz)</td>
</tr>
<tr>
<td>00100</td>
<td>LFINTOSC</td>
<td>LFINTOSC</td>
<td>LFINTOSC</td>
</tr>
<tr>
<td>00011</td>
<td>HFINTOSC</td>
<td>HFINTOSC</td>
<td>HFINTOSC</td>
</tr>
<tr>
<td>00010</td>
<td>Fosc</td>
<td>Fosc</td>
<td>Fosc</td>
</tr>
<tr>
<td>00001</td>
<td>Fosc/4</td>
<td>Fosc/4</td>
<td>Fosc/4</td>
</tr>
<tr>
<td>00000</td>
<td>T1CKIPPS</td>
<td>T3CKIPPS</td>
<td>T5CKIPPS</td>
</tr>
</tbody>
</table>
REGISTER 21-4: TxGATE: TIMERx GATE ISM REGISTER

<table>
<thead>
<tr>
<th>GSS</th>
<th>Timer1 Gate Source</th>
<th>Timer3 Gate Source</th>
<th>Timer5 Gate Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>11111-11011</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>11010</td>
<td>CLC4_out</td>
<td>CLC4_out</td>
<td>CLC4_out</td>
</tr>
<tr>
<td>11001</td>
<td>CLC3_out</td>
<td>CLC3_out</td>
<td>CLC3_out</td>
</tr>
<tr>
<td>11000</td>
<td>CLC2_out</td>
<td>CLC2_out</td>
<td>CLC2_out</td>
</tr>
<tr>
<td>10111</td>
<td>CLC1_out</td>
<td>CLC1_out</td>
<td>CLC1_out</td>
</tr>
<tr>
<td>10110</td>
<td>ZCDOUT</td>
<td>ZCDOUT</td>
<td>ZCDOUT</td>
</tr>
<tr>
<td>10101</td>
<td>CMP2OUT</td>
<td>CMP2OUT</td>
<td>CMP2OUT</td>
</tr>
<tr>
<td>10100</td>
<td>CMP1OUT</td>
<td>CMP1OUT</td>
<td>CMP1OUT</td>
</tr>
<tr>
<td>10011</td>
<td>NCO1OUT</td>
<td>NCO1OUT</td>
<td>NCO1OUT</td>
</tr>
<tr>
<td>10010-10001</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>10000</td>
<td>PWM8OUT</td>
<td>PWM8OUT</td>
<td>PWM8OUT</td>
</tr>
<tr>
<td>01111</td>
<td>PWM7OUT</td>
<td>PWM7OUT</td>
<td>PWM7OUT</td>
</tr>
<tr>
<td>01110</td>
<td>PWM6OUT</td>
<td>PWM6OUT</td>
<td>PWM6OUT</td>
</tr>
<tr>
<td>01101</td>
<td>PWM5OUT</td>
<td>PWM5OUT</td>
<td>PWM5OUT</td>
</tr>
<tr>
<td>01100</td>
<td>CCP4OUT</td>
<td>CCP4OUT</td>
<td>CCP4OUT</td>
</tr>
<tr>
<td>01011</td>
<td>CCP3OUT</td>
<td>CCP3OUT</td>
<td>CCP3OUT</td>
</tr>
<tr>
<td>01010</td>
<td>CCP2OUT</td>
<td>CCP2OUT</td>
<td>CCP2OUT</td>
</tr>
<tr>
<td>01001</td>
<td>CCP1OUT</td>
<td>CCP1OUT</td>
<td>CCP1OUT</td>
</tr>
<tr>
<td>01000</td>
<td>SMT1_match</td>
<td>SMT1_match</td>
<td>SMT1_match</td>
</tr>
<tr>
<td>00111</td>
<td>TMR6OUT (post-scaled)</td>
<td>TMR6OUT (post-scaled)</td>
<td>TMR6OUT (post-scaled)</td>
</tr>
<tr>
<td>00110</td>
<td>TMR5 overflow</td>
<td>TMR5 overflow</td>
<td>Reserved</td>
</tr>
<tr>
<td>00101</td>
<td>TMR4OUT (post-scaled)</td>
<td>TMR4OUT (post-scaled)</td>
<td>TMR4OUT (post-scaled)</td>
</tr>
<tr>
<td>00100</td>
<td>TMR3 overflow</td>
<td>Reserved</td>
<td>TMR3 overflow</td>
</tr>
<tr>
<td>00011</td>
<td>TMR2OUT (post-scaled)</td>
<td>TMR2OUT (post-scaled)</td>
<td>TMR2OUT (post-scaled)</td>
</tr>
<tr>
<td>00010</td>
<td>Reserved</td>
<td>TMR1 overflow</td>
<td>TMR1 overflow</td>
</tr>
<tr>
<td>00001</td>
<td>TMR0 overflow</td>
<td>TMR0 overflow</td>
<td>TMR0 overflow</td>
</tr>
<tr>
<td>00000</td>
<td>Pin selected by T1GPPS</td>
<td>Pin selected by T3GPPS</td>
<td>Pin selected by T5GPPS</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **u** = unchanged

bit 7-5 Unimplemented: Read as ‘0’

bit 4-0 GSS<4:0>: Timerx Gate Source Selection bits
REGISTER 21-5:  **TMRxL: TIMERx LOW BYTE REGISTER**

<table>
<thead>
<tr>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TMRxL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

<table>
<thead>
<tr>
<th>bit 7</th>
<th></th>
<th>bit 0</th>
<th></th>
</tr>
</thead>
</table>

* bit 7-0  **TMRxL<7:0>: Timerx Low Byte bits**

REGISTER 21-6:  **TMRxH: TIMERx HIGH BYTE REGISTER**

<table>
<thead>
<tr>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TMRxH&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

<table>
<thead>
<tr>
<th>bit 7</th>
<th></th>
<th>bit 0</th>
<th></th>
</tr>
</thead>
</table>

* bit 7-0  **TMRxH<7:0>: Timerx High Byte bits**
### TABLE 21-3: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1/3/5 AS A TIMER/COUNTER

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Reset Values on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>TxCON</td>
<td>—</td>
<td>—</td>
<td>CKPS&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>SYNC</td>
<td>RD16</td>
<td>ON</td>
<td>298</td>
</tr>
<tr>
<td>TxGCON</td>
<td>GE</td>
<td>GPOL</td>
<td>GTM</td>
<td>GSPM</td>
<td>GO/DONE</td>
<td>GVAL</td>
<td>—</td>
<td>—</td>
<td>299</td>
</tr>
<tr>
<td>TxCLK</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CS&lt;4:0&gt;</td>
<td>—</td>
<td>—</td>
<td>300</td>
</tr>
<tr>
<td>TxGATE</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>GSS&lt;4:0&gt;</td>
<td>—</td>
<td>—</td>
<td>301</td>
</tr>
<tr>
<td>TMRxL</td>
<td>Least Significant Byte of the 16-bit TMR3 Register</td>
<td>302</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMRxH</td>
<td>Holding Register for the Most Significant Byte of the 16-bit TMR3 Register</td>
<td>302</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:** — = Unimplemented location, read as ’0’. Shaded cells are not used by TIMER1/3/5.
22.0 TIMER2/4/6 MODULE

The Timer2/4/6 modules are 8-bit timers that can operate as free-running period counters or in conjunction with external signals that control start, run, freeze, and reset operation in One-Shot and Monostable modes of operation. Sophisticated waveform control such as pulse density modulation are possible by combining the operation of these timers with other internal peripherals such as the comparators and CCP modules. Features of the timer include:

- 8-bit timer register
- 8-bit period register
- Selectable external hardware timer resets
- Programmable prescaler (1:1 to 1:128)
- Programmable postscaler (1:1 to 1:16)
- Selectable synchronous/asynchronous operation
- Alternate clock sources
- Interrupt on period

Three modes of operation:
- Free Running Period
- One-Shot
- Monostable

See Figure 22-1 for a block diagram of Timer2. See Figure 22-2 for the clock source block diagram.

Note: Three identical Timer2 modules are implemented on this device. The timers are named Timer2, Timer4, and Timer6. All references to Timer2 apply as well to Timer4 and Timer6. All references to T2PR apply as well to T4PR and T6PR.

FIGURE 22-1: TIMER2 BLOCK DIAGRAM
22.1 Timer2 Operation

Timer2 operates in three major modes:
- Free Running Period
- One-Shot
- Monostable

Within each mode there are several options for starting, stopping, and reset. Table 22-1 lists the options.

In all modes the T2TMR count register is incremented on the rising edge of the clock signal from the programmable prescaler. When T2TMR equals T2PR then a high level is output to the postscaler counter. T2TMR is cleared on the next clock input.

An external signal from hardware can also be configured to gate the timer operation or force a T2TMR count Reset. In gate modes the counter stops when the gate is disabled and resumes when the gate is enabled. In Reset modes the T2TMR count is reset on either the level or edge from the external source.

The T2TMR and T2PR registers are both directly readable and writable. The T2TMR register is cleared and the T2PR register initializes to FFh on any device Reset. Both the prescaler and postscaler counters are cleared on the following events:
- a write to the T2TMR register
- a write to the TxCON register
- any device Reset
- External Reset Source event that resets the timer.

Note: T2TMR is not cleared when TxCON is written.

22.1.1 FREE RUNNING PERIOD MODE

The value of T2TMR is compared to that of the Period register, T2PR, on each clock cycle. When the two values match, the comparator resets the value of T2TMR to 00h on the next cycle and increments the output postscaler counter. When the postscaler count equals the value in the OUTPS bits of the TxCON register then a one clock period wide pulse occurs on the T2TMR_postscaled output, and the postscaler count is cleared.

22.1.2 ONE-SHOT MODE

The One-Shot mode is identical to the Free Running Period mode except that the ON bit is cleared and the timer is stopped when T2TMR matches T2PR and will not restart until the T2ON bit is cycled off and on. Postscaler OUTPS values other than 0 are meaningless in this mode because the timer is stopped at the first period event and the postscaler is reset when the timer is restarted.

22.1.3 MONOSTABLE MODE

Monostable modes are similar to One-Shot modes except that the ON bit is not cleared and the timer can be restarted by an external Reset event.

22.2 Timer2 Output

The Timer2 module’s primary output is T2TMR_postscaled, which pulses for a single T2TMR_clk period when the postscaler counter matches the value in the OUTPS bits of the TxCON register. The T2PR postscaler is incremented each time the T2TMR value matches the T2PR value. This signal can be selected as an input to several other input modules.

Timer2 is also used by the CCP module for pulse generation in PWM mode. Both the actual T2TMR value as well as other internal signals are sent to the CCP module to properly clock both the period and pulse width of the PWM signal. See Section 23.0 “Capture/Compare/PWM Module” for more details on setting up Timer2 for use with the CCP, as well as the timing diagrams in Section 22.5 “Operation Examples” for examples of how the varying Timer2 modes affect CCP PWM output.

22.3 External Reset Sources

In addition to the clock source, the Timer2 also takes in an external Reset source. This external Reset source is selected for Timer2, Timer4, and Timer6 with the T2RST, T4RST, and T6RST registers, respectively. This source can control starting and stopping of the timer, as well as resetting the timer, depending on which mode the timer is in. The mode of the timer is controlled by the MODE bits of the T2HLT register. Edge Triggered modes require six Timer clock periods between external triggers. Level Triggered modes require the triggering level to be at least three Timer clock periods long. External triggers are ignored while in Debug Freeze mode.
### TABLE 22-1: TIMER2 OPERATING MODES

<table>
<thead>
<tr>
<th>Mode</th>
<th>MODE&lt;4:0&gt;</th>
<th>Output Operation</th>
<th>Operation</th>
<th>Timer Control</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>&lt;4:3&gt;</td>
<td></td>
<td></td>
<td>Start</td>
</tr>
<tr>
<td></td>
<td>&lt;2:0&gt;</td>
<td></td>
<td></td>
<td>—</td>
</tr>
<tr>
<td>Free Running Period</td>
<td>000</td>
<td>Period Pulse</td>
<td>Software gate (Figure 22-6)</td>
<td>ON = 1</td>
</tr>
<tr>
<td></td>
<td>001</td>
<td>Period Pulse</td>
<td>Hardware gate, active-high (Figure 22-7)</td>
<td>ON = 1 &amp; TMRx_ers = 1</td>
</tr>
<tr>
<td></td>
<td>010</td>
<td></td>
<td>Hardware gate, active-low</td>
<td>ON = 1 &amp; TMRx_ers = 0</td>
</tr>
<tr>
<td></td>
<td>011</td>
<td>Period Pulse with Hardware Reset</td>
<td>Rising or Falling Edge Reset</td>
<td>ON = 1</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>Period Pulse</td>
<td>Rising Edge Reset (Figure 22-8)</td>
<td>ON = 1</td>
</tr>
<tr>
<td></td>
<td>101</td>
<td>Period Pulse</td>
<td>Falling Edge Reset</td>
<td>ON = 1</td>
</tr>
<tr>
<td></td>
<td>110</td>
<td>Period Pulse</td>
<td>Low Level Reset</td>
<td>ON = 1</td>
</tr>
<tr>
<td></td>
<td>111</td>
<td>Period Pulse</td>
<td>High Level Reset (Figure 22-9)</td>
<td>ON = 1</td>
</tr>
<tr>
<td>One-shot</td>
<td>000</td>
<td>One-Shot</td>
<td>Software Start (Figure 22-10)</td>
<td>ON = 1</td>
</tr>
<tr>
<td></td>
<td>001</td>
<td>One-Shot</td>
<td>Rising Edge Start (Figure 22-9)</td>
<td>ON = 1 &amp; TMRx_ers ↑</td>
</tr>
<tr>
<td></td>
<td>010</td>
<td>One-Shot</td>
<td>Falling Edge Start</td>
<td>ON = 1 &amp; TMRx_ers ↓</td>
</tr>
<tr>
<td></td>
<td>011</td>
<td>One-Shot</td>
<td>Any eEdge Start</td>
<td>ON = 1 &amp; TMRx_ers ↑</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>One-Shot</td>
<td>Rising Edge Start &amp; Rising Edge Reset (Figure 22-12)</td>
<td>ON = 1 &amp; TMRx_ers ↑</td>
</tr>
<tr>
<td></td>
<td>101</td>
<td>One-Shot</td>
<td>Falling Edge Start &amp; Falling Edge Reset</td>
<td>ON = 1 &amp; TMRx_ers ↓</td>
</tr>
<tr>
<td></td>
<td>110</td>
<td>One-Shot</td>
<td>Rising Edge Start &amp; Low Level Reset (Figure 22-13)</td>
<td>ON = 1 &amp; TMRx_ers ↑</td>
</tr>
<tr>
<td></td>
<td>111</td>
<td>One-Shot</td>
<td>Falling Edge Start &amp; High Level Reset</td>
<td>ON = 1 &amp; TMRx_ers ↓</td>
</tr>
<tr>
<td>Mono-stable</td>
<td>000</td>
<td>Reserved</td>
<td></td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>001</td>
<td>Mono-stable</td>
<td>Rising Edge Start (Figure 22-12)</td>
<td>ON = 1 &amp; TMRx_ers ↑</td>
</tr>
<tr>
<td></td>
<td>010</td>
<td>Mono-stable</td>
<td>Falling Edge Start</td>
<td>ON = 1 &amp; TMRx_ers ↓</td>
</tr>
<tr>
<td></td>
<td>011</td>
<td>Mono-stable</td>
<td>Any Edge Start</td>
<td>ON = 1 &amp; TMRx_ers ↑</td>
</tr>
<tr>
<td>Reserved</td>
<td>100</td>
<td>Reserved</td>
<td></td>
<td>—</td>
</tr>
<tr>
<td>Reserved</td>
<td>101</td>
<td>Reserved</td>
<td></td>
<td>—</td>
</tr>
<tr>
<td>One-shot</td>
<td>110</td>
<td>One-shot</td>
<td>Level Triggered Start and Hardware Reset (Figure 22-13)</td>
<td>ON = 1 &amp; TMRx_ers = 1</td>
</tr>
<tr>
<td>Reserved</td>
<td>111</td>
<td>One-shot</td>
<td>Low Level Start &amp; High Level Reset</td>
<td>ON = 1 &amp; TMRx_ers = 1</td>
</tr>
</tbody>
</table>

**Note:**
1. If ON = 0 then an edge is required to restart the timer after ON = 1.
2. When TxTMR = TxPR then the next clock clears ON and stops TxTMR at 00h.
3. When TxTMR = TxPR then the next clock stops TxTMR at 00h but does not clear ON.
22.4 Timer2 Interrupt

Timer2 can also generate a device interrupt. The interrupt is generated when the postscaler counter matches one of 16 postscale options (from 1:1 through 1:16), which is selected with the postscaler control bits, OUTPS of the T2CON register. The interrupt is enabled by setting the T2TMR Interrupt Enable bit, TMR2IE, of the respective PIE register. The interrupt timing is illustrated in Figure 22-3.

FIGURE 22-3: TIMER2 PRESCALER, POSTSCALER, AND INTERRUPT TIMING DIAGRAM

<table>
<thead>
<tr>
<th>CKPS</th>
<th>0b010</th>
</tr>
</thead>
<tbody>
<tr>
<td>TxPR</td>
<td>1</td>
</tr>
<tr>
<td>OUTPS</td>
<td>0b0001</td>
</tr>
<tr>
<td>TMRx_clk</td>
<td></td>
</tr>
<tr>
<td>TxTMR</td>
<td>0 1 0 1 0 1 0</td>
</tr>
<tr>
<td>TMRx_postscaled</td>
<td></td>
</tr>
<tr>
<td>TMRxIF</td>
<td>(1) (2) (3)</td>
</tr>
</tbody>
</table>

Note 1: Setting the interrupt flag is synchronized with the instruction clock. Synchronization may take as many as 2 instruction cycles

2: Cleared by software.
22.5 Operation Examples

Unless otherwise specified, the following notes apply to the following timing diagrams:

- Both the prescaler and postscaler are set to 1:1 (both the CKPS and OUTPS bits in the T2CON register are cleared).
- The diagrams illustrate any clock except FOSC/4 and show clock-sync delays of at least two full cycles for both ON and T2TMR_ers. When using FOSC/4, the clock-sync delay is at least one instruction period for T2TMR_ers; ON applies in the next instruction period.
- ON and T2TMR_ers are somewhat generalized, and clock-sync delays may produce results that are slightly different than illustrated.
- The PWM Duty Cycle and PWM output are illustrated assuming that the timer is used for the PWM function of the CCP module as described in Section 23.0 “Capture/Compare/PWM Module” and Section 24.0 “Pulse-Width Modulation (PWM)”.
  The signals are not a part of the T2TMR module.
22.5.1 SOFTWARE GATE MODE

The timer increments with each clock input when ON = 1 and does not increment when ON = 0. When the T2TMR count equals the T2PR period count the timer resets on the next clock and continues counting from 0. Operation with the ON bit software controlled is illustrated in Figure 22-4. With T2PR = 5, the counter advances until T2TMR = 5, and goes to zero with the next clock.

FIGURE 22-4: SOFTWARE GATE MODE TIMING DIAGRAM

Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.
22.5.2 HARDWARE GATE MODE

The Hardware Gate modes operate the same as the Software Gate mode except the T2TMR_ers external signal can also gate the timer. When used with the CCP the gating extends the PWM period. If the timer is stopped when the PWM output is high then the duty cycle is also extended.

When MODE<4:0> = 00001 then the timer is stopped when the external signal is high. When MODE<4:0> = 00010 then the timer is stopped when the external signal is low.

Figure 22-5 illustrates the Hardware Gating mode for MODE<4:0>= 00001 in which a high input level starts the counter.

**FIGURE 22-5: HARDWARE GATE MODE TIMING DIAGRAM (MODE = 00001)**
22.5.3 EDGE-TRIGGERED HARDWARE LIMIT MODE

In Hardware Limit mode the timer can be reset by the TMRx_ers external signal before the timer reaches the period count. Three types of Resets are possible:

- Reset on rising or falling edge (MODE<4:0> = 00011)
- Reset on rising edge (MODE<4:0> = 0010)
- Reset on falling edge (MODE<4:0> = 00101)

When the timer is used in conjunction with the CCP in PWM mode then an early Reset shortens the period and restarts the PWM pulse after a two clock delay. Refer to Figure 22-6.

FIGURE 22-6: EDGE TRIGGERED HARDWARE LIMIT MODE TIMING DIAGRAM (MODE=00100)

Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.
22.5.4 LEVEL-TRIGGERED HARDWARE LIMIT MODE

In the level triggered Hardware Limit Timer modes the counter is reset by high or low levels of the external signal TMR2_ers, as shown in Figure 22-7. Selecting MODE<4:0> = 00110 will cause the timer to reset on a low level external signal. Selecting MODE<4:0> = 00111 will cause the timer to reset on a high level external signal. In the example, the counter is reset while TMR2_ers = 1. ON is controlled by BSF and BCF instructions. When ON=0 the external signal is ignored.

When the CCP uses the timer as the PWM time base then the PWM output will be set high when the timer starts counting and then set low only when the timer count matches the CCPRx value. The timer is reset when either the timer count matches the T2PR value or two clock periods after the external Reset signal goes true and stays true.

The timer starts counting, and the PWM output is set high, on either the clock following the T2PR match or two clocks after the external Reset signal relinquishes the Reset. The PWM output will remain high until the timer counts up to match the CCPRx pulse width value. If the external Reset signal goes true while the PWM output is high then the PWM output will remain high until the Reset signal is released allowing the timer to count up to match the CCPRx value.

FIGURE 22-7: LEVEL TRIGGERED HARDWARE LIMIT MODE TIMING DIAGRAM (MODE = 00111)

<table>
<thead>
<tr>
<th>MODE</th>
<th>0b00111</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMRx_clk</td>
<td></td>
</tr>
<tr>
<td>TxPR</td>
<td>5</td>
</tr>
<tr>
<td>Instruction(1)</td>
<td>BSF</td>
</tr>
<tr>
<td>ON</td>
<td></td>
</tr>
<tr>
<td>TMRx_ers</td>
<td></td>
</tr>
<tr>
<td>TxTMR</td>
<td>0 1 2 3 4 5 0 0 1 2 3 4 5 0</td>
</tr>
<tr>
<td>TMRx_postscaled</td>
<td></td>
</tr>
<tr>
<td>PWM Duty Cycle</td>
<td>3</td>
</tr>
<tr>
<td>PWM Output</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.
22.5.5 SOFTWARE START ONE-SHOT MODE

In One-Shot mode the timer resets and the ON bit is cleared when the timer value matches the T2PR period value. The ON bit must be set by software to start another timer cycle. Setting MODE<4:0> = 01000 selects One-Shot mode which is illustrated in Figure 22-8. In the example, ON is controlled by BSF and BCF instructions. In the first case, a BSF instruction sets ON and the counter runs to completion and clears ON. In the second case, a BSF instruction starts the cycle, BCF/BSF instructions turn the counter off and on during the cycle, and then it runs to completion.

When One-Shot mode is used in conjunction with the CCP PWM operation the PWM pulse drive starts concurrent with setting the ON bit. Clearing the ON bit while the PWM drive is active will extend the PWM drive. The PWM drive will terminate when the timer value matches the CCPRx pulse width value. The PWM drive will remain off until software sets the ON bit to start another cycle. If software clears the ON bit after the CCPRx match but before the T2PR match then the PWM drive will be extended by the length of time the ON bit remains cleared. Another timing cycle can only be initiated by setting the ON bit after it has been cleared by a T2PR period count match.

FIGURE 22-8: SOFTWARE START ONE-SHOT MODE TIMING DIAGRAM (MODE = 01000)

Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.
22.5.6 EDGE-TRIGGERED ONE-SHOT MODE

The Edge-Triggered One-Shot modes start the timer on an edge from the external signal input, after the ON bit is set, and clear the ON bit when the timer matches the T2PR period value. The following edges will start the timer:
- Rising edge (MODE<4:0> = 01001)
- Falling edge (MODE<4:0> = 01010)
- Rising or Falling edge (MODE<4:0>='01011')

If the timer is halted by clearing the ON bit then another TMRx_ers edge is required after the ON bit is set to resume counting. Figure 22-9 illustrates operation in the rising edge One-Shot mode.

When Edge-Triggered One-Shot mode is used in conjunction with the CCP then the edge-trigger will activate the PWM drive and the PWM drive will deactivate when the timer matches the CCPRx pulse width value and stay deactivated when the timer halts at the T2PR period count match.

FIGURE 22-9: EDGE TRIGGERED ONE-SHOT MODE TIMING DIAGRAM (MODE = 01001)

Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.
22.5.7  EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE

In Edge-Triggered Hardware Limit One-Shot modes the timer starts on the first external signal edge after the ON bit is set and resets on all subsequent edges. Only the first edge after the ON bit is set is needed to start the timer. The counter will resume counting automatically two clocks after all subsequent external Reset edges. Edge triggers are as follows:

- Rising edge Start and Reset \( (\text{MODE}<4:0> = 01100) \)
- Falling edge Start and Reset \( (\text{MODE}<4:0> = 01101) \)

The timer resets and clears the ON bit when the timer value matches the T2PR period value. External signal edges will have no effect until after software sets the ON bit. Figure 22-10 illustrates the rising edge hardware limit one-shot operation.

When this mode is used in conjunction with the CCP then the first starting edge trigger, and all subsequent Reset edges, will activate the PWM drive. The PWM drive will deactivate when the timer matches the CCPRx pulse width value and stay deactivated until the timer halts at the T2PR period match unless an external signal edge resets the timer before the match occurs.

**FIGURE 22-10:  EDGE TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = 01100)**

Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.
22.5.8  LEVEL RESET, EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODES

In Level Triggered One-Shot mode the timer count is reset on the external signal level and starts counting on the rising/falling edge of the transition from reset level to the active level while the ON bit is set. Reset levels are selected as follows:

- Low reset level (MODE<4:0> = 01110)
- High reset level (MODE<4:0> = 01111)

When the timer count matches the T2PR period count, the timer is reset and the ON bit is cleared. When the ON bit is cleared by either a T2PR match or by software control a new external signal edge is required after the ON bit is set to start the counter.

When Level Triggered Reset One-Shot mode is used in conjunction with the CCP PWM operation the PWM drive goes active with the external signal edge that starts the timer. The PWM drive goes inactive when the timer count equals the CCPRx pulse-width count. The PWM drive does not go active when the timer count clears at the T2PR period count match.

Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.
22.5.9 EDGE-TRIGGERED MONOSTABLE MODES

The Edge-Triggered Monostable modes start the timer on an edge from the external Reset signal input, after the ON bit is set, and stop incrementing the timer when the timer matches the T2PR period value. The following edges will start the timer:

- Rising edge (MODE<4:0> = 10001)
- Falling edge (MODE<4:0> = 10010)
- Rising or Falling edge (MODE<4:0> = 10011)

When an Edge-Triggered Monostable mode is used in conjunction with the CCP PWM operation the PWM drive goes active with the external Reset signal edge that starts the timer, but will not go active when the timer matches the T2PR value. While the timer is incrementing, additional edges on the external Reset signal will not affect the CCP PWM.

FIGURE 22-12: RISING EDGE-TRIGGERED MONOSTABLE MODE TIMING DIAGRAM (MODE = 10001)

Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.
22.5.10 LEVEL-TRIGGERED HARDWARE LIMIT ONE-SHOT MODES

The Level Triggered Hardware Limit One-Shot modes hold the timer in Reset on an external Reset level and start counting when both the ON bit is set and the external signal is not at the Reset level. If one of either the external signal is not in reset or the ON bit is set then the other signal being set/made active will start the timer. Reset levels are selected as follows:
- Low reset level (MODE<4:0> = 10110)
- High reset level (MODE<4:0> = 10111)

When the timer count matches the T2PR period count, the timer is reset and the ON bit is cleared. When the ON bit is cleared by either a T2PR match or by software control the timer will stay in Reset until both the ON bit is set and the external signal is not at the Reset level.

When Level Triggered Hardware Limit One-Shot modes are used in conjunction with the CCP PWM operation the PWM drive goes active with either the external signal edge or the setting of the ON bit, whichever of the two starts the timer.

FIGURE 22-13: LEVEL-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = 10110)

Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.
22.6 Timer2 Operation During Sleep

When PSYNC = 1, Timer2 cannot be operated while the processor is in Sleep mode. The contents of the T2TMR and T2PR registers will remain unchanged while processor is in Sleep mode.

When PSYNC = 0, Timer2 will operate in Sleep as long as the clock source selected is also still running. Selecting the LFINTOSC, MFINTOSC, or HFINTOSC oscillator as the timer clock source will keep the selected oscillator running during Sleep.
22.7 Register Definitions: Timer2/4/6 Control

Long bit name prefixes for the Timer2/4/6 peripherals are shown in Table 22-2. Refer to Section 1.3.2.2 “Long Bit Names” for more information.

**TABLE 22-2: OPERATING MODES**

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Bit Name Prefix</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer2</td>
<td>T2</td>
</tr>
<tr>
<td>Timer4</td>
<td>T4</td>
</tr>
<tr>
<td>Timer6</td>
<td>T6</td>
</tr>
</tbody>
</table>

**REGISTER 22-1: TxCLK: TIMERx CLOCK SELECTION REGISTER**

<table>
<thead>
<tr>
<th></th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>CS&lt;3:0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>U-0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>U-0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>U-0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>R/W-0/0</td>
<td>U-0 U-0 U-0 U-0 R/W-0/0 R/W-0/0 R/W-0/0 R/W-0/0</td>
<td>CS&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**

R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared

**bit 7-4**  **Unimplemented**: Read as ‘0’

**bit 3-0**  **CS<3:0>**: Timerx Clock Selection bits

<table>
<thead>
<tr>
<th>CS&lt;3:0&gt;</th>
<th>T2MR Clock Source</th>
<th>TMR4 Clock Source</th>
<th>TMR6 Clock Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>1110</td>
<td>CLC4_out</td>
<td>CLC4_out</td>
<td>CLC4_out</td>
</tr>
<tr>
<td>1101</td>
<td>CLC3_out</td>
<td>CLC3_out</td>
<td>CLC3_out</td>
</tr>
<tr>
<td>1100</td>
<td>CLC2_out</td>
<td>CLC2_out</td>
<td>CLC2_out</td>
</tr>
<tr>
<td>1011</td>
<td>CLC1_out</td>
<td>CLC1_out</td>
<td>CLC1_out</td>
</tr>
<tr>
<td>1010</td>
<td>ZCD_OUT</td>
<td>ZCD_OUT</td>
<td>ZCD_OUT</td>
</tr>
<tr>
<td>1001</td>
<td>NCO1OUT</td>
<td>NCO1OUT</td>
<td>NCO1OUT</td>
</tr>
<tr>
<td>1000</td>
<td>CLKREF_OUT</td>
<td>CLKREF_OUT</td>
<td>CLKREF_OUT</td>
</tr>
<tr>
<td>0111</td>
<td>SOSC</td>
<td>SOSC</td>
<td>SOSC</td>
</tr>
<tr>
<td>0110</td>
<td>MFINTOSC (32 kHz)</td>
<td>MFINTOSC (32 kHz)</td>
<td>MFINTOSC (32 kHz)</td>
</tr>
<tr>
<td>0101</td>
<td>MFINTOSC (500 kHz)</td>
<td>MFINTOSC (500 kHz)</td>
<td>MFINTOSC (500 kHz)</td>
</tr>
<tr>
<td>0100</td>
<td>LFINTOSC</td>
<td>LFINTOSC</td>
<td>LFINTOSC</td>
</tr>
<tr>
<td>0011</td>
<td>HFINTOSC</td>
<td>HFINTOSC</td>
<td>HFINTOSC</td>
</tr>
<tr>
<td>0010</td>
<td>Fosc</td>
<td>Fosc</td>
<td>Fosc</td>
</tr>
<tr>
<td>0001</td>
<td>Fosc/4</td>
<td>Fosc/4</td>
<td>Fosc/4</td>
</tr>
<tr>
<td>0000</td>
<td>Pin selected by T2INPPS</td>
<td>Pin selected by T4INPPS</td>
<td>Pin selected by T6INPPS</td>
</tr>
</tbody>
</table>
REGISTER 22-2: TxRST: TIMER2 EXTERNAL RESET SIGNAL SELECTION REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>RSEL&lt;4:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

bit 7-5  **Unimplemented**: Read as ‘0’

bit 4-0  **RSEL<4:0>**: Timer2 External Reset Signal Source Selection bits

<table>
<thead>
<tr>
<th>RSEL&lt;4:0&gt;</th>
<th>T2TMR</th>
<th>TMR4</th>
<th>TMR6</th>
</tr>
</thead>
<tbody>
<tr>
<td>11111-11001</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>11000</td>
<td>UART2_tx_edge</td>
<td>UART2_tx_edge</td>
<td>UART2_tx_edge</td>
</tr>
<tr>
<td>10111</td>
<td>UART2_rx_edge</td>
<td>UART2_rx_edge</td>
<td>UART2_rx_edge</td>
</tr>
<tr>
<td>10110</td>
<td>UART1_tx_edge</td>
<td>UART1_tx_edge</td>
<td>UART1_tx_edge</td>
</tr>
<tr>
<td>10101</td>
<td>UART1_rx_edge</td>
<td>UART1_rx_edge</td>
<td>UART1_rx_edge</td>
</tr>
<tr>
<td>10100</td>
<td>CLC4_out</td>
<td>CLC4_out</td>
<td>CLC4_out</td>
</tr>
<tr>
<td>10011</td>
<td>CLC3_out</td>
<td>CLC3_out</td>
<td>CLC3_out</td>
</tr>
<tr>
<td>10010</td>
<td>CLC2_out</td>
<td>CLC2_out</td>
<td>CLC2_out</td>
</tr>
<tr>
<td>10001</td>
<td>CLC1_out</td>
<td>CLC1_out</td>
<td>CLC1_out</td>
</tr>
<tr>
<td>10000</td>
<td>ZCD_OUT</td>
<td>ZCD_OUT</td>
<td>ZCD_OUT</td>
</tr>
<tr>
<td>01111</td>
<td>CMP2OUT</td>
<td>CMP2OUT</td>
<td>CMP2OUT</td>
</tr>
<tr>
<td>01110</td>
<td>CMP1OUT</td>
<td>CMP1OUT</td>
<td>CMP1OUT</td>
</tr>
<tr>
<td>01101-01100</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>01011</td>
<td>PWM8OUT</td>
<td>PWM8OUT</td>
<td>PWM8OUT</td>
</tr>
<tr>
<td>01010</td>
<td>PWM7OUT</td>
<td>PWM7OUT</td>
<td>PWM7OUT</td>
</tr>
<tr>
<td>01001</td>
<td>PWM6OUT</td>
<td>PWM6OUT</td>
<td>PWM6OUT</td>
</tr>
<tr>
<td>01000</td>
<td>PWM5OUT</td>
<td>PWM5OUT</td>
<td>PWM5OUT</td>
</tr>
<tr>
<td>00111</td>
<td>CCP4OUT</td>
<td>CCP4OUT</td>
<td>CCP4OUT</td>
</tr>
<tr>
<td>00110</td>
<td>CCP3OUT</td>
<td>CCP3OUT</td>
<td>CCP3OUT</td>
</tr>
<tr>
<td>00101</td>
<td>CCP2OUT</td>
<td>CCP2OUT</td>
<td>CCP2OUT</td>
</tr>
<tr>
<td>00100</td>
<td>CCP1OUT</td>
<td>CCP1OUT</td>
<td>CCP1OUT</td>
</tr>
<tr>
<td>00011</td>
<td>TMR6 postscaled</td>
<td>TMR6 postscaled</td>
<td>Reserved</td>
</tr>
<tr>
<td>00010</td>
<td>TMR4 postscaled</td>
<td>Reserved</td>
<td>TMR4 postscaled</td>
</tr>
<tr>
<td>00001</td>
<td>Reserved</td>
<td>T2TMR postscaled</td>
<td>T2TMR postscaled</td>
</tr>
<tr>
<td>00000</td>
<td>Pin selected by T2INPPS</td>
<td>Pin selected by T4INPPS</td>
<td>Pin selected by T6INPPS</td>
</tr>
</tbody>
</table>
REGISTER 22-3:  TxTMR: TIMERx COUNTER REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td>R</td>
<td>W</td>
</tr>
<tr>
<td>bit 0</td>
<td>TMRx&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

bit 7-0  TMRx<7:0>: Timerx Counter bits

REGISTER 22-4:  TxPR: TIMERx PERIOD REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td>R</td>
</tr>
<tr>
<td>bit 0</td>
<td>PRx&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

bit 7-0  PRx<7:0>: Timerx Period Register bits
## REGISTER 22-5: TxCN: TIMERx CONTROL REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6-4</th>
<th>bit 3-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CKPS&lt;2:0&gt;</td>
<td>OUTPS&lt;3:0&gt;</td>
<td></td>
</tr>
<tr>
<td>ON</td>
<td>CKPS&lt;2:0&gt;</td>
<td>OUTPS&lt;3:0&gt;</td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **HC** = Bit is cleared by hardware

### Bit 7: ON: Timerx On bit(1)
- **1** = Timerx is On
- **0** = Timerx is Off: all counters and state machines are reset

### Bit 6-4: CKPS<2:0>: Timerx-type Clock Prescale Select bits
- **111** = 1:128 Prescaler
- **110** = 1:64 Prescaler
- **101** = 1:32 Prescaler
- **100** = 1:16 Prescaler
- **011** = 1:8 Prescaler
- **010** = 1:4 Prescaler
- **001** = 1:2 Prescaler
- **000** = 1:1 Prescaler

### Bit 3-0: OUTPS<3:0>: Timerx Output Postscaler Select bits
- **1111** = 1:16 Postscaler
- **1110** = 1:15 Postscaler
- **1101** = 1:14 Postscaler
- **1100** = 1:13 Postscaler
- **1011** = 1:12 Postscaler
- **1010** = 1:11 Postscaler
- **1001** = 1:10 Postscaler
- **1000** = 1:9 Postscaler
- **0111** = 1:8 Postscaler
- **0110** = 1:7 Postscaler
- **0101** = 1:6 Postscaler
- **0100** = 1:5 Postscaler
- **0011** = 1:4 Postscaler
- **0010** = 1:3 Postscaler
- **0001** = 1:2 Postscaler
- **0000** = 1:1 Postscaler

**Note 1:** In certain modes, the ON bit will be auto-cleared by hardware. See Section 22.1.2 “One-Shot Mode”.
### REGISTER 22-6: TxHLT: TIMERx HARDWARE LIMIT CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSYNC</td>
<td>CKPOL</td>
<td>CKSYNC</td>
<td>MODE&lt;4:0&gt;</td>
<td>bit 7</td>
<td>bit 6</td>
<td>bit 5</td>
<td>bit 4-0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**Legend:**
- **PSYNC**: Timerx Prescaler Synchronization Enable bit\(^{(1, 2)}\)
  - 1 = TxTMR Prescaler Output is synchronized to Fosc/4
  - 0 = TxTMR Prescaler Output is not synchronized to Fosc/4

**Legend:**
- **CKPOL**: Timerx Clock Polarity Selection bit\(^{(3)}\)
  - 1 = Falling edge of input clock clocks timer/prescaler
  - 0 = Rising edge of input clock clocks timer/prescaler

**Legend:**
- **CKSYNC**: Timerx Clock Synchronization Enable bit\(^{(4, 5)}\)
  - 1 = ON register bit is synchronized to T2TMR_clk input
  - 0 = ON register bit is not synchronized to T2TMR_clk input

**Legend:**
- **MODE<4:0>**: Timerx Control Mode Selection bits\(^{(6, 7)}\)
  - See Table 22-1 for all operating modes.

**Note 1:** Setting this bit ensures that reading TxTMR will return a valid data value.

**Note 2:** When this bit is ‘1’, Timer2 cannot operate in Sleep mode.

**Note 3:** CKPOL should not be changed while ON = 1.

**Note 4:** Setting this bit ensures glitch-free operation when the ON is enabled or disabled.

**Note 5:** When this bit is set then the timer operation will be delayed by two TxTMR input clocks after the ON bit is set.

**Note 6:** Unless otherwise indicated, all modes start upon ON = 1 and stop upon ON = 0 (stops occur without affecting the value of TxTMR).

**Note 7:** When TxTMR = TxPR, the next clock clears TxTMR, regardless of the operating mode.
### TABLE 22-3: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>TxPR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>305*</td>
</tr>
<tr>
<td>TxTMR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>305*</td>
</tr>
<tr>
<td>TxCON</td>
<td>ON</td>
<td>CKPS&lt;2:0&gt;</td>
<td></td>
<td>OUTPS&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>323</td>
</tr>
<tr>
<td>TxCLK</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CS&lt;2:0&gt;</td>
<td></td>
<td>320</td>
</tr>
<tr>
<td>TxRST</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>RSEL&lt;3:0&gt;</td>
<td></td>
<td>321</td>
</tr>
<tr>
<td>TxHLT</td>
<td>PSYNC</td>
<td>CPOL</td>
<td>CSYNC</td>
<td></td>
<td></td>
<td></td>
<td>MODE&lt;4:0&gt;</td>
<td></td>
<td>324</td>
</tr>
</tbody>
</table>

**Legend:**
- — = unimplemented location, read as ‘0’. Shaded cells are not used for Timer2 module.
- * Page provides register information.
23.0 CAPTURE/COMPARE/PWM MODULE

The Capture/Compare/PWM module is a peripheral that allows the user to time and control different events, and to generate Pulse-Width Modulation (PWM) signals. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate pulse-width modulated signals of varying frequency and duty cycle.

This family of devices contains four standard Capture/Compare/PWM modules (CCP1, CCP2, CCP3 and CCP4). Each individual CCP module can select the timer source that controls the module. Each module has an independent timer selection which can be accessed using the CxTSEL bits in the CCPTMRS0 register (Register 23-2). The default timer selection is TMR1 when using Capture/Compare mode and TMR2 when using PWM mode in the CCPx module.

Please note that the Capture/Compare mode operation is described with respect to TMR1 and the PWM mode operation is described with respect to TMR2 in the following sections.

The Capture and Compare functions are identical for all CCP modules.

23.1 CCP Module Configuration

Each Capture/Compare/PWM module is associated with a control register (CCPxCON), a capture input selection register (CCPxCAP) and a data register (CCPRx). The data register, in turn, is comprised of two 8-bit registers: CCPRxL (low byte) and CCPRxH (high byte).

23.1.1 CCP MODULES AND TIMER RESOURCES

The CCP modules utilize Timers 1 through 6 that vary with the selected mode. Various timers are available to the CCP modules in Capture, Compare or PWM modes, as shown in Table 23-1.

| CCP Mode | Timer Resource
|----------|----------------
| Capture  | Timer1, Timer3 or Timer5 |
| Compare  | Timer2, Timer4 or Timer6 |

The assignment of a particular timer to a module is determined by the timer to CCP enable bits in the CCPTMRS0 register (see Register 23-2). All of the modules may be active at once and may share the same timer resource if they are configured to operate in the same mode (Capture/Compare or PWM) at the same time.

23.1.2 OPEN-DRAIN OUTPUT OPTION

When operating in Output mode (the Compare or PWM modes), the drivers for the CCPx pins can be optionally configured as open-drain outputs. This feature allows the voltage level on the pin to be pulled to a higher level through an external pull-up resistor and allows the output to communicate with external circuits without the need for additional level shifters.

Note 1: In devices with more than one CCP module, it is very important to pay close attention to the register names used. A number placed after the module acronym is used to distinguish between separate modules. For example, the CCP1CON and CCP2CON control the same operational aspects of two completely different CCP modules.

2: Throughout this section, generic references to a CCP module in any of its operating modes may be interpreted as being equally applicable to CCPx module. Register names, module signals, I/O pins, and bit names may use the generic designator ‘x’ to indicate the use of a numeral to distinguish a particular module, when required.
23.2 Capture Mode

Capture mode makes use of the 16-bit Timer1 resource. When an event occurs on the capture source, the 16-bit CCPRxH:CCPRxL register pair captures and stores the 16-bit value of the TMRxH:TMRxL register pair, respectively. An event is defined as one of the following and is configured by the MODE<3:0> bits of the CCPxCON register:

- Every falling edge of CCPx input
- Every rising edge of CCPx input
- Every 4th rising edge of CCPx input
- Every 16th rising edge of CCPx input
- Every edge of CCPx input (rising or falling)

When a capture is made, the Interrupt Request Flag bit CCPxF of the respective PIR register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH:CCPRxL register pair is read, the old captured value is overwritten by the new captured value.

**Note:** If an event occurs during a 2-byte read, the high and low-byte data will be from different events. It is recommended while reading the CCPRxH:CCPRxL register pair to either disable the module or read the register pair twice for data integrity.

Figure 23-1 shows a simplified diagram of the capture operation.

23.2.1 CAPTURE SOURCES

In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

**Note:** If the CCPx pin is configured as an output, a write to the port can cause a capture condition.

The capture source is selected by configuring the CTS<2:0> bits of the CCPxCAP register. Refer to CCPxCAP register (Register 23-4) for a list of sources that can be selected.

23.2.2 TIMER1 MODE RESOURCE

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

- See Section 21.0 “Timer1/3/5 Module with Gate Control” for more information on configuring Timer1.

**Note:** Clocking Timer1 from the system clock (Fosc) should not be used in Capture mode. In order for Capture mode to recognize the trigger event on the CCPx pin, Timer1 must be clocked from the instruction clock (Fosc/4) or from an external clock source.
FIGURE 23-1: CAPTURE MODE OPERATION BLOCK DIAGRAM
23.2.3 SOFTWARE INTERRUPT MODE

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE Interrupt Priority bit of the respective PIE register clear to avoid false interrupts. Additionally, the user should clear the CCPxIF interrupt flag bit of the respective PIR register following any change in Operating mode.

23.2.4 CAPTURE DURING SLEEP

Capture mode depends upon the Timer1 module for proper operation. There are two options for driving the Timer1 module in Capture mode. It can be driven by the instruction clock (Fosc/4), or by an external clock source. When Timer1 is clocked by Fosc/4, Timer1 will not increment during Sleep. When the device wakes from Sleep, Timer1 will continue from its previous state. Capture mode will operate during Sleep as long as the clock source for Timer1 is active in Sleep.

23.3 Compare Mode

Compare mode makes use of the 16-bit Timer1 resource. The 16-bit value of the CCPRxH:CCPRxL register pair is constantly compared against the 16-bit value of the TMRxH:TMRxL register pair. When a match occurs, one of the following events can occur:

- Toggle the CCPx output, clear TMRx
- Toggle the CCPx output
- Set the CCPx output
- Clear the CCPx output
- Pulse output
- Pulse output, clear TMRx

The action on the pin is based on the value of the MODE<3:0> control bits of the CCPxCON register. At the same time, the interrupt flag CCPxIF bit is set, and an ADC conversion can be triggered, if selected.

All Compare modes can generate an interrupt and trigger an ADC conversion. When MODE = 0b0001 or 0b1011, the CCP resets the TMR register pair.

Figure 23-2 shows a simplified diagram of the compare operation.
23.3.1 CCPx PIN CONFIGURATION

The software must configure the CCPx pin as an output by clearing the associated TRIS bit and defining the appropriate output pin through the RxYPPS registers. See Section 17.0 “Peripheral Pin Select (PPS) Module” for more details.

Note: Clearing the CCPxCON register will force the CCPx compare output latch to the default low level. This is not the PORT I/O data latch.

23.3.2 TIMER1 MODE RESOURCE

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

See Section 21.0 “Timer1/3/5 Module with Gate Control” for more information on configuring Timer1.

Note: Clocking Timer1 from the system clock (Fosc) should not be used in Compare mode. In order for Compare mode to recognize the trigger event on the CCPx pin, Timer1 must be clocked from the instruction clock (Fosc/4) or from an external clock source.

23.3.3 AUTO-CONVERSION TRIGGER

All CCPx modes set the CCP interrupt flag (CCPxIF). When this flag is set and a match occurs, an auto-conversion trigger can take place if the CCP module is selected as the conversion trigger source.

Refer to Section 37.2.5 “Auto-Conversion Trigger” for more information.

Note: Removing the match condition by changing the contents of the CCPRxH and CCPRxL register pair, between the clock edge that generates the Auto-conversion Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.

23.3.4 COMPARE DURING SLEEP

Since FOSC is shut down during Sleep mode, the Compare mode will not function properly during Sleep, unless the timer is running. The device will wake on interrupt (if enabled).

23.4 PWM Overview

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully ON and fully OFF states. The PWM signal resembles a square wave where the high portion of the signal is considered the ON state and the low portion of the signal is considered the OFF state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse-width time and in turn the power that is applied to the load.

The term duty cycle describes the proportion of the on time to the off time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

Figure 23-3 shows a typical waveform of the PWM signal.

23.4.1 STANDARD PWM OPERATION

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCPx pin with up to ten bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- T2PR registers
- T2CON registers
- CCPRxH and CCPRxL registers
- CCPxRCON registers

It is required to have Fosc/4 as the clock input to TMR2/4/6 for correct PWM operation. Figure 23-4 shows a simplified block diagram of PWM operation.

Note: The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin.

FIGURE 23-3: CCP PWM OUTPUT SIGNAL

![Diagram of CCP PWM Output Signal]

Note: The diagram shows the relationship between the period, pulse width, and the CCPxCON registers.
FIGURE 23-4: SIMPLIFIED PWM BLOCK DIAGRAM

Notes:
1. 8-bit timer is concatenated with two bits generated by Fosc or two bits of the internal prescaler to create 10-bit time-base.
2. The alignment of the 10 bits from the CCPR register is determined by the CCPxFMT bit.
23.4.2 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for standard PWM operation:

1. Use the desired output pin RxyPPS control to select CCPx as the source and disable the CCPx pin output driver by setting the associated TRIS bit.
2. Load the T2PR register with the PWM period value.
3. Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
4. Load the CCPRxL register, and the CCPRxH register with the PWM duty cycle value and configure the FMT bit of the CCPxCON register to set the proper register alignment.
5. Configure and start Timer2:
   - Clear the TMR2IF interrupt flag bit of the respective PIR register. See Note below.
   - Select the timer clock source to be as Fos/4 using the T2CLK register. This is required for correct operation of the PWM module.
   - Configure the CKPS bits of the T2CON register with the Timer prescale value.
   - Enable the Timer by setting the ON bit of the T2CON register.
6. Enable PWM output pin:
   - Wait until the Timer overflows and the TMR2IF bit of the PIR4 register is set. See Note below.
   - Enable the CCPx pin output driver by clearing the associated TRIS bit.

23.4.3 TIMER2 TIMER RESOURCE

The PWM standard mode makes use of the 8-bit Timer2 timer resources to specify the PWM period.

23.4.4 PWM PERIOD

The PWM period is specified by the T2PR register of Timer2. The PWM period can be calculated using the formula of Equation 23-1.

**EQUATION 23-1: PWM PERIOD**

\[
\text{PWM Period} = \left(\frac{T2PR + 1}{4}\right) \cdot \frac{T_{OSC}}{T_{M2R \text{ Prescale Value}}}
\]

**Note 1:**

\[ T_{OSC} = \frac{1}{F_{OSC}} \]

When T2TMR is equal to T2PR, the following three events occur on the next increment cycle:

- T2TMR is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is transferred from the CCPRxL/H register pair into a 10-bit buffer.

**Note:** The Timer postscaler (see Section 22.3 “External Reset Sources”) is not used in the determination of the PWM frequency.

**Note:** In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.
23.4.5 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to the CCPRxH:CCPRxL register pair. The alignment of the 10-bit value is determined by the FMT bit of the CCPxCON register (see Figure 23-5). The CCPRxH:CCPRxL register pair can be written to at any time; however the duty cycle value is not latched into the 10-bit buffer until after a match between T2PR and T2TMR.

Equation 23-2 is used to calculate the PWM pulse width. Equation 23-3 is used to calculate the PWM duty cycle ratio.

**FIGURE 23-5: PWM 10-BIT ALIGNMENT**

![PWM 10-BIT ALIGNMENT Diagram]

**EQUATION 23-2: PULSE WIDTH**

\[
\text{Pulse Width} = (\text{CCPRxH:CCPRxL register pair}) \cdot \frac{T_{OSC}}{T_{MR2 \text{ Prescale Value}}}
\]

**EQUATION 23-3: DUTY CYCLE RATIO**

\[
\text{Duty Cycle Ratio} = \frac{(\text{CCPRxH:CCPRxL register pair})}{4(T2PR + 1)}
\]

CCPRxH:CCPRxL register pair are used to double buffer the PWM duty cycle. This double buffering provides glitchless PWM operation.

The 8-bit timer T2TMR register is concatenated with either the 2-bit internal system clock (Fosc), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH:CCPRxL register pair, then the CCPx pin is cleared (see Figure 23-4).

23.4.6 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is ten bits when T2PR is 255. The resolution is a function of the T2PR register value as shown by Equation 23-4.

**EQUATION 23-4: PWM RESOLUTION**

\[
\text{Resolution} = \log\left(\frac{4(T2PR + 1)}{\log(2)}\right)
\]

**Note:** If the pulse-width value is greater than the period, the assigned PWM pin(s) will remain unchanged.
23.4.7 OPERATION IN SLEEP MODE

In Sleep mode, the T2TMR register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, T2TMR will continue from its previous state.

23.4.8 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See Section 7.0 "Oscillator Module (with Fail-Safe Clock Monitor)" for additional details.

23.4.9 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

### TABLE 23-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 20 MHz)

<table>
<thead>
<tr>
<th>PWM Frequency</th>
<th>1.22 kHz</th>
<th>4.88 kHz</th>
<th>19.53 kHz</th>
<th>78.12 kHz</th>
<th>156.3 kHz</th>
<th>208.3 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer Prescale</td>
<td>16</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>T2PR Value</td>
<td>0xFF</td>
<td>0xFF</td>
<td>0xFF</td>
<td>0x3F</td>
<td>0x1F</td>
<td>0x17</td>
</tr>
<tr>
<td>Maximum Resolution (bits)</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>8</td>
<td>7</td>
<td>6.6</td>
</tr>
</tbody>
</table>

### TABLE 23-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 MHz)

<table>
<thead>
<tr>
<th>PWM Frequency</th>
<th>1.22 kHz</th>
<th>4.90 kHz</th>
<th>19.61 kHz</th>
<th>76.92 kHz</th>
<th>153.85 kHz</th>
<th>200.0 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer Prescale</td>
<td>16</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>T2PR Value</td>
<td>0x65</td>
<td>0x65</td>
<td>0x65</td>
<td>0x19</td>
<td>0x0C</td>
<td>0x09</td>
</tr>
<tr>
<td>Maximum Resolution (bits)</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>6</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>
### 23.5 Register Definitions: CCP Control

Long bit name prefixes for the CCP peripherals are shown below. Refer to Section 1.3.2.2 “Long Bit Names” for more information.

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Bit Name Prefix</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCP1</td>
<td>CCP1</td>
</tr>
<tr>
<td>CCP2</td>
<td>CCP2</td>
</tr>
<tr>
<td>CCP3</td>
<td>CCP3</td>
</tr>
<tr>
<td>CCP4</td>
<td>CCP4</td>
</tr>
</tbody>
</table>

#### REGISTER 23-1: CCPxCON: CCPx CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value at POR</th>
<th>Writeable</th>
<th>Readable</th>
<th>Unimplemented</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>EN: CCP Module Enable bit</td>
<td>1 = CCP is enabled</td>
<td>R</td>
<td>W</td>
<td>U</td>
</tr>
<tr>
<td>6</td>
<td>— Unimplemented</td>
<td>Read as ‘0’</td>
<td>U</td>
<td>R</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>OUT: CCPx Output Data bit (read-only)</td>
<td>'1' = Bit is set</td>
<td>U</td>
<td>R</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>FMT: CCPW (pulse-width) Alignment bit</td>
<td>MODE = Capture mode: Unused</td>
<td>R</td>
<td>W</td>
<td>U</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MODE = Compare mode: Unused</td>
<td>R</td>
<td>W</td>
<td>U</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MODE = PWM mode:</td>
<td>R</td>
<td>W</td>
<td>U</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Left-aligned format</td>
<td>R</td>
<td>W</td>
<td>U</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Right-aligned format</td>
<td>R</td>
<td>W</td>
<td>U</td>
</tr>
<tr>
<td>3-0</td>
<td>MODE&lt;3:0&gt;: CCPx Mode Select bits</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### MODE<3:0>: CCPx Mode Select bits

<table>
<thead>
<tr>
<th>MODE</th>
<th>Operating Mode</th>
<th>Operation</th>
<th>Set CCPxIF</th>
</tr>
</thead>
<tbody>
<tr>
<td>11xx</td>
<td>PWM</td>
<td>PWM operation</td>
<td>Yes</td>
</tr>
<tr>
<td>1011</td>
<td>Compare</td>
<td>Pulse output; clear TMR1&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>Yes</td>
</tr>
<tr>
<td>1010</td>
<td></td>
<td>Pulse output</td>
<td>Yes</td>
</tr>
<tr>
<td>1001</td>
<td></td>
<td>Clear output&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>Yes</td>
</tr>
<tr>
<td>1000</td>
<td></td>
<td>Set output&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>Yes</td>
</tr>
<tr>
<td>0111</td>
<td>Capture</td>
<td>Every 16th rising edge of CCPx input</td>
<td>Yes</td>
</tr>
<tr>
<td>0110</td>
<td></td>
<td>Every 4th rising edge of CCPx input</td>
<td>Yes</td>
</tr>
<tr>
<td>0101</td>
<td></td>
<td>Every rising edge of CCPx input</td>
<td>Yes</td>
</tr>
<tr>
<td>0100</td>
<td></td>
<td>Every falling edge of CCPx input</td>
<td>Yes</td>
</tr>
<tr>
<td>0011</td>
<td></td>
<td>Every edge of CCPx input</td>
<td>Yes</td>
</tr>
<tr>
<td>0010</td>
<td>Compare</td>
<td>Toggle output</td>
<td>Yes</td>
</tr>
<tr>
<td>0001</td>
<td></td>
<td>Toggle output; clear TMR1&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>Yes</td>
</tr>
<tr>
<td>0000</td>
<td>Disabled</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Note 1:** The set and clear operations of the Compare mode are reset by setting MODE = 4'b0000 or EN = 0.

**Note 2:** When MODE = 0001 or 1011, then the timer associated with the CCP module is cleared. TMR1 is the default selection for the CCP module, so it is used for indication purpose only.
## REGISTER 23-2: CCPTMRS0: CCP TIMERS CONTROL REGISTER 0

<table>
<thead>
<tr>
<th></th>
<th>R/W-0/0</th>
<th>R/W-1/1</th>
<th>R/W-0/0</th>
<th>R/W-1/1</th>
<th>R/W-0/0</th>
<th>R/W-1/1</th>
<th>R/W-0/0</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>C4TSEL&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C3TSEL&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C2TSEL&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C1TSEL&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 7-6</th>
<th>C4TSEL&lt;1:0&gt;: CCP4 Timer Selection bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>CCP4 is based off Timer5 in Capture/Compare mode and Timer6 in PWM mode</td>
</tr>
<tr>
<td>10</td>
<td>CCP4 is based off Timer3 in Capture/Compare mode and Timer4 in PWM mode</td>
</tr>
<tr>
<td>01</td>
<td>CCP4 is based off Timer1 in Capture/Compare mode and Timer2 in PWM mode</td>
</tr>
<tr>
<td>00</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 5-4</th>
<th>C3TSEL&lt;1:0&gt;: CCP3 Timer Selection bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>CCP3 is based off Timer5 in Capture/Compare mode and Timer6 in PWM mode</td>
</tr>
<tr>
<td>10</td>
<td>CCP3 is based off Timer3 in Capture/Compare mode and Timer4 in PWM mode</td>
</tr>
<tr>
<td>01</td>
<td>CCP3 is based off Timer1 in Capture/Compare mode and Timer2 in PWM mode</td>
</tr>
<tr>
<td>00</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 3-2</th>
<th>C2TSEL&lt;1:0&gt;: CCP2 Timer Selection bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>CCP2 is based off Timer5 in Capture/Compare mode and Timer6 in PWM mode</td>
</tr>
<tr>
<td>10</td>
<td>CCP2 is based off Timer3 in Capture/Compare mode and Timer4 in PWM mode</td>
</tr>
<tr>
<td>01</td>
<td>CCP2 is based off Timer1 in Capture/Compare mode and Timer2 in PWM mode</td>
</tr>
<tr>
<td>00</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 1-0</th>
<th>C1TSEL&lt;1:0&gt;: CCP1 Timer Selection bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>CCP1 is based off Timer5 in Capture/Compare mode and Timer6 in PWM mode</td>
</tr>
<tr>
<td>10</td>
<td>CCP1 is based off Timer3 in Capture/Compare mode and Timer4 in PWM mode</td>
</tr>
<tr>
<td>01</td>
<td>CCP1 is based off Timer1 in Capture/Compare mode and Timer2 in PWM mode</td>
</tr>
<tr>
<td>00</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
**REGISTER 23-3: CCPTMRS1: CCP TIMERS CONTROL REGISTER 1**

<table>
<thead>
<tr>
<th>Bit 7-6</th>
<th>P8TSEL&lt;1:0&gt;</th>
<th>Bit 5-4</th>
<th>P7TSEL&lt;1:0&gt;</th>
<th>Bit 3-2</th>
<th>P6TSEL&lt;1:0&gt;</th>
<th>Bit 1-0</th>
<th>P5TSEL&lt;1:0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>PWM8 based on TMR8</td>
<td>11</td>
<td>PWM7 based on TMR8</td>
<td>11</td>
<td>PWM6 based on TMR8</td>
<td>11</td>
<td>PWM5 based on TMR8</td>
</tr>
<tr>
<td>10</td>
<td>PWM8 based on TMR6</td>
<td>10</td>
<td>PWM7 based on TMR6</td>
<td>10</td>
<td>PWM6 based on TMR6</td>
<td>10</td>
<td>PWM5 based on TMR6</td>
</tr>
<tr>
<td>01</td>
<td>PWM8 based on TMR4</td>
<td>01</td>
<td>PWM7 based on TMR4</td>
<td>01</td>
<td>PWM6 based on TMR4</td>
<td>01</td>
<td>PWM5 based on TMR4</td>
</tr>
<tr>
<td>00</td>
<td>PWM8 based on TMR2</td>
<td>00</td>
<td>PWM7 based on TMR2</td>
<td>00</td>
<td>PWM6 based on TMR2</td>
<td>00</td>
<td>PWM5 based on TMR2</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown
**REGISTER 23-4: CCPxCAP: CAPTURE INPUT SELECTION MULTIPLEXER REGISTER**

<table>
<thead>
<tr>
<th>bit 7-3</th>
<th>bit 2-0</th>
<th>Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111-1001</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>1000</td>
<td>CAN_rx_timestamp</td>
<td></td>
</tr>
<tr>
<td>0111</td>
<td>CLC4_out</td>
<td></td>
</tr>
<tr>
<td>0110</td>
<td>CLC3_out</td>
<td></td>
</tr>
<tr>
<td>0101</td>
<td>CLC2_out</td>
<td></td>
</tr>
<tr>
<td>0100</td>
<td>CLC1_out</td>
<td></td>
</tr>
<tr>
<td>0011</td>
<td>IOC_Interrupt</td>
<td></td>
</tr>
<tr>
<td>0010</td>
<td>CMP2_output</td>
<td></td>
</tr>
<tr>
<td>0001</td>
<td>CMP1_output</td>
<td></td>
</tr>
<tr>
<td>0000</td>
<td>Pin selected by CCP1PPS</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pin selected by CCP2PPS</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pin selected by CCP3PPS</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pin selected by CCP4PPS</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**REGISTER 23-5: CCPRxL: CCPx REGISTER LOW BYTE**

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th>MODE = Capture Mode:</th>
</tr>
</thead>
<tbody>
<tr>
<td>RL&lt;7:0&gt;: LSb of captured TMR1 value</td>
<td></td>
</tr>
<tr>
<td>MODE = Compare Mode:</td>
<td></td>
</tr>
<tr>
<td>RL&lt;7:0&gt;: LSb compared to TMR1 value</td>
<td></td>
</tr>
<tr>
<td>MODE = PWM Mode &amp;&amp; FMT = 0:</td>
<td></td>
</tr>
<tr>
<td>RL&lt;7:0&gt;: CCPW&lt;7:0&gt; – Pulse-Width LS 8 bits</td>
<td></td>
</tr>
<tr>
<td>MODE = PWM Mode &amp;&amp; FMT = 1:</td>
<td></td>
</tr>
<tr>
<td>RL&lt;7:6&gt;: CCPW&lt;1:0&gt; – Pulse-Width LS 2 bits</td>
<td></td>
</tr>
<tr>
<td>RL&lt;5:0&gt;: Not used</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown
REGISTER 23-6: CCPRxH: CCPx REGISTER HIGH BYTE

<table>
<thead>
<tr>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RH&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7-0

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **-n** = Value at POR
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **x** = Bit is unknown

**bit 7-0**
- **MODE** = Capture Mode:
  - **RH<7:0>**: MSB of captured TMR1 value
- **MODE** = Compare Mode:
  - **RH<7:0>**: MSB compared to TMR1 value
- **MODE** = PWM Mode && **FMT** = 0:
  - **RH<7:2>**: Not used
- **MODE** = PWM Mode && **FMT** = 1:
  - **RH<7:0>**: CCPW<9:2> – Pulse-Width MS 8 bits

TABLE 23-4: SUMMARY OF REGISTERS ASSOCIATED WITH CCPx

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCPxCON</td>
<td>EN</td>
<td>—</td>
<td>OUT</td>
<td>FMT</td>
<td>MODE&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>335</td>
</tr>
<tr>
<td>CCPxCAP</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>338</td>
</tr>
<tr>
<td>CCPRxL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CTS&lt;1:0&gt;</td>
<td>338</td>
</tr>
<tr>
<td>CCPRxH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>339</td>
</tr>
<tr>
<td>CCPTMRS0</td>
<td>C4TSEL&lt;1:0&gt;</td>
<td>C3TSEL&lt;1:0&gt;</td>
<td>C2TSEL&lt;1:0&gt;</td>
<td>C1TSEL&lt;1:0&gt;</td>
<td>336</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **—** = Unimplemented location, read as '0'. Shaded cells are not used by the CCP module.
24.0 PULSE-WIDTH MODULATION (PWM)

The PWM module generates a pulse-width modulated signal determined by the duty cycle, period, and resolution that are configured by the following registers:

- TxPR
- TxCON
- PWMxDCH
- PWMxDCL
- PWMxCON

Note: The corresponding TRIS bit must be cleared to enable the PWM output on the PWMx pin.

Each PWM module can select the timer source that controls the module. Each module has an independent timer selection which can be accessed using the CCPTMR1 register (Register 23-2). Please note that the PWM mode operation is described with respect to T2TMR in the following sections.

Figure 24-1 shows a simplified block diagram of PWM operation.

Figure 24-2 shows a typical waveform of the PWM signal.

For a step-by-step procedure on how to set up this module for PWM operation, refer to Section 24.1.9 “Setup for PWM Operation using PWMx Pins”.

Note 1: 8-bit timer is concatenated with two bits generated by Fosc or two bits of the internal prescaler to create 10-bit time-base.
24.1 PWMx Pin Configuration

All PWM outputs are multiplexed with the PORT data latch. The user must configure the pins as outputs by clearing the associated TRIS bits.

24.1.1 FUNDAMENTAL OPERATION

The PWM module produces a 10-bit resolution output. The PWM timer can be selected using the PxTSEL bits in the CCPTMRS1 register. The default selection for PWMx is T2TMR. Please note that the PWM module operation in the following sections is described with respect to T2TMR. Timer2 and T2PR set the period of the PWM. The PWMxDCL and PWMxDCH registers configure the duty cycle. The period is common to all PWM modules, whereas the duty cycle is independently controlled.

Note: The Timer2 postscaler is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

All PWM outputs associated with Timer2 are set when T2TMR is cleared. Each PWMx is cleared when T2TMR is equal to the value specified in the corresponding PWMxDCH (8 MSb) and PWMxDCL<7:6> (2 LSb) registers. When the value is greater than or equal to T2PR, the PWM output is never cleared (100% duty cycle).

Note: The PWMxDCH and PWMxDCL registers are double buffered. The buffers are updated when Timer2 matches T2PR. Care should be taken to update both registers before the timer match occurs.

24.1.2 PWM OUTPUT POLARITY

The output polarity is inverted by setting the PWMxPOL bit of the PWMxCON register.

24.1.3 PWM PERIOD

The PWM period is specified by the T2PR register of Timer2. The PWM period can be calculated using the formula of Equation 24-1. It is required to have Fosc/4 as clock input to Timer2/4/6 for correct PWM operation.

EQUATION 24-1: PWM PERIOD

\[
PWM\ Period = \left[ \frac{(T2PR + 1) \times Tosc}{(TMR2\ Prescale\ Value)} \right]
\]

Note: Tosc = 1/Fosc

When T2TMR is equal to T2PR, the following three events occur on the next increment cycle:

- T2TMR is cleared
- The PWM output is active. (Exception: When the PWM duty cycle = 0%, the PWM output will remain inactive.)
- The PWMxDCH and PWMxDCL register values are latched into the buffers.

Note: The Timer2 postscaler has no effect on the PWM operation.

24.1.4 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to the PWMxDCH and PWMxDCL register pair. The PWMxDCH register contains the eight MSbs and the PWMxDCL<7:6>, the two LSbs. The PWMxDCH and PWMxDCL registers can be written to at any time. Equation 24-2 is used to calculate the PWM pulse width. Equation 24-3 is used to calculate the PWM duty cycle ratio.

EQUATION 24-2: PULSE WIDTH

\[
\text{Pulse Width} = (\text{PWMxDCHumerator} : \text{PWMxDenominator}<7:6>) \times Tosc \times (\text{TMR2\ Prescale\ Value})
\]

Note: Tosc = 1/Fosc

EQUATION 24-3: DUTY CYCLE RATIO

\[
\text{Duty Cycle Ratio} = \left( \frac{\text{PWMxDCHumerator} : \text{PWMxDenominator}<7:6>}{4(T2PR + 1)} \right)
\]

The 8-bit timer T2TMR register is concatenated with the two Least Significant bits of 1/Fosc, adjusted by the Timer2 prescaler to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.
24.1.5  PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is ten bits when T2PR is 255. The resolution is a function of the T2PR register value as shown by Equation 24-4.

**EQUATION 24-4: PWM RESOLUTION**

\[
\text{Resolution} = \frac{\log(4(T2PR + 1))}{\log(2)} \text{ bits}
\]

**Note:** If the pulse-width value is greater than the period, the assigned PWM pin(s) will remain unchanged.

### TABLE 24-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)

<table>
<thead>
<tr>
<th>PWM Frequency</th>
<th>0.31 kHz</th>
<th>4.88 kHz</th>
<th>19.53 kHz</th>
<th>78.12 kHz</th>
<th>156.3 kHz</th>
<th>208.3 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer Prescale</td>
<td>64</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>T2PR Value</td>
<td>0xFF</td>
<td>0xFF</td>
<td>0xFF</td>
<td>0x3F</td>
<td>0x1F</td>
<td>0x17</td>
</tr>
<tr>
<td>Maximum Resolution (bits)</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>8</td>
<td>7</td>
<td>6.6</td>
</tr>
</tbody>
</table>

### TABLE 24-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)

<table>
<thead>
<tr>
<th>PWM Frequency</th>
<th>0.31 kHz</th>
<th>4.90 kHz</th>
<th>19.61 kHz</th>
<th>76.92 kHz</th>
<th>153.85 kHz</th>
<th>200.0 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer Prescale</td>
<td>64</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>T2PR Value</td>
<td>0x65</td>
<td>0x65</td>
<td>0x65</td>
<td>0x19</td>
<td>0x0C</td>
<td>0x09</td>
</tr>
<tr>
<td>Maximum Resolution (bits)</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>6</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

24.1.6  OPERATION IN SLEEP MODE

In Sleep mode, the T2TMR register will not increment and the state of the module will not change. If the PWMx pin is driving a value, it will continue to drive that value. When the device wakes up, T2TMR will continue from its previous state.

24.1.7  CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency (Fosc). Any changes in the system clock frequency will result in changes to the PWM frequency. Refer to **Section 7.0 “Oscillator Module (with Fail-Safe Clock Monitor)”** for additional details.

24.1.8  EFFECTS OF RESET

Any Reset will force all ports to Input mode and the PWM registers to their Reset states.
24.1.9 SETUP FOR PWM OPERATION USING PWMx PINS

The following steps should be taken when configuring the module for PWM operation using the PWMx pins:

1. Disable the PWMx pin output driver(s) by setting the associated TRIS bit(s).
2. Clear the PWMxCON register.
3. Load the T2PR register with the PWM period value.
4. Load the PWMxDCH register and bits <7:6> of the PWMxDCL register with the PWM duty cycle value.
5. Configure and start Timer2:
   • Clear the TMR2IF interrupt flag bit of the respective PIR register. See Note 1 below.
   • Select the timer clock source to be as Fosc/4 using the TxCLK register. This is required for correct operation of the PWM module.
   • Configure the CKPS bits of the T2CON register with the Timer2 prescale value.
   • Enable Timer2 by setting the ON bit of the T2CON register.
6. Enable PWM output pin and wait until Timer2 overflows, TMR2IF bit of the respective PIR register is set. See Note 1 below.
7. Enable the PWMx pin output driver(s) by clearing the associated TRIS bit(s) and setting the desired pin PPS control bits.
8. Configure the PWM module by loading the PWMxCON register with the appropriate values.

24.1.10 SETUP FOR PWM OPERATION TO OTHER DEVICE PERIPHERALS

The following steps should be taken when configuring the module for PWM operation to be used by other device peripherals:

1. Disable the PWMx pin output driver(s) by setting the associated TRIS bit(s).
2. Clear the PWMxCON register.
3. Load the T2PR register with the PWM period value.
4. Load the PWMxDCH register and bits <7:6> of the PWMxDCL register with the PWM duty cycle value.
5. Configure and start Timer2:
   • Clear the TMR2IF interrupt flag bit of the respective PIR register. See Note 1 below.
   • Select the timer clock source to be as Fosc/4 using the TxCLK register. This is required for correct operation of the PWM module.
   • Configure the CKPS bits of the T2CON register with the Timer2 prescale value.
   • Enable Timer2 by setting the ON bit of the T2CON register.
6. Enable PWM output pin:
   • Wait until Timer2 overflows, TMR2IF bit of the respective PIR register is set. See Note 1 below.
7. Configure the PWM module by loading the PWMxCON register with the appropriate values.

Note 1: In order to send a complete duty cycle and period on the first PWM output, the above steps must be followed in the order given. If it is not critical to start with a complete PWM signal, then move Step 8 to replace Step 4.

Note 2: For operation with other peripherals only, disable PWMx pin outputs.
24.2 Register Definitions: PWM Control

Long bit name prefixes for the PWM peripherals are shown below. Refer to Section 1.3.2.2 “Long Bit Names” for more information.

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Bit Name Prefix</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM3</td>
<td>PWM3</td>
</tr>
<tr>
<td>PWM4</td>
<td>PWM4</td>
</tr>
</tbody>
</table>

REGISTER 24-1: PWMxCON: PWM CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td></td>
<td>OUT</td>
<td>POL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

<table>
<thead>
<tr>
<th>bit 7</th>
<th>EN: PWM Module Enable bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PWM module is enabled</td>
</tr>
<tr>
<td>0</td>
<td>PWM module is disabled</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 6</th>
<th>Unimplemented: Read as ‘0’</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>bit 5</th>
<th>OUT: PWM Module Output Level When Bit is Read</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>bit 4</th>
<th>POL: PWM Output Polarity Select bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PWM output is inverted</td>
</tr>
<tr>
<td>0</td>
<td>PWM output is normal</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 3-0</th>
<th>Unimplemented: Read as ‘0’</th>
</tr>
</thead>
</table>
## REGISTER 24-2: CCPTMRS1: CCP TIMERS CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>P8TSEL&lt;1:0&gt;</th>
<th>P7TSEL&lt;1:0&gt;</th>
<th>P6TSEL&lt;1:0&gt;</th>
<th>P5TSEL&lt;1:0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>R/W-0/0</td>
<td>R/W-1/1</td>
<td>R/W-0/0</td>
<td>R/W-1/1</td>
</tr>
<tr>
<td>6</td>
<td>R/W-0/0</td>
<td>R/W-1/1</td>
<td>R/W-0/0</td>
<td>R/W-1/1</td>
</tr>
<tr>
<td>5</td>
<td>R/W-0/0</td>
<td>R/W-1/1</td>
<td>R/W-0/0</td>
<td>R/W-1/1</td>
</tr>
<tr>
<td>4</td>
<td>R/W-0/0</td>
<td>R/W-1/1</td>
<td>R/W-0/0</td>
<td>R/W-1/1</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

- **P8TSEL<1:0>: PWM8 Timer Selection bits**
  - 11 = PWM8 based on TMR6
  - 10 = PWM8 based on TMR4
  - 01 = PWM8 based on TMR2
  - 00 = Reserved

- **P7TSEL<1:0>: PWM7 Timer Selection bits**
  - 11 = PWM7 based on TMR6
  - 10 = PWM7 based on TMR4
  - 01 = PWM7 based on TMR2
  - 00 = Reserved

- **P6TSEL<1:0>: PWM6 Timer Selection bits**
  - 11 = PWM6 based on TMR6
  - 10 = PWM6 based on TMR4
  - 01 = PWM6 based on TMR2
  - 00 = Reserved

- **P5TSEL<1:0>: PWM5 Timer Selection bits**
  - 11 = PWM5 based on TMR6
  - 10 = PWM5 based on TMR4
  - 01 = PWM5 based on TMR2
  - 00 = Reserved
REGISTER 24-3: PWMxDCH: PWM DUTY CYCLE HIGH BITS

| Bit 7-0 | DC<9:2> | bit 7-0 DC<9:2>: PWM Duty Cycle Most Significant bits  
These bits are the MSbs of the PWM duty cycle. The two LSbs are found in PWMxDCL Register.

REGISTER 24-4: PWMxDCL: PWM DUTY CYCLE LOW BITS

| Bit 7-6 | DC<1:0> | bit 7-6 DC<1:0>: PWM Duty Cycle Least Significant bits  
These bits are the LSbs of the PWM duty cycle. The MSbs are found in PWMxDCH Register.

bit 5-0 Unimplemented: Read as ‘0’

TABLE 24-3: SUMMARY OF REGISTERS ASSOCIATED WITH PWM

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWMxCON</td>
<td>EN</td>
<td>—</td>
<td>OUT</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>344</td>
</tr>
<tr>
<td>PWMxDCH</td>
<td></td>
<td></td>
<td>DC&lt;9:2&gt;</td>
<td></td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>346</td>
</tr>
<tr>
<td>PWMxDCL</td>
<td>DC&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>346</td>
</tr>
<tr>
<td>CCPTMRS1</td>
<td>P8TSEL&lt;1:0&gt;</td>
<td>P7TSEL&lt;1:0&gt;</td>
<td>P6TSEL&lt;1:0&gt;</td>
<td>P5TSEL&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>345</td>
</tr>
</tbody>
</table>

Legend: - = Unimplemented locations, read as ‘0’, u = unchanged, x = unknown. Shaded cells are not used by the PWM.
25.0 SIGNAL MEASUREMENT TIMER (SMTx)

The SMT is a 24-bit counter with advanced clock and gating logic, which can be configured for measuring a variety of digital signal parameters such as pulse width, frequency and duty cycle, and the time difference between edges on two signals. The device has only one SMT module implemented.

Features of the SMT include:

- 24-bit timer/counter
  - Three 8-bit registers (SMTxL/H/U)
  - Readable and writable
  - Optional 16-bit operating mode

- Two 24-bit measurement capture registers
- One 24-bit period match register
- Multi-mode operation, including relative timing measurement
- Interrupt on period match
- Multiple clock, gate and signal sources
- Interrupt on acquisition complete
- Ability to read current input values
FIGURE 25-1: SMT BLOCK DIAGRAM

FIGURE 25-2: SMT SIGNAL AND WINDOW BLOCK DIAGRAM
25.1 SMT Operation

The core of the module is the 24-bit counter, SMTxTMR combined with a complex data acquisition front-end. Depending on the mode of operation selected, the SMT can perform a variety of measurements summarized in Table 25-1.

25.1.1 CLOCK SOURCES

Clock sources available to the SMT include:

- Fosc
- Fosc/4
- HFINTOSC 16 MHz
- LFINTOSC
- MFINTOSC 31.25 kHz

The SMT clock source is selected by configuring the CSEL<2:0> bits in the SMTxCLK register. The clock source can also be prescaled using the PS<1:0> bits of the SMTxCON0 register. The prescaled clock source is used to clock both the counter and any synchronization logic used by the module.

25.1.2 PERIOD MATCH INTERRUPT

Similar to other timers, the SMT triggers an interrupt when SMTxTMR rolls over to '0'. This happens when SMTxTMR = SMTxPR, regardless of mode. Hence, in any mode that relies on an external signal or a window to reset the timer, proper operation requires that SMTxPR be set to a period larger than that of the expected signal or window.

25.2 Basic Timer Function Registers

The SMTxTMR time base and the SMTxCPW/SMTxPR/SMTxCPR buffer registers serve several functions and can be manually updated using software.

25.2.1 TIME BASE

The SMTxTMR is the 24-bit counter that is the center of the SMT. It is used as the basic counter/timer for measurement in each of the modes of the SMT. It can be reset to a value of 24'h00_0000 by setting the RST bit of the SMTxSTAT register. It can be written to and read from software, but it is not guarded for atomic access, therefore reads and writes to the SMTxTMR should only be made when the GO = 0, or the software should have other measures to ensure integrity of SMTxTMR reads/writes.

25.2.2 PULSE-WIDTH LATCH REGISTERS

The SMTxCPW registers are the 24-bit SMT pulse-width latch. They are used to latch in the value of the SMTxTMR when triggered by various signals, which are determined by the mode the SMT is currently in. The SMTxCPW registers can also be updated with the current value of the SMTxTMR value by setting the CPWUP bit of the SMTxSTAT register.

25.2.3 PERIOD LATCH REGISTERS

The SMTxCPR registers are the 24-bit SMT period latch. They are used to latch in other values of the SMTxTMR when triggered by various other signals, which are determined by the mode the SMT is currently in.

The SMTxCPR registers can also be updated with the current value of the SMTxTMR value by setting the CPRUP bit in the SMTxSTAT register.

25.3 Halt Operation

The counter can be prevented from rolling-over using the STP bit in the SMTxCON0 register. When halting is enabled, the period match interrupt persists until the SMTxTMR is reset (either by a manual Reset, Section 25.2.1 "Time Base") or by clearing the GO bit of the SMTxCON1 register and writing the SMTxTMR values in software.

25.4 Polarity Control

The three input signals for the SMT have polarity control to determine whether or not they are active-high/positive edge or active-low/negative edge signals.

The following bits apply to Polarity Control:

- WSEL bit (Window Polarity)
- SSEL bit (Signal Polarity)
- CSEL bit (Clock Polarity)

These bits are located in the SMTxCON0 register.

25.5 Status Information

The SMT provides input status information for the user without requiring the need to deal with the polarity of the incoming signals.

25.5.1 WINDOW STATUS

Window status is determined by the WS bit of the SMTxSTAT register. This bit is only used in Windowed Measure, Gated Counter and Gated Window Measure modes, and is only valid when TS = 1, and will be delayed in time by synchronizer delays in non-Counter modes.

25.5.2 SIGNAL STATUS

Signal status is determined by the AS bit of the SMTxSTAT register. This bit is used in all modes except Window Measure, Time of Flight and Capture modes, and is only valid when TS = 1, and will be delayed in time by synchronizer delays in non-Counter modes.

25.5.3 GO STATUS

Timer run status is determined by the TS bit of the SMTxSTAT register, and will be delayed in time by synchronizer delays in non-Counter modes.
25.6 Modes of Operation

The modes of operation are summarized in Table 25-1. The following sections provide detailed descriptions, examples of how the modes can be used. Note that all waveforms assume WPOL/SPOL/CPOL = 0. When WPOL/SPOL/CPOL = 1, all SMTSIGx, SMTWINx and SMT clock signals will have a polarity opposite to that indicated. For all modes, the REPEAT bit controls whether the acquisition is repeated or single. When REPEAT = 0 (Single Acquisition mode), the timer will stop incrementing and the GO bit will be reset upon the completion of an acquisition. Otherwise, the timer will continue and allow for continued acquisitions to overwrite the previous ones until the timer is stopped in software.

25.6.1 TIMER MODE

Timer mode is the simplest mode of operation where the SMTxTMR is used as a 16/24-bit timer. No data acquisition takes place in this mode. The timer increments as long as the GO bit has been set by software. No SMT window or SMT signal events affect the GO bit. Everything is synchronized to the SMT clock source. When the timer experiences a period match (SMTxTMR = SMTxPR), SMTxTMR is reset and the period match interrupt trips. See Figure 25-3.

<table>
<thead>
<tr>
<th>MODE</th>
<th>Mode of Operation</th>
<th>Synchronous Operation</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>Timer</td>
<td>Yes</td>
<td>Section 25.6.1 “Timer Mode”</td>
</tr>
<tr>
<td>0001</td>
<td>Gated Timer</td>
<td>Yes</td>
<td>Section 25.6.2 “Gated Timer Mode”</td>
</tr>
<tr>
<td>0010</td>
<td>Period and Duty Cycle Acquisition</td>
<td>Yes</td>
<td>Section 25.6.3 “Period and Duty Cycle Mode”</td>
</tr>
<tr>
<td>0011</td>
<td>High and Low Time Measurement</td>
<td>Yes</td>
<td>Section 25.6.4 “High and Low Measure Mode”</td>
</tr>
<tr>
<td>0100</td>
<td>Windowed Measurement</td>
<td>Yes</td>
<td>Section 25.6.5 “Windowed Measure Mode”</td>
</tr>
<tr>
<td>0101</td>
<td>Gated Windowed Measurement</td>
<td>Yes</td>
<td>Section 25.6.6 “Gated Windowed Measure Mode”</td>
</tr>
<tr>
<td>0110</td>
<td>Time of Flight</td>
<td>Yes</td>
<td>Section 25.6.7 “Time of Flight Measure Mode”</td>
</tr>
<tr>
<td>0111</td>
<td>Capture</td>
<td>Yes</td>
<td>Section 25.6.8 “Capture Mode”</td>
</tr>
<tr>
<td>1000</td>
<td>Counter</td>
<td>No</td>
<td>Section 25.6.9 “Counter Mode”</td>
</tr>
<tr>
<td>1001</td>
<td>Gated Counter</td>
<td>No</td>
<td>Section 25.6.10 “Gated Counter Mode”</td>
</tr>
<tr>
<td>1010</td>
<td>Windowed Counter</td>
<td>No</td>
<td>Section 25.6.11 “Windowed Counter Mode”</td>
</tr>
<tr>
<td>1011-1111</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>
FIGURE 25-3: TIMER MODE TIMING DIAGRAM

- SMTx Clock
- SMTxEN
- SMTxGO
- SMTxGO_sync
- SMTxPR
- SMTxTMR
- SMTxF
25.6.2 GATED TIMER MODE

Gated Timer mode uses the SMTSIGx input to control whether or not the SMTxTMR will increment. Upon a falling edge of the external signal, the SMTxCPW register will update to the current value of the SMTxTMR. Example waveforms for both repeated and single acquisitions are provided in Figure 25-4 and Figure 25-5.
FIGURE 25-4:  GATED TIMER MODE REPEAT ACQUISITION TIMING DIAGRAM
FIGURE 25-5: GATED TIMER MODE SINGLE ACQUISITION TIMING DIAGRAM

- SMTx_signal
- SMTx_signalsync
- SMTx_Clock
- SMTxEN
- SMTxGO
- SMTxGO_sync
- SMTxPR
- 0xFFFFFFF
- SMTxTMR
- 0
- 1 2 3 4 5
- SMTxCPW
- 5
- SMTxPWAIF
25.6.3 PERIOD AND DUTY CYCLE MODE

In Duty Cycle mode, either the duty cycle or period (depending on polarity) of the SMTx_signal can be acquired relative to the SMT clock. The CPW register is updated on a falling edge of the signal, and the CPR register is updated on a rising edge of the signal, along with the SMTxTMR resetting to 0x0001. In addition, the GO bit is reset on a rising edge when the SMT is in Single Acquisition mode. See Figure 25-6 and Figure 25-7.
FIGURE 25-6: PERIOD AND DUTY-CYCLE REPEAT ACQUISITION MODE TIMING DIAGRAM

SMTx_signal
SMTx_signal_sync
SMTx_Clock
SMTxEN
SMTxGO
SMTxGO_sync
SMTxTMR
0 1 2 3 4 5 6 7 8 9 10 11 1 2 3 4 5
SMTxCPW
5 2
SMTxCPR
11
SMTxPWAIF
SMTxPRAIF
FIGURE 25-7: PERIOD AND DUTY-CYCLE SINGLE ACQUISITION TIMING DIAGRAM
25.6.4 HIGH AND LOW MEASURE MODE

This mode measures the high and low pulse time of the SMTSIGx relative to the SMT clock. It begins incrementing the SMTxTMR on a rising edge on the SMTSIGx input, then updates the SMTxCPW register with the value and resets the SMTxTMR on a falling edge, starting to increment again. Upon observing another rising edge, it updates the SMTxCPR register with its current value and once again resets the SMTxTMR value and begins incrementing again. See Figure 25-8 and Figure 25-9.
FIGURE 25-8: HIGH AND LOW MEASURE MODE REPEAT ACQUISITION TIMING DIAGRAM

SMTx_signal
SMTx_signalsync
SMTx Clock
SMTxEN
SMTxGO
SMTxGO_sync
SMTxTMR
SMTxCPW
SMTxCPR
SMTxPWAIF
SMTxPRAIF

0 1 2 3 4 5 1 2 3 4 5 6 1 2 1 2 3
5 2
6
FIGURE 25-9: HIGH AND LOW MEASURE MODE SINGLE ACQUISITION TIMING DIAGRAM

SMTx_signal
SMTx_signalsync
SMTx_Clock
SMTxEN
SMTxGO
SMTxGO_sync
SMTxTMR
SMTxCPW
SMTxCPR
SMTxPWAIF
SMTxPRAIF
25.6.5  WINDOWED MEASURE MODE

This mode measures the window duration of the SMTWINx input of the SMT. It begins incrementing the timer on a rising edge of the SMTWINx input and updates the SMTxCPR register with the value of the timer and resets the timer on a second rising edge. See Figure 25-10 and Figure 25-11.
FIGURE 25-10: WINDOWED MEASURE MODE REPEAT ACQUISITION TIMING DIAGRAM

SMTxWIN
SMTxWIN_sync
SMTx Clock
SMTxEN
SMTxGO
SMTxGO_sync
SMTxTMR
0 1 2 3 4 5 6 7 8 9 10 11 12 1 2 3 4 5 6 7 8 1 2 3 4
SMTxCPR
SMTxPRAIF
12
8
FIGURE 25-11: WINDOWED MEASURE MODE SINGLE ACQUISITION TIMING DIAGRAM

SMTxWIN
SMTxWIN_sync
SMTx Clock
SMTxEN
SMTxGO
SMTxGO_sync
SMTxTMR
SMTxCPR
SMTxPRAIF

0 1 2 3 4 5 6 7 8 9 10 11 12

12
25.6.6  GATED WINDOWED MEASURE MODE

This mode measures the duty cycle of the SMTx_signal input over a known input window. It does so by incrementing the timer on each pulse of the clock signal while the SMTx_signal input is high, updating the SMTxCPR register and resetting the timer on every rising edge of the SMTWINx input after the first. See Figure 25-12 and Figure 25-13.
FIGURE 25-13: GATED WINDOWED MEASURE MODE SINGLE ACQUISITION TIMING DIAGRAMS
25.6.7 TIME OF FLIGHT MEASURE MODE

This mode measures the time interval between a rising edge on the SMTWINx input and a rising edge on the SMTx_signal input, beginning to increment the timer upon observing a rising edge on the SMTWINx input, while updating the SMTxCPR register and resetting the timer upon observing a rising edge on the SMTx_signal input. In the event of two SMTWINx rising edges without an SMTx_signal rising edge, it will update the SMTxCPW register with the current value of the timer and reset the timer value. See Figure 25-14 and Figure 25-15.
FIGURE 25-14: TIME OF FLIGHT MODE REPEAT ACQUISITION TIMING DIAGRAM
FIGURE 25-15: TIME OF FLIGHT MODE SINGLE ACQUISITION TIMING DIAGRAM
25.6.8 CAPTURE MODE

This mode captures the Timer value based on a rising or falling edge on the SMTWINx input and triggers an interrupt. This mimics the capture feature of a CCP module. The timer begins incrementing upon the GO bit being set, and updates the value of the SMTxCPR register on each rising edge of SMTWINx, and updates the value of the CPW register on each falling edge of the SMTWINx. The timer is not reset by any hardware conditions in this mode and must be reset by software, if desired. See Figure 25-16 and Figure 25-17.
FIGURE 25-16: CAPTURE MODE REPEAT ACQUISITION TIMING DIAGRAM

SMTxWIN
SMTxWIN_sync
SMTx Clock
SMTxEN
SMTxGO
SMTxGO_sync
SMTxTMR
SMTxCPW
SMTxCPR
SMTxPWAIF
SMTxPRAIF
FIGURE 25-17: CAPTURE MODE SINGLE ACQUISITION TIMING DIAGRAM

SMTxWIN

SMTxWIN_sync

SMTx Clock

SMTxEN

SMTxGO

SMTxGO_sync

SMTxTMR

0 1 2 3

SMTxCPW

3

SMTxCPR

2

SMTxPWAIF

SMTxPRAIF
25.6.9 COUNTER MODE

This mode increments the timer on each pulse of the SMTx_signal input. This mode is asynchronous to the SMT clock and uses the SMTx_signal as a time source. The SMTxCPW register will be updated with the current SMTxTMR value on the rising edge of the SMTxWIN input. See Figure 25-18.

FIGURE 25-18: COUNTER MODE TIMING DIAGRAM
25.6.10 GATED COUNTER MODE

This mode counts pulses on the SMTx_signal input, gated by the SMTxWIN input. It begins incrementing the timer upon seeing a rising edge of the SMTxWIN input and updates the SMTxCPW register upon a falling edge on the SMTxWIN input. See Figure 25-19 and Figure 25-20.
FIGURE 25-19: GATED COUNTER MODE REPEAT ACQUISITION TIMING DIAGRAM

FIGURE 25-20: GATED COUNTER MODE SINGLE ACQUISITION TIMING DIAGRAM
25.6.11 WINDOWED COUNTER MODE

This mode counts pulses on the SMTx_signal input, within a window dictated by the SMTxWIN input. It begins counting upon seeing a rising edge of the SMTxWIN input, updates the SMTxCPW register on a falling edge of the SMTxWIN input, and updates the SMTxCPR register on each rising edge of the SMTxWIN input beyond the first. See Figure 25-21 and Figure 25-22.
FIGURE 25-21: WINDOWED COUNTER MODE REPEAT ACQUISITION TIMING DIAGRAM
FIGURE 25-22: WINDOWED COUNTER MODE SINGLE ACQUISITION TIMING DIAGRAM
25.7 Interrupts

The SMT can trigger an interrupt under three different conditions:

- PW Acquisition Complete
- PR Acquisition Complete
- Counter Period Match

The interrupts are controlled by the PIR and PIE registers of the device.

25.7.1 PW AND PR ACQUISITION INTERRUPTS

The SMT can trigger interrupts whenever it updates the SMTxCPW and SMTxCPR registers, the circumstances for which are dependent on the SMT mode, and are discussed in each mode’s specific section. The SMTxCPW interrupt is controlled by SMTxPWAIF and SMTxPWAIE bits in the respective PIR and PIE registers. The SMTxCPR interrupt is controlled by the SMTxPRAIF and SMTxPRAIE bits, also located in the respective PIR and PIE registers.

In synchronous SMT modes, the interrupt trigger is synchronized to the SMTxCLK. In Asynchronous modes, the interrupt trigger is asynchronous. In either mode, once triggered, the interrupt will be synchronized to the CPU clock.

25.7.2 COUNTER PERIOD MATCH INTERRUPT

As described in Section 25.1.2 “Period Match interrupt”, the SMT will also interrupt upon SMTxTMR, matching SMTxPR with its period match limit functionality described in Section 25.3 “Halt Operation”. The period match interrupt is controlled by SMTxIF and SMTxEIE, located in the respective PIR and PIE registers.
25.8 Register Definitions: SMT Control

Long bit name prefixes for the Signal Measurement Timer peripherals are shown in Section 1.3 “Register and Bit naming conventions”.

TABLE 25-2: LONG BIT NAMES PREFIXES FOR SMT PERIPHERALS

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Bit Name Prefix</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMT1</td>
<td>SMT1</td>
</tr>
<tr>
<td>SMT2</td>
<td>SMT2</td>
</tr>
</tbody>
</table>

REGISTER 25-1: SMTxCON0: SMT CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN[1]</td>
<td>—</td>
<td>STP</td>
<td>WPOL</td>
<td>SPOL</td>
<td>CPOL</td>
<td>PS&lt;1:0&gt;</td>
<td></td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
u = Bit is unchanged
x = Bit is unknown
-1/n/n = Value at POR and BOR/Value at all other Resets

‘1’ = Bit is set
‘0’ = Bit is cleared

bit 7 EN: SMT Enable bit[1]
1 = SMT is enabled
0 = SMT is disabled; internal states are reset, clock requests are disabled

bit 6 Unimplemented: Read as ‘0’

bit 5 STP: SMT Counter Halt Enable bit
When SMTxTMR = SMTxPR:
1 = Counter remains SMTxPR; period match interrupt occurs when clocked
0 = Counter resets to 24'h000000; period match interrupt occurs when clocked

bit 4 WPOL: SMTxWIN Input Polarity Control bit
1 = SMTxWIN signal is active-low/falling edge enabled
0 = SMTxWIN signal is active-high/rising edge enabled

bit 3 SPOL: SMTxSIG Input Polarity Control bit
1 = SMTxSignal is active-low/falling edge enabled
0 = SMTxSignal is active-high/rising edge enabled

bit 2 CPOL: SMT Clock Input Polarity Control bit
1 = SMTxTMR increments on the falling edge of the selected clock signal
0 = SMTxTMR increments on the rising edge of the selected clock signal

bit 1-0 PS<1:0>: SMT Prescale Select bits
11 = Prescaler = 1:8
10 = Prescaler = 1:4
01 = Prescaler = 1:2
00 = Prescaler = 1:1

Note 1: Setting EN to ‘0’ does not affect the register contents.
## REGISTER 25-2: SMTxCON1: SMT CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>GO</td>
<td></td>
<td>GO Data Acquisition bit</td>
</tr>
<tr>
<td>6</td>
<td>REPEAT</td>
<td></td>
<td>SMT Repeat Acquisition Enable bit</td>
</tr>
<tr>
<td>5-4</td>
<td>Unimplemented</td>
<td></td>
<td>Read as ‘0’</td>
</tr>
<tr>
<td>3-0</td>
<td>MODE&lt;3:0&gt;</td>
<td></td>
<td>SMT Operation Mode Select bits</td>
</tr>
</tbody>
</table>

Legend:
- **HC**: Bit is cleared by hardware
- **HS**: Bit is set by hardware
- **R**: Readable bit
- **W**: Writable bit
- **U**: Unimplemented bit, read as ‘0’
- **u**: Bit is unchanged
- **x**: Bit is unknown
- **-n/n**: Value at POR and BOR/Value at all other Resets
- **‘1’**: Bit is set
- **‘0’**: Bit is cleared
- **q**: Value depends on condition

- **bit 7**
  - **GO**: GO Data Acquisition bit
  - **1**: Incrementing, acquiring data is enabled
  - **0**: Incrementing, acquiring data is disabled

- **bit 6**
  - **REPEAT**: SMT Repeat Acquisition Enable bit
  - **1**: Repeat Data Acquisition mode is enabled
  - **0**: Single Acquisition mode is enabled

- **bit 5-4**
  - **Unimplemented**: Read as ‘0’

- **bit 3-0**
  - **MODE<3:0>**: SMT Operation Mode Select bits
  - **1111**: Reserved
  - **1011**: Reserved
  - **1010**: Windowed counter
  - **1001**: Gated counter
  - **1000**: Counter
  - **0111**: Capture
  - **0110**: Time of flight
  - **0101**: Gated windowed measure
  - **0100**: Windowed measure
  - **0011**: High and low time measurement
  - **0010**: Period and Duty-Cycle Acquisition
  - **0001**: Gated Timer
  - **0000**: Timer
### REGISTER 25-3: SMTxSTAT: SMT STATUS REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4-3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPRUP</td>
<td>CPWUP</td>
<td>RST</td>
<td>—</td>
<td>TS</td>
<td>WS</td>
<td>AS</td>
</tr>
</tbody>
</table>

#### Legend:
- **HC** = Bit is cleared by hardware
- **HS** = Bit is set by hardware
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **q** = Value depends on condition
- **-n/n** = Value at POR and BOR/Value at all other Resets

#### Bit 7: CPRUP: SMT Manual Period Buffer Update bit
- **1** = Request update to SMTxPRx registers
- **0** = SMTxPRx registers update is complete

#### Bit 6: CPWUP: SMT Manual Pulse Width Buffer Update bit
- **1** = Request update to SMTxCPW registers
- **0** = SMTxCPW registers update is complete

#### Bit 5: RST: SMT Manual Timer Reset bit
- **1** = Request Reset to SMTxTMR registers
- **0** = SMTxTMR registers update is complete

#### Bit 4-3: Unimplemented: Read as ‘0’

#### Bit 2: TS: GO Value Status bit
- **1** = SMT timer is incrementing
- **0** = SMT timer is not incrementing

#### Bit 1: WS: SMTxWIN Value Status bit
- **1** = SMT window is open
- **0** = SMT window is closed

#### Bit 0: AS: SMT_signal Value Status bit
- **1** = SMT acquisition is in progress
- **0** = SMT acquisition is not in progress
### REGISTER 25-4: SMTxCLK: SMT CLOCK SELECTION REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>CSEL&lt;2:0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **q** = Value depends on condition

#### bit 7-3
**Unimplemented**: Read as ‘0’

#### bit 2-0
**CSEL<2:0>:** SMT Clock Selection bits
- **111** = Reference Clock Output
- **110** = SO SC
- **101** = MFINTOSC/16 (32 kHz)
- **100** = MFINTOSC (500 kHz)
- **011** = LFINTOSC
- **010** = HFINTOSC 16 MHz
- **001** = Fosc
- **000** = Fosc/4
## REGISTER 25-5: SMTxWIN: SMTx WINDOW INPUT SELECT REGISTER

<table>
<thead>
<tr>
<th>Bit 7-5</th>
<th>Unimplemented: Read as '0'</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 4-0</td>
<td>WSEL&lt;4:0&gt;: SMTx Window Selection bits</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11111</td>
<td>Reserved</td>
</tr>
<tr>
<td>11110</td>
<td>CLC4_out</td>
</tr>
<tr>
<td>11101</td>
<td>CLC3_out</td>
</tr>
<tr>
<td>11100</td>
<td>CLC2_out</td>
</tr>
<tr>
<td>10111</td>
<td>CLC1_out</td>
</tr>
<tr>
<td>10110</td>
<td>ZCD1_out</td>
</tr>
<tr>
<td>10101</td>
<td>CMP2_out</td>
</tr>
<tr>
<td>10100</td>
<td>CMP1_out</td>
</tr>
<tr>
<td>10011</td>
<td>NCO1_out</td>
</tr>
<tr>
<td>10010</td>
<td>Reserved</td>
</tr>
<tr>
<td>10001</td>
<td>Reserved</td>
</tr>
<tr>
<td>10000</td>
<td>PWM8_out</td>
</tr>
<tr>
<td>01111</td>
<td>PWM7_out</td>
</tr>
<tr>
<td>01110</td>
<td>PWM6_out</td>
</tr>
<tr>
<td>01101</td>
<td>PWM5_out</td>
</tr>
<tr>
<td>01100</td>
<td>CCP4_out</td>
</tr>
<tr>
<td>01011</td>
<td>CCP3_out</td>
</tr>
<tr>
<td>01010</td>
<td>CCP2_out</td>
</tr>
<tr>
<td>01001</td>
<td>CCP1_out</td>
</tr>
<tr>
<td>01000</td>
<td>TMR6_postscaled</td>
</tr>
<tr>
<td>00111</td>
<td>TMR4_postscaled</td>
</tr>
<tr>
<td>00110</td>
<td>TMR2_postscaled</td>
</tr>
<tr>
<td>00101</td>
<td>TMR0_overflow</td>
</tr>
<tr>
<td>00100</td>
<td>CLKREF</td>
</tr>
<tr>
<td>00011</td>
<td>SOSC</td>
</tr>
<tr>
<td>00010</td>
<td>MFINTOSC/16 (32 kHz)</td>
</tr>
<tr>
<td>00001</td>
<td>LFINTOSC</td>
</tr>
<tr>
<td>00000</td>
<td>SMTxWINPPS</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared
- q = Value depends on condition
## REGISTER 25-6: SMTxSIG: SMTx SIGNAL INPUT SELECT REGISTER

<table>
<thead>
<tr>
<th>Bit 7-5</th>
<th>Bit 4-0</th>
<th>Legend:</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>Unimplemented: Read as '0'</td>
</tr>
<tr>
<td>U-0</td>
<td>U-0</td>
<td></td>
</tr>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td></td>
</tr>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td></td>
</tr>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **q** = Value depends on condition

**SSEL<4:0>: SMTx Signal Selection bits**

- **11111** = Reserved
- **11010** = CAN_rx_timestamp
- **11001** = CLC4_out
- **11000** = CLC3_out
- **10111** = CLC2_out
- **10110** = CLC1_out
- **10101** = ZCD1_out
- **10100** = CMP2_out
- **10011** = CMP1_out
- **10010** = NCO1_out
- **10001** = Reserved
- **10000** = Reserved
- **01111** = PWM8_out
- **01110** = PWM7_out
- **01101** = PWM6_out
- **01100** = PWM5_out
- **01011** = CCP4_out
- **01010** = CCP3_out
- **01001** = CCP2_out
- **01000** = CCP1_out
- **00111** = TMR6_postscaled
- **00110** = TMR5_overflow
- **00101** = TMR4_postscaled
- **00100** = TMR3_overflow
- **00011** = TMR2_postscaled
- **00010** = TMR1_overflow
- **00001** = TMR0_overflow
- **00000** = SMTxSIGPPS
### REGISTER 25-7: SMTxTMR: SMT TIMER REGISTER – LOW BYTE

| bit 7-0 | SMTxTMR<7:0> | Significant bits of the SMT Counter – Low Byte |

### REGISTER 25-8: SMTxTMRH: SMT TIMER REGISTER – HIGH BYTE

| bit 7-0 | SMTxTMR<15:8> | Significant bits of the SMT Counter – High Byte |

### REGISTER 25-9: SMTxTMRU: SMT TIMER REGISTER – UPPER BYTE

| bit 7-0 | SMTxTMR<23:16> | Significant bits of the SMT Counter – Upper Byte |
**REGISTER 25-10: SMTxCPRL: SMT CAPTURED PERIOD REGISTER – LOW BYTE**

<table>
<thead>
<tr>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
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<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>x/x</td>
<td>x/x</td>
<td>x/x</td>
<td>x/x</td>
<td>x/x</td>
<td>x/x</td>
<td>x/x</td>
</tr>
<tr>
<td>SMTxCPR&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

| bit 7-0 | SMTxCPR<7:0>: Significant bits of the SMT Period Latch – Low Byte |

**REGISTER 25-11: SMTxCPRH: SMT CAPTURED PERIOD REGISTER – HIGH BYTE**

<table>
<thead>
<tr>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
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<tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>x/x</td>
<td>x/x</td>
<td>x/x</td>
<td>x/x</td>
<td>x/x</td>
<td>x/x</td>
<td>x/x</td>
</tr>
<tr>
<td>SMTxCPR&lt;15:8&gt;</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

| bit 7-0 | SMTxCPR<15:8>: Significant bits of the SMT Period Latch – High Byte |

**REGISTER 25-12: SMTxCPRU: SMT CAPTURED PERIOD REGISTER – UPPER BYTE**

<table>
<thead>
<tr>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
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<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>x/x</td>
<td>x/x</td>
<td>x/x</td>
<td>x/x</td>
<td>x/x</td>
<td>x/x</td>
<td>x/x</td>
</tr>
<tr>
<td>SMTxCPR&lt;23:16&gt;</td>
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</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

| bit 7-0 | SMTxCPR<23:16>: Significant bits of the SMT Period Latch – Upper Byte |
### REGISTER 25-13: SMTxCPWL: SMT CAPTURED PULSE WIDTH REGISTER – LOW BYTE

<table>
<thead>
<tr>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
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<td></td>
<td>bit 7</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td>bit 0</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7-0 SMTxCPW<7:0>:** Significant bits of the SMT PW Latch – Low Byte

### REGISTER 25-14: SMTxCPWH: SMT CAPTURED PULSE WIDTH REGISTER – HIGH BYTE

<table>
<thead>
<tr>
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<th>R-x/x</th>
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<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
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<td></td>
<td>bit 7</td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit 0</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7-0 SMTxCPW<15:8>:** Significant bits of the SMT PW Latch – High Byte

### REGISTER 25-15: SMTxCPWU: SMT CAPTURED PULSE WIDTH REGISTER – UPPER BYTE

<table>
<thead>
<tr>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
<th>R-x/x</th>
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<td></td>
<td>bit 7</td>
</tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit 0</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7-0 SMTxCPW<23:16>:** Significant bits of the SMT PW Latch – Upper Byte
**REGISTER 25-16: SMTxPRL: SMT PERIOD REGISTER – LOW BYTE**

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>SMTxPR&lt;7:0&gt;</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- n/n = Value at POR and BOR/Value at all other Resets

**bit 7-0 SMTxPR<7:0>: Significant bits of the SMT Timer Value for Period Match – Low Byte**

**REGISTER 25-17: SMTxPRH: SMT PERIOD REGISTER – HIGH BYTE**

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>SMTxPR&lt;15:8&gt;</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- n/n = Value at POR and BOR/Value at all other Resets

**bit 7-0 SMTxPR<15:8>: Significant bits of the SMT Timer Value for Period Match – High Byte**

**REGISTER 25-18: SMTxPRU: SMT PERIOD REGISTER – UPPER BYTE**

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>R/W-x/1</td>
<td>SMTxPR&lt;23:16&gt;</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- n/n = Value at POR and BOR/Value at all other Resets

**bit 7-0 SMTxPR<23:16>: Significant bits of the SMT Timer Value for Period Match – Upper Byte**
### TABLE 25-3: SUMMARY OF REGISTERS ASSOCIATED WITH SMTx

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMT1CON0</td>
<td>EN</td>
<td>—</td>
<td>STP</td>
<td>WPOL</td>
<td>SPOL</td>
<td>CPOL</td>
<td>SMT1PS&lt;1:0&gt;</td>
<td>—</td>
<td>380</td>
</tr>
<tr>
<td>SMT1CON1</td>
<td>GO</td>
<td>REPEAT</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>MODE&lt;3:0&gt;</td>
<td>—</td>
<td>381</td>
</tr>
<tr>
<td>SMT1STAT</td>
<td>CPRUP</td>
<td>CPWUP</td>
<td>RST</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TS</td>
<td>WS</td>
<td>AS</td>
</tr>
<tr>
<td>SMT1CLK</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CSEL&lt;2:0&gt;</td>
<td>382</td>
</tr>
<tr>
<td>SMT1SIG</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>383</td>
</tr>
<tr>
<td>SMT1WIN</td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
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<td>WSEL&lt;4:0&gt;</td>
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<tr>
<td>SMT1MRL</td>
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<td></td>
<td></td>
<td></td>
<td>TMR&lt;7:0&gt;</td>
<td>—</td>
<td>385</td>
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<tr>
<td>SMT1MRH</td>
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<td></td>
<td></td>
<td></td>
<td>TMR&lt;15:8&gt;</td>
<td>—</td>
<td>386</td>
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<tr>
<td>SMT1MRU</td>
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<td></td>
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<td></td>
<td>TMR&lt;23:16&gt;</td>
<td>—</td>
<td>387</td>
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<tr>
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<td>CPR</td>
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<td>388</td>
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<tr>
<td>SMT1CPRH</td>
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<tr>
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<tr>
<td>SMT1CPWH</td>
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<td></td>
<td></td>
<td>CPW&lt;15:8&gt;</td>
<td>—</td>
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<tr>
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<td></td>
<td>CPW&lt;23:16&gt;</td>
<td>—</td>
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<tr>
<td>SMT1PRL</td>
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<td>WPOL</td>
<td>SPOL</td>
<td>CPOL</td>
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<td>—</td>
<td>—</td>
<td>MODE&lt;3:0&gt;</td>
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<td>381</td>
</tr>
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<td>SMT2STAT</td>
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<td>CPWUP</td>
<td>RST</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TS</td>
<td>WS</td>
<td>AS</td>
</tr>
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<td>SMT2CLK</td>
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<td>—</td>
<td>CSEL&lt;2:0&gt;</td>
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<td>SMT2MRL</td>
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<td>TMR&lt;7:0&gt;</td>
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<td>SMT2MRH</td>
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<td>388</td>
</tr>
<tr>
<td>SMT2CPRH</td>
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<td>CPW&lt;7:0&gt;</td>
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<td>CPW&lt;23:16&gt;</td>
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<td>388</td>
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<tr>
<td>SMT2PRL</td>
<td>PR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>389</td>
</tr>
<tr>
<td>SMT2PRH</td>
<td>PR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>390</td>
</tr>
<tr>
<td>SMT2PRU</td>
<td>PR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>391</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented read as ‘0’. Shaded cells are not used for the SMTx module.
26.0 COMPLEMENTARY WAVEFORM GENERATOR (CWG) MODULE

The Complementary Waveform Generator (CWG) produces half-bridge, full-bridge, and steering of PWM waveforms. It is backwards compatible with previous CCP functions. The PIC18(L)F25/26K83 family has three instances of the CWG module.

Each of the CWG modules has the following features:

- Six operating modes:
  - Synchronous Steering mode
  - Asynchronous Steering mode
  - Full-Bridge mode, Forward
  - Full-Bridge mode, Reverse
  - Half-Bridge mode
  - Push-Pull mode
- Output polarity control
- Output steering
- Independent 6-bit rising and falling event dead-band timers
  - Clocked dead band
  - Independent rising and falling dead-band enables
- Auto-shutdown control with:
  - Selectable shutdown sources
  - Auto-restart option
  - Auto-shutdown pin override control

26.1 Fundamental Operation

The CWG generates two output waveforms from the selected input source.

The off-to-on transition of each output can be delayed from the on-to-off transition of the other output, thereby, creating a time delay immediately where neither output is driven. This is referred to as dead time and is covered in Section 26.6 “Dead-Band Control”.

It may be necessary to guard against the possibility of circuit faults or a feedback event arriving too late or not at all. In this case, the active drive must be terminated before the Fault condition causes damage. This is referred to as auto-shutdown and is covered in Section 26.10 “Auto-Shutdown”.

26.2 Operating Modes

The CWG module can operate in six different modes, as specified by the MODE<2:0> bits of the CWGxCON0 register:

- Half-Bridge mode
- Push-Pull mode
- Asynchronous Steering mode
- Synchronous Steering mode
- Full-Bridge mode, Forward
- Full-Bridge mode, Reverse

All modes accept a single pulse data input, and provide up to four outputs as described in the following sections.

All modes include auto-shutdown control as described in Section 26.10 “Auto-Shutdown”.

Note: Except as noted for Full-bridge mode (Section 26.2.3 “Full-Bridge Modes”), mode changes should only be performed while EN = 0 (Register 26-1).

26.2.1 HALF-BRIDGE MODE

In Half-Bridge mode, two output signals are generated as true and inverted versions of the input as illustrated in Figure 26-2. A non-overlap (dead-band) time is inserted between the two outputs as described in Section 26.6 “Dead-Band Control”. The output steering feature cannot be used in this mode. A basic block diagram of this mode is shown in Figure 26-1.

The unused outputs CWGxC and CWGxD drive similar signals as CWGxA and CWGxB, with polarity independently controlled by the POLC and POLD bits of the CWGxCON1 register, respectively.
FIGURE 26-1: SIMPLIFIED CWG BLOCK DIAGRAM (HALF-BRIDGE MODE, MODE<2:0> = 100)
26.2.2 PUSH-PULL MODE

In Push-Pull mode, two output signals are generated, alternating copies of the input as illustrated in Figure 26-4. This alternation creates the push-pull effect required for driving some transformer-based power supply designs. Steering modes are not used in Push-Pull mode. A basic block diagram for the Push-Pull mode is shown in Figure 26-3.

The push-pull sequencer is reset whenever EN = 0 or if an auto-shutdown event occurs. The sequencer is clocked by the first input pulse, and the first output appears on CWGxA.

The unused outputs CWGxC and CWGxD drive copies of CWGxA and CWGxB, respectively, but with polarity controlled by the POLC and POLD bits of the CWGxCON1 register, respectively.

FIGURE 26-2: CWGx HALF-BRIDGE MODE OPERATION

Diagram showing CWGx_clock, CWGxA, CWGxC, CWGxB, CWGxD, and CWGx_data with notes: CWGx_rising_src = CCP1_out, CWGx_falling_src = ~CCP1_out.
FIGURE 26-3: SIMPLIFIED CWG BLOCK DIAGRAM (PUSH-PULL MODE, MODE<2:0> = 101)
26.2.3 FULL-BRIDGE MODES

In Forward and Reverse Full-Bridge modes, three outputs drive static values while the fourth is modulated by the input data signal. The mode selection may be toggled between forward and reverse by toggling the MODE<0> bit of the CWGxCON0 while keeping MODE<2:1> static, without disabling the CWG module. When connected as shown in Figure 26-5, the outputs are appropriate for a full-bridge motor driver. Each CWG output signal has independent polarity control, so the circuit can be adapted to high-active and low-active drivers. A simplified block diagram for the Full-Bridge modes is shown in Figure 26-6.

FIGURE 26-5: EXAMPLE OF FULL-BRIDGE APPLICATION
FIGURE 26-6: SIMPLIFIED CWG BLOCK DIAGRAM (FORWARD AND REVERSE FULL-BRIDGE MODES)

MODE<2:0> = 010: Forward
MODE<2:0> = 011: Reverse

- CWG Clock
- CWG Data
- CWG Data Input
- REN
- SHUTDOWN = 0
- Auto-shutdown source (CWGxAS1 register)
- EN

- Rising Dead-Band Block
- Falling Dead-Band Block

- CWG Clock signal in
- CWG Clock signal out
- CWG Data signal in
- CWG Data signal out
- cwg data

- CWG Clock signal in
- CWG Clock signal out
- CWG Data signal in
- CWG Data signal out

- LSAC<1:0>
- LSBD<1:0>

- CWG Clock signal in
- CWG Clock signal out
- CWG Data signal in
- CWG Data signal out

- CWG Data A
- POLA
- CWG1A

- CWG Data B
- POLB
- CWG1B

- CWG Data C
- POLC
- CWG1C

- CWG Data D
- POLD
- CWG1D

- FREEZE
- SHUTDOWN
- AUTO-SHUTDOWN
- CWG Data

- DQ

- '1'
- '0'

- High-Z

- MODE<2:0> = 010: Forward
- MODE<2:0> = 011: Reverse
In Forward Full-Bridge mode (MODE<2:0> = 010), CWGxA is driven to its active state, CWGxB and CWGxC are driven to their inactive state, and CWGxD is modulated by the input signal, as shown in Figure 26-7.

In Reverse Full-Bridge mode (MODE<2:0> = 011), CWGxC is driven to its active state, CWGxA and CWGxD are driven to their inactive states, and CWGxB is modulated by the input signal, as shown in Figure 26-7.

In Full-Bridge mode, the dead-band period is used when there is a switch from forward to reverse or vice-versa. This dead-band control is described in Section 26.6 "Dead-Band Control", with additional details in Section 26.7 "Rising Edge and Reverse Dead Band" and Section 26.8 "Falling Edge and Forward Dead Band". Steering modes are not used with either of the Full-Bridge modes. The mode selection may be toggled between forward and reverse toggling the MODE<0> bit of the CWGxCON0 while keeping MODE<2:1> static, without disabling the CWG module.

**FIGURE 26-7: EXAMPLE OF FULL-BRIDGE OUTPUT**

<table>
<thead>
<tr>
<th></th>
<th>CWG1A(2)</th>
<th>CWG1B(2)</th>
<th>CWG1C(2)</th>
<th>CWG1D(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Forward Mode</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Period</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pulse Width</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Reverse Mode</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Period</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pulse Width</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** A rising CWG data input creates a rising event on the modulated output.
**Note 2:** Output signals shown as active-high; all POLy bits are clear.
26.2.3.1 Direction Change in Full-Bridge Mode

In Full-Bridge mode, changing MODE<2:0> controls the forward/reverse direction. Changes to MODE<2:0> change to the new direction on the next rising edge of the modulated input.

A direction change is initiated in software by changing the MODE<2:0> bits of the CWGxCON0 register. The sequence is illustrated in Figure 26-8.

- The associated active output CWGxA and the inactive output CWGxC are switched to drive in the opposite direction.
- The previously modulated output CWGxD is switched to the inactive state, and the previously inactive output CWGxB begins to modulate.
- CWG modulation resumes after the direction-switch dead band has elapsed.

26.2.3.2 Dead-Band Delay in Full-Bridge Mode

Dead-band delay is important when either of the following conditions is true:

1. The direction of the CWG output changes when the duty cycle of the data input is at or near 100%, or
2. The turn-off time of the power switch, including the power device and driver circuit, is greater than the turn-on time.

The dead-band delay is inserted only when changing directions, and only the modulated output is affected. The statically-configured outputs (CWGxA and CWGxC) are not afforded dead band, and switch essentially simultaneously.

Figure 26-8 shows an example of the CWG outputs changing directions from forward to reverse, at near 100% duty cycle. In this example, at time t1, the output of CWGxA and CWGxD become inactive, while output CWGxC becomes active. Since the turn-off time of the power devices is longer than the turn-on time, a shoot-through current will flow through power devices QC and QD for the duration of ‘t’. The same phenomenon will occur to power devices QA and QB for the CWG direction change from reverse to forward.

When changing the CWG direction at high duty cycle is required for an application, two possible solutions for eliminating the shoot-through current are:

1. Reduce the CWG duty cycle for one period before changing directions.
2. Use switch drivers that can drive the switches off faster than they can drive them on.

FIGURE 26-8: EXAMPLE OF PWM DIRECTION CHANGE AT NEAR 100% DUTY CYCLE

![Diagram of PWM direction change at near 100% duty cycle]
26.2.4 STEERING MODES

In both Synchronous and Asynchronous Steering modes, the modulated input signal can be steered to any combination of four CWG outputs and a fixed-value will be presented on all the outputs not used for the PWM output. Each output has independent polarity, steering, and shutdown options. Dead-band control is not used in either steering mode.

When STRx = 0 (Register 26-5), then the corresponding pin is held at the level defined by OVRx (Register 26-5). When STRx = 1, then the pin is driven by the modulated input signal.

The POLx bits (Register 26-2) control the signal polarity only when STRx = 1.

The CWG auto-shutdown operation also applies to steering modes as described in Section 26.14 “Register Definitions: CWG Control”.

Note: Only the STRx bits are synchronized; the SDATx (data) bits are not synchronized.

The CWG auto-shutdown operation also applies in steering modes as described in Section 26.10 “Auto-Shutdown”. An auto-shutdown event will only affect pins that have STRx = 1.

FIGURE 26-9: EXAMPLE OF SYNCHRONOUS STEERING (MODE<2:0> = 001)

26.2.4.1 Synchronous Steering Mode

In Synchronous Steering mode (MODE<2:0> bits = 001, Register 26-1), changes to steering selection registers take effect on the next rising edge of the modulated data input (Figure 26-9). In Synchronous Steering mode, the output will always produce a complete waveform.
26.2.4.2 Asynchronous Steering Mode

In Asynchronous mode (MODE<2:0> bits = 000, Register 26-1), steering takes effect at the end of the instruction cycle that writes to STR. In Asynchronous Steering mode, the output signal may be an incomplete waveform (Figure 26-10). This operation may be useful when the user firmware needs to immediately remove a signal from the output pin.

**FIGURE 26-10: EXAMPLE OF ASYNCHRONOUS STEERING (MODE<2:0>= 000)**

26.2.4.3 Start-up Considerations

The application hardware must use the proper external pull-up and/or pull-down resistors on the CWG output pins. This is required because all I/O pins are forced to high-impedance at Reset.

The POLy bits (Register 26-2) allow the user to choose whether the output signals are active-high or active-low.
FIGURE 26-11: SIMPLIFIED CWG BLOCK DIAGRAM (OUTPUT STEERING MODES)

MODE<2:0> = 000: Asynchronous
MODE<2:0> = 001: Synchronous
26.3 Clock Source

The clock source is used to drive the dead-band timing circuits. The CWG module allows the following clock sources to be selected:

- Fosc (system clock)
- HFINTOSC

When the HFINTOSC is selected, the HFINTOSC will be kept running during Sleep. Therefore, CWG modes requiring dead band can operate in Sleep, provided that the CWG data input is also active during Sleep. The clock sources are selected using the CS bit of the CWGxCLKCON register (Register 26-3). The system clock Fosc, is disabled in Sleep and thus dead-band control cannot be used.

26.4 Selectable Input Sources

The CWG generates the output waveforms from the following input sources:

<table>
<thead>
<tr>
<th>Source Peripheral</th>
<th>Signal Name</th>
<th>ISM&lt;2:0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>CWGxPPS</td>
<td>Pin selected by CWGxPPS</td>
<td>000</td>
</tr>
<tr>
<td>CCP1</td>
<td>CCP1 Output</td>
<td>001</td>
</tr>
<tr>
<td>CCP2</td>
<td>CCP2 Output</td>
<td>010</td>
</tr>
<tr>
<td>PWM3</td>
<td>PWM3 Output</td>
<td>011</td>
</tr>
<tr>
<td>PWM4</td>
<td>PWM4 Output</td>
<td>100</td>
</tr>
<tr>
<td>CMP1</td>
<td>Comparator 1 Output</td>
<td>101</td>
</tr>
<tr>
<td>CMP2</td>
<td>Comparator 2 Output</td>
<td>110</td>
</tr>
<tr>
<td>DSM</td>
<td>Data signal modulator output</td>
<td>111</td>
</tr>
</tbody>
</table>

The input sources are selected using the IS<4:0> bits in the CWGxISM register (Register 26-4).

26.5 Output Control

26.5.1 CWG OUTPUTS

Each CWG output can be routed to a Peripheral Pin Select (PPS) output via the RxyPPS register (see Section 17.0 “Peripheral Pin Select (PPS) Module”).

26.5.2 POLARITY CONTROL

The polarity of each CWG output can be selected independently. When the output polarity bit is set, the corresponding output is active-high. Clearing the output polarity bit configures the corresponding output as active-low. However, polarity does not affect the over-ride levels. Output polarity is selected with the POLy bits of the CWGxCON1. Auto-shutdown and steering options are unaffected by polarity.

26.6 Dead-Band Control

The dead-band control provides non-overlapping PWM signals to prevent shoot-through current in PWM switches. Dead-band operation is employed for Half-Bridge and Full-Bridge modes. The CWG contains two 6-bit dead-band counters. One is used for the rising edge of the input source control in Half-Bridge mode or for reverse dead-band Full-Bridge mode. The other is used for the falling edge of the input source control in Half-Bridge mode or for forward dead band in Full-Bridge mode.

Dead band is timed by counting CWG clock periods from zero up to the value in the rising or falling dead-band counter registers. See CWGxDBR and CWGxDBF registers, respectively.

26.6.1 DEAD-BAND FUNCTIONALITY IN HALF-BRIDGE MODE

In Half-Bridge mode, the dead-band counters dictate the delay between the falling edge of the normal output and the rising edge of the inverted output. This can be seen in Figure 26-2.

26.6.2 DEAD-BAND FUNCTIONALITY IN FULL-BRIDGE MODE

In Full-Bridge mode, the dead-band counters are used when undergoing a direction change. The MODE<0> bit of the CWGxCON0 register can be set or cleared while the CWG is running, allowing for changes from Forward to Reverse mode. The CWGxA and CWGxC signals will change immediately upon the first rising input edge following a direction change, but the modulated signals (CWGxB or CWGxD, depending on the direction of the change) will experience a delay dictated by the dead-band counters.
26.7 Rising Edge and Reverse Dead Band

In Half-Bridge mode, the rising edge dead band delays the turn-on of the CWGxA output after the rising edge of the CWG data input. In Full-Bridge mode, the reverse dead-band delay is only inserted when changing directions from Forward mode to Reverse mode, and only the modulated output CWGxB is affected.

The CWGxDBR register determines the duration of the dead-band interval on the rising edge of the input source signal. This duration is from 0 to 64 periods of the CWG clock.

Dead band is always initiated on the edge of the input source signal. A count of zero indicates that no dead band is present.

If the input source signal reverses polarity before the dead-band count is completed, then no signal will be seen on the respective output.

The CWGxDBR register value is double-buffered. When EN = 0 (Register 26-1), the buffer is loaded when CWGxDBR is written. If EN = 1, then the buffer will be loaded at the rising edge following the first falling edge of the data input, after the LD bit (Register 26-1) is set. Refer to Figure 26-12 for an example.

26.8 Falling Edge and Forward Dead Band

In Half-Bridge mode, the falling edge dead band delays the turn-on of the CWGxB output at the falling edge of the CWG data input. In Full-Bridge mode, the forward dead-band delay is only inserted when changing directions from Reverse mode to Forward mode, and only the modulated output CWGxD is affected.

The CWGxDBF register determines the duration of the dead-band interval on the falling edge of the input source signal. This duration is from zero to 64 periods of CWG clock.

Dead-band delay is always initiated on the edge of the input source signal. A count of zero indicates that no dead band is present.

If the input source signal reverses polarity before the dead-band count is completed, then no signal will be seen on the respective output.

The CWGxDBF register value is double-buffered. When EN = 0 (Register 26-1), the buffer is loaded when CWGxDBF is written. If EN = 1, then the buffer will be loaded at the rising edge following the first falling edge of the data input after the LD (Register 26-1) is set. Refer to Figure 26-13 for an example.
FIGURE 26-12: DEAD-BAND OPERATION, CWGxDBR = 0x01, CWGxDBF = 0x02

FIGURE 26-13: DEAD-BAND OPERATION, CWGxDBR = 0x03, CWGxDBF = 0x06, SOURCE SHORTER THAN DEAD BAND
26.9 Dead-Band Jitter

When the rising and falling edges of the input source are asynchronous to the CWG clock, it creates jitter in the dead-band time delay. The maximum jitter is equal to one CWG clock period. Refer to Equation 26-1 for more details.

**EQUATION 26-1: DEAD-BAND DELAY TIME CALCULATION**

\[
T_{\text{DEAD-BAND\_MIN}} = \frac{1}{F_{\text{CWG\_CLOCK}}} \cdot \text{DBx < 4:0>}
\]

\[
T_{\text{DEAD-BAND\_MAX}} = \frac{1}{F_{\text{CWG\_CLOCK}}} \cdot \text{DBx < 4:0> + 1}
\]

\[
T_{\text{JITTER}} = T_{\text{DEAD\_BAND\_MAX}} - T_{\text{DEAD\_BAND\_MIN}}
\]

\[
T_{\text{JITTER}} = \frac{1}{F_{\text{CWG\_CLOCK}}}
\]

\[
T_{\text{DEAD\_BAND\_MAX}} = T_{\text{DEAD\_BAND\_MIN}} + T_{\text{JITTER}}
\]

**EXAMPLE**

\[DBR<4:0> = 0000\] = 10

\[F_{\text{CWG\_CLOCK}} = 8 \text{ MHz}\]

\[T_{\text{JITTER}} = \frac{1}{8 \text{ MHz}} = 125 \text{ ns}\]

\[T_{\text{DEAD\_BAND\_MIN}} = 125 \text{ ns} \times 10 = 1.25 \mu\text{s}\]

\[T_{\text{DEAD\_BAND\_MAX}} = 1.25 \mu\text{s} + 0.125 \mu\text{s} = 1.37 \mu\text{s}\]
26.10 Auto-Shutdown

Auto-shutdown is a method to immediately override the CWG output levels with specific overrides that allow for safe shutdown of the circuit. The shutdown state can be either cleared automatically or held until cleared by software. The auto-shutdown circuit is illustrated in Figure 26-14.

26.10.1 SHUTDOWN

The shutdown state can be entered by either of the following two methods:

• Software generated
• External Input

26.10.1.1 Software Generated Shutdown

Setting the SHUTDOWN bit of the CWGxAS0 register will force the CWG into the shutdown state.

When the auto-restart is disabled, the shutdown state will persist as long as the SHUTDOWN bit is set.

When auto-restart is enabled, the SHUTDOWN bit will clear automatically and resume operation on the next rising edge event. The SHUTDOWN bit indicates when a shutdown condition exists. The bit may be set or cleared in software or by hardware.

26.10.1.2 External Input Source

External shutdown inputs provide the fastest way to safely suspend CWG operation in the event of a Fault condition.

When any of the selected shutdown inputs goes active, the CWG outputs will immediately go to the specified override levels without software delay. The override levels are selected by the LSBD<1:0> and LSAC<1:0> bits of the CWGxAS0 register (Register 26-6). Several input sources can be selected to cause a shutdown condition. All input sources are active-low. The sources are:

• Pin selected by CWGxPPS
• Timer2 postscaled output
• Timer4 postscaled output
• Timer6 postscaled output
• Comparator 1 output
• Comparator 2 output
• CLC2 output

Shutdown input sources are individually enabled by the ASxE bits of the CWGxAS1 register (Register 26-7).

26.10.1.3 Pin Override Levels

The levels driven to the CWG outputs during an auto-shutdown event are controlled by the LSBD<1:0> and LSAC<1:0> bits of the CWGxAS0 register (Register 26-6). The LSBD<1:0> bits control CWGxB/D output levels, while the LSAC<1:0> bits control the CWGxA/C output levels.

26.10.1.4 Auto-Shutdown Interrupts

When an auto-shutdown event occurs, either by software or hardware setting SHUTDOWN, the CWGxIF flag bit of the respective PIR register is set.

26.11 Auto-Shutdown Restart

After an auto-shutdown event has occurred, there are two ways to resume operation:

• Software controlled
• Auto-restart

In either case, the shutdown source must be cleared before the restart can take place. That is, either the shutdown condition must be removed, or the corresponding ASxE bit must be cleared.

26.11.1 SOFTWARE-CONTROLLED RESTART

If the REN bit of the CWGxAS0 register is clear (REN = 0), the CWG module must be restarted after an auto-shutdown event through software.

Once all auto-shutdown sources are removed, the software must clear SHUTDOWN. Once SHUTDOWN is cleared, the CWG module will resume operation upon the first rising edge of the CWG data input.

Note: The SHUTDOWN bit cannot be cleared in software if the auto-shutdown condition is still present.

26.11.2 AUTO-RESTART

If the REN bit of the CWGxAS0 register is set (REN = 1), the CWG module will restart from the shutdown state automatically.

Once all auto-shutdown conditions are removed, the hardware will automatically clear SHUTDOWN. Once SHUTDOWN is cleared, the CWG module will resume operation upon the first rising edge of the CWG data input.

Note: The SHUTDOWN bit cannot be cleared in software if the auto-shutdown condition is still present.
26.12 Operation During Sleep

The CWG module operates independently from the system clock and will continue to run during Sleep, provided that the clock and input sources selected remain active.

The HFINTOSC remains active during Sleep when all the following conditions are met:

- CWG module is enabled
- Input source is active
- HFINTOSC is selected as the clock source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as system clock and CWG clock, when the CWG is enabled and the input source is active, then the CPU will go Idle during Sleep, but the HFINTOSC will remain active and the CWG will continue to operate. This will have a direct effect on the Sleep mode current.

26.13 Configuring the CWG

1. Ensure that the TRIS control bits corresponding to CWG outputs are set so that all are configured as inputs, ensuring that the outputs are inactive during setup. External hardware should ensure that pin levels are held to safe levels.
2. Clear the EN bit, if not already cleared.
3. Configure the MODE<2:0> bits of the CWGxCON0 register to set the output operating mode.
4. Configure the POLy bits of the CWGxCON1 register to set the output polarities.
5. Configure the ISM<4:0> bits of the CWGxISM register to select the data input source.
6. If a steering mode is selected, configure the STRx bits to select the desired output on the CWG outputs.
7. Configure the LSBD<1:0> and LSAC<1:0> bits of the CWGxASD0 register to select the auto-shutdown output override states (this is necessary even if not using auto-shutdown because start-up will be from a shutdown state).
8. If auto-restart is desired, set the REN bit of CWGxAS0.
9. If auto-shutdown is desired, configure the ASxE bits of the CWGxAS1 register to select the shutdown source.
10. Set the desired rising and falling dead-band times with the CWGxDBR and CWGxDBF registers.
11. Select the clock source in the CWGxCLKCON register.
12. Set the EN bit to enable the module.
13. Clear the TRIS bits that select the CWG outputs to set them as outputs.

If auto-restart is to be used, set the REN bit and the SHUTDOWN bit will be cleared automatically. Otherwise, clear the SHUTDOWN bit in software to start the CWG.
FIGURE 26-14: CWG SHUTDOWN BLOCK DIAGRAM

- Write '1' to SHUTDOWN bit
- CWGx INPPS
- AS0E
- CMP1_out
- AS4E
- CMP2_out
- AS5E
- TMR2_postscaled
- AS1E
- TMR4_postscaled
- AS2E
- TMR6_postscaled
- AS3E
- CLC2_out
- AS6E

FIGURE 26-15: SHUTDOWN FUNCTIONALITY, AUTO-RESTART DISABLED (REN = 0, LSAC = 01, LSBD = 01)

- CWG Input Source
- Shutdown Source
- SHUTDOWN
- CWGxA
- CWGxB
- CWGxC
- CWGxD

- Shutdown Event Ceases
- REN Cleared by Software
- Tri-State (No Pulse)
- No Shutdown
- Output Resumes
FIGURE 26-16: SHUTDOWN FUNCTIONALITY, AUTO-RESTART ENABLED (REN = 1, LSAC = 01, LSBD = 01)

- CWG Input Source
- Shutdown Source
- SHUTDOWN
- CWGxA
- CWGxC
- CWGxB
- CWGxD

Shutdown Event Ceases

REX auto-cleared by hardware

Tri-State (No Pulse)

No Shutdown

Shutdown

Output Resumes
26.14 Register Definitions: CWG Control

Long bit name prefixes for the CWG peripheral is shown below. Refer to Section 1.3.2.2 “Long Bit Names” for more information.

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Bit Name Prefix</th>
</tr>
</thead>
<tbody>
<tr>
<td>CWG1</td>
<td>CWG1</td>
</tr>
<tr>
<td>CWG2</td>
<td>CWG2</td>
</tr>
<tr>
<td>CWG3</td>
<td>CWG3</td>
</tr>
</tbody>
</table>

REGISTER 26-1: CWGxCON0: CWG CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W/HC-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LD</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>MODE&lt;2:0&gt;</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit   W = Writable bit   U = Unimplemented bit, read as ‘0’
u = Bit is unchanged   x = Bit is unknown   -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set   ‘0’ = Bit is cleared   HC = Bit is cleared by hardware

bit 7       EN: CWGx Enable bit
            1 = Module is enabled
            0 = Module is disabled

bit 6       LD: CWGx Load Buffers bit⁽¹⁾
            1 = Dead-band count buffers to be loaded on CWG data rising edge, following first falling edge after
            this bit is set
            0 = Buffers remain unchanged

bit 5-3    Unimplemented: Read as ‘0’

bit 2-0    MODE<2:0>: CWGx Mode bits
            111 = Reserved
            110 = Reserved
            101 = CWG outputs operate in Push-Pull mode
            100 = CWG outputs operate in Half-Bridge mode
            011 = CWG outputs operate in Reverse Full-Bridge mode
            010 = CWG outputs operate in Forward Full-Bridge mode
            001 = CWG outputs operate in Synchronous Steering mode
            000 = CWG outputs operate in Asynchronous Steering mode

Note 1: This bit can only be set after EN = 1; it cannot be set in the same cycle when EN is set.
## REGISTER 26-2: CWGxCON1: CWG CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R-x</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>IN</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **q** = Value depends on condition

- **bit 7-6**: Unimplemented: Read as ‘0’
- **bit 5**: IN: CWG Input Value bit (read-only)
- **bit 4**: Unimplemented: Read as ‘0’
- **bit 3**: POLD: CWGxD Output Polarity bit
  - 1 = Signal output is inverted polarity
  - 0 = Signal output is normal polarity
- **bit 2**: POLC: CWGxC Output Polarity bit
  - 1 = Signal output is inverted polarity
  - 0 = Signal output is normal polarity
- **bit 1**: POLB: CWGxB Output Polarity bit
  - 1 = Signal output is inverted polarity
  - 0 = Signal output is normal polarity
- **bit 0**: POLA: CWGxA Output Polarity bit
  - 1 = Signal output is inverted polarity
  - 0 = Signal output is normal polarity
REGISTER 26-3: CWGxCLK: CWGx CLOCK INPUT SELECTION REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CS</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
’1’ = Bit is set  ‘0’ = Bit is cleared  q = Value depends on condition

bit 7-1  Unimplemented: Read as ‘0’
bit 0  CS: CWG Clock Source Selection Select bits

<table>
<thead>
<tr>
<th>CS</th>
<th>CWG1</th>
<th>CWG2</th>
<th>CWG3</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>HFINTOSC (1)</td>
<td>HFINTOSC (1)</td>
<td>HFINTOSC (1)</td>
</tr>
<tr>
<td>0</td>
<td>Fosc</td>
<td>Fosc</td>
<td>Fosc</td>
</tr>
</tbody>
</table>

Note 1: HFINTOSC remains operating during Sleep.
# REGISTER 26-4: CWGxISM: CWGx INPUT SELECTION REGISTER

<table>
<thead>
<tr>
<th>IS&lt;4:0&gt;</th>
<th>CWG1</th>
<th>CWG2</th>
<th>CWG3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Input Selection</td>
<td>Input Selection</td>
<td>Input Selection</td>
</tr>
<tr>
<td>11111-10011</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>10010</td>
<td>CLC4_out</td>
<td>CLC4_out</td>
<td>CLC4_out</td>
</tr>
<tr>
<td>10001</td>
<td>CLC3_out</td>
<td>CLC3_out</td>
<td>CLC3_out</td>
</tr>
<tr>
<td>10000</td>
<td>CLC2_out</td>
<td>CLC2_out</td>
<td>CLC2_out</td>
</tr>
<tr>
<td>01111</td>
<td>CLC1_out</td>
<td>CLC1_out</td>
<td>CLC1_out</td>
</tr>
<tr>
<td>01110</td>
<td>DSM_out</td>
<td>DSM_out</td>
<td>DSM_out</td>
</tr>
<tr>
<td>01101</td>
<td>CMP2OUT</td>
<td>CMP2OUT</td>
<td>CMP2OUT</td>
</tr>
<tr>
<td>01100</td>
<td>CMP1OUT</td>
<td>CMP1OUT</td>
<td>CMP1OUT</td>
</tr>
<tr>
<td>01011</td>
<td>NCO1OUT</td>
<td>NCO1OUT</td>
<td>NCO1OUT</td>
</tr>
<tr>
<td>01010-01001</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>01000</td>
<td>PWM8OUT</td>
<td>PWM8OUT</td>
<td>PWM8OUT</td>
</tr>
<tr>
<td>00111</td>
<td>PWM7OUT</td>
<td>PWM7OUT</td>
<td>PWM7OUT</td>
</tr>
<tr>
<td>00110</td>
<td>PWM6OUT</td>
<td>PWM6OUT</td>
<td>PWM6OUT</td>
</tr>
<tr>
<td>00101</td>
<td>PWM5OUT</td>
<td>PWM5OUT</td>
<td>PWM5OUT</td>
</tr>
<tr>
<td>00100</td>
<td>CCP4_out</td>
<td>CCP4_out</td>
<td>CCP4_out</td>
</tr>
<tr>
<td>00011</td>
<td>CCP3_out</td>
<td>CCP3_out</td>
<td>CCP3_out</td>
</tr>
<tr>
<td>00010</td>
<td>CCP2_out</td>
<td>CCP2_out</td>
<td>CCP2_out</td>
</tr>
<tr>
<td>00001</td>
<td>CCP1_out</td>
<td>CCP1_out</td>
<td>CCP1_out</td>
</tr>
<tr>
<td>00000</td>
<td>Pin selected by CWG1PPS</td>
<td>Pin selected by CWG2PPS</td>
<td>Pin selected by CWG3PPS</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **’1’** = Bit is set
- **‘0’** = Bit is cleared
- **q** = Value depends on condition

bit 7-5: **Unimplemented** Read as ‘0’

bit 4-0: **IS<4:0>: CWG Data Input Selection Multiplexer Select bits**
<table>
<thead>
<tr>
<th>bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>OVRD</td>
<td>Steering Data D bit</td>
</tr>
<tr>
<td>6</td>
<td>OVRC</td>
<td>Steering Data C bit</td>
</tr>
<tr>
<td>5</td>
<td>OVRB</td>
<td>Steering Data B bit</td>
</tr>
<tr>
<td>4</td>
<td>OVRA</td>
<td>Steering Data A bit</td>
</tr>
<tr>
<td>3</td>
<td>STRD</td>
<td>Steering Enable bit D&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = CWGxD output has the CWG data input waveform with polarity control from POLD bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = CWGxD output is assigned to value of OVRD bit</td>
</tr>
<tr>
<td>2</td>
<td>STRC</td>
<td>Steering Enable bit C&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = CWGxC output has the CWG data input waveform with polarity control from POLC bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = CWGxC output is assigned to value of OVRC bit</td>
</tr>
<tr>
<td>1</td>
<td>STRB</td>
<td>Steering Enable bit B&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = CWGxB output has the CWG data input waveform with polarity control from POLB bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = CWGxB output is assigned to value of OVRB bit</td>
</tr>
<tr>
<td>0</td>
<td>STRA</td>
<td>Steering Enable bit A&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = CWGxA output has the CWG data input waveform with polarity control from POLA bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = CWGxA output is assigned to value of OVRA bit</td>
</tr>
</tbody>
</table>

**Note 1:** The bits in this register apply only when MODE<2:0> = 00x (Register 26-1, Steering modes).

**Note 2:** This bit is double-buffered when MODE<2:0> = 001.
**REGISTER 26-6: CWGxAS0: CWG AUTO-SHUTDOWN CONTROL REGISTER 0**

<table>
<thead>
<tr>
<th></th>
<th>R/W/HS/HC-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-1/1</th>
<th>R/W-0/0</th>
<th>R/W-1/1</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SHUTDOWN</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>REN</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>LSBD&lt;1:0&gt;</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>LSAC&lt;1:0&gt;</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **HS/HC** = Bit is set/cleared by hardware
- **q** = Value depends on condition

**bit 7**
- **SHUTDOWN:** Auto-Shutdown Event Status bit
  - **1** = An auto-shutdown state is in effect
  - **0** = No auto-shutdown event has occurred

**bit 6**
- **REN:** Auto-Restart Enable bit
  - **1** = Auto-restart is enabled
  - **0** = Auto-restart is disabled

**bit 5-4**
- **LSBD<1:0>:** CWGxB and CWGxD Auto-Shutdown State Control bits
  - **11** = A logic '1' is placed on CWGxB/D when an auto-shutdown event occurs.
  - **10** = A logic '0' is placed on CWGxB/D when an auto-shutdown event occurs.
  - **01** = Pin is tri-stated on CWGxB/D when an auto-shutdown event occurs.
  - **00** = The inactive state of the pin, including polarity, is placed on CWGxB/D after the required dead-band interval when an auto-shutdown event occurs.

**bit 3-2**
- **LSAC<1:0>:** CWGxA and CWGxC Auto-Shutdown State Control bits
  - **11** = A logic '1' is placed on CWGxA/C when an auto-shutdown event occurs.
  - **10** = A logic '0' is placed on CWGxA/C when an auto-shutdown event occurs.
  - **01** = Pin is tri-stated on CWGxA/C when an auto-shutdown event occurs.
  - **00** = The inactive state of the pin, including polarity, is placed on CWGxA/C after the required dead-band interval when an auto-shutdown event occurs.

**bit 1-0**
- **Unimplemented:** Read as '0'

**Note 1:** This bit may be written while EN = 0 (Register 26-1), to place the outputs into the shutdown configuration.

**Note 2:** The outputs will remain in auto-shutdown state until the next rising edge of the CWG data input after this bit is cleared.
### REGISTER 26-7: CWGxAS1: CWG AUTO-SHUTDOWN CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>—</td>
<td>AS6E</td>
<td>AS5E</td>
<td>AS4E</td>
<td>AS3E</td>
<td>AS2E</td>
<td>AS1E</td>
<td>AS0E</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **q** = Value depends on condition
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

#### bit 7
- **Unimplemented** Read as ‘0’

#### bit 6
- **AS6E**: CWG Auto-shutdown Source 6 Enable bit
  - **1** = Auto-shutdown for Source 6 is enabled
  - **0** = Auto-shutdown for Source 6 is disabled

<table>
<thead>
<tr>
<th>CWG Module</th>
<th>CWG1</th>
<th>CWG2</th>
<th>CWG3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Auto-shutdown Source 6</td>
<td>CLC2 OUT</td>
<td>CLC3 OUT</td>
<td>CLC4 OUT</td>
</tr>
</tbody>
</table>

#### bit 5
- **AS5E**: CWG Auto-shutdown Source 5 (CMP2 OUT) Enable bit
  - **1** = Auto-shutdown for CMP2 OUT is enabled
  - **0** = Auto-shutdown for CMP2 OUT is disabled

#### bit 4
- **AS4E**: CWG Auto-shutdown Source 4 (CMP1 OUT) Enable bit
  - **1** = Auto-shutdown for CMP1 OUT is enabled
  - **0** = Auto-shutdown for CMP1 OUT is disabled

#### bit 3
- **AS3E**: CWG Auto-shutdown Source 3 (TMR6_Postscaled) Enable bit
  - **1** = Auto-shutdown for TMR6_Postscaled is enabled
  - **0** = Auto-shutdown for TMR6_Postscaled is disabled

#### bit 2
- **AS2E**: CWG Auto-shutdown Source 2 (TMR4_Postscaled) Enable bit
  - **1** = Auto-shutdown for TMR4_Postscaled is enabled
  - **0** = Auto-shutdown for TMR4_Postscaled is disabled

#### bit 1
- **AS1E**: CWG Auto-shutdown Source 1 (TMR2<Postscaled) Enable bit
  - **1** = Auto-shutdown for TMR2<Postscaled is enabled
  - **0** = Auto-shutdown for TMR2<Postscaled is disabled

#### bit 0
- **AS0E**: CWG Auto-shutdown Source 0 (Pin selected by CWGxPPS) Enable bit
  - **1** = Auto-shutdown for CWGxPPS Pin is enabled
  - **0** = Auto-shutdown for CWGxPPS Pin is disabled
### REGISTER 26-8: CWGxDBR: CWG RISING DEAD-BAND COUNT REGISTER

<p>| | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>DBR&lt;5:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **q** = Value depends on condition

**bit 7-6**
- **Unimplemented:** Read as ‘0’

**bit 5-0**
- **DBR<5:0>:** CWG Rising Edge Triggered Dead-Band Count bits
  - **11 1111 = 63-64 CWG clock periods**
  - **11 1110 = 62-63 CWG clock periods**
  - ...
  - **00 0010 = 2-3 CWG clock periods**
  - **00 0001 = 1-2 CWG clock periods**
  - **00 0000 = 0 CWG clock periods. Dead-band generation is by-passed**

### REGISTER 26-9: CWGxDBF: CWG FALLING DEAD-BAND COUNT REGISTER

<p>| | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>DBF&lt;5:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **q** = Value depends on condition

**bit 7-6**
- **Unimplemented:** Read as ‘0’

**bit 5-0**
- **DBF<5:0>:** CWG Falling Edge Triggered Dead-Band Count bits
  - **11 1111 = 63-64 CWG clock periods**
  - **11 1110 = 62-63 CWG clock periods**
  - ...
  - **00 0010 = 2-3 CWG clock periods**
  - **00 0001 = 1-2 CWG clock periods**
  - **00 0000 = 0 CWG clock periods. Dead-band generation is by-passed.**
### TABLE 26-2: SUMMARY OF REGISTERS ASSOCIATED WITH CWG

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CWGxCON0</td>
<td>EN</td>
<td>LD</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>410</td>
</tr>
<tr>
<td>CWGxCON1</td>
<td>—</td>
<td>—</td>
<td>IN</td>
<td>—</td>
<td>POLD</td>
<td>POLC</td>
<td>POLB</td>
<td>POLA</td>
<td>411</td>
</tr>
<tr>
<td>CWGxCLK</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>412</td>
</tr>
<tr>
<td>CWGxISM</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>413</td>
</tr>
<tr>
<td>CWGxSTR</td>
<td>OVRD</td>
<td>OVRB</td>
<td>OVRA</td>
<td>STRD</td>
<td>STRC</td>
<td>STRB</td>
<td>STRA</td>
<td>—</td>
<td>414</td>
</tr>
<tr>
<td>CWGxAS0</td>
<td>SHUTDOWN</td>
<td>REN</td>
<td>LSBD&lt;1:0&gt;</td>
<td>LSAC&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>415</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CWGxAS1</td>
<td>—</td>
<td>AS6E</td>
<td>AS5E</td>
<td>AS4E</td>
<td>AS3E</td>
<td>AS2E</td>
<td>AS1E</td>
<td>AS0E</td>
<td>416</td>
</tr>
<tr>
<td>CWGxDBR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DBR&lt;5:0&gt;</td>
<td>—</td>
<td>—</td>
<td>417</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CWGxDBF</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DBF&lt;5:0&gt;</td>
<td>—</td>
<td>—</td>
<td>417</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:** — unimplemented locations read as ‘0’. Shaded cells are not used by CWG.
27.0 CONFIGURABLE LOGIC CELL (CLC)

The Configurable Logic Cell (CLCx) module provides programmable logic that operates outside the speed limitations of software execution. The logic cell takes up to 32 input signals and, through the use of configurable gates, reduces the 32 inputs to four logic lines that drive one of eight selectable single-output logic functions.

Input sources are a combination of the following:

- I/O pins
- Internal clocks
- Peripherals
- Register bits

The output can be directed internally to peripherals and to an output pin.

There are four CLC modules available on this device - CLC1, CLC2, CLC3 and CLC4.

Note: The CLC1, CLC2, CLC3 and CLC4 are four separate module instances of the same CLC module design. Throughout this section, the lower case 'x' in register names is a generic reference to the CLC number (which should be substituted with 1, 2, 3, or 4 during code development). For example, the control register is generically described in this chapter as CLCxCON, but the actual device registers are CLC1CON, CLC2CON, CLC3CON and CLC4CON.

Refer to Figure 27-1 for a simplified diagram showing signal flow through the CLCx.

Possible configurations include:

- Combinatorial Logic
  - AND
  - NAND
  - AND-OR
  - AND-OR-INVERT
  - OR-XOR
  - OR-XNOR
- Latches
  - S-R
  - Clocked D with Set and Reset
  - Transparent D with Set and Reset
27.1 CLCx Setup

Programming the CLCx module is performed by configuring the four stages in the logic signal flow. The four stages are:

- Data selection
- Data gating
- Logic function selection
- Output polarity

Each stage is setup at run time by writing to the corresponding CLCx Special Function Registers. This has the added advantage of permitting logic reconfiguration on-the-fly during program execution.

27.1.1 DATA SELECTION

There are 32 signals available as inputs to the configurable logic. Four 32-input multiplexers are used to select the inputs to pass on to the next stage.

Data selection is through four multiplexers as indicated on the left side of Figure 27-2. Data inputs in the figure are identified by a generic numbered input name.

Table 27-1 correlates the generic input name to the actual signal for each CLC module. The column labeled ‘DyS<4:0> Value’ indicates the MUX selection code for the selected data input. DyS is an abbreviation for the MUX select input codes: D1S<4:0> through D4S<4:0>.
### TABLE 27-1: CLCx DATA INPUT SELECTION

<table>
<thead>
<tr>
<th>DyS&lt;5:0&gt; Value</th>
<th>CLCx Input Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>111111 [63]</td>
<td>Reserved</td>
</tr>
<tr>
<td>·</td>
<td></td>
</tr>
<tr>
<td>·</td>
<td></td>
</tr>
<tr>
<td>110110 [55]</td>
<td></td>
</tr>
<tr>
<td>110110 [54]</td>
<td>CAN_tx1</td>
</tr>
<tr>
<td>110101 [53]</td>
<td>CAN_tx0</td>
</tr>
<tr>
<td>110100 [52]</td>
<td>CGW3B_out</td>
</tr>
<tr>
<td>110011 [51]</td>
<td>CGW3A_out</td>
</tr>
<tr>
<td>110010 [50]</td>
<td>CGW2B_out</td>
</tr>
<tr>
<td>110001 [49]</td>
<td>CGW2A_out</td>
</tr>
<tr>
<td>110000 [48]</td>
<td>CGW1B_out</td>
</tr>
<tr>
<td>101111 [47]</td>
<td>CGW1A_out</td>
</tr>
<tr>
<td>101110 [46]</td>
<td>SS1</td>
</tr>
<tr>
<td>101101 [45]</td>
<td>SCK1</td>
</tr>
<tr>
<td>101100 [44]</td>
<td>SDO1</td>
</tr>
<tr>
<td>101101 [43]</td>
<td>Reserved</td>
</tr>
<tr>
<td>101100 [42]</td>
<td>UART2_tx_out</td>
</tr>
<tr>
<td>101001 [41]</td>
<td>UART1_tx_out</td>
</tr>
<tr>
<td>101000 [40]</td>
<td>CLC4_out</td>
</tr>
<tr>
<td>100111 [39]</td>
<td>CLC3_out</td>
</tr>
<tr>
<td>100110 [38]</td>
<td>CLC2_out</td>
</tr>
<tr>
<td>100101 [37]</td>
<td>CLC1_out</td>
</tr>
<tr>
<td>100100 [36]</td>
<td>DSM1_out</td>
</tr>
<tr>
<td>100011 [35]</td>
<td>IOC_flag</td>
</tr>
<tr>
<td>100010 [34]</td>
<td>ZCD_out</td>
</tr>
<tr>
<td>100001 [33]</td>
<td>CMP2_out</td>
</tr>
<tr>
<td>100000 [32]</td>
<td>CMP1_out</td>
</tr>
<tr>
<td>011111 [31]</td>
<td>NCO1_out</td>
</tr>
<tr>
<td>011110 [30]</td>
<td>Reserved</td>
</tr>
<tr>
<td>011101 [29]</td>
<td>Reserved</td>
</tr>
<tr>
<td>011100 [28]</td>
<td>PWM8_out</td>
</tr>
<tr>
<td>011011 [27]</td>
<td>PWM7_out</td>
</tr>
<tr>
<td>011010 [26]</td>
<td>PWM6_out</td>
</tr>
<tr>
<td>011001 [25]</td>
<td>PWM5_out</td>
</tr>
<tr>
<td>011000 [24]</td>
<td>CCP4_out</td>
</tr>
<tr>
<td>010111 [23]</td>
<td>CCP3_out</td>
</tr>
<tr>
<td>010110 [22]</td>
<td>CCP2_out</td>
</tr>
<tr>
<td>010101 [21]</td>
<td>CCP1_out</td>
</tr>
<tr>
<td>010100 [20]</td>
<td>SMT2_out</td>
</tr>
<tr>
<td>010011 [19]</td>
<td>SMT1_out</td>
</tr>
<tr>
<td>010010 [18]</td>
<td>TMR6_out</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DyS&lt;5:0&gt; Value</th>
<th>CLCx Input Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>010001 [17]</td>
<td>TMR5_overflow</td>
</tr>
<tr>
<td>010000 [16]</td>
<td>TMR4_out</td>
</tr>
<tr>
<td>001111 [15]</td>
<td>TMR3_overflow</td>
</tr>
<tr>
<td>001110 [14]</td>
<td>TMR2_out</td>
</tr>
<tr>
<td>001101 [13]</td>
<td>TMR1_overflow</td>
</tr>
<tr>
<td>001100 [12]</td>
<td>TMR0_overflow</td>
</tr>
<tr>
<td>001010 [10]</td>
<td>ADCRC</td>
</tr>
<tr>
<td>001001 [9]</td>
<td>SOSC</td>
</tr>
<tr>
<td>001000 [8]</td>
<td>MFINTOSC (32 kHz)</td>
</tr>
<tr>
<td>000111 [7]</td>
<td>MFINTOSC (500 kHz)</td>
</tr>
<tr>
<td>000110 [6]</td>
<td>LFINTOSC</td>
</tr>
<tr>
<td>000101 [5]</td>
<td>HFINTOSC</td>
</tr>
<tr>
<td>000100 [4]</td>
<td>Fosc</td>
</tr>
<tr>
<td>000011 [3]</td>
<td>CLCIN3PPS</td>
</tr>
<tr>
<td>000010 [2]</td>
<td>CLCIN2PPS</td>
</tr>
<tr>
<td>000001 [1]</td>
<td>CLCIN1PPS</td>
</tr>
<tr>
<td>000000 [0]</td>
<td>CLCIN0PPS</td>
</tr>
</tbody>
</table>
27.1.2 DATA GATING

Outputs from the input multiplexers are directed to the desired logic function input through the data gating stage. Each data gate can direct any combination of the four selected inputs.

Note: Data gating is undefined at power-up.

The gate stage is more than just signal direction. The gate can be configured to direct each input signal as inverted or non-inverted data. Directed signals are ANDed together in each gate. The output of each gate can be inverted before going on to the logic function stage.

The gating is in essence a 1-to-4 input AND/NAND/OR/NOR gate. When every input is inverted and the output is inverted, the gate is an OR of all enabled data inputs. When the inputs and output are not inverted, the gate is an AND or all enabled inputs.

Table 27-2 summarizes the basic logic that can be obtained in gate 1 by using the gate logic select bits. The table shows the logic of four input variables, but each gate can be configured to use less than four. If no inputs are selected, the output will be zero or one, depending on the gate output polarity bit.

**TABLE 27-2: DATA GATING LOGIC**

<table>
<thead>
<tr>
<th>CLCxGLSy</th>
<th>GyPOL</th>
<th>Gate Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x55</td>
<td>1</td>
<td>AND</td>
</tr>
<tr>
<td>0x55</td>
<td>0</td>
<td>NAND</td>
</tr>
<tr>
<td>0xAA</td>
<td>1</td>
<td>NOR</td>
</tr>
<tr>
<td>0xAA</td>
<td>0</td>
<td>OR</td>
</tr>
<tr>
<td>0x00</td>
<td>0</td>
<td>Logic 0</td>
</tr>
<tr>
<td>0x00</td>
<td>1</td>
<td>Logic 1</td>
</tr>
</tbody>
</table>

It is possible (but not recommended) to select both the true and negated values of an input. When this is done, the gate output is zero, regardless of the other inputs, but may emit logic glitches (transient-induced pulses). If the output of the channel must be zero or one, the recommended method is to set all gate bits to zero and use the gate polarity bit to set the desired level.

Data gating is configured with the logic gate select registers as follows:

- Gate 1: CLCxGLS0 (Register 27-7)
- Gate 2: CLCxGLS1 (Register 27-8)
- Gate 3: CLCxGLS2 (Register 27-9)
- Gate 4: CLCxGLS3 (Register 27-10)

Register number suffixes are different than the gate numbers because other variations of this module have multiple gate selections in the same register.

Data gating is indicated in the right side of Figure 27-2. Only one gate is shown in detail. The remaining three gates are configured identically with the exception that the data enables correspond to the enables for that gate.

27.1.3 LOGIC FUNCTION

There are eight available logic functions including:

- AND-OR
- OR-XOR
- AND
- S-R Latch
- D Flip-Flop with Set and Reset
- D Flip-Flop with Reset
- J-K Flip-Flop with Reset
- Transparent Latch with Set and Reset

Logic functions are shown in Figure 27-2. Each logic function has four inputs and one output. The four inputs are the four data gate outputs of the previous stage. The output is fed to the inversion stage and from there to other peripherals, an output pin, and back to the CLCx itself.

27.1.4 OUTPUT POLARITY

The last stage in the Configurable Logic Cell is the output polarity. Setting the POL bit of the CLCxPOL register inverts the output signal from the logic stage. Changing the polarity while the interrupts are enabled will cause an interrupt for the resulting output transition.
27.2 CLCx Interrupts

An interrupt will be generated upon a change in the output value of the CLCx when the appropriate interrupt enables are set. A rising edge detector and a falling edge detector are present in each CLC for this purpose. The CLCxIF bit of the associated PIR5 register will be set when either edge detector is triggered and its associated enable bit is set. The INTP enables rising edge interrupts and the INTN bit enables falling edge interrupts. Both are located in the CLCxCON register.

To fully enable the interrupt, set the following bits:
- CLCxIE bit of the respective PIE register
- INTP bit of the CLCxCON register (for a rising edge detection)
- INTN bit of the CLCxCON register (for a falling edge detection)
- GIE bits of the INTCON0 register

The CLCxIF bit of the respective PIR register must be cleared in software as part of the interrupt service. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

27.3 Output Mirror Copies

Mirror copies of all CON output bits are contained in the CLCxDATA register. Reading this register reads the outputs of all CLCs simultaneously. This prevents any reading skew introduced by testing or reading the OUT bits in the individual CLCxCON registers.

27.4 Effects of a Reset

The CLCxCON register is cleared to zero as the result of a Reset. All other selection and gating values remain unchanged.

27.5 Operation During Sleep

The CLC module operates independently from the system clock and will continue to run during Sleep, provided that the input sources selected remain active.

The HFINTOSC remains active during Sleep when the CLC module is enabled and the HFINTOSC is selected as an input source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and as a CLC input source, when the CLC is enabled, the CPU will go Idle during Sleep, but the CLC will continue to operate and the HFINTOSC will remain active.

This will have a direct effect on the Sleep mode current.

27.6 CLCx Setup Steps

The following steps should be followed when setting up the CLCx:
- Disable CLCx by clearing the EN bit.
- Select desired inputs using CLCxSEL0 through CLCxSEL3 registers (See Table 27-1).
- Clear any associated ANSEL bits.
- Set all TRIS bits associated with inputs.
- Clear all TRIS bits associated with outputs.
- Enable the chosen inputs through the four gates using CLCxGLS0, CLCxGLS1, CLCxGLS2, and CLCxGLS3 registers.
- Select the gate output polarities with the GyPOL bits of the CLCxPOL register.
- Select the desired logic function with the MODE<2:0> bits of the CLCxCON register.
- Select the desired polarity of the logic output with the POL bit of the CLCxPOL register.
- If driving a device pin, set the desired pin PPS control register and also clear the TRIS bit corresponding to that output.
- If interrupts are desired, configure the following bits:
  - Set the INTP bit in the CLCxCON register for rising event.
  - Set the INTN bit in the CLCxCON register for falling event.
  - Set the CLCxIE bit of the respective PIE register.
  - Set the GIE bits of the INTCON0 register.
- Enable the CLCx by setting the EN bit of the CLCxCON register.
FIGURE 27-2: INPUT DATA SELECTION AND GATING

Data Selection

Note: All controls are undefined at power-up.
FIGURE 27-3: PROGRAMMABLE LOGIC FUNCTIONS

- **AND-OR**
  - Mode<2:0> = 000

- **OR-XOR**
  - Mode<2:0> = 001

- **4-input AND**
  - Mode<2:0> = 010

- **S-R Latch**
  - Mode<2:0> = 011

- **1-Input D Flip-Flop with S and R**
  - Mode<2:0> = 100

- **2-Input D Flip-Flop with R**
  - Mode<2:0> = 101

- **J-K Flip-Flop with R**
  - Mode<2:0> = 110

- **1-Input Transparent Latch with S and R**
  - Mode<2:0> = 111
### Register Definitions: CLC Control

#### REGISTER 27-1: CLCxCON: CONFIGURABLE LOGIC CELL CONTROL REGISTER

<table>
<thead>
<tr>
<th>EN</th>
<th>OUT</th>
<th>INTP</th>
<th>INTN</th>
<th>MODE&lt;2:0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>U-0</td>
<td>R-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
</tbody>
</table>

**Legend:**

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

**bit 7**

**EN:** Configurable Logic Cell Enable bit

- 1 = Configurable logic cell is enabled and mixing input signals
- 0 = Configurable logic cell is disabled and has logic zero output

**bit 6**

**Unimplemented:** Read as ‘0’

**bit 5**

**OUT:** Configurable Logic Cell Data Output bit

Read-only: logic cell output data, after LCPO; sampled from CLCxOUT

**bit 4**

**INTP:** Configurable Logic Cell Positive Edge Going Interrupt Enable bit

- 1 = CLCxIF will be set when a rising edge occurs on CLCxOUT
- 0 = CLCxIF will not be set

**bit 3**

**INTN:** Configurable Logic Cell Negative Edge Going Interrupt Enable bit

- 1 = CLCxIF will be set when a falling edge occurs on CLCxOUT
- 0 = CLCxIF will not be set

**bit 2-0**

**MODE<2:0>:** Configurable Logic Cell Functional Mode bits

- 111 = Cell is 1-input transparent latch with S and R
- 110 = Cell is J-K flip-flop with R
- 101 = Cell is 2-input D flip-flop with R
- 100 = Cell is 1-input D flip-flop with S and R
- 011 = Cell is S-R latch
- 010 = Cell is 4-input AND
- 001 = Cell is OR-XOR
- 000 = Cell is AND-OR
**REGISTER 27-2: CLC\text{CxPOL}: SIGNAL POLARITY CONTROL REGISTER**

<table>
<thead>
<tr>
<th></th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>POL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>G4POL</td>
<td>G3POL</td>
<td>G2POL</td>
<td>G1POL</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

bit 7 **POL**: CLC\text{CxOUT} Output Polarity Control bit
- 1 = The output of the logic cell is inverted
- 0 = The output of the logic cell is not inverted

bit 6-4 **Unimplemented**: Read as '0'

bit 3 **G4POL**: Gate 3 Output Polarity Control bit
- 1 = The output of gate 3 is inverted when applied to the logic cell
- 0 = The output of gate 3 is not inverted

bit 2 **G3POL**: Gate 2 Output Polarity Control bit
- 1 = The output of gate 2 is inverted when applied to the logic cell
- 0 = The output of gate 2 is not inverted

bit 1 **G2POL**: Gate 1 Output Polarity Control bit
- 1 = The output of gate 1 is inverted when applied to the logic cell
- 0 = The output of gate 1 is not inverted

bit 0 **G1POL**: Gate 0 Output Polarity Control bit
- 1 = The output of gate 0 is inverted when applied to the logic cell
- 0 = The output of gate 0 is not inverted
### REGISTER 27-3: CLCxSEL0: GENERIC CLCx DATA 0 SELECT REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

- **bit 7-6**: Unimplemented: Read as '0'
- **bit 5-0**: D1S<5:0>: CLCx Data0 Input Selection bits 
  See Table 27-1.

### REGISTER 27-4: CLCxSEL1: GENERIC CLCx DATA 1 SELECT REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

- **bit 7-6**: Unimplemented: Read as '0'
- **bit 5-0**: D2S<5:0>: CLCx Data 1 Input Selection bits 
  See Table 27-1.

### REGISTER 27-5: CLCxSEL2: GENERIC CLCx DATA 2 SELECT REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

- **bit 7-6**: Unimplemented: Read as '0'
- **bit 5-0**: D3S<5:0>: CLCx Data 2 Input Selection bits 
  See Table 27-1.

### REGISTER 27-6: CLCxSEL3: GENERIC CLCx DATA 3 SELECT REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

- **bit 7-6**: Unimplemented: Read as '0'
- **bit 5-0**: D4S<5:0>: CLCx Data 3 Input Selection bits 
  See Table 27-1.
### REGISTER 27-7: CLCxGLS0: GATE 0 LOGIC SELECT REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
</tr>
<tr>
<td>G1D4T</td>
<td>G1D4N</td>
<td>G1D3T</td>
<td>G1D3N</td>
<td>G1D2T</td>
<td>G1D2N</td>
<td>G1D1T</td>
<td>G1D1N</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

- **bit 7**
  - **G1D4T**: Gate 0 Data 4 True (non-inverted) bit
  - 1 = CLCIN3 (true) is gated into CLCx Gate 0
  - 0 = CLCIN3 (true) is not gated into CLCx Gate 0

- **bit 6**
  - **G1D4N**: Gate 0 Data 4 Negated (inverted) bit
  - 1 = CLCIN3 (inverted) is gated into CLCx Gate 0
  - 0 = CLCIN3 (inverted) is not gated into CLCx Gate 0

- **bit 5**
  - **G1D3T**: Gate 0 Data 3 True (non-inverted) bit
  - 1 = CLCIN2 (true) is gated into CLCx Gate 0
  - 0 = CLCIN2 (true) is not gated into CLCx Gate 0

- **bit 4**
  - **G1D3N**: Gate 0 Data 3 Negated (inverted) bit
  - 1 = CLCIN2 (inverted) is gated into CLCx Gate 0
  - 0 = CLCIN2 (inverted) is not gated into CLCx Gate 0

- **bit 3**
  - **G1D2T**: Gate 0 Data 2 True (non-inverted) bit
  - 1 = CLCIN1 (true) is gated into CLCx Gate 0
  - 0 = CLCIN1 (true) is not gated into CLCx Gate 0

- **bit 2**
  - **G1D2N**: Gate 0 Data 2 Negated (inverted) bit
  - 1 = CLCIN1 (inverted) is gated into CLCx Gate 0
  - 0 = CLCIN1 (inverted) is not gated into CLCx Gate 0

- **bit 1**
  - **G1D1T**: Gate 0 Data 1 True (non-inverted) bit
  - 1 = CLCIN0 (true) is gated into CLCx Gate 0
  - 0 = CLCIN0 (true) is not gated into CLCx Gate 0

- **bit 0**
  - **G1D1N**: Gate 0 Data 1 Negated (inverted) bit
  - 1 = CLCIN0 (inverted) is gated into CLCx Gate 0
  - 0 = CLCIN0 (inverted) is not gated into CLCx Gate 0
REGISTER 27-8: CLCxGLS1: GATE 1 LOGIC SELECT REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>G2D4T</td>
<td>G2D4N</td>
<td>G2D3T</td>
<td>G2D3N</td>
<td>G2D2T</td>
<td>G2D2N</td>
<td>G2D1T</td>
<td>G2D1N</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

- **bit 7**
  - **G2D4T**: Gate 1 Data 4 True (noninverted) bit
    - 1 = CLCIN3 (true) is gated into CLCx Gate 1
    - 0 = CLCIN3 (true) is not gated into CLCx Gate 1

- **bit 6**
  - **G2D4N**: Gate 1 Data 4 Negated (inverted) bit
    - 1 = CLCIN3 (inverted) is gated into CLCx Gate 1
    - 0 = CLCIN3 (inverted) is not gated into CLCx Gate 1

- **bit 5**
  - **G2D3T**: Gate 1 Data 3 True (noninverted) bit
    - 1 = CLCIN2 (true) is gated into CLCx Gate 1
    - 0 = CLCIN2 (true) is not gated into CLCx Gate 1

- **bit 4**
  - **G2D3N**: Gate 1 Data 3 Negated (inverted) bit
    - 1 = CLCIN2 (inverted) is gated into CLCx Gate 1
    - 0 = CLCIN2 (inverted) is not gated into CLCx Gate 1

- **bit 3**
  - **G2D2T**: Gate 1 Data 2 True (noninverted) bit
    - 1 = CLCIN1 (true) is gated into CLCx Gate 1
    - 0 = CLCIN1 (true) is not gated into CLCx Gate 1

- **bit 2**
  - **G2D2N**: Gate 1 Data 2 Negated (inverted) bit
    - 1 = CLCIN1 (inverted) is gated into CLCx Gate 1
    - 0 = CLCIN1 (inverted) is not gated into CLCx Gate 1

- **bit 1**
  - **G2D1T**: Gate 1 Data 1 True (noninverted) bit
    - 1 = CLCIN0 (true) is gated into CLCx Gate 1
    - 0 = CLCIN0 (true) is not gated into CLCx Gate 1

- **bit 0**
  - **G2D1N**: Gate 1 Data 1 Negated (inverted) bit
    - 1 = CLCIN0 (inverted) is gated into CLCx Gate 1
    - 0 = CLCIN0 (inverted) is not gated into CLCx Gate 1
## REGISTER 27-9: CLCxGLS2: GATE 2 LOGIC SELECT REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value at POR/BOR</th>
<th>Value at all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>G3D4T: Gate 2 Data 4 True (noninverted) bit</td>
<td>1</td>
<td>= CLCIN3 (true) is gated into CLCx Gate 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>= CLCIN3 (true) is not gated into CLCx Gate 2</td>
</tr>
<tr>
<td>6</td>
<td>G3D4N: Gate 2 Data 4 Negated (inverted) bit</td>
<td>1</td>
<td>= CLCIN3 (inverted) is gated into CLCx Gate 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>= CLCIN3 (inverted) is not gated into CLCx Gate 2</td>
</tr>
<tr>
<td>5</td>
<td>G3D3T: Gate 2 Data 3 True (noninverted) bit</td>
<td>1</td>
<td>= CLCIN2 (true) is gated into CLCx Gate 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>= CLCIN2 (true) is not gated into CLCx Gate 2</td>
</tr>
<tr>
<td>4</td>
<td>G3D3N: Gate 2 Data 3 Negated (inverted) bit</td>
<td>1</td>
<td>= CLCIN2 (inverted) is gated into CLCx Gate 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>= CLCIN2 (inverted) is not gated into CLCx Gate 2</td>
</tr>
<tr>
<td>3</td>
<td>G3D2T: Gate 2 Data 2 True (noninverted) bit</td>
<td>1</td>
<td>= CLCIN1 (true) is gated into CLCx Gate 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>= CLCIN1 (true) is not gated into CLCx Gate 2</td>
</tr>
<tr>
<td>2</td>
<td>G3D2N: Gate 2 Data 2 Negated (inverted) bit</td>
<td>1</td>
<td>= CLCIN1 (inverted) is gated into CLCx Gate 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>= CLCIN1 (inverted) is not gated into CLCx Gate 2</td>
</tr>
<tr>
<td>1</td>
<td>G3D1T: Gate 2 Data 1 True (noninverted) bit</td>
<td>1</td>
<td>= CLCIN0 (true) is gated into CLCx Gate 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>= CLCIN0 (true) is not gated into CLCx Gate 2</td>
</tr>
<tr>
<td>0</td>
<td>G3D1N: Gate 2 Data 1 Negated (inverted) bit</td>
<td>1</td>
<td>= CLCIN0 (inverted) is gated into CLCx Gate 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>= CLCIN0 (inverted) is not gated into CLCx Gate 2</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **n/n** = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

- **G3D4T**: Gate 2 Data 4 True (noninverted) bit
- **G3D4N**: Gate 2 Data 4 Negated (inverted) bit
- **G3D3T**: Gate 2 Data 3 True (noninverted) bit
- **G3D3N**: Gate 2 Data 3 Negated (inverted) bit
- **G3D2T**: Gate 2 Data 2 True (noninverted) bit
- **G3D2N**: Gate 2 Data 2 Negated (inverted) bit
- **G3D1T**: Gate 2 Data 1 True (noninverted) bit
- **G3D1N**: Gate 2 Data 1 Negated (inverted) bit
### REGISTER 27-10: CLCxGLS3: GATE 3 LOGIC SELECT REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Legend</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7   | G4D4T: Gate 3 Data 4 True (non-inverted) bit | 1 = CLCIN3 (true) is gated into CLCx Gate 3  
|     |        | 0 = CLCIN3 (true) is not gated into CLCx Gate 3 |
| 6   | G4D4N: Gate 3 Data 4 Negated (inverted) bit | 1 = CLCIN3 (inverted) is gated into CLCx Gate 3  
|     |        | 0 = CLCIN3 (inverted) is not gated into CLCx Gate 3 |
| 5   | G4D3T: Gate 3 Data 3 True (non-inverted) bit | 1 = CLCIN2 (true) is gated into CLCx Gate 3  
|     |        | 0 = CLCIN2 (true) is not gated into CLCx Gate 3 |
| 4   | G4D3N: Gate 3 Data 3 Negated (inverted) bit | 1 = CLCIN2 (inverted) is gated into CLCx Gate 3  
|     |        | 0 = CLCIN2 (inverted) is not gated into CLCx Gate 3 |
| 3   | G4D2T: Gate 3 Data 2 True (non-inverted) bit | 1 = CLCIN1 (true) is gated into CLCx Gate 3  
|     |        | 0 = CLCIN1 (true) is not gated into CLCx Gate 3 |
| 2   | G4D2N: Gate 3 Data 2 Negated (inverted) bit | 1 = CLCIN1 (inverted) is gated into CLCx Gate 3  
|     |        | 0 = CLCIN1 (inverted) is not gated into CLCx Gate 3 |
| 1   | G4D1T: Gate 4 Data 1 True (non-inverted) bit | 1 = CLCIN0 (true) is gated into CLCx Gate 3  
|     |        | 0 = CLCIN0 (true) is not gated into CLCx Gate 3 |
| 0   | G4D1N: Gate 3 Data 1 Negated (inverted) bit | 1 = CLCIN0 (inverted) is gated into CLCx Gate 3  
|     |        | 0 = CLCIN0 (inverted) is not gated into CLCx Gate 3 |
### REGISTER 27-11: CLCDATA: CLC DATA OUTPUT

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>CLC4OUT</th>
<th>CLC3OUT</th>
<th>CLC2OUT</th>
<th>CLC1OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CLC4OUT</td>
<td>CLC3OUT</td>
<td>CLC2OUT</td>
<td>CLC1OUT</td>
</tr>
</tbody>
</table>

#### bit 7
- **Legend:**
  - R = Readable bit
  - W = Writable bit
  - U = Unimplemented bit, read as '0'
  - u = Bit is unchanged
  - x = Bit is unknown
  - -n/n = Value at POR and BOR/Value at all other Resets
  - '1' = Bit is set
  - '0' = Bit is cleared

- bit 7-4 **Unimplemented:** Read as '0'
- bit 3 **CLC4OUT:** Mirror copy of OUT bit of CLC4CON register
- bit 2 **CLC3OUT:** Mirror copy of OUT bit of CLC3CON register
- bit 1 **CLC2OUT:** Mirror copy of OUT bit of CLC2CON register
- bit 0 **CLC1OUT:** Mirror copy of OUT bit of CLC1CON register

### TABLE 27-3: SUMMARY OF REGISTERS ASSOCIATED WITH CLCx

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLCxCON</td>
<td>EN</td>
<td>—</td>
<td>—</td>
<td>OUT</td>
<td>INTP</td>
<td>INTN</td>
<td>MODE&lt;2:0&gt;</td>
<td></td>
<td>&lt;Blue&gt;426</td>
</tr>
<tr>
<td>CLCxPOL</td>
<td>POL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>&lt;Blue&gt;427</td>
</tr>
<tr>
<td>CLCxSEL0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>D1S&lt;5:0&gt;</td>
<td>&lt;Blue&gt;428</td>
</tr>
<tr>
<td>CLCxSEL1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>D2S&lt;5:0&gt;</td>
<td>&lt;Blue&gt;428</td>
</tr>
<tr>
<td>CLCxSEL2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>D3S&lt;5:0&gt;</td>
<td>&lt;Blue&gt;428</td>
</tr>
<tr>
<td>CLCxSEL3</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>D4S&lt;5:0&gt;</td>
<td>&lt;Blue&gt;428</td>
</tr>
<tr>
<td>CLCxGLS0</td>
<td>G1D4T</td>
<td>G1D4N</td>
<td>G1D3T</td>
<td>G1D3N</td>
<td>G1D2T</td>
<td>G1D2N</td>
<td>G1D1T</td>
<td>G1D1N</td>
<td>&lt;Blue&gt;429</td>
</tr>
<tr>
<td>CLCxGLS1</td>
<td>G2D4T</td>
<td>G2D4N</td>
<td>G2D3T</td>
<td>G2D3N</td>
<td>G2D2T</td>
<td>G2D2N</td>
<td>G2D1T</td>
<td>G2D1N</td>
<td>&lt;Blue&gt;430</td>
</tr>
<tr>
<td>CLCxGLS2</td>
<td>G3D4T</td>
<td>G3D4N</td>
<td>G3D3T</td>
<td>G3D3N</td>
<td>G3D2T</td>
<td>G3D2N</td>
<td>G3D1T</td>
<td>G3D1N</td>
<td>&lt;Blue&gt;431</td>
</tr>
<tr>
<td>CLCxGLS3</td>
<td>G4D4T</td>
<td>G4D4N</td>
<td>G4D3T</td>
<td>G4D3N</td>
<td>G4D2T</td>
<td>G4D2N</td>
<td>G4D1T</td>
<td>G4D1N</td>
<td>&lt;Blue&gt;432</td>
</tr>
<tr>
<td>CLCDATA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CLC4OUT</td>
<td>CLC3OUT</td>
</tr>
</tbody>
</table>

#### Legend:
- — = unimplemented, read as '0'. Shaded cells are unused by the CLCx modules.
28.0 NUMERICALLY CONTROLLED OSCILLATOR (NCO) MODULE

The Numerically Controlled Oscillator (NCO) module is a timer that uses overflow from the addition of an increment value to divide the input frequency. The advantage of the addition method over simple counter driven timer is that the output frequency resolution does not vary with the divider value. The NCO is most useful for application that requires frequency accuracy and fine resolution at a fixed duty cycle.

Features of the NCO include:

• 20-bit Increment Function
• Fixed Duty Cycle mode (FDC) mode
• Pulse Frequency (PF) mode
• Output Pulse-Width Control
• Multiple Clock Input Sources
• Output Polarity Control
• Interrupt Capability

Figure 28-1 is a simplified block diagram of the NCO module.
**Note 1:** The increment registers are double-buffered to allow for value changes to be made without first disabling the NCO module. The full increment value is loaded into the buffer registers on the second rising edge of the NCOx_clk signal that occurs immediately after a write to NCOxINCL register. The buffers are not user-accessible and are shown here for reference.
28.1 NCO Operation

The NCO operates by repeatedly adding a fixed value to an accumulator. Additions occur at the input clock rate. The accumulator will overflow with a carry periodically, which is the raw NCO output (NCO_overflow). This effectively reduces the input clock by the ratio of the addition value to the maximum accumulator value. See Equation 28-1.

The NCO output can be further modified by stretching the pulse or toggling a flip-flop. The modified NCO output is then distributed internally to other peripherals and can be optionally output to a pin. The accumulator overflow also generates an interrupt (NCO_overflow).

The NCO period changes in discrete steps to create an average frequency. This output depends on the ability of the receiving circuit (i.e., CWG or external resonant converter circuitry) to average the NCO output to reduce uncertainty.

**EQUATION 28-1: NCO OVERFLOW FREQUENCY**

\[
F_{OVERFLOW} = \frac{NCO \text{ Clock Frequency} \times \text{Increment Value}}{2^{20}}
\]

28.1.1 NCO CLOCK SOURCES

Clock sources available to the NCO include:

- Fosc
- HFINTOSC
- LFINTOSC
- MFINTOSC/4 (32 kHz)
- MFINTOSC (500 kHz)
- CLC1/2/3/4_out
- CLKREF
- SOSC

The NCO clock source is selected by configuring the N1CKS<2:0> bits in the NCO1CLK register.

28.1.2 ACCUMULATOR

The accumulator is a 20-bit register. Read and write access to the accumulator is available through three registers:

- NCO1ACCL
- NCO1ACCH
- NCO1ACCU

28.1.3 ADDER

The NCO Adder is a full adder, which operates independently from the source clock. The addition of the previous result and the increment value replaces the accumulator value on the rising edge of each input clock.

28.1.4 INCREMENT REGISTERS

The increment value is stored in three registers making up a 20-bit incrementer. In order of LSB to MSB they are:

- NCO1INCL
- NCO1INCH
- NCO1INCU

When the NCO module is enabled, the NCO1INCU and NCO1INCH registers should be written first, then the NCO1INCL register. Writing to the NCO1INCL register initiates the increment buffer registers to be loaded simultaneously on the second rising edge of the NCO_clk signal.

The registers are readable and writable. The increment registers are double-buffered to allow value changes to be made without first disabling the NCO module.

When the NCO module is disabled, the increment buffers are loaded immediately after a write to the increment registers.

**Note:** The increment buffer registers are not user-accessible.
28.2 FIXED DUTY CYCLE MODE

In Fixed Duty Cycle (FDC) mode, every time the accumulator overflows (NCO_overflow), the output is toggled. This provides a 50% duty cycle, provided that the increment value remains constant. For more information, see Figure 28-2.

28.3 PULSE FREQUENCY MODE

In Pulse Frequency (PF) mode, every time the Accumulator overflows, the output becomes active for one or more clock periods. Once the clock period expires, the output returns to an inactive state. This provides a pulsed output. The output becomes active on the rising clock edge immediately following the overflow event. For more information, see Figure 28-2.

The value of the active and inactive states depends on the polarity bit, POL in the NCO1CON register.

The PF mode is selected by setting the PFM bit in the NCO1CON register.

28.3.1 OUTPUT PULSE-WIDTH CONTROL

When operating in PF mode, the active state of the output can vary in width by multiple clock periods. Various pulse widths are selected with the PWS<2:0> bits in the NCO1CLK register.

When the selected pulse width is greater than the Accumulator overflow time frame, then DDS operation is undefined.

28.4 OUTPUT POLARITY CONTROL

The last stage in the NCO module is the output polarity. The POL bit in the NCO1CON register selects the output polarity. Changing the polarity while the interrupts are enabled will cause an interrupt for the resulting output transition. The NCO output signal is available to most of the other peripherals available on the device.

28.5 Interrupts

When the accumulator overflows (NCO_overflow), the NCO Interrupt Flag bit, NCO1IF, of the PIR4 register is set. To enable the interrupt event (NCO_interrupt), the following bits must be set:

- EN bit of the NCO1CON register
- NCO1IE bit of the PIE4 register
- GIE/GIEH bit of the INTCON0 register

The interrupt must be cleared by software by clearing the NCO1IF bit in the Interrupt Service Routine.

28.6 Effects of a Reset

All of the NCO registers are cleared to zero as the result of a Reset.

28.7 Operation in Sleep

The NCO module operates independently from the system clock and will continue to run during Sleep, provided that the clock source selected remains active.

The HFINTOSC remains active during Sleep when the NCO module is enabled and the HFINTOSC is selected as the clock source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and the NCO clock source, when the NCO is enabled, the CPU will go Idle during Sleep, but the NCO will continue to operate and the HFINTOSC will remain active.

This will have a direct effect on the Sleep mode current.
FIGURE 28-2: FDC OUTPUT MODE OPERATION DIAGRAM

- NCOx Clock Source
- NCOx Increment Value
- NCOx Accumulator Value
- NCO Overflow
- NCO Interrupt
- NCOx Output FDC Mode
- NCOx Output PF Mode
- NCOxPWS = 000
- NCOx Output PF Mode
- NCOxPWS = 001
## 28.8 NCO Control Registers

**REGISTER 28-1: NCO1CON: NCO CONTROL REGISTER**

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>PFM</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>—</td>
<td>OUT</td>
<td>POL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7   | **EN**: NCO1 Enable bit  
   1 = NCO1 module is enabled  
   0 = NCO1 module is disabled  |
| 6   | **Unimplemented**: Read as '0'  |
| 5   | **OUT**: NCO1 Output bit  
   Displays the current output value of the NCO1 module.  |
| 4   | **POL**: NCO1 Polarity  
   1 = NCO1 output signal is inverted  
   0 = NCO1 output signal is not inverted  |
| 3-1 | **Unimplemented**: Read as '0'  |
| 0   | **PFM**: NCO1 Pulse Frequency Mode bit  
   1 = NCO1 operates in Pulse Frequency mode  
   0 = NCO1 operates in Fixed Duty Cycle mode, divide by 2  |
## REGISTER 28-2: NCO1CLK: NCO1 INPUT CLOCK CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWS&lt;2:0&gt;(1,2)</td>
<td>—</td>
<td>—</td>
<td>CKS&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

**bit 7-5**  
**PWS<2:0>:** NCO1 Output Pulse Width Select bits

- **111** = NCO1 output is active for 128 input clock periods
- **110** = NCO1 output is active for 64 input clock periods
- **101** = NCO1 output is active for 32 input clock periods
- **100** = NCO1 output is active for 16 input clock periods
- **011** = NCO1 output is active for 8 input clock periods
- **010** = NCO1 output is active for 4 input clock periods
- **001** = NCO1 output is active for 2 input clock periods
- **000** = NCO1 output is active for 1 input clock period

**bit 4**  
**Unimplemented:** Read as ‘0’

**bit 3-0**  
**CKS<3:0>:** NCO1 Clock Source Select bits

- **1111** = Reserved
- **1110** = CLC4_out
- **1101** = CLC3_out
- **1100** = CLC2_out
- **1011** = CLC1_out
- **1010** = CLKREF_out
- **1001** = SOSC
- **1000** = MFINTOSC/4 (32 kHz)
- **0111** = MFINTOSC (500 kHz)
- **0110** = LFINTOSC
- **0101** = HFINTOSC
- **0100** = FOSC

**Note 1:** N1PWS applies only when operating in Pulse Frequency mode.
**Note 2:** If NCO1 pulse width is greater than NCO1 overflow period, operation is undefined.
## REGISTER 28-3: NCO1ACCL: NCO1 ACCUMULATOR REGISTER – LOW BYTE

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Readable</th>
<th>Writable</th>
<th>Unimplemented</th>
<th>Unknown</th>
<th>Value at POR and BOR/Value at all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>ACC&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

Bit 7-0 **ACC<7:0>**: NCO1 Accumulator, Low Byte

## REGISTER 28-4: NCO1ACCH: NCO1 ACCUMULATOR REGISTER – HIGH BYTE

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Readable</th>
<th>Writable</th>
<th>Unimplemented</th>
<th>Unknown</th>
<th>Value at POR and BOR/Value at all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>ACC&lt;15:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

Bit 7-0 **ACC<15:8>**: NCO1 Accumulator, High Byte
### REGISTER 28-5: NCO1ACCU: NCO1 ACCUMULATOR REGISTER – UPPER BYTE \(^{(1)}\)

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 0</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared

**Unimplemented:** Read as ‘0’

Note 1: The accumulator spans registers NCO1ACCUB: NCO1ACCU: NCO1ACCL. The 24 bits are reserved but not all are used. This register updates in real time, asynchronously to the CPU; there is no provision to guarantee atomic access to this 24-bit space using an 8-bit bus. Writing to this register while the module is operating will produce undefined results.

### REGISTER 28-6: NCO1INCL: NCO1 INCREMENT REGISTER – LOW BYTE \(^{(1,2)}\)

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 0</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared

**INC<7:0>: NCO1 Increment, Low Byte**

Note 1: The logical increment spans NCO1INCU:NCO1INCH:NCO1INCL.

2: NCO1INC is double-buffered as INCBUF; INCBUF is updated on the next falling edge of NCOCLK after writing to NCO1INCL; NCO1INCU and NCO1INCH should be written prior to writing NCO1INCL.

### REGISTER 28-7: NCO1INCH: NCO1 INCREMENT REGISTER – HIGH BYTE \(^{(1)}\)

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 0</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared

**INC<15:8>: NCO1 Increment, High Byte**

Note 1: The logical increment spans NCO1INCU:NCO1INCH:NCO1INCL.
REGISTER 28-8: NCO1INCU: NCO1 INCREMENT REGISTER – UPPER BYTE\(^{(1)}\)

<table>
<thead>
<tr>
<th>Bit 7-4</th>
<th>Unimplemented: Read as ‘0’</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 3-0</td>
<td>(\text{INC&lt;19:16&gt;}): NCO1 Increment, Upper Byte</td>
</tr>
</tbody>
</table>

**Note 1:** The logical increment spans NCO1INCU:NCO1INCH:NCO1INCL.

### TABLE 28-1: SUMMARY OF REGISTERS ASSOCIATED WITH NCO

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCO1CON</td>
<td></td>
<td></td>
<td>N1EN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>439</td>
</tr>
<tr>
<td>NCO1CLK</td>
<td></td>
<td></td>
<td></td>
<td>N1OUT</td>
<td>N1POL</td>
<td></td>
<td></td>
<td></td>
<td>440</td>
</tr>
<tr>
<td>NCO1ACCL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>N1PWS&lt;2:0&gt;</td>
<td>N1CKS&lt;2:0&gt;</td>
<td>441</td>
</tr>
<tr>
<td>NCO1ACCH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>NCO1ACC&lt;15:8&gt;</td>
<td></td>
<td>441</td>
</tr>
<tr>
<td>NCO1ACCU</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>NCO1ACC&lt;19:16&gt;</td>
<td>442</td>
</tr>
<tr>
<td>NCO1INCL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>NCO1INC&lt;7:0&gt;</td>
<td></td>
<td>442</td>
</tr>
<tr>
<td>NCO1INCH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>NCO1INC&lt;15:8&gt;</td>
<td></td>
<td>442</td>
<td></td>
</tr>
<tr>
<td>NCO1INCU</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>NCO1INC&lt;19:16&gt;</td>
<td>443</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented read as ‘0’. Shaded cells are not used for NCO module.
29.0 ZERO-CROSS DETECTION (ZCD) MODULE

The ZCD module detects when an A/C signal crosses through the ground potential. The actual zero-crossing threshold is the zero-crossing reference voltage, VCPINV, which is typically 0.75V above ground.

The connection to the signal to be detected is through a series current-limiting resistor. The module applies a current source or sink to the ZCD pin to maintain a constant voltage on the pin, thereby preventing the pin voltage from forward biasing the ESD protection diodes. When the applied voltage is greater than the reference voltage, the module sinks current. When the applied voltage is less than the reference voltage, the module sources current. The current source and sink action keeps the pin voltage constant over the full range of the applied voltage. The ZCD module is shown in the simplified block diagram Figure 29-2.

The ZCD module is useful when monitoring an A/C waveform for, but not limited to, the following purposes:

- A/C period measurement
- Accurate long term time measurement
- Dimmer phase delayed drive
- Low EMI cycle switching

29.1 External Resistor Selection

The ZCD module requires a current-limiting resistor in series with the external voltage source. The impedance and rating of this resistor depends on the external source peak voltage. Select a resistor value that will drop all of the peak voltage when the current through the resistor is nominally 300 μA. Refer to Equation 29-1 and Figure 29-1. Make sure that the ZCD I/O pin internal weak pull-up is disabled so it does not interfere with the current source and sink.

**EQUATION 29-1: EXTERNAL RESISTOR**

\[ R_{S\text{ERIES}} = \frac{V_{\text{PEAK}}}{3 \times 10^{-4}} \]

**FIGURE 29-1: EXTERNAL VOLTAGE**

![External Voltage Diagram]
29.2 ZCD Logic Output

The ZCD module includes a Status bit, which can be read to determine whether the current source or sink is active. The OUT bit of the ZCDCON register is set when the current sink is active, and cleared when the current source is active. The OUT bit is affected by the polarity bit, even if the module is disabled.

The OUT signal can also be used as input to other modules. This is controlled by the registers of the corresponding module. OUT can be used as follows:

- Gate source for TMR1/3/5
- Clock source for TMR2/4/6
- Reset source for TMR2/4/6

29.3 ZCD Logic Polarity

The POL bit of the ZCDCON register inverts the OUT bit relative to the current source and sink output. When the POL bit is set, a OUT high indicates that the current source is active, and a low output indicates that the current sink is active.

The POL bit affects the ZCD interrupts.
29.4 ZCD Interrupts

An interrupt will be generated upon a change in the ZCD logic output when the appropriate interrupt enables are set. A rising edge detector and a falling edge detector are present in the ZCD for this purpose.

The ZCDIF bit of the respective PIR register will be set when either edge detector is triggered and its associated enable bit is set. The INTP enables rising edge interrupts and the INTN bit enables falling edge interrupts. Both are located in the ZCDCON register. Priority of the interrupt can be changed if the IPEN bit of the INTCON register is set. The ZCD interrupt can be made high or low priority by setting or clearing the ZCDIP bit of the respective IPR register.

To fully enable the interrupt, the following bits must be set:

- ZCDIE bit of the respective PIE register
- INTP bit of the ZCDCON register (for a rising edge detection)
- INTN bit of the ZCDCON register (for a falling edge detection)
- GIE bits of the INTCON0 register

Changing the POL bit can cause an interrupt, regardless of the level of the SEN bit.

The ZCDIF bit of the respective PIR register must be cleared in software as part of the interrupt service. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

29.5 Correcting for VCPINV offset

The actual voltage at which the ZCD switches is the reference voltage at the noninverting input of the ZCD op amp. For external voltage source waveforms other than square waves, this voltage offset from zero causes the zero-cross event to occur either too early or too late. When the waveform is varying relative to Vss, then the zero cross is detected too early as the waveform falls and too late as the waveform rises. When the waveform is varying relative to Vdd, then the zero cross is detected too late as the waveform rises and too early as the waveform falls. The actual offset time can be determined for sinusoidal waveforms with the corresponding equations shown in Equation 29-2.

**EQUATION 29-2: ZCD EVENT OFFSET**

When External Voltage Source is relative to Vss:

\[
T_{\text{OFFSET}} = \frac{\arcsin\left(\frac{\text{VCPINV}}{\text{VPEAK}}\right)}{2\pi \cdot \text{Freq}}
\]

When External Voltage Source is relative to Vdd:

\[
T_{\text{OFFSET}} = \frac{\arcsin\left(\frac{\text{VDD} - \text{VCPINV}}{\text{VPEAK}}\right)}{2\pi \cdot \text{Freq}}
\]

This offset time can be compensated for by adding a pull-up or pull-down biasing resistor to the ZCD pin. A pull-up resistor is used when the external voltage source is varying relative to Vss. A pull-down resistor is used when the voltage is varying relative to Vdd. The resistor adds a bias to the ZCD pin so that the target external voltage source must go to zero to pull the pin voltage to the VCPINV switching voltage. The pull-up or pull-down value can be determined with the equations shown in Equation 29-3 or Equation 29-4.

**EQUATION 29-3: ZCD PULL-UP/DOWN**

When External Signal is relative to Vss:

\[
R_{\text{PULLUP}} = \frac{R_{\text{SERIES}}(\text{VPULLUP} - \text{VCPINV})}{\text{VCPINV}}
\]

When External Signal is relative to Vdd:

\[
R_{\text{PULLDOWN}} = \frac{R_{\text{SERIES}}(\text{VCPINV})}{(\text{VDD} - \text{VCPINV})}
\]
Measuring VCPINV can be difficult, especially when the waveform is relative to VDD. However, by combining Equations 29-2 and 29-3, the resistor value can be determined from the time difference between the ZCD output high and low intervals. Note that the time difference, $\Delta T$, is $4 \times \text{OFFSET}$. The equation for determining the pull-up and pull-down resistor values from the high and low ZCD_output periods is shown in Equation 29-4.

**EQUATION 29-4: PULL-UP/DOWN RESISTOR VALUES**

$$R = \frac{V_{BIAS}}{V_{PEAK} \sin \left( \pi \text{Freq} \left( \frac{\Delta T}{2} \right) \right)} R_{\text{series}} - 1$$

$R$ is pull-up or pull-down resistor.

$V_{BIAS}$ is $V_{\text{PULLUP}}$ when $R$ is pull-up or VDD when $R$ is pull-down.

$\Delta T$ is the ZCDOUT high and low period difference.

### 29.6 Handling $V_{\text{PEAK}}$ Variations

If the peak amplitude of the external voltage is expected to vary, the series resistor must be selected to keep the ZCD current source and sink below the design maximum range of $\pm 600 \mu A$ and above a reasonable minimum range. A general rule of thumb is that the maximum peak voltage can be no more than six times the minimum peak voltage. To ensure that the maximum current does not exceed $\pm 600 \mu A$ and the minimum is at least $\pm 100 \mu A$, compute the series resistance as shown in Equation 29-5. The compensating pull-up for this series resistance can be determined with Equation 29-3 because the pull-up value is not dependent to the peak voltage.

**EQUATION 29-5: SERIES $R$ FOR $V$ RANGE**

$$R_{\text{series}} = \frac{V_{\text{MAXPEAK}} + V_{\text{MINPEAK}}}{7 \times 10^{-4}}$$

### 29.7 Operation During Sleep

The ZCD current sources and interrupts are unaffected by Sleep.

### 29.8 Effects of a Reset

The ZCD circuit can be configured to default to the active or inactive state on Power-on-Reset (POR). When the ZCD Configuration bit is cleared, the ZCD circuit will be active at POR. When the ZCD Configuration bit is set, the SEN bit of the ZCDCON register must be set to enable the ZCD module.

### 29.9 Disabling the ZCD Module

The ZCD module can be disabled in two ways:

1. Configuration Word 2H has the ZCD bit which disables the ZCD module when set, but it can be enabled using the SEN bit of the ZCDCON register (Register 29-1). If the ZCD bit is clear, the ZCD is always enabled.

2. The ZCD can also be disabled using the ZCDMD bit of the respective PMD2 register (Register 19-3). This is subject to the status of the ZCD bit.
29.10 Register Definitions: ZCD Control

REGISTER 29-1: ZCDCON: ZERO-CROSS DETECT CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R-x</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEN</td>
<td></td>
<td>OUT</td>
<td>POL</td>
<td></td>
<td></td>
<td>INTN</td>
<td>INTN</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 7  **SEN**: Zero-Cross Detect Software Enable bit
This bit is ignored when ZCDSEN Configuration bit is set.

- 1: Zero-cross detect is enabled.
- 0: Zero-cross detect is disabled. ZCD pin operates according to PPS and TRIS controls.

bit 6  **Unimplemented**: Read as ‘0’

bit 5  **OUT**: Zero-Cross Detect Data Output bit

- **ZCDPOL** bit = 0:
  - 1: ZCD pin is sinking current
  - 0: ZCD pin is sourcing current

- **ZCDPOL** bit = 1:
  - 1: ZCD pin is sourcing current
  - 0: ZCD pin is sinking current

bit 4  **POL**: Zero-Cross Detect Polarity bit

- 1: ZCD logic output is inverted
- 0: ZCD logic output is not inverted

bit 3-2  **Unimplemented**: Read as ‘0’

bit 1  **INTP**: Zero-Cross Detect Positive-Going Edge Interrupt Enable bit

- 1: ZCDIF bit is set on low-to-high ZCD_output transition
- 0: ZCDIF bit is unaffected by low-to-high ZCD_output transition

bit 0  **INTN**: Zero-Cross Detect Negative-Going Edge Interrupt Enable bit

- 1: ZCDIF bit is set on high-to-low ZCD_output transition
- 0: ZCDIF bit is unaffected by high-to-low ZCD_output transition

TABLE 29-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE ZCD MODULE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZCDCON</td>
<td>SEN</td>
<td>―</td>
<td>OUT</td>
<td>POL</td>
<td>―</td>
<td>―</td>
<td>―</td>
<td>―</td>
<td>448</td>
</tr>
</tbody>
</table>

Legend:  — = unimplemented, read as ‘0’. Shaded cells are unused by the ZCD module.
30.0 DATA SIGNAL MODULATOR (DSM) MODULE

The Data Signal Modulator (DSM) is a peripheral which allows the user to mix a data stream, also known as a modulator signal, with a carrier signal to produce a modulated output.

Both the carrier and the modulator signals are supplied to the DSM module either internally, from the output of a peripheral, or externally through an input pin.

The modulated output signal is generated by performing a logical "AND" operation of both the carrier and modulator signals and then provided to the MDOUT pin.

The carrier signal is comprised of two distinct and separate signals. A carrier high (CARH) signal and a carrier low (CARL) signal. During the time in which the modulator (MOD) signal is in a logic high state, the DSM mixes the carrier high signal with the modulator signal. When the modulator signal is in a logic low state, the DSM mixes the carrier low signal with the modulator signal.

Using this method, the DSM can generate the following types of Key Modulation schemes:

- Frequency-Shift Keying (FSK)
- Phase-Shift Keying (PSK)
- On-Off Keying (OOK)

Additionally, the following features are provided within the DSM module:

- Carrier Synchronization
- Carrier Source Polarity Select
- Programmable Modulator Data
- Modulated Output Polarity Select
- Peripheral Module Disable, which provides the ability to place the DSM module in the lowest power consumption mode

Figure 30-1 shows a Simplified Block Diagram of the Data Signal Modulator peripheral.
FIGURE 30-1: SIMPLIFIED BLOCK DIAGRAM OF THE DATA SIGNAL MODULATOR

Data Signal Modulator

CH<3:0>

See MD1CARH Register

0000

CL<4:0>

See MD1CARL Register

0000

CH<3:0>

See MD1SRC Register

00000

CH<3:0>

MS<4:0>

See MD1SRC Register

00000

CL<4:0>

0000

CarH

CHPOL

1 0

SYNC

ChSYNC

1 0

RxyPPS

OPOL

CarL

CLPOL

1 0

MOD

PPS
30.1 DSM Operation

The DSM module can be enabled by setting the EN bit in the MD1CON0 register. Clearing the EN bit in the MD1CON0 register, disables the DSM module output and switches the carrier high and carrier low signals to the default option of MD1CARHPPS and MD1CARLPPS, respectively. The modulator signal source is also switched to the BIT in the MD1CON0 register.

The values used to select the carrier high, carrier low, and modulator sources held by the Modulation Source, Modulation High Carrier, and Modulation Low Carrier control registers are not affected when the EN bit is cleared and the DSM module is disabled. The values inside these registers remain unchanged while the DSM is inactive. The sources for the carrier high, carrier low and modulator signals will once again be selected when the EN bit is set and the DSM module is again enabled and active.

30.2 Modulator Signal Sources

The modulator signal can be supplied from the sources specified in Table 30-3.

The modulator signal is selected by configuring the MS<4:0> bits in the MD1SRC register.

30.3 Carrier Signal Sources

The carrier high signal and carrier low signal can be supplied from the sources specified in Table 30-1.

The carrier high signal is selected by configuring the CH<4:0> bits in the MD1CARH register. The carrier low signal is selected by configuring the CL<4:0> bits in the MD1CARL register.

30.4 Carrier Synchronization

During the time when the DSM switches between carrier high and carrier low signal sources, the carrier data in the modulated output signal can become truncated. To prevent this, the carrier signal can be synchronized to the modulator signal. When synchronization is enabled, the carrier pulse that is being mixed at the time of the transition is allowed to transition low before the DSM switches over to the next carrier source.

Synchronization is enabled separately for the carrier high and carrier low signal sources. Synchronization for the carrier high signal is enabled by setting the CHSYNC bit in the MD1CON1 register. Synchronization for the carrier low signal is enabled by setting the CLSYNC bit in the MD1CON1 register.

Figure 30-2 through Figure 30-6 show timing diagrams of using various synchronization methods.
FIGURE 30-2: On Off Keying (OOK) Synchronization

![Diagram showing On Off Keying (OOK) Synchronization]

FIGURE 30-3: No Synchronization (CHSYNC = 0, CLSYNC = 0)

![Diagram showing No Synchronization]

FIGURE 30-4: Carrier High Synchronization (CHSYNC = 1, CLSYNC = 0)

![Diagram showing Carrier High Synchronization]
FIGURE 30-5: Carrier Low Synchronization (CHSYNC = 0, CLSYNC = 1)

<table>
<thead>
<tr>
<th>carrier_high</th>
<th>carrier_low</th>
<th>modulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDCHSYNC = 0</td>
<td>MDCLSYNC = 1</td>
<td></td>
</tr>
</tbody>
</table>

Active Carrier State: carrier_high carrier_low carrier_high carrier_low

FIGURE 30-6: Full Synchronization (CHSYNC = 1, CLSYNC = 1)

<table>
<thead>
<tr>
<th>carrier_high</th>
<th>carrier_low</th>
<th>modulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDCHSYNC = 1</td>
<td>MDCLSYNC = 1</td>
<td></td>
</tr>
</tbody>
</table>

Active Carrier State: carrier_high carrier_low carrier_high carrier_low

Falling edges used to sync
30.5 Carrier Source Polarity Select
The signal provided from any selected input source for the carrier high and carrier low signals can be inverted. Inverting the signal for the carrier high source is enabled by setting the CHPOL bit of the MD1CON1 register. Inverting the signal for the carrier low source is enabled by setting the CLPOL bit of the MD1CON1 register.

30.6 Programmable Modulator Data
The BIT of the MD1CON0 register can be selected as the source for the modulator signal. This gives the user the ability to program the value used for modulation.

30.7 Modulated Output Polarity
The modulated output signal provided on the DSM pin can also be inverted. Inverting the modulated output signal is enabled by setting the OPOL bit of the MD1CON0 register.

30.8 Operation in Sleep Mode
The DSM module is not affected by Sleep mode. The DSM can still operate during Sleep, if the Carrier and Modulator input sources are also still operable during Sleep. Refer to Section 10.0 “Power-Saving Operation Modes” for more details.

30.9 Effects of a Reset
Upon any device Reset, the DSM module is disabled. The user’s firmware is responsible for initializing the module before enabling the output. The registers are reset to their default values.

30.10 Peripheral Module Disable
The DSM module can be completely disabled using the PMD module to achieve maximum power saving. The DSMMD bit of PMD6 (Register 19-7) when set disables the DSM module completely. When enabled again all the registers of the DSM module default to POR status.
30.11 Register Definitions: Modulation Control

Long bit name prefixes for the Modulation peripheral is shown below. Refer to Section 1.3.2.2 "Long Bit Names" for more information.

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Bit Name Prefix</th>
</tr>
</thead>
<tbody>
<tr>
<td>MD1</td>
<td>MD1</td>
</tr>
</tbody>
</table>

REGISTER 30-1: MD1CON0: MODULATION CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>—</td>
<td>OUT</td>
<td>OPOL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>BIT</td>
</tr>
</tbody>
</table>

Legend:

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

bit 7  **EN:** Modulator Module Enable bit

1 = Modulator module is enabled and mixing input signals
0 = Modulator module is disabled and has no output

bit 6  **Unimplemented:** Read as '0'

bit 5  **OUT:** Modulator Output bit

Displays the current output value of the Modulator module.(1)

bit 4  **OPOL:** Modulator Output Polarity Select bit

1 = Modulator output signal is inverted; idle high output
0 = Modulator output signal is not inverted; idle low output

bit 3-1 **Unimplemented:** Read as '0'

bit 0  **BIT:** Allows software to manually set modulation source input to module(2)

1 = Modulator selects Carrier High
0 = Modulator selects Carrier Low

**Note 1:** The modulated output frequency can be greater and asynchronous from the clock that updates this register bit, the bit value may not be valid for higher speed modulator or carrier signals.

**2:** BIT bit must be selected as the modulation source in the MD1SRC register for this operation.
**REGISTER 30-2: MD1CON1: MODULATION CONTROL REGISTER 1**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>CHPOL</td>
<td>CHSYNC</td>
<td>—</td>
<td>—</td>
<td>CLPOL</td>
<td>CLSYNC</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

<table>
<thead>
<tr>
<th>bit 7-6</th>
<th><strong>Unimplemented</strong>: Read as '0'</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 5</td>
<td><strong>CHPOL</strong>: Modulator High Carrier Polarity Select bit</td>
</tr>
<tr>
<td></td>
<td>1 = Selected high carrier signal is inverted</td>
</tr>
<tr>
<td></td>
<td>0 = Selected high carrier signal is not inverted</td>
</tr>
<tr>
<td>bit 4</td>
<td><strong>CHSYNC</strong>: Modulator High Carrier Synchronization Enable bit</td>
</tr>
<tr>
<td></td>
<td>1 = Modulator waits for a falling edge on the high time carrier signal before allowing a switch to the low time carrier</td>
</tr>
<tr>
<td></td>
<td>0 = Modulator output is not synchronized to the high time carrier signal(1)</td>
</tr>
<tr>
<td>bit 3-2</td>
<td><strong>Unimplemented</strong>: Read as '0'</td>
</tr>
<tr>
<td>bit 1</td>
<td><strong>CLPOL</strong>: Modulator Low Carrier Polarity Select bit</td>
</tr>
<tr>
<td></td>
<td>1 = Selected low carrier signal is inverted</td>
</tr>
<tr>
<td></td>
<td>0 = Selected low carrier signal is not inverted</td>
</tr>
<tr>
<td>bit 0</td>
<td><strong>CLSYNC</strong>: Modulator Low Carrier Synchronization Enable bit</td>
</tr>
<tr>
<td></td>
<td>1 = Modulator waits for a falling edge on the low time carrier signal before allowing a switch to the high time carrier</td>
</tr>
<tr>
<td></td>
<td>0 = Modulator output is not synchronized to the low time carrier signal(1)</td>
</tr>
</tbody>
</table>

**Note 1**: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.
REGISTER 30-3: MD1CARH: MODULATION HIGH CARRIER CONTROL REGISTER

<table>
<thead>
<tr>
<th>bit</th>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>CH&lt;4:0&gt;=(1)</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set  '0' = Bit is cleared

bit 7-5  Unimplemented: Read as '0'
bit 4-0  CH<4:0>: Modulator Carrier High Selection bits(1)
See Table 30-1 for signal list

Note 1: Unused selections provide an input value.

REGISTER 30-4: MD1CARL: MODULATION LOW CARRIER CONTROL REGISTER

<table>
<thead>
<tr>
<th>bit</th>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>CL&lt;4:0&gt;=(1)</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set  '0' = Bit is cleared

bit 7-5  Unimplemented: Read as '0'
bit 4-0  CL<4:0>: Modulator Carrier Low Input Selection bits(1)
See Table 30-1 for signal list

Note 1: Unused selections provide a zero as the input value.
### TABLE 30-1: MD1CARH/MD1CARL SELECTION MUX CONNECTIONS

<table>
<thead>
<tr>
<th>MD1CARH</th>
<th>MD1CARL</th>
</tr>
</thead>
<tbody>
<tr>
<td>CH&lt;4:0&gt;</td>
<td>Connection</td>
</tr>
<tr>
<td>11111-10011</td>
<td>31-19 Reserved</td>
</tr>
<tr>
<td>10010</td>
<td>18</td>
</tr>
<tr>
<td>10001</td>
<td>17</td>
</tr>
<tr>
<td>10000</td>
<td>16</td>
</tr>
<tr>
<td>01111</td>
<td>15</td>
</tr>
<tr>
<td>01110</td>
<td>14</td>
</tr>
<tr>
<td>01101-01100</td>
<td>13-12 Reserved</td>
</tr>
<tr>
<td>01011</td>
<td>11</td>
</tr>
<tr>
<td>01010</td>
<td>10</td>
</tr>
<tr>
<td>01001</td>
<td>9</td>
</tr>
<tr>
<td>01000</td>
<td>8</td>
</tr>
<tr>
<td>00111</td>
<td>7</td>
</tr>
<tr>
<td>00110</td>
<td>6</td>
</tr>
<tr>
<td>00101</td>
<td>5</td>
</tr>
<tr>
<td>00100</td>
<td>4</td>
</tr>
<tr>
<td>00011</td>
<td>3</td>
</tr>
<tr>
<td>00010</td>
<td>2</td>
</tr>
<tr>
<td>00001</td>
<td>1</td>
</tr>
<tr>
<td>00000</td>
<td>0</td>
</tr>
</tbody>
</table>

### REGISTER 30-5: MD1SRC: MODULATION SOURCE CONTROL REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

#### bit 7-5
- **Unimplemented**: Read as ‘0’

#### bit 4-0
- **MS<4:0>**: Modulator Source Selection bits (1)
  - See Table 30-2 for signal list

**Note 1**: Unused selections provide a zero as the input value.
### TABLE 30-2: MD1SRC SELECTION MUX CONNECTIONS

<table>
<thead>
<tr>
<th>MS&lt;4:0&gt;</th>
<th>Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1111</td>
<td>31 Reserved</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1 1000</td>
<td>24</td>
</tr>
<tr>
<td>1 0111</td>
<td>23 CAN_tx0</td>
</tr>
<tr>
<td>1 0110</td>
<td>22 SPI1 SDO</td>
</tr>
<tr>
<td>1 0101</td>
<td>21 Reserved</td>
</tr>
<tr>
<td>1 0100</td>
<td>20 UART2 TX</td>
</tr>
<tr>
<td>1 0011</td>
<td>19 UART1 TX</td>
</tr>
<tr>
<td>1 0010</td>
<td>18 CLC4 OUT</td>
</tr>
<tr>
<td>1 0001</td>
<td>17 CLC3 OUT</td>
</tr>
<tr>
<td>1 0000</td>
<td>16 CLC2 OUT</td>
</tr>
<tr>
<td>0 1111</td>
<td>15 CLC1 OUT</td>
</tr>
<tr>
<td>0 1110</td>
<td>14 CMP2 OUT</td>
</tr>
<tr>
<td>0 1101</td>
<td>13 CMP1 OUT</td>
</tr>
<tr>
<td>0 1100</td>
<td>12 NCO1 OUT</td>
</tr>
<tr>
<td>0 1011</td>
<td>11 Reserved</td>
</tr>
<tr>
<td>0 1010</td>
<td>10 Reserved</td>
</tr>
<tr>
<td>0 1001</td>
<td>9 PWM8 OUT</td>
</tr>
<tr>
<td>0 1000</td>
<td>8 PWM7 OUT</td>
</tr>
<tr>
<td>0 0111</td>
<td>7 PWM6 OUT</td>
</tr>
<tr>
<td>0 0110</td>
<td>6 PWM5 OUT</td>
</tr>
<tr>
<td>0 0101</td>
<td>5 CCP4 OUT</td>
</tr>
<tr>
<td>0 0100</td>
<td>4 CCP3 OUT</td>
</tr>
<tr>
<td>0 0011</td>
<td>3 CCP2 OUT</td>
</tr>
<tr>
<td>0 0010</td>
<td>2 CCP1 OUT</td>
</tr>
<tr>
<td>0 0001</td>
<td>1 DSM1 BIT</td>
</tr>
<tr>
<td>0 0000</td>
<td>0 Pin selected by MDSRCPPS</td>
</tr>
</tbody>
</table>

### TABLE 30-3: SUMMARY OF REGISTERS ASSOCIATED WITH DATA SIGNAL MODULATOR MODE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>MD1CON0</td>
<td>EN</td>
<td>—</td>
<td>OUT</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>BIT 455</td>
</tr>
<tr>
<td>MD1CON1</td>
<td>—</td>
<td>—</td>
<td>CHPOL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CLPOL</td>
<td>456</td>
</tr>
<tr>
<td>MD1CARH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CHS&lt;2:0&gt;</td>
<td>457</td>
</tr>
<tr>
<td>MD1CARL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CLS&lt;2:0&gt;</td>
<td>457</td>
</tr>
<tr>
<td>MDSRC</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SRCS&lt;3:0&gt;</td>
<td>458</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented, read as ‘0’. Shaded cells are not used in the Data Signal Modulator mode.
31.0 **UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART) WITH PROTOCOL SUPPORT**

The Universal Asynchronous Receiver Transmitter (UART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer, independent of device program execution. The UART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or one of several automated protocols. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers.

Supported protocols include:
- LIN Master and Slave
- DMX mode
- DALI control gear and control device

The UART module includes the following capabilities:
- Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- Programmable 7-bit or 8-bit character length
- 9th bit Address detection
- 9th bit even or odd parity
- Input buffer overrun error detection
- Received character framing error detection
- Hardware and software flow control
- Automatic checksums
- Programmable 1, 1.5, and 2 Stop bits
- Programmable data polarity
- Manchester encoder/decoder
- Operation in Sleep
- Automatic detection and calibration of the baud rate
- Wake-up on Break reception
- Automatic and user timed Break period generation
- RX and TX inactivity timeouts (with Timer2)

Block diagrams of the UART transmitter and receiver are shown in **Figure 31-1** and **Figure 31-2**.

The UART transmit output (TX_out) is available to the TX pin and internally to various peripherals.
The operation of the UART module is controlled through nineteen registers:

- Three control registers (UxCON0-UxCON2)
- Error enable and status (UxERRIE, UxERRIR, UxUIR)
- UART buffer status and control (UxFIFO)
- Three 9-bit protocol parameters (UxP1-UxP3)
- 16-bit baud rate generator (UxBRGH:L)
- Transmit buffer write (UxTXB)
- Receive buffer read (UxRXB)
- Receive checksum (UxRXCHK)
- Transmit checksum (UxTXCHK)

These registers are detailed in Section 31.21 “Register Definitions: UART Control”.

### 31.1 UART I/O Pin Configuration

The RX input pin is selected with the UxRPPS register. The TX output pin is selected with each pin’s RxyPPS register. When the TRIS control for the pin corresponding to the TX output is cleared, then the UART will maintain control and the logic level on the TX pin. Changing the TXPOL bit in UxCON2 will immediately change the TX pin logic level regardless of the value of EN or TXEN.

### 31.2 UART Asynchronous Modes

The UART has five asynchronous modes:

- 7-bit
- 8-bit
- 8-bit with even parity in the 9th bit
- 8-bit with odd parity in the 9th bit
- 8-bit with address indicator in the 9th bit

The UART transmits and receives data using the standard Non-Return-to-Zero (NRZ) format. NRZ represents a ‘1’ data bit, and a Vol. Space state, which represents a ‘0’ data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the Mark state. Each character transmission consists of one Start bit followed by seven or eight data bits, one optional parity or address bit, and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is eight bits with no parity. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 16-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. See Section 31.17 “UART Baud Rate Generator (BRG)” for more information.

In all the Asynchronous modes, the UART transmits and receives the LSBs first. The UART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is supported by the hardware by even and odd parity modes.

### 31.2.1 UART ASYNCHRONOUS TRANSMITTER

The UART transmitter block diagram is shown in Figure 31-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the UxTXB register.
31.2.1.1 Enabling the Transmitter

The UART transmitter is enabled for asynchronous operations by configuring the following control bits:

- TXEN = 1
- MODE<3:0> = 0h through 3h
- UxBRGH:L = desired baud rate
- UxBRGS = desired baud rate multiplier
- RxyPPS = code for desired output pin
- ON = 1

All other UART control bits are assumed to be in their default state.

Setting the TXEN bit in the UxCON0 register enables the transmitter circuitry of the UART. The MODE<3:0> bits in the UxCON0 register select the desired mode. Setting the ON bit in the UxCON1 register enables the UART. When TXEN is set and the transmitter is not idle, the TX pin is automatically configured as an output. When the transmitter is idle, the TX pin drive is relinquished to the port TRIS control. If the TX pin is shared with an analog peripheral, the analog I/O function should be disabled by clearing the corresponding ANSEL bit.

31.2.1.2 Transmitting Data

A transmission is initiated by writing a character to the UxTXB register. If this is the first character, or the previous character has been completely transmitted from the TSR, the data in the UxTXB is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the UxTXB until the previous character transmission is complete. The pending character in the UxTXB is then transferred to the TSR at the beginning of the previous character Stop bit transmission. The transmission of the Start bit, data bits and Stop bit sequence commences immediately following the completion of all of the previous character’s Stop bits.

31.2.1.3 Transmit Data Polarity

The polarity of the transmit data is controlled with the TXPOL bit in the UxCON2 register. The default state of this bit is ‘0’ which selects high true transmit idle and data bits. Setting the TXPOL bit to ‘1’ will invert the transmit data, resulting in low true idle and data bits. The TXPOL bit controls transmit data polarity in all modes.

31.2.1.4 Transmit Interrupt Flag

The UxTXIF interrupt flag bit in the PIR register is set whenever the UART transmitter is enabled and no character is being held for transmission in the UxTXB. In other words, the UxTXIF bit is clear only when the TSR is busy with a character and a new character has been queued for transmission in the UxTXB.

The UxTXIF interrupt can be enabled by setting the UxTXIE interrupt enable bit in the PIE register. However, the UxTXIF flag bit will be set whenever the UxTXB is empty, regardless of the state of UxTXIE enable bit. The UxTXIF bit is read-only and cannot be set or cleared by software.

To use interrupts when transmitting data, set the UxTXIE bit only when there is more data to send. Clear the UxTXIE interrupt enable bit upon writing UxTXB with the last character of the transmission.

31.2.1.5 TSR Status

The TXMTIF bit in the UxERRIR register indicates the status of the TSR. This is a read-only bit. The TXMTIF bit is set when the TSR is empty and idle. The TXMTIF bit is cleared when a character is transferred to the TSR from the UxTXB. The TXMTIF bit remains clear until all bits, including the Stop bits, have been shifted out of the TSR and a byte is not waiting in the UxTXB register.

The TXMTIF will generate an interrupt when the TXMTIE bit in the UxERRIE register is set.

31.2.1.6 Transmitter 7-bit Mode

7-Bit mode is selected when the MODE<3:0> bits are set to ‘0001’. In 7-bit mode, only the seven Least Significant bits of the data written to UxTXB are transmitted. The Most Significant bit is ignored.

31.2.1.7 Transmitter Parity Modes

When the Odd or even Parity mode is selected, all data is sent as nine bits. The first eight bits are data and the 9th bit is parity. Even and odd parity is selected when the MODE<3:0> bits are set to ‘0011’ and ‘0010’, respectively. Parity is automatically determined by the module and inserted in the serial data stream.
31.2.1.8 Asynchronous Transmission Setup

1. Initialize the UxBRGH, UxBRGL register pair and the BRGS bit to achieve the desired baud rate (see Section 31.17 “UART Baud Rate Generator (BRG)”).
2. Set the MODE<3:0> bits to the desired asynchronous mode.
3. Set TXPOL bit if inverted TX output is desired.
4. Enable the asynchronous serial port by setting the ON bit.
5. Enable the transmitter by setting the TXEN control bit. This will cause the UxTXIF interrupt flag to be set.
6. If the device has PPS, configure the desired I/O pin RxyPPS register with the code for TX output.
7. If interrupts are desired, set the UxTXIE interrupt enable bit in the respective PIE register. An interrupt will occur immediately provided that the GIE bits in the INTCON0 register are also set.
8. Write one byte of data into the UxTXB register. This will start the transmission.
9. Subsequent bytes may be written when the UxTXIF bit is ‘1’.

FIGURE 31-3: ASYNCHRONOUS TRANSMISSION

FIGURE 31-4: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)

Note: This timing diagram shows the first transmission and the start of the second consecutive transmission.
31.2.2 UART ASYNCHRONOUS RECEIVER

The Asynchronous mode is typically used in RS-232 systems. The receiver block diagram is shown in Figure 31-2. The data is received on the RX pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at 4 or 16 times the baud rate, whereas the serial Receive Shift Register (RSR) operates at the bit rate. When all bits of the character have been shifted in, they are immediately transferred to a two character First-In-First-Out (FIFO) memory. The FIFO buffering allows reception of two complete characters and the start of a third character before software must start servicing the UART receiver. The FIFO registers and RSR are not directly accessible by software. Access to the received data is via the UxRXB register.

31.2.2.1 Enabling the Receiver

The UART receiver is enabled for asynchronous operation by configuring the following control bits:

- RXEN = 1
- MODE<3:0> = 0h through 3h
- UxBRGH:L = desired baud rate
- RXPPS = code for desired input pin
- Input pin ANSEL bit = 0
- ON = 1

All other UART control bits are assumed to be in their default state.

Setting the RXEN bit in the UxCON0 register enables the receiver circuitry of the UART. Setting the MODE<3:0> bits in the UxCON0 register configures the UART for the desired Asynchronous mode. Setting the ON bit in the UxCON1 register enables the UART. The TRIS bit corresponding to the selected RX I/O pin must be set to configure the pin as an input.

Note: If the RX function is on an analog pin, the corresponding ANSEL bit must be cleared for the receiver to function.

31.2.2.2 Receiving Data

Data is recovered from the bit stream by timing to the center of the bits and sampling the input level. In High-Speed mode, there are four BRG clocks per bit and only one sample is taken per bit. In Normal-Speed mode, there are 16 BRG clocks per bit and three samples are taken per bit.

The receiver data recovery circuit initiates character reception on the falling edge of the Start bit. The Start bit, is always a '0'. The Start bit is qualified in the middle of the bit. In Normal-Speed mode only, the Start bit is also qualified at the leading edge of the bit. The following paragraphs describe the majority detect sampling of Normal-Speed mode.

The falling edge starts the baud rate generator (BRG) clock. The input is sampled at the first and second BRG clocks.

If both samples are high then the falling edge is deemed a glitch and the UART returns to the Start bit detection state without generating an error.

If either sample is low, the data recovery circuit continues counting BRG clocks and takes samples at clock counts 7, 8, and 9. When less than two samples are low, the Start bit is deemed invalid and the data recovery circuit aborts character reception, without generating an error, and resumes looking for the falling edge of the Start bit.

When two or more samples are low, the Start bit is deemed valid and the data recovery continues. After a valid Start bit is detected, the BRG clock counter continues and resets at count 16. This is the beginning of the first data bit.

The data recovery circuit counts BRG clocks from the beginning of the bit and takes samples at clocks 7, 8, and 9. The bit value is determined from the majority of the samples. The resulting '0' or '1' is shifted into the RSR. The BRG clock counter continues and resets at count 16. This sequence repeats until all data bits have been sampled and shifted into the RSR.

After all data bits have been shifted in, the first Stop bit is sampled. Stop bits are always a '1'. If the bit sampling determines that a '0' is in the Stop bit position, the framing error is set for this character. Otherwise, the framing error is cleared for this character. See Section 31.2.2.4 “Receive Framing Error” for more information on framing errors.

31.2.2.3 Receive Interrupts

Immediately after all data bits and the Stop bit have been received, the character in the RSR is transferred to the UART receive FIFO. The UxRXIF interrupt flag in the respective PIR register is set at this time, provided it is not being suppressed.

The UxRXIF is suppressed by any of the following:

- FERIF if FERIE is set
- PERIF if PERIE is set

This suspends DMA transfer of data until software processes the error and reads UxRXB to advance the FIFO beyond the error.

UxRXIF interrupts are enabled by setting all of the following bits:

- UxRXIE, Interrupt Enable bit in the PIE register
- GIE, Global Interrupt Enable bits in the INTCON0 register

The UxRXIF interrupt flag bit will be set when not suppressed and there is an unread character in the FIFO, regardless of the state of interrupt enable bits. Reading the UxRXB register will transfer the top character out of the FIFO and reduce the FIFO contents by one. The UxRXIF interrupt flag bit is read-only, it cannot be set or cleared by software.
31.2.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error flag bit. A framing error indicates that the Stop bit was not seen at the expected time. The framing error flag is accessed via the FERIF bit in the UxERRIR register. The FERIF bit represents the frame status of the top unread character of the receive FIFO. Therefore, the FERIF bit must be read before reading UxRXB.

The FERIF bit is read-only and only applies to the top unread character of the receive FIFO. A framing error (FERIF = 1) does not preclude reception of additional characters. It is neither necessary nor possible to clear the FERIF bit directly. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERIF bit is cleared when the character at the top of the FIFO does not have a framing error or when all bytes in the receive FIFO have been read. Clearing the ON bit resets the receive FIFO, thereby also clearing the FERIF bit.

A framing error will generate a summary UxERR interrupt when the FERIE bit in the UxERRIE register is set. The summary error is reset when the FERIF bit of the top of the FIFO is '0' or when all FIFO characters have been retrieved.

When FERIE is set, UxRXIF interrupts are suppressed when FERIF is '1'.

31.2.2.5 Receiver Parity Modes

Even and odd parity is automatically detected when the MODE<3:0> bits are set to '0011' and '0010', respectively. Parity modes receive eight data bits and one parity bit for a total of nine bits for each character. The PERIF bit in the UxERRIR register represents the parity error of the top unread character of the receive FIFO rather than the parity bit itself. The parity error must be read before reading the UxRXB register advances the FIFO.

A parity error will generate a summary UxERR interrupt when the PERIE bit in the UxERRIE register is set. The summary error is reset when the PERIF bit of the top of the FIFO is '0' or when all FIFO characters have been retrieved.

When PERIE is set, UxRXIF interrupts are suppressed when PERIF is '1'.

31.2.2.6 Receive FIFO Overflow

When more characters are received than the receive FIFO can hold, the RXFOIF bit in the UxERRIR register is set. The character causing the overflow condition is discarded. The RUNOVF bit in the UxCON2 register determines how the receive circuit responds to characters while the overflow condition persists. When RUNOVF is set, the receive shifter stays synchronized to the incoming data stream by responding to Start, data, and Stop bits. However, all received bytes not already in the FIFO are discarded. When RUNOVF is cleared, the receive shifter ceases operation and Start, data, and Stop bits are ignored. The receive overflow condition is cleared by reading the UxRXB register and clearing the RXFOIF bit. If the UxRXB register is not read to open a space in the FIFO, the next character received will be discarded and cause another overflow condition.

A receive overflow error will generate a summary UxEIF interrupt when the RXFOIE bit in the UxERRIE register is set.

31.2.2.7 Asynchronous Reception Setup

1. Initialize the UxBRGH, UxBRGL register pair and the BRGS bit to achieve the desired baud rate (see Section 31.17 “UART Baud Rate Generator (BRG)”).
2. Configure the RXPPS register for the desired RX pin
3. Clear the ANSEL bit for the RX pin (if applicable).
4. Set the MODE<3:0> bits to the desired Asynchronous mode.
5. Set the RXPOL bit if the data stream is inverted.
6. Enable the serial port by setting the ON bit.
7. If interrupts are desired, set the UxRXIE bit in the PIEX register and the GIE bits in the INTCON0 register.
8. Enable reception by setting the RXEN bit.
9. The UxRXIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the UxRXIE interrupt enable bit is also set.
10. Read the UxERRIR register to get the error flags.
11. Read the UxRXB register to get the received byte.
12. If an overrun occurred, clear the RXFOIF bit.
FIGURE 31-5: ASYNCHRONOUS RECEPTION

![Timing Diagram]

**Note:** This timing diagram shows three words appearing on the RX input. The UxRXB (receive buffer) is not read before the third word is received, causing the RXFOIF (FIFO overrun) bit to be set. STPMD = 0, STP<1:0> = 0,0.
31.3  Asynchronous Address Mode

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems.

When Asynchronous Address mode is enabled, all data is transmitted and received as 9-bit characters. The 9th bit determines whether the character is an address or data. When the 9th bit is set, the eight Least Significant bits are the address. When the 9th bit is clear, the Least Significant bits are data. In either case, the 9th bit is stored in PERIF when the byte is written to the receive FIFO. When PERIE is also set, the RXIF will be suppressed, thereby suspending DMA transfers allowing software to process the received address.

An address character will enable all receivers that match the address and disable all other receivers. Once a receiver is enabled, all non-address characters will be received until an address character is received that does not match.

31.3.1  ADDRESS MODE TRANSMIT

The UART transmitter is enabled for asynchronous address operation by configuring the following control bits:

- \( \text{TXEN} = 1 \)
- \( \text{MODE<3:0>} = 0100 \)
- \( \text{UxBRGH:L} = \text{desired baud rate} \)
- \( \text{RxyPPS} = \text{code for desired output pin} \)
- \( \text{ON} = 1 \)

Addresses are sent by writing to the \( \text{UxP1L} \) register. This transmits the written byte with the 9th bit set, which indicates that the byte is an address.

Data is sent by writing to the \( \text{UxTXB} \) register. This transmits the written byte with the 9th bit cleared, which indicates that the byte is data.

To send data to a particular device on the transmission bus, first transmit the address of the intended device. All subsequent data will be accepted only by that device until an address character is received that does not match.

Writes to \( \text{UxP1L} \) take precedence over writes to \( \text{UxTXB} \). When both the \( \text{UxP1L} \) and \( \text{UxTXB} \) registers are written while the TSR is busy, the next byte to be transmitted will be from \( \text{UxP1L} \).

To ensure that all data intended for one device is sent before the address is changed, wait until the TXMTIF bit is high before writing \( \text{UxP1L} \) with the new address.

31.3.2  ADDRESS MODE RECEIVE

The UART receiver is enabled for asynchronous address operation by configuring the following control bits:

- \( \text{RXEN} = 1 \)
- \( \text{MODE<3:0>} = 0100 \)
- \( \text{UxBRGH:L} = \text{desired baud rate} \)
- \( \text{RXPPS} = \text{code for desired input pin} \)
- \( \text{Input pin ANSEL bit} = 0 \)
- \( \text{UxP2L} = \text{receiver address} \)
- \( \text{UxP3L} = \text{address mask} \)
- \( \text{ON} = 1 \)

In Address mode, no data will be transferred to the input FIFO until a valid address is received. This is the default state. Any of the following conditions will cause the UART to revert to the default state:

- \( \text{ON} = 0 \)
- \( \text{RXEN} = 0 \)
- Received address does not match

When a character with the 9th bit set is received, the Least Significant eight bits of that character will be qualified by the values in the \( \text{UxP2L} \) and \( \text{UxP3L} \) registers.

The byte is XOR’d with \( \text{UxP2L} \) then AND’d with \( \text{UxP3L} \). A match occurs when the result is 0h, in which case, the unaltered received character is stored in the receive FIFO, thereby setting the \( \text{UxRXIF} \) interrupt bit. The 9th bit is stored in the corresponding PERIF bit, identifying this byte as an address.

An address match also enables the receiver for all data such that all subsequent characters without the 9th bit set will be stored in the receive FIFO.

When the 9th bit is set and a match does not occur, the character is not stored in the receive FIFO and all subsequent data is ignored.

The \( \text{UxP3L} \) register mask allows a range of addresses to be accepted. Software can then determine the sub-address of the range by processing the received address character.
### 31.4 DMX Mode

DMX is a protocol used in stage and show equipment. This includes lighting, fog machines, motors, etc. The protocol consists of a controller that sends out commands, and receiver such as theater lights that receive these commands. DMX protocol is usually unidirectional, but can be a bidirectional protocol in either Half or Full-Duplex modes. An example of Half-Duplex mode is the RDM (Remote Device Management) protocol that sits on DMX512A. The controller transmits commands and the receiver receives them. Also there are no error conditions or retransmit mechanisms.

DMX, or DMX512A as it is known, consists of a “Universe” of 512 channels. This means that one controller can output up to 512 bytes on a single DMX link. Each equipment on the line is programmed to listen to a consecutive sequence of one or more of these bytes.

For example, a fog machine connected to one of the universes may be programmed to receive one byte, starting at byte number 10, and a lighting unit may be programmed to receive four bytes starting at byte number 22.

#### 31.4.1 DMX Controller

DMX Controller mode is configured with the following settings:

- **MODE<3:0>** = 1010
- **TXEN** = 1
- **RXEN** = 0
- **RXPOL** = 1
- **UxP1** = One less than the number of bytes to transmit (excluding the Start code)
- **UxBRGH:L** = Value to achieve 250K baud rate
- **STP<1:0>** = 10 for 2 Stop bits
- **ON** = 1
- **UxRXPPS** = code for desired input pin
- **Input pin ANSEL bit** = 0

Each DMX transmission begins with a Break followed by a byte called the ‘Start Code’. The width of the BREAK is fixed at 25 bit times. The Break is followed by a “Mark After Break” (MAB) Idle period. After this Idle period, the 1st through ‘n’th byte is transmitted, where ‘n-1’ is the value in UxP1. See Figure 31-6.

Software sends the Start Code and the ‘n’ data bytes by writing the UxTXB register with each byte to be sent in the desired order. A UxTXIF value of ‘1’ indicates when the UxTXB is ready to accept the next byte.

The internal byte counter is not accessible to software. Software needs to keep track of the number of bytes written to UxTXB to ensure that no more and no less than ‘n’ bytes are sent because the DMX state machine will automatically insert a Break and reset its internal counter after ‘n’ bytes are written. One way to ensure synchronization between hardware and software is to toggle TXEN after the last byte of the universe is completely free of the transmit shift register as indicated by the TXMTIF bit.

#### 31.4.2 DMX Receiver

DMX Receiver mode is configured with the following settings:

- **MODE<3:0>** = 1010
- **TXEN** = 0
- **RXEN** = 1
- **RXPOL** = 1
- **UxP2** = number of first byte to receive
- **UxP3** = number of last byte to receive
- **UxBRGH:L** = Value to achieve 250K baud rate
- **STP<1:0>** = 10 for 2 Stop bits
- **ON** = 1
- **UxRXPPS** = code for desired input pin

When configured as DMX Receiver, the UART listens for a Break character that is at least 23 bit periods wide. If the Break is shorter than 23 bit times, the Break is ignored and the DMX state machine remains in Idle mode. Upon receiving the Break, the DMX counters will be reset to align with the incoming data stream. Immediately after the Break, the UART will see the “Mark after Break” (MAB). This space is ignored by the UART. The Start Code follows the MAB and will always be stored in the receive FIFO.

After the Start Code, the 1st through 512th byte will be received, but not all of them are stored in the receive FIFO. The UART ignores all received bytes until the ones of interest are received. This is done using the UxP2 and UxP3 registers. The UxP2 register holds the value of the byte number to start the receive process and the UxP3 register holds the value of the byte number to end the receive process. The byte counter starts at 0 for the first byte after the Start Code. For example, to receive four bytes starting at the 10th byte after the Start Code, write 009h (9 decimal) to UxP2H:L and 00Ch (12 decimal) to UxP3H:L. The receive FIFO is only 2 bytes deep, therefore the bytes must be retrieved by reading UxRXB as they come in to avoid a receive FIFO overrun condition.

Typically two Stop bits are inserted between bytes. If either Stop bit is detected as a ‘0’ then the framing error for that byte will be set.

Since the DMX sequence always starts with a Break, the software can verify that it is in sync with the sequence by monitoring the RXBKIF flag to ensure that the next byte received after the RXBKIF is processed as the Start Code and subsequent bytes are processed as the expected data.
31.5 LIN Modes

LIN is a protocol used primarily in automotive applications. The LIN network consists of two kinds of software processes: a Master process and a Slave process. Each network has only one Master process and one or more Slave processes.

From a physical layer point of view, the UART on one processor may be driven by both a Master and a Slave process, as long as only one Master process exists on the network.

A LIN transaction consists of a Master process followed by a Slave process. The Slave process may involve more than one slave where one is transmitting and the other(s) are receiving. The transaction begins by the following Master process transmission sequence:

1. Break
2.Delimiter bit
3. Sync Field
4. PID byte

The PID determines which Slave processes are expected to respond to the Master. When the PID byte is complete, the TX output remains in the Idle state. One or more of the Slave processes may respond to the Master process. If no one responds within the inter-byte period, the Master is free to start another transmission. The inter-byte period is timed by software using a means other than the UART.

The Slave process follows the Master process. When the slave software recognizes the PID then that Slave process responds by either transmitting the required response or by receiving the transmitted data. Only Slave processes send data. Therefore, Slave processes receiving data are receiving that of another Slave process.

When a slave sends data, the checksum is accumulated on each byte as it is received using the same algorithm as the sending process. The last byte, which is the inverted checksum value calculated by the sending process, is added to the locally calculated checksum by the UART. The check passes when the result is all '1's, otherwise the check fails and the CERIF bit is set.

Two methods for computing the checksum are available: legacy and enhanced. The legacy checksum includes only the data bytes. The enhanced checksum includes the PID and the data. The C0EN control bit in the UxCON2 register determines the checksum method. Setting C0EN to '1' selects the enhanced method. Software must select the appropriate method before the Start bit of the checksum byte is received.

31.5.1 LIN MASTER/SLAVE MODE

The LIN Master mode includes capabilities to generate Slave processes. The Master process stops at the PID transmission. Any data that is transmitted in Master/Slave mode is done as a Slave process. LIN Master/Slave mode is configured by the following settings:

- **MODE<3:0> = 1100**
- **TXEN = 1**
- **RXEN = 1**
- **UxBRGH:L = Value to achieve desired baud rate**
- **TXPOL = 0** (for high Idle state)
- **STP = desired Stop bits selection**
- **C0EN = desired checksum mode**
- **RxyPPS = TX pin selection code**
- **TX pin TRIS control = 0**
- **ON = 1**

**Note:** The TXEN bit must be set before the Master process is received and remain set while in LIN mode whether or not the Slave process is a transmitter.
The Master process is started by writing the PID to the UxP1L register when UxP2 is '0' and the UART is Idle. The UxTXIF will not be set in this case. Only the six Least Significant bits of UxP1L are used in the PID transmission.

The two Most Significant bits of the transmitted PID are PID parity bits. PID<6> is the exclusive-or of PID bits 0,1,2,and 4. PID<7> is the inverse of the exclusive-or of PID bits 1,3,4, and 5.

The UART calculates and inserts these bits in the serial stream.

Writing UxP1L automatically clears the UxTXCHK and UxRXCHK registers and generates the Break, delimiter bit, Sync character (55h), and PID transmission portion of the transaction. The data portion of the transaction that follows, if there is one, is a Slave process. See Section 31.5.2 “LIN Slave Mode” for more details of that process. The master receives its own PID when RXEN is set. Software performs the Slave process corresponding to the PID that was sent and received. Attempting to write UxP1L before an active master process is complete will not succeed. Instead, the TXWRE bit will be set.

31.5.2 LIN SLAVE MODE

LIN Slave mode is configured by the following settings:

- **MODE<3:0> = 1011**
- **TXEN = 1**
- **RXEN = 1**
- **UxP2 = Number of data bytes to transmit**
- **UxP3 = Number of data bytes to receive**
- **UxBRGH:L = Value to achieve default baud rate**
- **TXPOL = 0** (for high Idle state)
- **STP = desired Stop bits selection**
- **C0EN = desired checksum mode**
- **RxyPPS = TX pin selection code**
- **TX pin TRIS control = 0**
- **ON = 1**

The Slave process starts upon detecting a Break on the RX pin. The Break clears the UxTXCHK, UxRXCHK, UxP2, and UxP3 registers. At the end of the Break, the auto-baud circuity is activated and the baud rate is automatically set using the Sync character following the Break. The character following the Sync character is received as the PID code and is saved in the receive FIFO. The UART computes the two PID parity bits from the six Least Significant bits of the PID. If either parity bit does not match the corresponding bit of the received PID code, the PERIF flag is set and saved at the same FIFO location as the PID code. The UxRXIF bit is set indicating that the PID is available.

Software retrieves the PID by reading the UxRXB register and determines the Slave process to execute from that. The checksum method, number of data bytes, and whether to send or receive data, is defined by software according to the PID code.

31.5.2.1 LIN Slave Receiver

When the Slave process is a receiver, the software performs the following tasks:

- UxP3 register is written with a value equal to the number of data bytes to receive.
- C0EN bit is set or cleared to select the appropriate checksum. This must be completed before the Start bit of the checksum byte is received.
- Each byte of the process response is read from UxRXB when UxRXIF is set.

The UART updates the checksum on each received byte. When the last data byte is received, the computed checksum total is stored in the UxRXCHK register. The next received byte is saved in the receive FIFO and added with the value in UxRXCHK. The result of this addition is not accessible. However, if the result is not all ‘1’s, the CERIF bit in the UxERRIR is set. The CERIF flag persists until cleared by software. Software needs to read UxRXB to remove the checksum byte from the FIFO, but the byte can be discarded if not needed for any other purpose.

After the checksum is received, the UART ignores all activity on the RX pin until a Break starts the next transaction.

31.5.2.2 LIN Slave Transmitter

When the Slave process is a transmitter, software performs the following tasks in the order shown:

- UxP2 register is written with a value equal to the number of bytes to transmit. This will enable TXIF flag which is disabled when UxP2 is ‘0’.
- C0EN bit is set or cleared to select the appropriate checksum
- Inter-byte delay is performed
- Each byte of the process response is written to UxTXB when UxTXIF is set

The UART accumulates the checksum as each byte is written to UxTXB. After the last byte is written, the UART stores the calculated checksum in the UxTXCHK register and transmits the inverted result as the last byte in the response.

The TXIF flag is disabled when UxP2 bytes have been written. Any writes to UxTXB that exceed the UxP2 count will be ignored and set the TXWRE flag in the UxFIFO register.
31.6 DALI Mode

DALI is a protocol used for intelligent lighting control for building automation. The protocol consists of ‘Control Devices’ and ‘Control Gear’. A Control Device is an application controller that sends out commands to the light fixtures. The light fixture itself is termed as a control gear. The communication is done using Manchester encoding, which is performed by the UART hardware.

Manchester encoding consists of the clock and data in a single bit stream. A high-to-low or a low-to-high transition always occurs in the middle of the bit period and is not guaranteed to occur at the bit period boundaries.

When the consecutive bits in the bit stream are of the same value (i.e., consecutive ’1’s or consecutive ’0’s), a transition occurs at the bit boundary. However, when the bit value changes, there is no transition at the bit boundary. According to the standard, a half-bit time is typically 416.7 µs long. A double half-bit time or a single bit is typically 833.3 µs.

The protocol is inherently half-duplex. Communication over the bus occurs in the form of forward and backward frames. Wait times between the frames are defined in the standard to prevent collision between the frames.

A Control Device transmission is termed as the ‘Forward Frame’. In the DALI 2.0 standard, a forward frame can be two or three bytes in length. The two-byte forward frame is used for communication between control device and control gear, whereas the three-byte forward frame is used for communication between Control Devices on the bus. The first byte in the forward frame is the control byte and is followed by either one or two data bytes. The transaction begins when the Control Device starts a transmission. Unlike other protocols, each byte in the frame is transmitted MSB first. Typical frame timing is as shown in Figure 31-8.

During communication between two control devices, three bytes are required to be transmitted. In this case, the software must write the third byte to UxTXB as soon as UxTXIF goes True and before the output shifter becomes empty. This ensures that the three bytes of the forward frame are transmitted back-to-back, without any interruption.

All control gear on the bus receive the forward frame. If the forward frame requires a reply to be sent, one of the control gear may respond with a single byte, called the ‘Backward Frame’. The 2.0 standard requires the control gear to begin transmission of the backward frame between 5.5 ms to 10.5 ms (~14 to 22 half-bit times) after reception of the forward frame. Once the backward frame is received by the Control Device, it is required to wait a minimum of 2.4 ms (~6 half-bit times). After this wait time, the Control Device is free to transmit another forward frame (see Figure 31-9).

A Start bit is used to indicate the start of the forward and backward frames. When ABDEN = 0, the receiver bit rate is determined by the BRG register. When ABDEN = 1, the first bit synchronizes the receiver with the transmitter and sets the receiver bit rate. The low period of the Start bit is measured and is used as the timing reference for all data bits in the forward and backward frames. The ABDOVF bit is set if the Start bit low period causes the measurement counter to overflow. All bits following the Start bit are data bits. The bit stream terminates when no transition is detected in the middle of a bit period (see Figure 31-7).

Forward and backward frames are terminated by two Idle bit periods or Stop bits. Normally, these start in the first bit period of a byte. If both Stop bits are valid, the byte reception is terminated.

If either of the Stop bits is invalid, the frame is tagged as invalid by saving it as a null byte and setting the framing error in the receive FIFO.

A framing error also occurs when no transition is detected on the bus in the middle of a bit period when the byte reception is not complete. In such a scenario, the byte will be saved with the FERIF bit.

31.6.1 CONTROL DEVICE

Control Device mode is configured with the following settings:

- MODE<3:0> = 1000
- TXEN = 1
- RXEN = 1
- UxP1 = Forward frames are held for transmission this number of half-bit periods after the completion of a forward or backward frame.
- UxP2 = Forward/backward frame threshold delimiter. Any reception that starts this number of half bit periods after the completion of a forward or backward frame is detected as forward frame and sets the PERIF flag of the corresponding received byte.
- UxBRGH:L = Value to achieve 1200 baud rate
- TXPOL = appropriate polarity for interface circuit
- STP<1:0> = 10 for two Stop bits
- RxyPPS = TX pin selection code
- TX pin TRIS control = 0
- ON = 1

A forward frame is initiated by writing the control byte to the UxTXB register. Each data byte after the control byte must be written to the UxTXB register as soon as UxTXIF goes true. It is necessary to perform every write after UxTXIF goes true to ensure the transmit buffer is ready to accept the byte. Each write must also occur before the TXMTIF bit goes true, to ensure that the bit stream of forward frame is generated without interruption.
When TXMTIF goes true, indicating the transmit shift register has completed sending the last byte in the frame, the TX output is held in the Idle state for the number of half-bit periods selected by the STP bits in the UxCON2 register.

After the last Stop bit, the TX output is held in the Idle state for an additional wait time determined by the half-bit period count in the UxP1 register. For example, a 2450 µs delay (~6 half-bit times) requires a value of 6 in UxP1L.

Any writes to the UxTXB register that occur after TXMTIF goes true, but before the UxP1 wait time, will be held and then transmitted immediately following the wait time. If a backward frame is received during the wait time, any bytes that may have been written to UxTXB will be transmitted after completion of the backward frame reception the backward frame plus the UxP1 wait time.

The wait timer is reset by the backward frame and starts over immediately following the Stop bits of the backward frame. Data pending in the transmit shift register will be sent when the wait time elapses.

To replace or delete any pending forward frame data, the TXBE bit needs to be set to flush the shift register and transmit buffer, then write the new control byte to the UxTXB register. The new control byte will be held in the buffer and sent as the beginning of the next forward frame following the UxP1 wait time.

In Control Device mode, PERIF is set when a forward frame is received. This helps the software distinguish whether the received byte is part of a forward frame from a Control Device (either from the Control Device under consideration or from another Control Device on the bus) or a backward frame from a Control Gear.

31.6.2 CONTROL GEAR

The Control Gear mode is configured with the following settings:

- **MODE<3:0> = 1001**
- **TXEN = 1**
- **RXEN = 1**
- **UxP1 = Backward frames are held for transmission this number of half-bit periods after the completion of a forward frame.**
- **UxP2 = Forward/backward frame threshold delimiter. Idle periods more than this number of half-bit periods are detected as forward frames.**
- **UxBRGH:L = Value to achieve 1200 baud rate**
- **TXPOL = appropriate polarity for interface circuit**
- **RXPOL = same as TXPOL**
- **STP = 10 for two Stop bits**
- **RxyPPS = TX pin output code**
- **TX pin TRIS control = 0**
- **RXPPS = RX pin selection code**
- **RX pin TRIS control = 1**
- **Input pin ANSEL bit = 0**
- **ON = 1**

The UART starts listening for a forward frame when the Control Gear mode is entered. Only the frames that follow an Idle period longer than UxP2 half-bit periods are detected as forward frames. Backward frames from other Control Gear are ignored. Only forward frames will be stored in UxRXB. This is necessary because a backward frame can be sent only as a response to a forward frame.

The forward frame is received one byte at a time in the receive FIFO and retrieved by reading the UxRXB register. The end of the forward frame starts a timer to delay the backward frame response by wait time equal to the number of half-bit periods stored in UxP1. The data received in the forward frame is processed by the application software. If the application decides to send a backward frame in response to the forward frame, the value of the backward frame is written to UxTXB. This value is held for transmission in the transmit shift register until the wait time expires and is then transmitted.

If the backward frame data is written to UxTXB after the wait time has expired, it is held in the UxTXB register until the end of the wait time following the next forward frame. The TXMTIF bit is false when the backward frame data is held in the transmit shift register. Receiving a UxRXIF interrupt before the TXMTIF goes true indicates that the backward frame write was too late and another forward frame was received before sending the backward frame. The pending backward frame has to be flushed by setting the TXBE bit, to prevent it from being sent after the next Forward Frame.
FIGURE 31-7: MANCHESTER TIMING

FIGURE 31-8: DALI FRAME TIMING

FIGURE 31-9: DALI FORWARD/BACK FRAME TIMING
31.7 General Purpose Manchester

General purpose Manchester is a subset of the DALI mode. When the UxP1L register is cleared, there is no minimum wait time between frames. This allows full and half-duplex operation because writes to the UxTXB are not held waiting for a receive operation to complete.

General purpose Manchester operation maintains all other aspects of DALI mode such as:

- Single-pulse Start bit
- Most Significant bit first
- No stop periods between back-to-back bytes

General purpose Manchester mode is configured with the following settings:

- \( \text{MODE}_{3:0} = 1000 \)
- \( \text{TXEN} = 1 \)
- \( \text{RXEN} = 1 \)
- \( \text{UxP1} = 0h \)
- \( \text{UxBRGH:L} = \text{desired baud rate} \)
- \( \text{TXPOL} \) and \( \text{RXPOL} = \text{desired Idle state} \)
- \( \text{STP} = \text{desired number of stop periods} \)
- \( \text{RxyPPS} = \text{TX pin selection code} \)
- \( \text{TX pin TRIS control} = 0 \)
- \( \text{RXPPS} = \text{RX pin selection code} \)
- \( \text{RX pin TRIS control} = 1 \)
- \( \text{Input pin ANSEL bit} = 0 \)
- \( \text{ON} = 1 \)

The Manchester bit stream timing is shown in Figure 31-7.

31.8 Polarity

Receive and transmit polarity is user selectable and affects all modes of operation.

The idle level is programmable with the polarity control bits in the UxCON2 register. The control bits default to ‘0’, which select a high idle level. The low level Idle state is selected by setting the control bit to ‘1’. TXPOL controls the TX idle level. RXPOL controls the RX idle level.

31.9 Stop Bits

The number of Stop bits is user selectable with the STP bits in the UxCON2 register. The STP bits affect all modes of operation.

Stop bits selections include:

- 1 transmit with receive verify on first
- 1.5 transmit with receive verify on first
- 2 transmit with receive verify on both
- 2 transmit with receive verify on first only

In all modes, except DALI, the transmitter is idle for the number of Stop bit periods between each consecutively transmitted word. In DALI, the Stop bits are generated after the last bit in the transmitted data stream.

The input is checked for the idle level in the middle of the first Stop bit, when receive verify on first is selected, as well as in the middle of the second Stop bit, when verify on both is selected. If any Stop bit verification indicates a non-idle level, the framing error FERIF bit is set for the received word.

31.9.1 DELAYED UXRXIF

When operating in Half-Duplex mode, where the microcontroller needs to reverse the transceiver direction after a reception, it may be more convenient to hold off the UxRXIF interrupt until the end of the Stop bits to avoid line contention. The user selects when the UxRXIF interrupt occurs with the STPMD bit in the UxFIFO register. When STPMD is ‘1’, the UxRXIF occurs at the end of the last Stop bit. When STPMD is ‘0’, UxRXIF occurs when the received byte is stored in the receive FIFO. When STP<1:0> = 10, the store operation is performed in the middle of the second Stop bit, otherwise, it is performed in the middle of the first Stop bit. The FERIF and PERIF interrupts are not delayed with STPMD. Only UxRXIF is delayed when STPMD is set and should be the only indicator for reversing transceiver direction.

31.10 Operation after FIFO overflow

The Receive Shift Register (RSR) can be configured to stop or continue running during a receive FIFO overflow condition. Stopped operation is the Legacy mode.

When the RSR continues to run during an overflow condition, the first word received after clearing the overflow will always be valid.

When the RSR is stopped during an overflow condition, synchronization with the Start bits is lost. Therefore, the first word received after the overflow is cleared may start in the middle of a word.

Operation during overflow is selected with the RUNOVF bit in the UxCON2 register. Setting the RUNOVF bit selects the run during overflow method.
31.11 Receive and Transmit Buffers

The UART uses small buffer areas to transmit and receive data. These are sometimes referred to as FIFOs.

The receiver has a Receive Shift Register (RSR) and two buffer registers. The buffer at the top of the FIFO (earliest byte to enter the FIFO) is by retrieved by reading the UxRXB register.

The transmitter has one Transmit Shift Register (TSR) and one buffer register. Writes to UxTXB go to the transmit buffer then immediately to the TSR, if it is empty. When the TSR is not empty, writes to UxTXB are held then transferred to the TSR when it becomes available.

31.11.1 FIFO STATUS

The UxFIFO register contains several Status bits for determining the state of the receive and transmit buffers.

The RXBE bit indicates that the receive FIFO is empty. This bit is essentially the inverse of UxRXIF. The RXBF bit indicates that the receive FIFO is full.

The transmitter has only one buffer register so the Status bits are essentially a copy and inverse of the UxTXIF bit. The TXBE bit indicates that the buffer is empty (same as UxTXIF) and the TXBF bit indicates that the buffer is full (UxTXIF inverse). A third transmitter Status bit, TXWRE (transmit write error), is set whenever a UxTXB write is performed when the TXBF bit is set. This indicates that the write was unsuccessful.

31.11.2 FIFO RESET

All modes support resetting the receive and transmit buffers.

The receive buffer is flushed and all unread data discarded when the RXBE bit in the UxFIFO register is written to ‘1’. The MOVWF instruction with the TXBE bit cleared should be used to avoid inadvertently clearing a byte pending in the TSR when UxTXB is empty.

Data written to UxTXB when TXEN is low will be held in the Transmit Shift Register (TSR) then sent when TXEN is set. The transmit buffer and inactive TSR are flushed by setting the TXBE bit in the UxFIFO register. Setting TXBE while a character is actively transmitting from the TSR will complete the transmission without being flushed.

Clearing the ON bit will discard all received data and transmit data pending in the TSR and UxTXB.

31.12 Flow Control

This section does not apply to the LIN, DALI, or DMX modes.

Flow control is the means by which a sending UART data stream can be suspended by a receiving UART. Flow control prevents input buffers from overflowing without software intervention. The UART supports both hardware and XON/XOFF methods of flow control.

The flow control method is selected with the FLO<1:0> bits in the UxCON2 register. Flow control is disabled when both bits are cleared.

31.12.1 HARDWARE FLOW CONTROL

Hardware flow control is selected by setting the FLO<1:0> bits to ‘10’.

Hardware flow control consists of three lines. The RS-232 signal names for two of these are RTS, and CTS. Both are low true. The third line may be used to control an RS-485 transceiver. The signal name for this is TXDE for transmit drive enable. This output is high when the TX output is actively sending a character and low at all other times. The UART is configured as DTE (computer) equipment which means RTS is an output and CTS is an input.

The RTS and CTS signals work as a pair to control the transmission flow. A DTE-to-DTE configuration connects the RTS output of the receiving UART to the CTS input of the sending UART. Refer to Figure 31-10.

The UART receiving data asserts the RTS output low when the input FIFO is empty. When a character is received, the RTS output goes high until the UxRXB is read to free up both FIFO locations.

When the CTS input goes high after a byte has started to transmit, the transmission will complete normally. The receiver accommodates this by accepting the character in the second FIFO location even when the CTS input is high.
31.12.2 RS-485 TRANSCEIVER CONTROL

Hardware flow control can be used to control the direction of an RS-485 transceiver as shown in Figure 31-11. Configure the CTS input to be always enabled by setting the UxCTSPPS selection to an unimplemented port pin such as RD0. When the signal and control lines are configured as shown in Figure 31-11, then the UART will not receive its own transmissions. To verify that there are no collisions on the RS-485 lines then the transceiver RE control can be disconnected from TXDE and tied low thereby enabling loop-back reception of all transmissions. See Section 31.14 “Collision Detection” for more information.

31.12.3 XON/XOFF FLOW CONTROL

XON/XOFF flow control is selected by setting the FLO<1:0> bits to '01'.

XON/XOFF is a data based flow control method. The signals to suspend and resume transmission are special characters sent by the receiver to the transmitter. The advantage is that additional hardware lines are not needed.

XON/XOFF flow control requires full-duplex operation because the transmitter must be able to receive the signal to suspend transmitting while the transmission is in progress. Although XON and XOFF are not defined in the ASCII code, the generally accepted values are 13h for XOFF and 11h for XON. The UART uses those codes.

The transmitter defaults to XON, or transmitter enabled. This state is also indicated by the read-only XON bit in the UxFIFO register.

When an XOFF character is received, the transmitter stops transmitting after completing the character actively being transmitted. The transmitter remains disabled until an XON character is received.

XON will be forced on when software toggles the TXEN bit.

When the RUNOVF bit in the UxCON2 register is set then XON and XOFF characters continue to be received and processed without the need to clear the input FIFO by reading the UxRXB. However, if the RUNOVF bit is clear then the UxRXB must be read to avoid a receive overflow which will suspend flow control when the receive buffer overflows.
31.13 Checksum

This section does not apply to the LIN mode, which handles checksums automatically.

The transmit and receive checksum adders are enabled when the C0EN bit in the UxCON2 register is set. When enabled, the adders accumulate every byte that is transmitted or received. The accumulated sum includes the carry of the addition. Software is responsible for clearing the checksum registers before a transaction and performing the check at the end of the transaction.

The following is an example of how the checksum registers could be used in the Asynchronous modes.

31.13.1 TRANSMIT CHECKSUM METHOD
1. Clear the UxTXCHK register.
2. Set the C0EN bit.
3. Send all bytes of the transaction output.
4. Invert UxTXCHK and send the result as the last byte of the transaction.

31.13.2 RECEIVE CHECKSUM METHOD
1. Clear the UxRXCHK register.
2. Set the C0EN bit.
3. Receive all bytes in the transaction including the checksum byte.
4. Set MSb of UxRXCHK if 7-bit mode is selected.
5. Add 1 to UxRXCHK.
6. If the result is '0', the checksum passes, otherwise it fails.

The CERIF checksum interrupt flag is not active in any mode other than LIN.

31.14 Collision Detection

External forces that interfere with the transmit line are detected in all modes of operation with collision detection. Collision detection is always active when RXEN and TXEN are both set.

When the receive input is connected to the transmit output through either the same I/O pin or external circuitry, a character will be received for every character transmitted. The collision detection circuit provides a warning when the word received does not match the word transmitted.

The TXCIF flag in the UxERRIR register is used to signal collisions. This signal is only useful when the TX output is looped back to the RX input and everything that is transmitted is expected to be received. If more than one transmitter is active at the same time, it can be assumed that the TX word will not match the RX word. The TXCIF detects this mismatch and flags an interrupt. The TXCIF bit will also be set in DALI mode transmissions when the received bit is missing the expected mid-bit transition.

Collision detection is always active, regardless of whether or not the RX input is connected to the TX output. It is up to the user to disable the TXCIE bit when collision interrupts are not required.

The software overhead of unloading the receive buffer of transmitted data is avoided by setting the RUNOVF bit in UxCON2 and ignoring the receive interrupt and letting the receive buffer overflow. When the transmission is complete, prepare for receiving data by flushing the receive buffer (see Section 31.11.2, FIFO Reset) and clearing the RXFOIF overflow flag in the UxERRIR register.

31.15 RX/TX Activity Timeout

The UART works in conjunction with the HLT timers to monitor activity on the RX and TX lines. Use this feature to determine when there has been no activity on the receive or transmit lines for a user specified period of time.

To use this feature, set the HLT to the desired timeout period by a combination of the HLT clock source, timer prescale value, and timer period registers. Configure the HLT to reset on the UART TX or RX line and start the HLT at the same time the UART is started. UART activity will keep resetting the HLT to prevent a full HLT period from elapsing. When there has been no activity on the selected TX or RX line for longer than the HLT period then an HLT interrupt will occur signaling the timeout event.

For example, the following register settings will configure HLT2 for a 5 ms timeout of no activity on U1RX:
- T2PR = 0x9C (156 prescale periods)
- T2CLKCON = 0x05 (500 kHz internal oscillator)
- T2HLT = 0x04 (free running, reset on rising edge)
- T2RST = 0x15 (reset on U1RX)
- T2CON = 0xC0 (Timer2 on with 1:16 prescale)
31.16 Clock Accuracy with Asynchronous Operation

The factory calibrates the internal oscillator block output (INTOSC). However, the INTOSC frequency may drift as VDD or temperature changes, and this directly affects the asynchronous baud rate. Two methods may be used to adjust the baud rate clock, but both require a reference clock source of some kind.

The first (preferred) method uses the OSCTUNE register to adjust the INTOSC output. Adjusting the value of the OSCTUNE register allows for fine resolution changes to the system clock source. See Section 7.2.2.3 “Internal Oscillator Frequency Adjustment” for more information.

The other method adjusts the value of the Baud Rate Generator. This can be done automatically with the Auto-Baud Detect feature (see Section 31.17.1 “Auto-Baud Detect”). There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change of the peripheral clock frequency.

31.17 UART Baud Rate Generator (BRG)

The Baud Rate Generator (BRG) is a 16-bit timer that is dedicated to the support of the UART operation.

The UxBRGH, UxBRGL register pair determines the period of the free running baud rate timer. The multiplier of the baud rate period is determined by the BRGS bit in the UxCON0 register.

Table 31-1 contains the formulas for determining the baud rate. Example 31-1 provides a sample calculation for determining the baud rate and baud rate error.

The high baud rate range (BRGS = 1) is intended to extend the baud rate range up to a faster rate when the desired baud rate is not possible otherwise. Using the normal baud rate range (BRGS = 0) is recommended when the desired baud rate is achievable with either range.

Writing a new value to the UxBRGH, UxBRGL register pair causes the BRG timer to be reset (or cleared). This ensures that the BRG does not wait for a timer overflow before outputting the new baud rate.

If the system clock is changed during an active receive operation, a receive error or data loss may result. To avoid this problem, check the status of the RXIDL bit to make sure that the receive operation is idle before changing the system clock.

### Example 31-1: Calculating Baud Rate Error

For a device with Fosc of 16 MHz, desired baud rate of 9600, Asynchronous mode, BRGS = 0:

\[
\begin{align*}
\text{Desired Baud Rate} &= \frac{F_{\text{OSC}}}{16(UxBRG) + 1} \\
X &= \frac{F_{\text{OSC}}}{\text{Desired Baud Rate}} - 1 \\
X &= \frac{16000000}{9600} - 1 \\
X &= [103.17] = 103 \\
\text{Calculated Baud Rate} &= \frac{16000000}{16(103 + 1)} \\
&= 9615 \\
\text{Error} &= \frac{\text{Calc. Baud Rate} - \text{Desired Baud Rate}}{\text{Desired Baud Rate}} \\
&= \frac{9615 - 9600}{9600} = 0.16\%
\end{align*}
\]

<table>
<thead>
<tr>
<th>BRGS</th>
<th>BRG/UART Mode</th>
<th>Baud Rate Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>High Rate</td>
<td>(F_{\text{OSC}}/[4(n+1)])</td>
</tr>
<tr>
<td>0</td>
<td>Normal Rate</td>
<td>(F_{\text{OSC}}/[16(n+1)])</td>
</tr>
</tbody>
</table>

Legend: \(n\) = value of UxBRGH, UxBRGL register pair.
31.17.1 AUTO-BAUD DETECT

The UART module supports automatic detection and calibration of the baud rate in the 8-bit Asynchronous and LIN modes. However, setting ABREN to start auto-baud detection is neither necessary, nor possible in LIN mode because that mode supports auto-baud detection automatically at the beginning of every data packet. Enabling auto-baud detect with the ABDEN bit applies to the Asynchronous modes only.

When Auto-Baud Detect (ABD) is active, the clock to the BRG is reversed. Rather than the BRG clocking the incoming RX signal, the RX signal is timing the BRG. The Baud Rate Generator is used to time the period of a received 55h (ASCII “U”), which is the Sync character for the LIN bus. The unique feature of this character is that it has five falling edges, including the Start bit edge, five rising edges including the Stop bit edge.

In 8-bit Asynchronous mode, setting the ABDEN bit in the UxCON0 register enables the auto-baud calibration sequence. The first falling edge of the RX input after ABREN is set will start the auto-baud calibration sequence. While the ABD sequence takes place, the UART state machine is held in idle. On the first falling edge of the receive line, the UxBRG begins counting up using the BRG counter clock as shown in Figure 31-12. The fifth falling edge will occur on the RX pin at the beginning of the bit 7 period. At that time, an accumulated value totaling the proper BRG period is left in the UxBRGH, UxBRGL register pair, the ABDEN bit is automatically cleared and the ABDIF interrupt flag is set. ABDIF must be cleared by software.

FIGURE 31-12: AUTOMATIC BAUD RATE CALIBRATION

<table>
<thead>
<tr>
<th>BRG Value</th>
<th>RX pin</th>
<th>BRG Clock</th>
<th>ABREN bit</th>
<th>RxdIL</th>
<th>ABDIF bit (Interrupt)</th>
<th>UxBRG</th>
</tr>
</thead>
<tbody>
<tr>
<td>XXXXh</td>
<td>0000h</td>
<td>Start</td>
<td>bit 0</td>
<td>bit 1</td>
<td>bit 2</td>
<td>bit 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Edge #1</td>
<td>bit 4</td>
<td>bit 5</td>
<td>bit 6</td>
<td>Stop bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Edge #2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Edge #3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Edge #4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Edge #5</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Auto-baud is supported in LIN and 8-bit Asynchronous modes only.

Note 1: If the WUE bit is set with the ABREN bit, auto-baud detection will occur on the byte following the Break character (see Section 31.17.3 “Auto-Wake-up on Break”).

2: It is up to the user to determine that the incoming character baud rate is within the range of the selected BRG clock source. Some combinations of oscillator frequency and UART baud rates are not possible.

TABLE 31-2: BRG COUNTER CLOCK RATES

<table>
<thead>
<tr>
<th>BRG</th>
<th>BRG Base Clock</th>
<th>BRG ABD Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Fosc/4</td>
<td>Fosc/32</td>
</tr>
<tr>
<td>0</td>
<td>Fosc/16</td>
<td>Fosc/128</td>
</tr>
</tbody>
</table>

RXIDL indicates that the sync input is active. RXIDL will go low on the first falling edge and go high on the fifth rising edge.

The BRG auto-baud clock is determined by the BRGS bit as shown in Table 31-2. During ABD, the internal BRG register is used as a 16-bit counter. However, the UxBRGH and UxBRGL registers retain the previous BRG value until the auto-baud process is successfully completed. While calibrating the baud rate period, the internal BRG register is clocked at 1/8th the BRG base clock rate. The resulting byte measurement is the average bit time when clocked at full speed and is transferred to the UxBRGH and UxBRGL registers when complete.
31.17.2 AUTO-BAUD OVERFLOW

During the course of automatic baud detection, the ABDOVF bit in the UxERRIR register will be set if the baud rate counter overflows before the fifth falling edge is detected on the RX pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the UxBRGH:UxBRGL register pair. After the ABDOVF bit has been set, the state machine continues to search until the fifth falling edge is detected on the RX pin. Upon detecting the fifth falling RX edge, the hardware will set the ABDEN bit in the UxCON0 register. The UxBRGH and UxBRGL register values retain their previous value. The ABDIF flag in the UxUIR register and ABDOVF flag in the UxERRIR register can be cleared by software directly. To generate an interrupt on an auto-baud overflow condition, all the following bits must be set:

- ABDOVE bit in the UxERRIE register
- UxEIE bit in the PIEx register
- PIE and GIE bits in the INTCON register

To terminate the auto-baud process before the ABDIF flag is set, clear the ABDEN bit, then clear the ABDOVF bit in the UxERRIR register.

31.17.3 AUTO-WAKE-UP ON BREAK

During Sleep mode, all clocks to the UART are suspended. Because of this, the Baud Rate Generator is inactive and a proper character reception cannot be performed. The Auto-Wake-up feature allows the controller to wake-up due to activity on the RX line. The Auto-Wake-up feature is enabled by setting both the WUE bit in the UxCON1 register and the UxE bit in the PIEx register. Once set, the normal receive sequence on RX is disabled, and the UART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a transition out of the Idle state on the RX line. (This coincides with the start of a Break or a wake-up signal character for the LIN protocol.)

The UART module generates a WUIF interrupt coincident with the wake-up event. The interrupt is generated synchronously to the Q clocks in normal CPU operating modes (Figure 31-13), and asynchronously, if the device is in Sleep mode (Figure 31-14). The interrupt condition is cleared by clearing the WUIF bit in the UxUIR register. To generate an interrupt on a wake-up event, all the following bits must be set:

- UxE bit in the PIEx register
- PIE and GIE bits in the INTCON register

The WUE bit is automatically cleared by the transition to the Idle state on the RX line at the end of the Break. This signals to the user that the Break event is over. At this point, the UART module is in Idle mode, waiting to receive the next character.

31.17.3.1 Special Considerations

**Break Character**

To avoid character errors or character fragments during a wake-up event, the wake-up character must be all zeros.

When the wake-up is enabled, the function works independent of the low time on the data stream. If the WUE bit is set and a valid non-zero character is received, the low time from the Start bit to the first rising edge will be interpreted as the wake-up event. The remaining bits of the character will be received as a fragmented character and subsequent characters can result in framing or overrun errors.

Therefore, the initial character of the transmission must be all zeros. This must be eleven or more bit times, 13-bit times recommended for LIN bus, or any number of bit times for standard RS-232 devices.

**Oscillator Start-up Time**

Oscillator start-up time must be considered, especially in applications using oscillators with longer start-up intervals (i.e., LP, XT or HS/PLL modes). The Sync Break (or wake-up signal) character must be of sufficient length, and be followed by a sufficient interval, to allow enough time for the selected oscillator to start and provide proper initialization of the UART.

**WUE Bit**

To ensure that no actual data is lost, check the RXIDL bit to verify that a receive operation is not in process before setting the WUE bit. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.
31.18 Transmitting a Break

The UART module has the capability of sending either a fixed length Break period or a software timed Break period. The fixed length Break consists of a Start bit, followed by 12 ‘0’ bits and a Stop bit. The software timed Break is generated by setting and clearing the BRKOV bit in the UxCON1 register.

To send the fixed length Break, set the SENDB and TXEN bits in the UxCON0 register. The Break sequence is then initiated by a write to UxTXB. The timed Break will occur first, followed by the character written to UxTXB that initiated the Break. The initiating character is typically the Sync character of the LIN specification.

SENB is disabled in the LIN and DMX modes because those modes generate the Break sequence automatically.

The SENDB bit is automatically reset by hardware after the Break Stop bit is complete.

The TXMTIF bit in the UxERRIR register indicates when the transmit operation is active or idle, just as it does during normal transmission. See Figure 31-15 for the timing of the Break sequence.

31.19 Receiving a Break

The UART has counters to detect when the RX input remains in the space state for an extended period of time. When this happens, the RXBKIF bit in the UxERRIR register is set.

A Break is detected when the RX input remains in the space state for 11 bit periods for Asynchronous and LIN modes, and 23 bit periods for DMX mode.

The user can select to receive the Break interrupt as soon as the Break is detected or at the end of the Break, when the RX input returns to the Idle state. When RXBIMD in the UxCON1 is ‘1’ then RXBKIF is set immediately upon Break detection. When RXBIMD is ‘0’ then RXBKIF is set when the RX input returns to the Idle state.

31.20 UART Operation During Sleep

The UART ceases to operate during Sleep. The safe way to wake the device from Sleep by a serial operation is to use the Wake-on-Break feature of the UART. See Section 31.17.3, Auto-Wake-up on Break.
**FIGURE 31-15: SEND BREAK CHARACTER SEQUENCE**

<table>
<thead>
<tr>
<th>Write to UxTXB</th>
<th>BRG Output (Shift Clock)</th>
<th>TX (pin)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Start bit</td>
</tr>
<tr>
<td>UxTXIF bit (Transmit Interrupt Flag)</td>
<td></td>
<td>Auto Cleared</td>
</tr>
<tr>
<td>TXMTIF bit (Transmit Shift Empty Flag)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SENDB (send Break control bit)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
31.21 Register Definitions: UART Control

Long bit name prefixes for the UART peripherals are shown below. Refer to Section 1.3 “Register and Bit naming conventions” for more information.

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Bit Name Prefix</th>
</tr>
</thead>
<tbody>
<tr>
<td>UART 1</td>
<td>U1</td>
</tr>
<tr>
<td>UART 2</td>
<td>U2</td>
</tr>
</tbody>
</table>

REGISTER 31-1: UxCON0: UART CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>BRGS</th>
<th>ABDEN</th>
<th>TXEN</th>
<th>RXEN</th>
<th>MODE&lt;3:0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- HC = Hardware clear

bit 7  | BRGS: Baud rate Generator Speed Select bit
| ‘1’ = Baud rate generator is high speed with 4 baud clocks per bit
| ‘0’ = Baud rate generator is normal speed with 16 baud clocks per bit

bit 6  | ABDEN: Auto-baud Detect Enable bit(2)
| ‘1’ = Auto-baud is enabled. Receiver is waiting for Sync character (0x55)
| ‘0’ = Auto-baud is not enabled or auto-baud is complete

bit 5  | TXEN: Transmit Enable Control bit(2)
| ‘1’ = Transmit is enabled. TX output pin drive is forced on when transmission is active, and controlled by PORT TRIS control when transmission is idle.
| ‘0’ = Transmit is disabled. TX output pin drive is controlled by PORT TRIS control

bit 4  | RXEN: Receive Enable Control bit(2)
| ‘1’ = Receiver is enabled
| ‘0’ = Receiver is disabled

bit 3-0 | MODE<3:0>: UART Mode Select bits(2)
| 1111 = Reserved
| 1110 = Reserved
| 1101 = Reserved
| 1100 = LIN Master/Slave mode
| 1011 = LIN Slave-Only mode
| 1010 = DMX mode
| 1001 = DALI Control Gear mode
| 1000 = DALI Control Device mode
| 0111 = Reserved
| 0110 = Reserved
| 0101 = Reserved
| 0100 = Asynchronous 9-bit UART Address mode. 9th bit: ‘1’ = address, ‘0’ = data
| 0011 = Asynchronous 8-bit UART mode with 9th bit even parity
| 0010 = Asynchronous 8-bit UART mode with 9th bit odd parity
| 0001 = Asynchronous 7-bit UART mode
| 0000 = Asynchronous 8-bit UART mode

Note 1: Changing the UART MODE while ON = 1 may cause unexpected results.
2: Clearing TXEN or RXEN will not clear the corresponding buffers. Use TXBE or RXBE to clear the buffers.
3: ABDEN is read-only when MODE = 1001. When MODE = 100x and ABDEN = 1, then auto-baud is determined from Start bit.
## REGISTER 31-2: UxCON1: UART CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W/HC-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W/HC-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td></td>
<td></td>
<td></td>
<td>WUE</td>
<td></td>
<td>RXBIMD</td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td>BRKOV R</td>
<td>SEND B</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **HC** = Hardware clear

### bit 7  **ON:** Serial Port Enable bit
- **1** = Serial port enabled
- **0** = Serial port disabled (held in Reset)

### bit 6-5  **Unimplemented:** Read as '0'

### bit 4  **WUE:** Wake-up Enable bit
- **1** = Receiver is waiting for falling RX input edge which will set the UxIF bit. Cleared by hardware on wake event. Also requires UxIE bit of PIEx to enable wake
- **0** = Receiver operates normally

### bit 3  **RXBIMD:** Receive Break Interrupt Mode Select bit
- **1** = Set RXBKIF immediately when RX in has been low for the minimum Break time
- **0** = Set RXBKIF on rising RX input after RX in has been low for the minimum Break time

### bit 2  **Unimplemented:** Read as '0'

### bit 1  **BRKOV R:** Send Break Software Override bit
- **1** = TX output is forced to non-idle state
- **0** = TX output is driven by transmit shift register

### bit 0  **SENDB:** Send Break Control bit<sup>(1)</sup>
- **1** = Output Break upon UxTXB write. Written byte follows Break. Bit is cleared by hardware.
- **0** = Break transmission completed or disabled

### Note 1:  This bit is read-only in LIN, DMX, and DALI modes.
**REGISTER 31-3: UxCON2: UART CONTROL REGISTER 2**

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RUNOVF</td>
<td>RXPOL</td>
<td>STP&lt;1:0&gt;</td>
<td>C0EN</td>
<td>TXPOL</td>
<td>FLO&lt;1:0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

- **RUNOVF**: Run During Overflow Control bit
  - 1 = RX input shifter continues to synchronize with Start bits after overflow condition
  - 0 = RX input shifter stops all activity on receiver overflow condition

- **RXPOL**: Receive Polarity Control bit
  - 1 = Invert RX polarity, Idle state is low
  - 0 = RX polarity is not inverted, Idle state is high

- **STP<1:0>**: Stop Bit Mode Control bits
  - 11 = Transmit 2 Stop bits, receiver verifies first Stop bit
  - 10 = Transmit 2 Stop bits, receiver verifies first and second Stop bits
  - 01 = Transmit 1.5 Stop bits, receiver verifies first Stop bit
  - 00 = Transmit 1 Stop bit, receiver verifies first Stop bit

- **C0EN**: Checksum Mode Select bit
  - **LIN mode:**
    - 1 = Checksum Mode 1, enhanced LIN checksum includes PID in sum
    - 0 = Checksum Mode 0, legacy LIN checksum does not include PID in sum
  - **Other modes:**
    - 1 = Add all TX and RX characters
    - 0 = Checksums disabled

- **TXPOL**: Transmit Polarity Control bit
  - 1 = Output data is inverted, TX output is low in Idle state
  - 0 = Output data is not inverted, TX output is high in Idle state

- **FLO<1:0>**: Handshake Flow Control bits
  - 11 = Reserved
  - 10 = RTS/CTS and TXDE Hardware flow control
  - 01 = XON/XOFF Software flow control
  - 00 = Flow control is off

**Note 1:** All modes transmit selected number of Stop bits. Only DMX and DALI receivers verify selected number of Stop bits and all others verify only the first Stop bit.
REGISTER 31-4: UxERRIR: UART ERROR INTERRUPT FLAG REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 = Transmit shift register is empty (Set at end of Stop bits)</td>
<td>1 = Unread byte at top of input FIFO has parity error (LIN and Parity modes)</td>
<td>1 = Start bit measurement overflowed counter (DALI mode)</td>
<td>1 = Checksum error (LIN mode only)</td>
<td>1 = Unread byte at top of input FIFO has framing error</td>
<td>1 = Break detected</td>
<td>1 = Receive FIFO has overflowed</td>
<td>1 = Transmitted word is not equal to the word received during transmission</td>
</tr>
<tr>
<td>0 = Transmit shift register is actively shifting data</td>
<td>0 = Unread byte at top of input FIFO does not have parity error</td>
<td>0 = No overflow during Start bit measurement</td>
<td>0 = No checksum error</td>
<td>0 = Unread byte at top of input FIFO has framing error</td>
<td>0 = No Break detected</td>
<td>0 = Receive FIFO has not overflowed</td>
<td>0 = Transmitted word equals the word received during transmission</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **’1’** = Bit is set
- **’0’** = Bit is cleared
- **S** = Hardware set
- **C** = Hardware clear
### REGISTER 31-5: UxERRIE: UART ERROR INTERRUPT ENABLE REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Readable</th>
<th>Writable</th>
<th>Unimplemented</th>
<th>Value at POR and BOR/Value at all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>TXMTIE</td>
<td>Transmit Shift Register Empty Interrupt Enable bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td>-n/n</td>
</tr>
<tr>
<td>6</td>
<td>PERIE</td>
<td>Parity Error Interrupt Enable bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td>-n/n</td>
</tr>
<tr>
<td>5</td>
<td>ABDONE</td>
<td>Auto-Baud Detect Overflow Interrupt Enable bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td>-n/n</td>
</tr>
<tr>
<td>4</td>
<td>CERIE</td>
<td>Checksum Error Interrupt Enable bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td>-n/n</td>
</tr>
<tr>
<td>3</td>
<td>FERIE</td>
<td>Framing Error Interrupt Enable bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td>-n/n</td>
</tr>
<tr>
<td>2</td>
<td>RXBKIE</td>
<td>Break Reception Interrupt Enable bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td>-n/n</td>
</tr>
<tr>
<td>1</td>
<td>RXFOIE</td>
<td>Receive FIFO Overflow Interrupt Enable bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td>-n/n</td>
</tr>
<tr>
<td>0</td>
<td>TXCIE</td>
<td>Transmit Collision Interrupt Enable bit</td>
<td>R</td>
<td>W</td>
<td>U</td>
<td>-n/n</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**Bit Descriptions:**
- **TXMTIE**: Transmit Shift Register Empty Interrupt Enable bit
  - **0** = Interrupt not enabled
  - **1** = Interrupt enabled
- **PERIE**: Parity Error Interrupt Enable bit
  - **0** = Interrupt not enabled
  - **1** = Interrupt enabled
- **ABDOVE**: Auto-Baud Detect Overflow Interrupt Enable bit
  - **0** = Interrupt not enabled
  - **1** = Interrupt enabled
- **CERIE**: Checksum Error Interrupt Enable bit
  - **0** = Interrupt not enabled
  - **1** = Interrupt enabled
- **FERIE**: Framing Error Interrupt Enable bit
  - **0** = Interrupt not enabled
  - **1** = Interrupt enabled
- **RXBKIE**: Break Reception Interrupt Enable bit
  - **0** = Interrupt not enabled
  - **1** = Interrupt enabled
- **RXFOIE**: Receive FIFO Overflow Interrupt Enable bit
  - **0** = Interrupt not enabled
  - **1** = Interrupt enabled
- **TXCIE**: Transmit Collision Interrupt Enable bit
  - **0** = Interrupt not enabled
  - **1** = Interrupt enabled
## REGISTER 31-6: UxUIR: UART GENERAL INTERRUPT REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value 1</th>
<th>Value 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>WUIF: Wake-up Interrupt bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Idle to non-idle transition on RX line detected when WUE is set. Also sets UxIF. (WUIF must be cleared by software to clear UxIF)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = WUE not enabled by software or no transition detected</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>ABDIF: Auto-Baud detect interrupt bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Auto-baud detection complete. Status shown in UxIF when ABDIE is set. (Must be cleared by software)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Auto-baud not enabled or auto-baud enabled and auto-baud detection not complete</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5-3</td>
<td>Unimplemented: Read as '0'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>ABDIE: Auto-Baud Detect Interrupt Enable bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = ABDIF will set UxIF bit in PIRx register</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = ABDIF will not set UxIF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1-0</td>
<td>Unimplemented: Read as '0'</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **’1’** = Bit is set
- **’0’** = Bit is cleared
- **S** = Hardware set
- **-n/n** = Value at POR and BOR/Value at all other Resets
REGISTER 31-7:  UxFIFO: UART FIFO STATUS REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W/S-0/0</th>
<th>R/W-0/0</th>
<th>R/W/S/C-1/1</th>
<th>R/S/C-0/0</th>
<th>R/S/C-1/1</th>
<th>R/W/S/C-1/1</th>
<th>R/S/C-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXWRE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>STPMD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TXBE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TXBF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RXIDL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XON</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RXBE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RXBF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- \( R \) = Readable bit
- \( W \) = Writable bit
- \( U \) = Unimplemented bit, read as ‘0’
- \( u \) = Bit is unchanged
- \( x \) = Bit is unknown
- \( -n/n \) = Value at POR and BOR/Value at all other Resets
- \( '1' \) = Bit is set
- \( '0' \) = Bit is cleared
- \( S \) = Hardware set
- \( C \) = Hardware clear

bit 7  \textbf{TXWRE}: Transmit Write Error Status bit (Must be cleared by software)

\textbf{Lin Master mode}:

- 1 = UxP1L was written when a master process was active

\textbf{Lin Slave mode}:

- 1 = UxTXB was written when UxP2 = 0 or more than UxP2 bytes have been written to UxTXB since last Break

\textbf{Address Detect mode}:

- 1 = UxP1L was written before the previous data in UxP1L was transferred to TX shifter

\textbf{All modes}:

- 1 = A new byte was written to UxTXB when the output FIFO was full
- 0 = No error

bit 6  \textbf{STPMD}: Stop Bit Detection Mode bit

- 1 = Assert UxRXIF at end of last Stop bit or end of first Stop bit when STP = 11
- 0 = Assert UxRXIF in middle of first Stop bit

bit 5  \textbf{TXBE}: Transmit Buffer Empty Status bit

- 1 = Transmit buffer is empty. Setting this bit will clear the transmit buffer and output shift register.
- 0 = Transmit buffer is not empty. Software cannot clear this bit.

bit 4  \textbf{TXBF}: Transmit Buffer Full Status bit

- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full

bit 3  \textbf{RXIDL}: Receive Pin Idle Status bit

- 1 = Receive pin is in Idle state
- 0 = UART is receiving Start, Stop, Data, Auto-baud, or Break

bit 2  \textbf{XON}: Software Flow Control Transmit Enable Status bit

- 1 = Transmitter is enabled
- 0 = Transmitter is disabled

bit 1  \textbf{RXBE}: Receive Buffer Empty Status bit

- 1 = Receive buffer is empty. Setting this bit will clear the RX buffer\(^{(4)}\)
- 0 = Receive buffer is not empty. Software cannot clear this bit.

bit 0  \textbf{RXBF}: Receive Buffer Full Status bit

- 1 = Receive buffer is full
- 0 = Receive buffer is not full

\textbf{Note 1}: The BSF instruction should not be used to set RXBE because doing so will clear a byte pending in the transmit shift register when the UxTXB register is empty. Instead, use the MOVWF instruction with a ‘0’ in the TXBE bit location.
### REGISTER 31-8: UxBRGL: UART BAUD RATE GENERATOR LOW REGISTER

<table>
<thead>
<tr>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

**bit 7-0 BRG<7:0>: Least Significant Byte of Baud Rate Generator**

### REGISTER 31-9: UxBRGH: UART BAUD RATE GENERATOR HIGH REGISTER

<table>
<thead>
<tr>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

**bit 7-0 BRG<15:8>: Most Significant Byte of Baud Rate Generator**

**Note 1:** The UxBRG registers should only be written when ON = 0.

**Note 2:** Maximum BRG value when MODE = ‘100x’ and BRGS = 1 is 0x7FFE.

**Note 3:** Maximum BRG value when MODE = ‘100x’ and BRGS = 0 is 0x1FFE.
## REGISTER 31-10: UxRXB: UART RECEIVE REGISTER

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th>RXB&lt;7:0&gt;</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R-0/0</td>
<td>R-0/0</td>
<td>R-0/0</td>
</tr>
<tr>
<td>R-0/0</td>
<td>R-0/0</td>
<td>R-0/0</td>
</tr>
<tr>
<td>R-0/0</td>
<td>R-0/0</td>
<td>R-0/0</td>
</tr>
<tr>
<td>R-0/0</td>
<td>R-0/0</td>
<td>R-0/0</td>
</tr>
<tr>
<td>R-0/0</td>
<td>R-0/0</td>
<td>R-0/0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **1/n** = Value at POR and BOR/Value at all other Resets
- **0/n** = Value at POR and BOR/Value at all other Resets

**Legend:**
- **1** = Bit is set
- **0** = Bit is cleared

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **1/n** = Value at POR and BOR/Value at all other Resets

**Legend:**
- **0/n** = Value at POR and BOR/Value at all other Resets

**Legend:**
- **1** = Bit is set
- **0** = Bit is cleared

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **1/n** = Value at POR and BOR/Value at all other Resets

**Legend:**
- **0/n** = Value at POR and BOR/Value at all other Resets

**Legend:**
- **1** = Bit is set
- **0** = Bit is cleared

### bit 7-0
**RXB<7:0>:** Top of Receive Buffer

### bit 7-0
**TXB<7:0>:** Bottom of Transmit Buffer
REGISTER 31-12: UxP1H: UART PARAMETER 1 HIGH REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-0/0</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

**bit 7-6**  
Unimplemented: Read as ‘0’

**bit 0**  
P1<8>: Most Significant Bit of Parameter 1
- **DMX mode:** Most Significant bit of number of bytes to transmit between Start Code and automatic Break generation
- **DALI Control Device mode:** Most Significant bit of idle time delay after which a Forward Frame is sent. Measured in half-bit periods
- **DALI Control Gear mode:** Most Significant bit of delay between the end of a Forward Frame and the start of the Back Frame
- **Other modes:** Not used

REGISTER 31-13: UxP1L: UART PARAMETER 1 LOW REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

**bit 7-0**  
P1<7:0>: Least Significant Bits of Parameter 1
- **DMX mode:** Least Significant Byte of number of bytes to transmit between Start Code and automatic Break generation
- **DALI Control Device mode:** Least Significant Byte of idle time delay after which a Forward Frame is sent. Measured in half-bit periods
- **DALI Control Gear mode:** Least Significant Byte of delay between the end of a Forward Frame and the start of the Back Frame
- **LIN mode:** PID to transmit (Only Least Significant 6 bits used)
- **Asynchronous Address mode:** Address to transmit (9th transmit bit automatically set to ‘1’)
- **Other modes:** Not used
## REGISTER 31-14: UxP2H: UART PARAMETER 2 HIGH REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>P2&lt;8&gt;</td>
</tr>
</tbody>
</table>

**Legend:**

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ’1’ = Bit is set
- ’0’ = Bit is cleared

**bit 7-6**

**Unimplemented:** Read as ‘0’

**bit 0**

**P2<8>:** Most Significant Bit of Parameter 2

**DMX mode:**
Most Significant bit of first address of receive block

**DALI mode:**
Most Significant bit of number of half-bit periods of idle time in Forward Frame detection threshold

**Other modes:**
Not used

## REGISTER 31-15: UxP2L: UART PARAMETER 2 LOW REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>P2&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ’1’ = Bit is set
- ’0’ = Bit is cleared

**bit 7-0**

**P2<7:0>:** Least Significant Bits of Parameter 2

**DMX mode:**
Least Significant Byte of first address of receive block

**LIN Slave mode:**
Number of data bytes to transmit

**DALI mode:**
Least Significant Byte of number of half-bit periods of idle time in Forward Frame detection threshold

**Asynchronous Address mode:**
Receiver address

**Other modes:**
Not used
**REGISTER 31-16: UxP3H: UART PARAMETER 3 HIGH REGISTER**

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th>bit 7-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>P3&lt;8&gt;</td>
<td>P3&lt;8&gt;</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

**bit 7-6** Unimplemented: Read as ‘0’

**bit 0**
- **P3<8>: Most Significant Bit of Parameter 3**
  - DMX mode:
    - Most Significant bit of last address of receive block
  - Other modes:
    - Not used

**REGISTER 31-17: UxP3L: UART PARAMETER 3 LOW REGISTER**

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th>bit 7-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

**bit 7-0**
- **P3<7:0>: Least Significant Bits of Parameter 3**
  - DMX mode:
    - Least Significant Byte of last address of receive block
  - LIN Slave mode:
    - Number of data bytes to receive
  - Asynchronous Address mode:
    - Receiver address mask. Received address is XOR’d with UxP2L then AND’d with UxP3L
    - Match occurs when result is zero
  - Other modes:
    - Not used
**REGISTER 31-18: UxTXCHK: UART TRANSMIT CHECKSUM RESULT REGISTER**

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th>TXCHK&lt;7:0&gt;</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>TXCHK&lt;7:0&gt;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

- **LIN mode and C0EN = 1:**
  - Sum of all transmitted bytes including PID
  - All other modes and C0EN = 1:
    - Sum of all transmitted bytes since last clear
  - Not used

**REGISTER 31-19: UxRXCHK: UART RECEIVE CHECKSUM RESULT REGISTER**

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th>RXCHK&lt;7:0&gt;</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>RXCHK&lt;7:0&gt;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

- **LIN mode and C0EN = 1:**
  - Sum of all received bytes including PID
  - All other modes and C0EN = 1:
    - Sum of all received bytes since last clear
  - Not used
<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>UxCON0</td>
<td>BRGS</td>
<td>ABDEN</td>
<td>TXEN</td>
<td>RXEN</td>
<td>MODE&lt;3:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>483</td>
</tr>
<tr>
<td>UxCON1</td>
<td>ON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WUE</td>
<td>RXBIMD</td>
<td>—</td>
<td>BRKOV R</td>
<td>SENDB</td>
</tr>
<tr>
<td>UxCON2</td>
<td>RUNOVF</td>
<td>RXPOL</td>
<td>STP&lt;1:0&gt;</td>
<td>COEN</td>
<td>TXPOL</td>
<td>FLO&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>485</td>
</tr>
<tr>
<td>UxERRIR</td>
<td>TXMTIF</td>
<td>PERIF</td>
<td>ABDOVF</td>
<td>CERIF</td>
<td>FERIF</td>
<td>RXBKIF</td>
<td>RXFOIF</td>
<td>TXCIF</td>
<td>486</td>
</tr>
<tr>
<td>UxERRIE</td>
<td>TXMTIE</td>
<td>PERIE</td>
<td>ABDOVE</td>
<td>CERIE</td>
<td>FERIE;</td>
<td>RXBKIE</td>
<td>RXFOIE</td>
<td>TXCIE</td>
<td>487</td>
</tr>
<tr>
<td>UxUIR</td>
<td>WUIF</td>
<td>ABDIF</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ABDIE</td>
<td>—</td>
<td>—</td>
<td>488</td>
</tr>
<tr>
<td>UxFIFO</td>
<td>TXWRE</td>
<td>STPMD</td>
<td>TXBE</td>
<td>TXBF</td>
<td>RXIDL</td>
<td>XON</td>
<td>RXBE</td>
<td>RXBF</td>
<td>489</td>
</tr>
<tr>
<td>UxBRGL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>490</td>
</tr>
<tr>
<td>UxBRGH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>490</td>
</tr>
<tr>
<td>UxRXB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RXB&lt;7:0&gt;</td>
<td>—</td>
<td>—</td>
<td>491</td>
</tr>
<tr>
<td>UxTXB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TXB&lt;7:0&gt;</td>
<td>—</td>
<td>—</td>
<td>491</td>
</tr>
<tr>
<td>UxP1H</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>492</td>
</tr>
<tr>
<td>UxP1L</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>P1&lt;8&gt;</td>
<td>492</td>
</tr>
<tr>
<td>UxP2H</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>493</td>
</tr>
<tr>
<td>UxP2L</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>P2&lt;8&gt;</td>
<td>493</td>
</tr>
<tr>
<td>UxP3H</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>494</td>
</tr>
<tr>
<td>UxP3L</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>P3&lt;8&gt;</td>
<td>494</td>
</tr>
<tr>
<td>UxTXCHK</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TXCHK&lt;7:0&gt;</td>
<td>—</td>
<td>—</td>
<td>495</td>
</tr>
<tr>
<td>UxRXCHK</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RXCHK&lt;7:0&gt;</td>
<td>—</td>
<td>—</td>
<td>495</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented, read as ‘0’; Shaded cells are unused by the UART module.
32.0 SERIAL PERIPHERAL INTERFACE (SPI) MODULE

32.1 SPI Module Overview

The SPI (Serial Peripheral Interface) module is a synchronous serial data communication bus that operates in Full-Duplex mode. Devices communicate in a master/slave environment where the master device initiates the communication. A slave device is controlled through a Chip Select known as Slave Select. Example slave devices include serial EEPROMs, shift registers, display drivers, A/D converters, or another PIC® device.

The SPI bus specifies four signal connections:

• Serial Clock (SCK)
• Serial Data Out (SDO)
• Serial Data IN (SDI)
• Slave Select (SS)

The SPI interface supports the following modes and features:

• Master mode
• Slave mode
• Clock Polarity and Edge Select
• SDI, SDO, and SS Polarity Control
• Separate Transmit and Receive Enables
• Slave Select Synchronization
• Daisy-chain connection of slave devices
• Separate Transmit and Receive Buffers with 2-byte FIFO and DMA capabilities

Figure 32-1 shows the block diagram of the SPI module.
FIGURE 32-1: SPI MODULE SIMPLIFIED BLOCK DIAGRAM

Data bus

Read

8

SDI

SPIxSDIPPS

Receive Shift Register

SDI

SPIxSDIPPS

Receive FIFO
(2 deep)

Transmit FIFO
(2 deep)

8

Write

SDO

SPIxSSPPS

SS(out)

SSP

SCK(in)

SPIxSCKPPS

SCK(out)

SCK Generator

CLKSEL<3:0>

SPIxBAUD

MST

SSET

RXR

TXR

SPI Control Module
and Transfer Counter

Note 1: If TXR=1 and the transmit FIFO is empty, the previous value of the receive shift register will be sent to the transmit serializer.
The SPI transmit output (SDO_out) is available to the remappable PPS SDO pin and internally to the following peripherals:

- Configurable Logic Cell (CLC)
- Data Signal Modulator (DSM)

The SPI bus typically operates with a single master device and one or more slave devices. When multiple slave devices are used, an independent Slave Select connection is required from the master device to each slave device.

The master selects only one slave at a time. Most slave devices have tri-state outputs so their output signal appears disconnected from the bus when they are not selected.

Transmissions typically involve shift registers, eight bits in size, one in the master and one in the slave. With either the master or the slave device, data is always shifted out one bit at a time, with the Most Significant bit (MSb) shifted out first. At the same time, a new bit is shifted into the device. Unlike older Microchip devices, the SPI on the PIC18(L)F2X/4X/5XK42 contains two separate registers for incoming and outgoing data. Both registers also have 2-byte FIFO buffers and allow for DMA bus connections.

Figure 32-2 shows a typical connection between two PIC18F2X/4XK42 devices configured as master and slave devices.

Data is shifted out of the transmit FIFO on the programmed clock edge and into the receive shift register on the opposite edge of the clock.

The master device transmits information on its SDO output pin which is connected to, and received by, the slave’s SDI input pin. The slave device transmits information on its SDO output pin, which is connected to, and received by, the master’s SDI input pin.

The master device sends out the clock signal. Both the master and the slave devices should be configured for the same clock polarity.

During each SPI clock cycle, a full-duplex data transmission occurs. This means that while the master device is sending out the MSb from its output register (on its SDO pin) and the slave device is reading this bit and saving as the LSB of its input register, that the slave device is also sending out the MSb from its shift register (on its SDO pin) and the master device is reading this bit and saving it as the LSB of its input register.

After eight bits have been shifted out, the master and slave have exchanged register values and stored the incoming data into the receiver FIFOs.

If there is more data to exchange, the registers are loaded with new data and the process repeats itself.

Whether the data is meaningful or not (dummy data) depends on the application software. This leads to three scenarios for data transmission:

- Master sends useful data and slave sends dummy data
- Master sends useful data and slave sends useful data
- Master sends dummy data and slave sends useful data

In this particular SPI module, dummy data may be sent without software involvement, by clearing either the RXR bit (for receiving dummy data) or the TXR bit (for sending dummy data) (see Table 32-1 as well as Section 32.5 “Master mode” and Section 32.6 “Slave Mode” for further TXR/RXR setting details).

This SPI module can send transmissions of any number of bits, and can send information in segments of varying size (from 1-8 bits in width). As such, transmissions may involve any number of clock cycles, depending on the amount of data to be transmitted.

When there is no more data to be transmitted, the master stops sending the clock signal and deselects the slave.

Every slave device connected to the bus that has not been selected through its Slave Select line disregards the clock and transmission signals and does not transmit out any data of its own.
FIGURE 32-2: SPI MASTER/SLAVE CONNECTION WITH FIFOs

Note 1: In some modes, if the Transmit FIFO is empty, the most recently received byte of data will be transmitted.

Note 2: This diagram assumes that the LSBF bit is cleared (communications are MSb-first). If LSBF is set, the communications will be LSb-first.
32.2 SPI REGISTERS

- SPI Interrupt Flag Register (SPIxINTF)
- SPI Interrupt Enable Register (SPIxINTE)
- SPI Byte Count High and Low Registers (SPIxTCTH/L)
- SPI Bit Count Register (SPIxTWIDTH)
- SPI Baud Rate Register (SPIxBAUD)
- SPI Control Register 0 (SPIxCON0)
- SPI Control Register 1 (SPIxCON1)
- SPI Control Register 2 (SPIxCON2)
- SPI FIFO Status Register (SPIxSTATUS)
- SPI Receiver Buffer Register (SPIxRB)
- SPI Transmit Buffer Register (SPIxB)
- SPI Clock Select Register (SPIxCLKSEL)

SPIxCON0, SPIxCON1, and SPIxCON2 are control registers for the SPI module.

SPIxSTATUS contains several Status bits that indicate the status of both the SPI module and the receive and transmit FIFOs.

SPIxBAUD and SPIxCLKSEL control the baud rate generator of the SPI module when in Master mode. The SPIxCLKSEL selects the clock source that is used. The SPIxBAUD configures the clock divider used on that clock. More information on the baud rate generator is available in Section 32.5.6 “Master Mode SPI Clock Configuration”.

SPIxTxB and SPIxRxB are the transmit and receive buffer registers used to send and receive data on the SPI bus. They both offer indirect access to shift registers that are used for shifting the data in and out. Both registers access the two-byte FIFOs, allowing for multiple transmissions/receptions to be stored between software transfers the data.

The SPIxTCTH:L register pair either count or control the number of bits or bytes in a data transfer. When BMODE = 1, the SPIxTCT value signifies bytes and the SPIxTWIDTH value signifies the number of bits in a byte. When BMODE = 0, the SPIxTCT value is concatenated with the SPIxTWIDTH register to signify bits. In Master Receive-only mode (TXR = 0 and RXR = 1), the data transfer is initiated by writing SPIxTCT with the desired bit or byte value to transfer. In Master Transmit mode (TXR = 1), the data transfer is initiated by writing the SPIxTxB register, in which case the SPIxTCT is a down counter for the bits or bytes transferred.

The SPIxINTF and SPIxINTE are the flags and enables, respectively, for SPI-specific interrupts. They are tied to the SPIxIF flag and SPIxIE enable in the PIR and PIE registers, which is triggered when any interrupt contained in the SPIxINTF/SPIxINTE registers is triggered. The PIR/PIE registers also contain SPIxTXIF/SPIxTXIE bits, which are the interrupt flag and enable for the SPI Transmit Interrupt, as well as the SPIxRXIF/SPIxRXIE bits, which are the interrupt flag and enable for the SPI Receive Interrupt.

32.3 SPI MODE OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SPIxCON0<2:0>, SPIxCON1<7:4>, SPIxCON1<2:0>, and SPIxCON2<2:0>). These control bits allow the following to be specified:
- Master mode (SCK is the clock output)
- Slave mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Input, Output, and Slave Select Polarity
- Data Input Sample Phase (middle or end of data output time)
- Clock Edge (output data on first/second edge of SCK)
- Clock Rate (Master mode only)
- Slave Select Mode (Master or Slave mode)
- MSB-First or LSB-First
- Receive/Transmit Modes
  - Full-duplex
  - Receive-without-transmit
  - Transmit-without-receive
- Transfer Counter Mode (Transmit-without-receive mode)
32.3.1 ENABLING AND DISABLING THE SPI MODULE

To enable the serial peripheral, the SPI enable bit (EN in SPIxCON0) must be set. To reset or reconfigure SPI mode, clear the EN bit, re-initialize the SSPxCONx registers and then set the EN bit. Setting the EN bit enables the SPI inputs and outputs: SDI, SDO, SCK(out), SCK(in), SS(out), and SS(in). All of these inputs and outputs are steered by PPS, and thus must have their functions properly mapped to device pins to function (see Section 17.0 “Peripheral Pin Select (PPS) Module”). In addition, SS(out) and SCK(out) must have the pins they are steered to set as outputs (TRIS bits must be ‘0’) in order to properly output. Clearing the TRIS bit of the SDO pin will cause the SPI module to always control that pin, but is not necessary for SDO functionality. (see Section 32.3.5 “Input and Output Polarity Bits”). Configurations selected by the following registers should not be changed while the EN bit is set:

- SPIxBAUD
- SPIxCON1
- SPIxCON0 (except to clear the EN bit)

Clearing the EN bit aborts any transmissions in progress, disabling the setting of interrupt flags by hardware, and resets the FIFO occupancy (see Section 32.3.3 “Transmit and Receive FIFOs” for more FIFO details).

32.3.2 BUSY BIT

While a data transfer is in progress, the SPI module sets the BUSY bit of SPIxCON2. This bit can be polled by the user to determine the current status of the SPI module, and to know when a communication is complete. The following registers/bits should not be written by software while the BUSY bit is set:

- SPIxTCNTH/L
- SPIxTWIDTH
- SPIxCON2
- The CLRBF bit of SPIxSTATUS

Note: It is also not recommended to read SPIx-TCNTH/L while the BUSY bit is set, as the value in the registers may not be a reliable indicator of the Transfer Counter. Use the Transfer Count Zero Interrupt Flag (the TCZIF bit of SPIxINTF) to accurately determine that the Transfer Counter has reached zero.

32.3.3 TRANSMIT AND RECEIVE FIFOS

The transmission and reception of data from the SPI module is handled by two FIFOs, one for reception and one for transmission (addressed by the SFRs SPIxRXB and SPIxTXB, respectively). The TXFIFO is written by software and is read by the SPI module to shift the data onto the SDO pin. The RXFIFO is written by the SPI module as it shifts in the data from the SDI pin and is read by software. Setting the CLRBF bit of SPIxSTATUS resets the occupancy for both FIFOs, emptying both buffers. The FIFOs are also reset by disabling the SPI module.

Note: TXFIFO occupancy and RXFIFO occupancy simply refer to the number of bytes that are currently being stored in each FIFO. These values are used in this chapter to illustrate the function of these FIFOs and are not directly accessible through software.

The SPIxRXB register addresses the receive FIFO and is read-only. Reading from this register will read from the first FIFO location that was written to by hardware and decrease the RXFIFO occupancy. If the FIFO is empty, reading from this register will instead return a value of zero and set the RXRE (Receive Buffer Read Error) bit of the SPIxSTATUS register. The RXRE bit must then be cleared in software in order to properly reflect the status of the read error. When RXFIFO is full, the RXBF bit of the SPIxSTATUS register will be set. When the device receives data on the SDI pin, the receive FIFO may be written to by hardware and the occupancy increased, depending on the mode and receiver settings, as summarized in Table 32-1.

The SPIxTXB register addresses the transmit FIFO and is write-only. Writing to the register will write to the first empty FIFO location and increase the occupancy. If the FIFO is full, writing to this register will not affect the data and will set the TXWE bit of the SPIxSTATUS register. When the TXFIFO is empty, the TXBE bit of SPIxSTATUS will be set. When a data transfer occurs, data may be read from the first FIFO location written to and the occupancy decreases, depending on mode and transmitter settings, as summarized in Table 32-1 and Section 32.6.1 “Slave Mode Transmit options”.

32.3.4 LSB VS. MSB-FIRST OPERATION

Typically, SPI communication is output Most-Significant bit first, but some devices/buses may not conform to this standard. In this case, the LSBF bit may be used to alter the order in which bits are shifted out during the data exchange. In both Master and Slave mode, the LSBF bit of SPIxCON0 controls if data is shifted MSb or LSb first. Clearing the bit (default) configures the data to transfer MSb first, which is traditional SPI operation, while setting the bit configures the data to transfer LSb first.
32.3.5  INPUT AND OUTPUT POLARITY BITS

SPIxCON1 has three bits that control the polarity of the SPI inputs and outputs. The SDIP bit controls the polarity of the SDI input, the SDOP bit controls the polarity of the SDO output, and the SSP bit controls the polarity of both the slave SS input and the master SS output. For all three bits, when the bit is clear, the input or output is active-high, and when the bit is set, the input or output is active-low. When the EN bit of SPIxCON0 is cleared, SS(out) and SCK(out) both revert to the inactive state dictated by their polarity bits. The SDO output state when the EN bit of SPIxCON0 is cleared is determined by several factors.

• When the associated TRIS bit for the SDO pin is cleared, and the SPI goes Idle after a transmission, the SDO output will remain at the last bit level. The SDO pin will revert to the Idle state if EN is cleared.

• When the associated TRIS bit for the SDO pin is set, behavior varies in Slave and Master mode.
  - In Slave mode, the SDO pin tri-states when:
    - Slave Select is inactive,
    - the EN bit of SPIxCON0 is cleared, or when
    - the TXR bit of SPIxCON2 is cleared.
  - In Master mode, the SDO pin tri-states when TXR = 0. When TXR = 1 and the SPI goes Idle after a transmission, the SDO output will remain at the last bit level. The SDO pin will revert to the Idle state if EN is cleared.

32.4  Transfer Counter

In all Master modes, the transfer counter can be used to determine how many data transfers the SPI will send/receive. The transfer counter is comprised of the SPIxTCTH/L set of registers, and is also partially controlled by the SPIxTWIDTH register. The Transfer Counter has two primary modes, determined by the BMODE bit of the SPIxCON0 register. Each mode uses the SPIxTCTH/L and SPIxTWIDTH registers to determine the number and size of the transfers. In both modes, when the transfer counter reaches zero, the TCZIF interrupt flag is set.

Note: When BMODE = 1 in all Master modes (and at all times in Slave modes), the Transfer Counter will still decrement as transfers occur and can be used to count the number of messages sent/received, as well as to control SS(out) and to trigger TCZIF. Also when BMODE = 1, the SPIxTWIDTH register can be used in Master and Slave modes to determine the size of messages sent and received by the SPI, even if the Transfer Counter is not being actively used to control the number of messages being sent/received by the SPI module.

32.4.1  TOTAL BIT COUNT MODE
(BMODE = 0)

In this mode, SPIxTCTH/L and SPIxTWIDTH are concatenated to determine the total number of bits to be transferred. These bits will be loaded from/into the transmit/receive FIFOs in 8-bit increments and the transfer counter will be decremented by eight until the total number of remaining bits is less than eight. If there are any remaining bits (SPIxTWIDTH ≠ 0), the transmit FIFO will send out one final message with any extra bits greater than the remainder ignored. The SPIxTWIDTH is the remaining bit count but the value does not change as it does for the SPIxTCT value. Similarly, the receiver will load a final byte into the receiver FIFO, and pad the extra bits with zeros. The LSBF bit of SPIxCON0 determines whether the Most Significant or Least Significant bits of this final byte are ignored/padded. For example, when LSBF = 0 and the final transfer contains only two bits then if the last byte sent was 5Fh then the RXB of the receiver will contain 40h which are the two MSbits of the final byte padded with zeros in the LSbits.

In this mode, the SPI master will only transmit messages when the SPIxTCT value is greater than zero, regardless of TXR and RXR settings. In Master Transmit mode, the transfer starts with the data write to the SPIxTXB register or the count value written to the SPIxTCTL register, which ever occurs last. In Master Receive-only mode, the transfer clocks start when the SPIxTCTL value is written. Transfer clocks are suspended when the receive FIFO is full and resume as the FIFO is read.
32.4.2 VARIABLE TRANSFER SIZE MODE (BMODE = 1)

In this mode, SPIxTWIDTH specifies the width of every individual piece of the data transfer in bits. SPIxTCTL specifies the number of transfers of this bit length. If SPIxTWIDTH = 0, each piece is a full byte of data. If SPIxTWIDTH ≠ 0, then only the specified number of bits from the transmit FIFO are shifted out, with the unused bits ignored. Received data is padded with zeros in the unused bit areas when transferred into the receive FIFO. The LSBF bit of SPIxCON0 determines whether the Most Significant or Least Significant bits of the transfers are ignored/padded. In this mode, the transfer counter being zero only stops messages from being sent/received when in “Receive only” mode.

Note: With BMODE = 1, it is possible for the transfer counter (SPIxTCTL) to decrement below zero, although when in “Receive Only” Master mode, transfer clocks will cease when the transfer counter reaches zero.

32.4.3 TRANSFER COUNTER IN SLAVE MODE

In Slave mode, the transfer counter will still decrement as data is shifted in and out of the SPI module, but it will not control data transfers. In addition, in Slave mode, the BMODE bit along with the transfer counter is used to determine when the device should look for Slave Select faults. If BMODE = 0, the SSFLT bit will be set if Slave Select transitions from its active to inactive state during bytes of data, as well as if it transitions before the last bit sent during the final byte (if SPIxTWIDTH ≠ 0). If BMODE=1, the SSFLT bit will be set if Slave Select transitions from its active to inactive state before the final bit of each individual transfer is completed. Note that SSFLT does not have an associated interrupt, so it should be checked in software. An ideal time to do this is when the End of Slave Select Interrupt (EOSIF) is triggered (see Section 32.8.3.3 “Start of Slave Select and End of Slave Select Interrupts”).

32.5 Master mode

In Master mode, the device controls the SCK line, and as such, initiates data transfers and determines when any slaves broadcast data onto the SPI bus.

Master mode of this device can be configured in four different modes, configured by the TXR and RXR bits:
- Full-Duplex mode
- Receive Only mode
- Transmit Only mode
- Transfer Off mode

The modes are illustrated in Table 32-1, below:

<table>
<thead>
<tr>
<th>Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full-Duplex</td>
<td>Initiates both data transfers in both directions</td>
</tr>
<tr>
<td>Receive Only</td>
<td>Only initiates data transfer in receive direction</td>
</tr>
<tr>
<td>Transmit Only</td>
<td>Only initiates data transfer in transmit direction</td>
</tr>
<tr>
<td>Transfer Off</td>
<td>Disables data transfer initiation</td>
</tr>
</tbody>
</table>

Note: With BMODE = 1, it is possible for the transfer counter (SPIxTCTH/L) to decrement below zero, although when in “Receive Only” Master mode, transfer clocks will cease when the transfer counter reaches zero.
### TABLE 32-1: MASTER MODE TXR/RXR SETTINGS

<table>
<thead>
<tr>
<th>TXR = 1</th>
<th>TXR = 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXR = 1</td>
<td>Full-Duplex mode</td>
</tr>
<tr>
<td></td>
<td>If BMODE = 1, transfer when RxFIFO is not full and TxFIFO is not empty</td>
</tr>
<tr>
<td></td>
<td>If BMODE = 0, Transfer when RXFIFO is not full, TXFIFO is not empty, and the Transfer Counter is non-zero</td>
</tr>
<tr>
<td></td>
<td>Receive Only mode</td>
</tr>
<tr>
<td></td>
<td>Transfer when RxFIFO is not full and the Transfer Counter is non-zero</td>
</tr>
<tr>
<td></td>
<td>Transmitted data is either the top of the FIFO or the most recently received data</td>
</tr>
<tr>
<td>RXR = 0</td>
<td>Transmit Only mode</td>
</tr>
<tr>
<td></td>
<td>If BMODE = 1, transfer when TxFIFO is not empty</td>
</tr>
<tr>
<td></td>
<td>If BMODE = 0, Transfer when TXFIFO is not empty and the Transfer Counter is non-zero</td>
</tr>
<tr>
<td></td>
<td>Received data is not stored</td>
</tr>
<tr>
<td></td>
<td>No Transfers</td>
</tr>
</tbody>
</table>

#### 32.5.1 FULL-DUPLEX MODE

When both TXR and RXR are set, the SPI master is in Full-Duplex mode. In this mode, data transfer triggering is affected by the BMODE bit of SPIxCON0.

When BMODE = 1, data transfers will occur whenever both the RXFIFO is not full and there is data present in the TXFIFO. In practice, as long as the RXFIFO is not full, data will be transmitted/received as soon as the SPIxTxB register is written to, matching functionality of SPI (MSSP) modules on older 8-bit Microchip devices. The SPIxTCNT will decrement with each transfer. However, when SPIxTCNT is zero the next transfer is not inhibited and the corresponding SPIxTCNT decrement will cause the count to roll over to the maximum value. Figure 32-3 shows an example of a communication using this mode.

When BMODE = 0, the transfer counter (SPIxTCNTH/ SPIxTCNTL) must also be written to before transfers will occur, and transfers will cease when the transfer counter reaches ‘0’. For example, if SPIxTXB is written twice and then SPIxTCTL is written with ‘3’ then the transfer will start with the SPIxTCTL write. The two bytes in the TXFIFO will be sent after which the transfer will suspend until the third and last byte is written to SPIxTXB.
FIGURE 32-3: SPI MASTER OPERATION – DATA EXCHANGE, TXR/RXR = 1/1

32.5.2 TRANSMIT ONLY MODE

When TXR is set and RXR is clear, the SPI master is in Transmit Only mode. In this mode, data transfer triggering is affected by the BMODE bit of SPIxCON0.

When BMODE = 1, data transfers will occur whenever TXFIFO is not empty. Data will be transmitted as soon as the TXFIFO register is written to, matching functionality of SPI (MSSP) modules on previous 8-bit Microchip devices. The SPIxTCNT will decrement with each transfer. However, when SPIxTCNT is zero the next transfer is not inhibited and the corresponding SPIxTCNT decrement will cause the count to roll over to the maximum value. Any data received in this mode is not stored in RXFIFO. Figure 32-4 shows an example of sending a command and then sending a byte of data, using this mode.

When BMODE = 0, the transfer counter (SPIxTCNTH/L) must also be written to before transfers will occur, and transfers will cease when the transfer counter reaches '0'.

For example, if SPIxTXB is written twice and then SPIxTCTL is written with '3', the transfer will start with the SPIxTCTL write. The two bytes in the TXFIFO will be sent after which the transfer will suspend until the third and last byte is written to SPIxTXB.

Note: 1. SS(out) is not shown on this diagram
2. SPIxTCNT write is optional TXR/RXR = 1/1 and BMODE=1. If BMODE=0, a write to SPIxTCNT is required to start transmission; TCZIF signals the end of the transmission.
3. Transmission gap occurs while waiting for transmitter data.
FIGURE 32-4: SPI MASTER OPERATION, COMMAND+WRITE DATA, TXR/RXR=1/0

Note 1. SS(out) is not shown.
2. The byte counter is optional when TXR/RXR = 1/0.
3. After the command bytes, wait for SRMTIF before loading SPIxBYTESL otherwise the command bytes would decrement BYTES. Alternatively, load BC = 5 and count the command bytes also; TCZIF signals the end of the transmission.
4. Transmit data interrupt handler (or DMA) must write only the bytes necessary; the byte counter is not available as an indicator.
5. Reading the RXFIFO is not required because RXR = 0.
### 32.5.3 RECEIVE ONLY MODE

When RXR is set and TXR is clear, the SPI master is in Receive Only mode. In this mode, data transfers when the RXFIFO is not full and the Transfer Counter is non-zero. In this mode, writing a value to SPIxTCNTL will start the clocks for transfer. The clocks will suspend while the RXFIFO is full and cease when the SPIxTCNT reaches zero (see Section 32.4 “Transfer Counter”). If there is any data in the TXFIFO, the first data written to the TXFIFO will be transmitted on each data exchange, although the TXFIFO occupancy will not change, meaning that the same message will be sent on each transmission. If there is no data in the TXFIFO, the most recently received data will instead be transmitted. Figure 32-5 shows an example of sending a command using Section 32.5.2 “Transmit Only Mode” and then receiving a byte of data using this mode.

### 32.5.4 TRANSFER OFF MODE

When both TXR and RXR are cleared, the SPI master is in Transfer Off mode. In this mode, SCK will not toggle and no data is exchanged. However, writes to SPIxTXB will be transferred to the TXFIFO which will be transmitted if the TXR bit is set.

---

**FIGURE 32-5:** SPI MASTER OPERATION, COMMAND+READ DATA, TXR/RXR=0/1

Note 2

1. SS(out) is not shown
2. Software must wait for shift-register empty (SRMTIF) before changing TXR, RXR, BYTES and BITS controls.

This is not considered an imposition in this case, because the slave probably needs time to load output data (see also Figure 4-14).
32.5.5 MASTER MODE SLAVE SELECT CONTROL

32.5.5.1 Hardware Slave Select Control

This SPI module allows for direct hardware control of a Slave Select output. The Slave Select output SS(out) is controlled both directly, through the SSET bit of SPIxCON2, as well indirectly by the hardware while the transfer counter is non-zero (see Section 32.4 “Transfer Counter”). SS(out) is steered by the PPS registers to pins (see Section 17.2 “PPS Outputs”) and its polarity is controlled by the SSP bit of SPIxCON1. Setting the SSET bit will also assert SS(out). Clearing the SSET bit will leave SS(out) to be controlled by the Transfer Counter. When the Transfer Counter is loaded, the SPI module will automatically assert the SS. When the Transfer Counter decrements to zero, the SPI module will deassert SS either one baud period after the final SCK pulse of the final transfer (if CKE/SMP = 0/1) or one half baud period otherwise (see Figure 32-6).

FIGURE 32-6: SPI MASTER SS OPERATION- CKE = 0, BMODE = 1, TCWIDTH = 0, SSP = 0

32.5.5.2 Software Slave Select Control

Slave Select can also be controlled through software via a general purpose I/O pin. In this case, ensure that the pin in question is configured as a GPIO through PPS (see Section 17.2 “PPS Outputs”), and ensure that the pin is set as an output (clear the appropriate bit in the appropriate TRIS register). In this case, SSET will not affect the Slave Select, the Transfer Counter will not automatically control the Slave Select output, and all setting and clearing of the Slave Select output line must be directly controlled by software.

Note: 1. SDO bit number illustrates the transmitted bit number, and is not intended to imply SDO (out) tristate operation. 2. Assumes SPIxTXB holds data when SPIxTCNTL is written.
32.5.6  MASTER MODE SPI CLOCK CONFIGURATION

32.5.6.1  SPI Clock Selection

The clock source for SPI Master modes is selected by the SPIxCLK register. Selections include the following:

- FOSC
- HFINTOSC
- CLKREF
- Timer0_overflow
- Timer2_Postscaled
- Timer4_Postscaled
- Timer6_Postscaled
- SMT_match

The SPIxBAUD register allows for dividing this clock. The frequency of the SCK output is defined by Equation 32-1:

\[
F_{BAUD} = \frac{F_{CSSEL}}{\left(2 \cdot (BAUD + 1)\right)}
\]

where \(F_{BAUD}\) is the baud rate frequency output on the SCK pin, \(F_{CSSEL}\) is the frequency of the input clock selected by the SPIxCLK register, and BAUD is the value contained in the SPIxBAUD register.

32.5.6.2  CKE, CKP and SMP

The CKP, CKE, and SMP bits control the relationship between the SCK clock output, SDO output data changes, and SDI input data sampling. The bit functions are as follows:

- CKP - SCK output polarity
- CKE - SDO output change relative to the SCK clock
- SMP - SDI input sampling relative to the clock edges

The CKE bit, when set, inverts the low Idle state of the SCK output to a high Idle state.

Figure 32-7 through Figure 32-10 illustrate the eight possible combinations of the CKP, CKE, and SMP bit selections.

When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. When the CKE bit is cleared, the SDO data is undefined prior to the first SCK edge.

**Note:** All timing diagrams assume the LSBF bit of SPIxCON0 is cleared.
FIGURE 32-7: CLOCKING DETAIL – MASTER MODE, CKE/SMP = 0/0

FIGURE 32-8: CLOCKING DETAIL – MASTER MODE, CKE/SMP = 1/1
32.5.6.3 SCK Start-Up Delay

When starting an SPI data exchange, the master device sets the SS output (either through hardware or software) and then triggers the module to send data. These data triggers are synchronized to the clock selected by the SPIxCLK register before the first SCK pulse appears, usually requiring one or two clocks of the selected clock.

The SPI module includes synchronization delays on SCK generation specifically designed to ensure that the Slave Select output timing is correct, without requiring precision software timing loops.

When the value of the SPIxBAUD register is a small number (indicating higher SCK frequencies), the synchronization delay can be relatively long between setting SS and the first SCK. With larger values of SPIxBAUD (indicating lower SCK frequencies), this delay is much smaller and the first SCK can appear relatively quickly after SS is set.

By default, the SPI module inserts a ½ baud delay (half of the period of the clock selected by the SPIxCLK register) before the first SCK pulse. This allows for systems with a high SPIxBAUD value to have extra set-up time before the first clock. Setting the FST bit in SPIxCON1 removes this additional delay, allowing systems with low SPIxBAUD values (and thus, long synchronization delays) to forego this unnecessary extra delay.
32.6 Slave Mode

32.6.1 SLAVE MODE TRANSMIT OPTIONS

The SDO output of the SPI module in Slave mode is controlled by the TXR bit of SPIxCON2, the TRIS bit associated with the SDO pin, the Slave Select input, and the current state of the TXFIFO. This control is summarized in Table 32-2. In this table, TRISxn refers to the bit in the TRIS register corresponding to the pin that SDO has been assigned with PPS, TXR is the Transmit Data Required Control bit of SPIxCON2, SS is the state of the Slave Select input, and TXBE is the TXFIFO Buffer Empty bit of SPIxSTATUS.

32.6.1.1 SDO Drive/Tri-state

The TRIS bit associated with the SDO pin controls whether the SDO pin will tri-state. When this TRIS bit is cleared, the pin will always be driving to a level, even when the SPI module is inactive. When the SPI module is inactive (either due to the master not clocking the SCK line or the SS being false), the SDO pin will be driven to the value of the LAT bit associated with the SDO pin. When the SPI module is active, its output is determined by both TXR and whether there is data in the TXFIFO.

When the TRIS bit associated with the SDO pin is set, the pin will only have an output level driven to it when TXR = 1 and the Slave Select input is true. In all other cases, the pin will be tri-stated.

32.6.1.2 SDO Output Data

The TXR bit controls the nature of the data that is transmitted in Slave mode. When TXR is set, transmitted data is taken from the TXFIFO. If the FIFO is empty, the most recently received data will be transmitted and the TXUIF flag will be set to indicate that a transmit FIFO underflow has occurred.

When TXR is cleared, the data will be taken from the TXFIFO, and the TXFIFO occupancy will not decrease. If the TXFIFO is empty, the most recently received data will be transmitted, and the TXUIF bit will not be set. However, if the TRIS bit associated with the SDO pin is set, clearing the TXR bit will cause the SPI module to not output any data to the SDO pin.

<table>
<thead>
<tr>
<th>TRISxn(1)</th>
<th>TXR</th>
<th>SS</th>
<th>TXBE</th>
<th>SDO State</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>0</td>
<td>FALSE</td>
<td>0</td>
<td>Drives state determined by LATxn(2)</td>
</tr>
<tr>
<td>00</td>
<td>0</td>
<td>FALSE</td>
<td>1</td>
<td>Drives state determined by LATxn(2)</td>
</tr>
<tr>
<td>00</td>
<td>0</td>
<td>TRUE</td>
<td>0</td>
<td>Outputs the oldest byte in the TXFIFO Does not remove data from the TXFIFO</td>
</tr>
<tr>
<td>00</td>
<td>0</td>
<td>TRUE</td>
<td>1</td>
<td>Outputs the most recently received byte</td>
</tr>
<tr>
<td>00</td>
<td>1</td>
<td>FALSE</td>
<td>0</td>
<td>Drives state determined by LATxn(2)</td>
</tr>
<tr>
<td>00</td>
<td>1</td>
<td>FALSE</td>
<td>1</td>
<td>Drives state determined by LATxn(2)</td>
</tr>
<tr>
<td>01</td>
<td>1</td>
<td>TRUE</td>
<td>0</td>
<td>Outputs the oldest byte in the TXFIFO Removes transmitted byte from the TXFIFO Decrements occupancy of TXFIFO</td>
</tr>
<tr>
<td>01</td>
<td>1</td>
<td>TRUE</td>
<td>1</td>
<td>Outputs the most recently received byte Sets the TXUIF bit of SPIxINTF</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>FALSE</td>
<td>0</td>
<td>Tri-stated</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>FALSE</td>
<td>1</td>
<td>Tri-stated</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>TRUE</td>
<td>0</td>
<td>Tri-stated</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>TRUE</td>
<td>1</td>
<td>Tri-stated</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>FALSE</td>
<td>0</td>
<td>Tri-stated</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>FALSE</td>
<td>1</td>
<td>Tri-stated</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>TRUE</td>
<td>0</td>
<td>Outputs the oldest byte in the TXFIFO Removes transmitted byte from the TXFIFO Decrements occupancy of TXFIFO</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>TRUE</td>
<td>1</td>
<td>Outputs the most recently received byte Sets the TXUIF bit of SPIxINTF</td>
</tr>
</tbody>
</table>

Note 1: TRISxn is the bit in the TRISx register corresponding to the pin that SDO has been assigned with PPS.

2: LATxn is the bit in the LATx register corresponding to the pin that SDO has been assigned with PPS.
32.6.2 SLAVE MODE RECEIVE OPTIONS

The RXR bit controls the nature of receptions in Slave mode. When RXR is set, the SDI input data will be stored in the RXFIFO if it is not full. If the RXFIFO is full, the RXOIF bit will be set to indicate an RXFIFO overflow error and the data is discarded. When RXR is cleared, all received data will be ignored and not stored in the RXFIFO (although it may still be used for transmission if TXFIFO is empty). Figure 32-11 shows a typical Slave mode communication, showing a case where the master writes two then three bytes, showing interrupts as well as the behavior of the transfer counter in Slave mode (see Section 32.4.3 “Transfer Counter in Slave mode” for more details on the transfer counter in Slave mode as well as Section 32.8 “SPI Interrupts” for more information on interrupts).

**FIGURE 32-11: SPI SLAVE MODE OPERATION – INTERRUPT-DRIVEN, MASTER WRITES 2+3 BYTES**

![Diagram showing SPI Slave mode operation with interrupts and timing details](image-url)

Note: 1. This delay is exaggerated for illustration, and can be as short as 1/2 bit period.
2. If the device is sleeping, SOSIF will wake it up for interrupt service.
3. Setting SPIxTCNTL is optional in this example, otherwise it will count -3, -4, -5, and TCZIF will not occur.
32.6.3 SLAVE MODE SLAVE SELECT

In Slave mode, an external Slave Select Signal can be used to synchronize communication with the master device. The Slave Select line is held in its inactive state (high by default) until the master device is ready to communicate. When the Slave Select transitions to its active state, the slave knows that a new transmission is starting.

When the Slave Select goes false at the end of the transmission the receive function of the selected SPI slave device returns to the inactive state. The slave is then ready to receive a new transmission when the Slave Select goes True again.

The Slave Select signal is received on the SSS input pin. This pin is remappable with the SPIxSSPPS register (see Section 17.1 “PPS Inputs”). When the input on this pin is true, transmission and reception are enabled, and the SDO pin is driven. When the input on this pin is false, the SDO pin is either tri-stated (if the TRIS bit associated with the SDO pin is set) or driven to the value of the LAT bit associated with the SDO pin (if the TRIS bit associated with the SDO pin is cleared). In addition, the SCK input is ignored.

If the SS input goes False, while a data transfer is still in progress, it is considered a Slave Select fault. The SSFLT bit of SPIxCON2 indicates whether such an event has occurred. The transfer counter value determines the number of bits in a valid data transfer (see Section 32.4 “Transfer Counter” for more details).

The Slave Select polarity is controlled by the SSP bit of SPIxCON1. When SSP is set (its default state), the Slave Select input is active-low, and when it is cleared, the Slave Select input is active-high.

The Slave Select for the SPI module is controlled by the SSET bit of SPIxCON2. When the bit is cleared (its default state), the Slave Select will act as described above. When the bit is set, the SPI module will behave as if the SS input was always in its active state.

**Note:** When SSET is set, the effective SS(in) signal is always active. Hence, the SSFLT bit may be disregarded.

32.6.4 SLAVE MODE CLOCK CONFIGURATION

In Slave mode, SCK is an input, and must be configured to the same polarity and clock edge as the master device. As in Master mode, the polarity of the clock input is controlled by the CKP bit of SPIxCON1 and the clock edge used for transmitting data is controlled by the CKE bit of SPIxCON1.

32.6.5 DAISY-CHAIN CONFIGURATION

The SPI bus can be connected in a daisy-chain configuration. The first slave output is connected to the second slave input, the second slave output is connected to the third slave input, and so on. The final slave output is connected to the master input. Each slave sends out, during a second group of clock pulses, an exact copy of what was received during the first group of clock pulses. The whole chain acts as one large communication shift register. The daisy-chain feature only requires a single Slave Select line from the master device connected to all slave devices (alternately, the slave devices can be configured to ignore the Slave Select line by setting the SSET bit). In a typical Daisy-Chain configuration, the SCK signal from the master is connected to each of the slave device SCK inputs. However, the SCK input and output are separate signals selected by the PPS control. When the PPS selection is made to configure the SCK input and SCK output on separate pins then, the SCK output will follow the SCK input, allowing for SCK signals to be daisy-chained like the SDO/SDI signals.

Figure 32-12 shows the block diagram of a typical daisy-chain connection, and Figure 32-13 shows the block diagram of a daisy-chain connection possible using this SPI module.

Note: When SSET is set, the effective SS(in) signal is always active. Hence, the SSFLT bit may be disregarded.
FIGURE 32-12: TRADITIONAL SPI DAISY – CHAIN CONNECTION

FIGURE 32-13: SPI DAISY-CHAIN CONNECTION WITH CHAINED SCK
32.7 SPI Operation in Sleep Mode

SPI Master mode will operate in Sleep, provided the clock source selected by SPIxCLK is active in Sleep mode. FIFOs will operate as they would when the part is awake. When TXR = 1, the TXFIFO will need to contain data in order for transfers to take place in Sleep. All interrupts will still set the interrupt flags in Sleep but only enabled interrupts will wake the device from Sleep.

SPI Slave mode will operate in Sleep, because the clock is provided by an external master device. FIFOs will still operate and interrupts will set interrupt flags, and enabled interrupts will wake the device from Sleep.

32.8 SPI Interrupts

There are three top level SPI interrupts in the PIRx register:
- SPI Transmit
- SPI Receive
- SPI Module status

The status interrupts are enabled at the module level in the SPIxINTE register. Only enabled status interrupts will cause the single top level SPIxIF flag to be set.

32.8.1 SPI RECEIVER DATA INTERRUPT

The SPI Receiver Data Interrupt is set when RXFIFO contains data, and is cleared when the RXFIFO is empty. The interrupt flag SPI1RXIF is located in PIRx and the interrupt enable SPI1RXIE is located in PIEX. This interrupt flag is read-only.

32.8.2 SPI TRANSMITTER DATA INTERRUPT

The SPI Transmitter Data Interrupt is set when TXFIFO is not full, and is cleared when the TXFIFO is full. The interrupt flag SPI1TXIF is located in PIRx and the interrupt enable SPI1TXIE is located in PIEX. The interrupt flag is read-only.

32.8.3 SPI MODULE STATUS INTERRUPTS

The SPIxIF flag in the respective PIR register is set when any of the individual status flags in SPIxINTF and their respective SPIxINTE bits are set. In order for the setting of any specific interrupt flag to interrupt normal program flow both the SPIxIE bit as well as the specific bit in SPIxINTE associated with that interrupt must be set.

The Status Interrupts are:
- Shift Register Empty Interrupt
- Transfer Counter is Zero Interrupt
- Start of Slave Select Interrupt
- End of Slave Select Interrupt
- Receiver Overflow Interrupt
- Transmitter Underflow Interrupt
32.8.3.1 Shift Register Empty Interrupt

The Shift Register Empty interrupt flag and enable are the SRMTIF and SRMTIE bits, respectively. This interrupt is only available in Master mode and triggers when a data transfer completes and conditions are not present to start a new transfer, as dictated by the TXR and RXR bits (see Table 32-1 for conditions for starting a new Master mode data transfer with different TXR/RXR settings). This interrupt will be triggered at the end of the last full bit period, after SCK has been low for one ½-baud period. See Figure 32-14 for more details of the timing of this interrupt as well as other interrupts. This bit will not clear itself when the conditions for starting a new transfer occur, and must be cleared in software.

32.8.3.2 Transfer Counter is Zero Interrupt

The transfer counter is zero interrupt flag and enable are the TCZIF and TCZIE bits, respectively. This interrupt will trigger when the transfer counter (defined by BMODE, SPIxTCTH/L and SPIxTWIDTH) decrements from one to zero. See Figure 32-14 for more details on the timing of this interrupt as well as other interrupts. This bit must be cleared in software.

32.8.3.3 Start of Slave Select and End of Slave Select Interrupts

The start of Slave Select interrupt flag and enable are the SOSIF and SOSIE bits, respectively, and the end of Slave Select interrupt flag and enable are similarly designated by the EOSIF and EOSIE bits. These interrupts trigger at the leading and trailing edges of the Slave Select input. Note that the interrupts are active in both master and Slave mode, and will trigger on transitions of the Slave Select input regardless of which mode the SPI is in. In Master mode, PPS should be used to route the Slave Select input to the same pin as the Slave Select output, allowing these interrupts to trigger on changes to the Slave Select output. Also note that in Slave mode, changing the SSET bit can trigger these interrupts, as it changes the effective input value of Slave Select. Both SOSIF and EOSIF must be cleared in software.

Note: The TCZIF flag only indicates that the transfer counter has decremented from one to zero, and may not indicate that the entire data transfer process is complete. Either poll the BUSY bit of SPIxCON2 and wait for it to be cleared or use the Shift Register Empty Interrupt (SRMTIF) to determine if a data transfer is fully complete.

FIGURE 32-14: TRANSFER AND SLAVE SELECT INTERRUPT TIMINGS

Note 1: SRMTIF available only in Master mode
Note 2: Clearing of interrupt flags is shown for illustration; actual interrupt flags must be cleared in software
Note 3: SOSIF and EOSIF are set according to SS(in), even in Master mode.
32.8.3.4 Receiver Overflow and Transmitter Underflow Interrupts

The receiver overflow interrupt triggers if data is received when the RXFIFO is already full and RXR = 1. In this case, the data will be discarded and the RXOIF bit will be set. The receiver overflow interrupt flag is the RXOIF bit of SPIxINTF. The receiver overflow interrupt enable bit is the RXOIE bit of SPIxINTE.

The Transmitter Underflow interrupt flag triggers if a data transfer begins when the TXFIFO is empty and TXR = 1. In this case, the most recently received data will be transmitted and the TXUIF bit will be set. The transmitter underflow interrupt flag is the TXUIF bit of SPIxINTF. The transmitter underflow interrupt enable bit is the TXUIE bit of SPIxINTE.

Both of these interrupts will only occur in Slave mode, as Master mode will not allow the RXFIFO to overflow or the TXFIFO to underflow.
32.9  Register definitions: SPI

REGISTER 32-1:  SPIxINTF: SPI INTERRUPT FLAG REGISTER

<table>
<thead>
<tr>
<th>R/W/HS-0/0</th>
<th>R/W/HS-0/0</th>
<th>R/W/HS-0/0</th>
<th>R/W/HS-0/0</th>
<th>U-0</th>
<th>R/W/HS-0/0</th>
<th>R/W/HS-0/0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRMTIF</td>
<td>TCZIF</td>
<td>SOSIF</td>
<td>EOSIF</td>
<td>—</td>
<td>RXOIF</td>
<td>TXUIF</td>
<td>—</td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 6</td>
<td>bit 5</td>
<td>bit 4</td>
<td>bit 3</td>
<td>bit 2</td>
<td>bit 1</td>
<td>bit 0</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **HS** = Bit can be set by hardware

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Slave mode:</th>
<th>Master mode:</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>SRMTIF: Shift Register Empty Interrupt Flag bit</td>
<td>This bit is ignored</td>
<td>1 = The data transfer is complete 0 = Either no data transfers have occurred or a data transfer is in progress</td>
</tr>
<tr>
<td>6</td>
<td>TCZIF: Transfer Counter is Zero Interrupt Flag bit</td>
<td>1 = The transfer counter (as defined by BMODE in Register 32-7, TCNTH/L, and TWIDTH) has decremented to zero 0 = No interrupt pending</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>SOSIF: Start of Slave Select Interrupt Flag bit</td>
<td>1 = SS(in) transitioned from false to true 0 = No interrupt pending</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>EOSIF: End of Slave Select Interrupt Flag bit</td>
<td>1 = SS(in) transitioned from true to false 0 = No interrupt pending</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Unimplemented: Read as '0'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>RXOIF: Receiver Overflow Interrupt Flag bit</td>
<td>1 = Data transfer completed when RXBF = 1 (edge triggered) and RXR = 1 0 = No interrupt pending</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>TXUIF: Transmitter Underflow Interrupt Flag bit</td>
<td>1 = Slave Data transfer started when TXBE = 1 and TXR = 1 0 = No interrupt pending</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Unimplemented: Read as '0'</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
# REGISTER 32-2: SPIxINTE: SPI INTERRUPT ENABLE REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRMTIE</td>
<td>TCZIE</td>
<td>SOSIE</td>
<td>EOSIE</td>
<td>----</td>
<td>RXOIE</td>
<td>TXUIE</td>
<td>----</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’

- **bit 7**
  - **SRMTIE**: Shift Register Empty Interrupt Enable bit
    - **1** = Enables the Shift Register Empty Interrupt
    - **0** = Disables the Shift Register Empty Interrupt

- **bit 6**
  - **TCZIE**: Transfer Counter is Zero Interrupt Enable bit
    - **1** = Enables the Transfer Counter is Zero Interrupt
    - **0** = Disables the Transfer Counter is Zero Interrupt

- **bit 5**
  - **SOSIE**: Start of Slave Select Interrupt Enable bit
    - **1** = Enables the Start of Slave Select Interrupt
    - **0** = Disables the Start of Slave Select Interrupt

- **bit 4**
  - **EOSIE**: End of Slave Select Interrupt Enable bit
    - **1** = Enables the End of Slave Select Interrupt
    - **0** = Disables the End of Slave Select Interrupt

- **bit 3**
  - **Unimplemented**: Read as ‘0’

- **bit 2**
  - **RXOIE**: Receiver Overflow Interrupt Enable bit
    - **1** = Enables the Receiver Overflow Interrupt
    - **0** = Disables the Receiver Overflow Interrupt

- **bit 1**
  - **TXUIE**: Transmitter Underflow Interrupt Enable bit
    - **1** = Enables the Transmitter Underflow Interrupt
    - **0** = Disables the Transmitter Underflow Interrupt

- **bit 0**
  - **Unimplemented**: Read as ‘0’

# REGISTER 32-3: SPI<TCNTL – SPI TRANSFER COUNTER LSB REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCNT7</td>
<td>TCNT6</td>
<td>TCNT5</td>
<td>TCNT4</td>
<td>TCNT3</td>
<td>TCNT2</td>
<td>TCNT1</td>
<td>TCNT0</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’

- **bit 7-0**
  - **TCNT<7:0>:**
    - **BMODE = 0**
      - Bits 10-3 of the Transfer Counter, counting the total number of bits to transfer
    - **BMODE = 1**
      - Bits 7-0 of the Transfer Counter, counting the total number of bytes to transfer

**Note:** This register should not be written to while a transfer is in progress (BUSY bit of SPIxCON2 is set).
REGISTER 32-4: SPIxTCNTH: SPI TRANSFER COUNTER MSB REGISTER

<table>
<thead>
<tr>
<th>bit 7-3</th>
<th>bit 2-0</th>
</tr>
</thead>
</table>
| Unimplemented: Read as '0' | TCNT<10:8>:

- **BMODE = 0**: Bits 13-11 of the Transfer Counter, counting the total number of bits to transfer
- **BMODE = 1**: Bits 10-8 of the Transfer Counter, counting the total number of bytes to transfer

**Note:** This register should not be written to while a transfer is in progress (BUSY bit of SPIxCON2 is set).

REGISTER 32-5: SPIxTWIDTH: SPI TRANSFER WIDTH REGISTER

<table>
<thead>
<tr>
<th>bit 7-3</th>
<th>bit 2-0</th>
</tr>
</thead>
</table>
| Unimplemented: Read as '0' | TWIDTH<2:0>:

- **BMODE = 0**: Bits 2-0 of the Transfer Counter, counting the total number of bits to transfer
- **BMODE = 1**: Size (in bits) of each transfer counted by the transfer counter
  - 111 = 7 bits
  - 110 = 6 bits
  - 101 = 5 bits
  - 100 = 4 bits
  - 011 = 3 bits
  - 010 = 2 bits
  - 001 = 1 bit
  - 000 = 8 bits

**Note:** This register should not be written to while a transfer is in progress (BUSY bit of SPIxCON2 is set).
REGISTER 32-6:  SPIxBAUD: SPI BAUD RATE REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BAUD7</td>
<td>BAUD6</td>
<td>BAUD5</td>
<td>BAUD4</td>
<td>BAUD3</td>
<td>BAUD2</td>
<td>BAUD1</td>
<td>BAUD0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’

bit 7-0  **BAUD<7:0>:** Baud Clock Prescaler Select bits
SCK high or low time: TSC=SPI Clock Period*(BAUD+1)
SCK toggle frequency: FSCK=FBAUD= SPI Clock Frequency/(2*(BAUD+1))

**Note:** This register should not be written while the SPI is enabled (EN bit of SPIxCON0 = 1)

REGISTER 32-7:  SPIxCON0: SPI CONFIGURATION REGISTER 0

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>LSBF</td>
<td>MST</td>
<td>BMODE</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’

bit 7  **EN:** SPI Module Enable Control bit
1 = SPI is enabled
0 = SPI is disabled,

bit 6-3  **Unimplemented:** Read as ‘0’

bit 2  **LSBF:** LSb-First Data Exchange bit
1 = Data is exchanged LSb first
0 = Data is exchanged MSb first (traditional SPI operation)

bit 1  **MST:** SPI Operating Mode Master Select bit
1 = SPI module operates as the bus master
0 = SPI module operates as a bus slave

bit 0  **BMODE:** Bit-Length Mode Select bit
1 = SPIxTWIDTH setting applies to every byte: total bits sent is SPIxTWIDTH*SPIxTCNT, end-of-packet occurs when SPIxTCNT = 0
0 = SPIxTWIDTH setting applies only to the last byte exchanged; total bits sent is SPIxTWIDTH + (SPIxTCNT*8)

**Note:** This register should only be written when the EN bit is cleared, or to clear the EN bit.
<table>
<thead>
<tr>
<th>bit 7</th>
<th>SMP: SPI Input Sample Phase Control bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Slave mode:</td>
</tr>
<tr>
<td></td>
<td>1 = Reserved</td>
</tr>
<tr>
<td></td>
<td>0 = SDI input is sampled in the middle of data output time</td>
</tr>
<tr>
<td></td>
<td>Master mode:</td>
</tr>
<tr>
<td></td>
<td>1 = SDI input is sampled at the end of data output time</td>
</tr>
<tr>
<td></td>
<td>0 = SDI input is sampled in the middle of data output time</td>
</tr>
<tr>
<td>bit 6</td>
<td>CKE: Clock Edge Select bit</td>
</tr>
<tr>
<td></td>
<td>1 = Output data changes on transition from active to idle clock state</td>
</tr>
<tr>
<td></td>
<td>0 = Output data changes on transition from idle to active clock state</td>
</tr>
<tr>
<td>bit 5</td>
<td>CKP: Clock Polarity Select bit</td>
</tr>
<tr>
<td></td>
<td>1 = Idle state for SCK is high level</td>
</tr>
<tr>
<td></td>
<td>0 = Idle state for SCK is low level</td>
</tr>
<tr>
<td>bit 4</td>
<td>FST: Fast Start Enable bit</td>
</tr>
<tr>
<td></td>
<td>Slave mode:</td>
</tr>
<tr>
<td></td>
<td>This bit is ignored</td>
</tr>
<tr>
<td></td>
<td>Master mode:</td>
</tr>
<tr>
<td></td>
<td>1 = Delay to first SCK may be less than ½ baud period</td>
</tr>
<tr>
<td></td>
<td>0 = Delay to first SCK will be at least ½ baud period</td>
</tr>
<tr>
<td>bit 3</td>
<td>Unimplemented: Read as ‘0’</td>
</tr>
<tr>
<td>bit 2</td>
<td>SSP: SS Input/Output Polarity Control bit</td>
</tr>
<tr>
<td></td>
<td>1 = SS is active-low</td>
</tr>
<tr>
<td></td>
<td>0 = SS is active-high</td>
</tr>
<tr>
<td>bit 1</td>
<td>SDIP: SDI Input Polarity Control bit</td>
</tr>
<tr>
<td></td>
<td>1 = SDI input is active-low</td>
</tr>
<tr>
<td></td>
<td>0 = SDI input is active-high</td>
</tr>
<tr>
<td>bit 0</td>
<td>SDOP: SDI Output Polarity Control bit</td>
</tr>
<tr>
<td></td>
<td>1 = SDO output is active-low</td>
</tr>
<tr>
<td></td>
<td>0 = SDO output is active-high</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
REGISTER 32-9: SPIxCON2: SPI CONFIGURATION REGISTER 2

<table>
<thead>
<tr>
<th>R-0/0</th>
<th>R-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BUSY</td>
<td>SSFLT</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SSET</td>
<td>TXR(1)</td>
<td>RXR(1)</td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’

<table>
<thead>
<tr>
<th>bit 7</th>
<th>BUSY: SPI Module Busy Status bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Data exchange is busy</td>
</tr>
<tr>
<td>0</td>
<td>Data exchange is not taking place</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 6</th>
<th>SSFLT: SS(in) Fault Status bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>If SSET = 0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>SS(in) ended the transaction unexpectedly, and the data byte being received was lost</td>
</tr>
<tr>
<td>0</td>
<td>SS(in) ended normally</td>
</tr>
<tr>
<td>If SSET = 1</td>
<td></td>
</tr>
<tr>
<td>This bit is unchanged.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 5-3</th>
<th>Unimplemented: Read as ‘0’</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>bit 2</th>
<th>SSET: Slave Select Enable bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Master mode:</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>SS(out) is driven to the active state continuously</td>
</tr>
<tr>
<td>0</td>
<td>SS(out) is driven to the active state while the transmit counter is not zero</td>
</tr>
<tr>
<td>Slave mode:</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>SS(in) is ignored and data is clocked on all SCK(in) (as though SS = TRUE at all times)</td>
</tr>
<tr>
<td>0</td>
<td>SS(in) enables/disables data input and tri-states SDO if the TRIS bit associated with the SDO pin is set (see Table 32-2 for details)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 1</th>
<th>TXR: Transmit Data-Required Control bit(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TxFIFO data is required for a transfer</td>
</tr>
<tr>
<td>0</td>
<td>TxFIFO data is not required for a transfer</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 0</th>
<th>RXR: Receive FIFO Space-Required Control bit(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Data transfers are suspended if the RxFIFO is full</td>
</tr>
<tr>
<td>0</td>
<td>Received data is not stored in the FIFO</td>
</tr>
</tbody>
</table>

Note 1: See Table 32-1 as well as Section 32.5 “Master mode” and Section 32.6 “Slave Mode” for more details pertaining to TXR and RXR function.

2: This register should not be written to while a transfer is in progress (BUSY bit of SPIxCON2 is set).
**REGISTER 32-10: SPIxSTATUS: SPI STATUS REGISTER**

<table>
<thead>
<tr>
<th>R/C/HS-0/0</th>
<th>U-0</th>
<th>R-1/1</th>
<th>U-0</th>
<th>R/C/HS-0/0</th>
<th>S-0/0</th>
<th>U-0</th>
<th>R-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXWE</td>
<td>—</td>
<td>TXBE</td>
<td>—</td>
<td>RXRE</td>
<td>CLRBF</td>
<td>—</td>
<td>RXBF</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **C** = Clearable bit
- **S** = Settable bit
- **HS** = Bit can be set by hardware

<table>
<thead>
<tr>
<th>bit 7 TXWE: Transmit Buffer Write Error bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 = SPIxTxB was written while TxFIFO was full</td>
</tr>
<tr>
<td>0 = No error has occurred</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 6 Unimplemented: Read as ‘0’</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>bit 5 TXBE: Transmit Buffer Empty bit (read-only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 = Transmit buffer TxFIFO is empty</td>
</tr>
<tr>
<td>0 = Transmit buffer is not empty</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 4 Unimplemented: Read as ‘0’</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>bit 3 RXRE: Receive Buffer Read Error bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 = SPIxRB was read while RxFIFO was empty</td>
</tr>
<tr>
<td>0 = No error has occurred</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 2 CLRBF: Clear Buffer Control bit (write only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 = Reset the receive and transmit buffers, making both buffers empty</td>
</tr>
<tr>
<td>0 = Take no action</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 1 Unimplemented: Read as ‘0’</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>bit 0 RXBF: Receive Buffer Full bit (read-only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 = Receive buffer is full</td>
</tr>
<tr>
<td>0 = Receive buffer is not full</td>
</tr>
</tbody>
</table>

**REGISTER 32-11: SPIxRxB: SPI READ BUFFER REGISTER**

<table>
<thead>
<tr>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXB7</td>
<td>RXB6</td>
<td>RXB5</td>
<td>RXB4</td>
<td>RXB3</td>
<td>RXB2</td>
<td>RXB1</td>
<td>RXB0</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’

<table>
<thead>
<tr>
<th>bit 7-0 RXB&lt;7:0&gt;: Receiver Buffer bits (read-only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>If RX buffer is not empty:</td>
</tr>
<tr>
<td>Contains the top-most byte of RxFIFO, and reading this register will remove the top-most byte</td>
</tr>
<tr>
<td>RxFIFO and decrease the occupancy of the RxFIFO</td>
</tr>
<tr>
<td>If RX buffer is empty:</td>
</tr>
<tr>
<td>Reading this register will read as ‘0’, leave the occupancy unchanged, and set the RXRE bit of</td>
</tr>
<tr>
<td>SPIxSTATUS</td>
</tr>
</tbody>
</table>
REGISTER 32-12: SPIxTxB: SPI TRANSMIT BUFFER REGISTER

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>TXB7</th>
<th>TXB6</th>
<th>TXB5</th>
<th>TXB4</th>
<th>TXB3</th>
<th>TXB2</th>
<th>TXB1</th>
<th>TXB0</th>
</tr>
</thead>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'

bit 7-0  **TXB<7:0>:** Transmit Buffer bits (write only)

If TXFIFO is not full:
Writing to this register adds the data to the top of the TXFIFO and increases the occupancy of the TXFIFO write pointer

If TXFIFO is full:
Writing to this register does not affect the data in the TXFIFO or the write pointer, and the TXWE bit of SPIxSTATUS will be set

REGISTER 32-13: SPIxCLK: SPI CLOCK SELECTION REGISTER

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>CLKSEL3</th>
<th>CLKSEL2</th>
<th>CLKSEL1</th>
<th>CLKSEL0</th>
</tr>
</thead>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'

bit 7-4  **Unimplemented:** Read as '0'

bit 3-0  **CLKSEL<3:0>:** SPI Clock Source Selection bits

1111-1001 = Reserved
1000 = SMT_match
0111 = TMR6_Postscaled
0110 = TMR4_Postscaled
0101 = TMR2_Postscaled
0100 = TMR0_overflow
0011 = CLKREF
0010 = MFINTOSC
0001 = HFINTOSC
0000 = FOSC
### TABLE 32-3: SUMMARY OF REGISTERS ASSOCIATED WITH SPI

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPIxINTF</td>
<td>SRMTIF</td>
<td>TCZIF</td>
<td>SOSIF</td>
<td>EOSIF</td>
<td>—</td>
<td>RXOIF</td>
<td>TXUIF</td>
<td>—</td>
<td>520</td>
</tr>
<tr>
<td>SPIxINTE</td>
<td>SRMTIE</td>
<td>TCZIE</td>
<td>SOSIE</td>
<td>EOSIE</td>
<td>—</td>
<td>RXOIE</td>
<td>TXUIE</td>
<td>—</td>
<td>521</td>
</tr>
<tr>
<td>SPIxTCNTH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TCNT10</td>
<td>TCNT9</td>
<td>TCNT8</td>
</tr>
<tr>
<td>SPIxTCNTH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TCNT10</td>
<td>TCNT9</td>
<td>TCNT8</td>
</tr>
<tr>
<td>SPIxTCNTH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TWIDTH2</td>
<td>TWIDX1</td>
<td>TWIDX0</td>
</tr>
<tr>
<td>SPIxBAUD</td>
<td>BAUD7</td>
<td>BAUD6</td>
<td>BAUD5</td>
<td>BAUD4</td>
<td>BAUD3</td>
<td>BAUD2</td>
<td>BAUD1</td>
<td>BAUD0</td>
<td>523</td>
</tr>
<tr>
<td>SPIxBAUD</td>
<td>BAUD7</td>
<td>BAUD6</td>
<td>BAUD5</td>
<td>BAUD4</td>
<td>BAUD3</td>
<td>BAUD2</td>
<td>BAUD1</td>
<td>BAUD0</td>
<td>523</td>
</tr>
<tr>
<td>SPIxCON0</td>
<td>EN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>LSBF</td>
<td>MST</td>
<td>BMODE</td>
</tr>
<tr>
<td>SPIxCON0</td>
<td>EN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>LSBF</td>
<td>MST</td>
<td>BMODE</td>
</tr>
<tr>
<td>SPIxCON1</td>
<td>SMP</td>
<td>CKE</td>
<td>CKP</td>
<td>FST</td>
<td>—</td>
<td>—</td>
<td>SSP</td>
<td>SDIP</td>
<td>SDOP</td>
</tr>
<tr>
<td>SPIxCON2</td>
<td>BUSY</td>
<td>SSFLT</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SSET</td>
<td>TXR</td>
<td>RXR</td>
</tr>
<tr>
<td>SPIxSTATUS</td>
<td>TXWE</td>
<td>—</td>
<td>TXBE</td>
<td>—</td>
<td>RXRE</td>
<td>CLRBF</td>
<td>—</td>
<td>RXBF</td>
<td>526</td>
</tr>
<tr>
<td>SPIxRXB</td>
<td>RXB7</td>
<td>RXB6</td>
<td>RXB5</td>
<td>RXB4</td>
<td>RXB3</td>
<td>RXB2</td>
<td>RXB1</td>
<td>RXB0</td>
<td>526</td>
</tr>
<tr>
<td>SPIxTXB</td>
<td>TXB7</td>
<td>TXB6</td>
<td>TXB5</td>
<td>TXB4</td>
<td>TXB3</td>
<td>TXB2</td>
<td>TXB1</td>
<td>TXB0</td>
<td>527</td>
</tr>
<tr>
<td>SPIxCLK</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CLKSEL3</td>
<td>CLKSEL2</td>
<td>CLKSEL1</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented, read as ‘0’. Shaded cells are unused by the SPI module.
33.0 **I²C MODULE**

The device has two dedicated, independent I²C modules. Figure 33-1 is a block diagram of the I²C interface module. The figure shows both the Master and Slave modes together.

**FIGURE 33-1: I²C MODULE BLOCK DIAGRAM**
33.1 I2C Features

- Inter-Integrated Circuit (I2C) interface supports the following modes in hardware:
  - Master mode
  - Slave mode with byte NACKing
  - Multi-Master mode
- Dedicated Address, Receive and Transmit buffers
- Up to four slave addresses matching
- General Call address matching
- 7-bit and 10-bit addressing with masking
- Start, Restart, Stop, Address, Write, and ACK Interrupts
- Clock Stretching hardware for:
  - RX Buffer Full
  - TX Buffer Empty
  - After Address, Write, and ACK
- Bus Collision Detection with arbitration
- Bus Timeout Detection
- I2C, SMBus 2.0, and SMBus 3.0 input level selections

33.2 I2C Module Overview

The I2C module provides a synchronous interface between the microcontroller and other I2C-compatible devices using the two-wire I2C serial bus. Devices communicate in a master/slave environment. The I2C bus specifies two signal connections:

- Serial Clock (SCL)
- Serial Data (SDA)

Both the SCL and SDA connections are bidirectional open-drain lines, each requiring pull-up resistors to the supply voltage. Pulling the line to ground is considered a logical zero and letting the line float is considered a logical one. Every transaction on the I2C bus has to be initiated by the master.

Figure 33-2 shows a typical connection between a master and more than one slave.

**FIGURE 33-2: I2C MASTER/SLAVE CONNECTIONS**
There are four main operations based on the direction of the data being shared during I2C communication.

- Master Transmit (master is transmitting data to a slave)
- Master Receive (master is receiving data from a slave)
- Slave Transmit (slave is transmitting data to a master)
- Slave Receive (slave is receiving data from the master)

To begin any I2C communication, the master device sends out a Start bit followed by the address byte of the slave it intends to communicate with. This is followed by a single Read/Write bit, which determines whether the master intends to transmit to or receive data from the slave device.

If the requested slave exists on the bus, it will respond with an Acknowledge bit, otherwise known as an ACK. The master then continues to shift data in or out of the slave until it terminates the message with a Stop.

Further details about the I2C module are discussed in the section below.

### 33.3 I2C Mode Operation

All I2C communication is 8-bit data and 1-bit acknowledge and shifted out MSb first. The user can control the interaction between the software and the module using several control registers and interrupt flags. Two pins, SDA and SCL, are exercised by the module to communicate with other external I2C devices.

#### 33.3.1 DEFINITION OF I2C TERMINOLOGY

The I2C communication protocol terminologies are defined for reference below in Table 33-1. These terminologies are used throughout this document. Table 33-1 has been adapted from the Phillips I2C specification.

<table>
<thead>
<tr>
<th>TERM</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmitter</td>
<td>The device which shifts data out onto the bus</td>
</tr>
<tr>
<td>Receiver</td>
<td>The device which shifts data in from the bus</td>
</tr>
<tr>
<td>Master</td>
<td>The device that initiates a transfer, generates clock signals and terminates a transfer</td>
</tr>
<tr>
<td>Slave</td>
<td>The device addressed by the master</td>
</tr>
<tr>
<td>Multi-master</td>
<td>A bus with more than one device that can initiate data transfers</td>
</tr>
<tr>
<td>Arbitration</td>
<td>Procedure to ensure that only one master at a time controls the bus. Winning arbitration ensures that the message is not corrupted</td>
</tr>
<tr>
<td>Synchronization</td>
<td>Procedure to synchronize the clocks of two or more devices on the bus.</td>
</tr>
<tr>
<td>Idle</td>
<td>No master is controlling the bus, and both SDA and SCL lines are high</td>
</tr>
<tr>
<td>Active</td>
<td>Any time one or more master devices are controlling the bus</td>
</tr>
<tr>
<td>Addressed Slave</td>
<td>Slave device that has received a matching address and is actively being clocked by a master</td>
</tr>
<tr>
<td>Matching Address</td>
<td>Address byte that is clocked into a slave that matches the value stored in I2CxADR</td>
</tr>
<tr>
<td>Write Request</td>
<td>Slave receives a matching address with R/W bit clear and is ready to clock in data</td>
</tr>
<tr>
<td>Read Request</td>
<td>Master sends an address byte with the R/W bit set, indicating that it wishes to clock data out of the slave. This data is the next and all following bytes until a Restart or Stop.</td>
</tr>
<tr>
<td>Clock Stretching</td>
<td>When a device on the bus holds SCL low to stall communication</td>
</tr>
<tr>
<td>Bus Collision</td>
<td>Any time the SDA line is sampled low by the module while it is outputting and expected high state.</td>
</tr>
<tr>
<td>Bus Timeout</td>
<td>Any time the I2C module is reset and the module goes Idle.</td>
</tr>
</tbody>
</table>
33.3.2 BYTE FORMAT
All communication in I2C is done in 9-bit segments. A byte is sent from a master to a slave or vice-versa, followed by an Acknowledge bit sent by the receiver. After the 8th falling edge of the SCL line, the device transmitting data on the SDA line releases control of that pin to an input, and reads in an acknowledge value on the next clock pulse. The clock signal is provided by the master. Data is valid to change while the SCL line is low, and sampled on the rising edge of the clock. Changes on the SDA line while the SCL line is high define Start and Stop conditions on the bus which are explained further in the chapter.

33.3.3 SDA AND SCL PINS
The user must configure these pins as open-drain outputs. This is done by clearing the appropriate TRIS bits and setting the appropriate ODCON bits. The user may also select the input threshold, slew-rate and internal pull-up settings using the RxI2C control registers (Register 16-9).

33.3.4 SDA HOLD TIME
The hold time of the SDA pin is selected by the SDAHT<1:0> bits of the I2CxCON2 register. Hold time is the time SDA is held valid after the falling edge of SCL. A longer hold time setting may help on buses with large capacitance.

33.3.5 START CONDITION
The I2C specification defines a Start condition as a transition of SDA line from a high to a low state while SCL line is high. A Start condition is always generated by the master and signifies the transition of the bus from an Idle to an Active state. Figure 33-3 shows waveforms for Start conditions. Master hardware waits for the BFRE bit of I2CxSTAT0 to be set, before asserting a Start condition on the SCL and SDA lines. If two masters assert a start at the same time, a collision will occur during the addressing phase.

33.3.6 STOP CONDITION
A Stop condition is a transition of the SDA line from low to high while the SCL line is high. Figure 33-3 shows waveforms for Stop conditions.

FIGURE 33-3: START AND STOP CONDITIONS

![Waveforms for Start and Stop Conditions](image_url)

Note: At least one SCL low time must appear before a Stop is valid. Therefore, if the SDA line goes low then high again while the SCL line is high, only the Start condition is detected.
33.3.7 RESTART CONDITION

A Restart is valid any time that a Stop would be valid. A master can issue a Restart if it wishes to hold the bus after terminating the current transfer. A Restart has the same effect on the slave that a Start would, resetting all slave logic and preparing it to clock in an address. The master may want to address the same or another slave. Figure 33-4 shows the waveform for a Restart condition.

In 10-bit Addressing Slave mode a Restart is required for the master to clock data out of the addressed slave. Once a slave has been fully addressed, matching both high and low address bytes (SMA = 1), the master can issue a Restart and the high address byte with the R/W bit set. The slave logic will then hold the clock and prepare to clock out data.

FIGURE 33-4: RESTART CONDITION

33.3.8 ACKNOWLEDGE SEQUENCE

The ninth SCL pulse for any transferred byte in I^2C is dedicated as an Acknowledge. It allows receiving devices to respond back to the transmitter by pulling the SDA line low. The transmitter must release control of the line during this time to shift in the response. The Acknowledge (ACK) is an active-low signal, pulling the SDA line low indicates to the transmitter that the device has received the transmitted data and is ready to receive more.

The result of an ACK is placed in the ACKSTAT bit of the I^2CxCON1 register. The ACKSTAT bit is cleared when the receiving device sends an Acknowledge and is set when the receiving device does not Acknowledge. A slave sends an Acknowledge when it has recognized its address. When in a mode that is receiving data, the ACK data being sent to the transmitter depends on the value of I^2CxCNT register. ACKDT is the value sent when I^2CxCNT! = 0. When I^2CxCNT = 0, the ACKCNT value is used instead.

In Slave mode, if the ADRIE or WRIE bits are set, clock stretching is initiated when there is an address match or when there is an attempt to write to slave. This allows the user to set the ACK value sent back to the transmitter. The ACKDT bit of the I^2CxCON1 register is set/cleared to determine the response. Slave hardware will generate an ACK response if the ADRIE or WRIE bits are clear.

Certain conditions will cause a not-ACK (NACK) to be sent automatically. If any of the RXRE, TXRE, RXO, or TXU bits is set, the hardware response is forced to NACK. All subsequent responses from the device for address matches or data will be a NACK response.

33.3.9 BUS TIME-OUT

The I^2CxBTO register can be used to select the timeout source for the module. The I^2C module is reset when the selected bus timeout signal goes high. This feature is useful for SMBus and PMBus™ compatibility.

For example, Timer2 can be selected as the bus timeout source and configured to count when the SCL pin is low. If the timer runs over before the SCL pin transitioned high, the timer-out pulse will reset the module.

Note: The bus time-out source should produce a rising edge.

If the module is configured as a slave and a BTO event occurs when the slave is active (i.e., the SMA bit is set), the module is immediately reset. The SMA and CSTR bits are also cleared, and the BTOIF bit is set.
If a BTO event occurs when the module is configured as a master and is active, (i.e., MMA bit is set), and the module immediately tries to assert a Stop condition and also sets the BTOIF bit. The actual generation of the Stop condition may be delayed if the bus is been clock stretched by some slave device. The MMA bit will be cleared only after the Stop condition is generated.

### 33.3.10 ADDRESS BUFFERS

The I^2^C module has two address buffer registers, I2CxADB0 and I2CxADB1. Depending on the mode, these registers are used as either receive or transmit address buffers. See Table 33-2 for data flow directions in these registers. In Slave modes, these registers are only updated when there is an address match. The ADB bit in the I2CxCON2 register is used to enable/disable the address buffer functionality. When disabled, the address data is sourced from the transmit buffer and is stored in the receive buffer.

#### TABLE 33-2: ADDRESS BUFFER DIRECTION AS PER I^2^C MODE

<table>
<thead>
<tr>
<th>Modes</th>
<th>MODE&lt;2:0&gt;</th>
<th>I2CxADB0</th>
<th>I2CxADB1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slave (7-bit)</td>
<td>000</td>
<td>RX</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>001</td>
<td>RX</td>
<td>—</td>
</tr>
<tr>
<td>Slave (10-bit)</td>
<td>010</td>
<td>RX</td>
<td>RX</td>
</tr>
<tr>
<td></td>
<td>011</td>
<td>RX</td>
<td>RX</td>
</tr>
<tr>
<td>Master (7-bit)</td>
<td>100</td>
<td>—</td>
<td>TX</td>
</tr>
<tr>
<td>Master (10-bit)</td>
<td>101</td>
<td>TX</td>
<td>TX</td>
</tr>
<tr>
<td>Multi-Master (7-bit)</td>
<td>110</td>
<td>RX</td>
<td>TX</td>
</tr>
<tr>
<td></td>
<td>111</td>
<td>RX</td>
<td>TX</td>
</tr>
</tbody>
</table>

#### 33.3.10.1 Slave Mode (7-bit)

In 7-bit Slave mode, I2CxADB0 is loaded with the received matching address and R/W data. The I2CxADB1 register is ignored in this mode.

#### 33.3.10.2 Slave Mode (10-bit)

In 10-bit Slave mode, I2CxADB0 is loaded with the lower eight bits of the matching received address. I2CxADB1 is loaded with full eight bits of the high address byte, including the R/W bit.

#### 33.3.10.3 Master Mode (7-bit)

The I2CxADB0 register is ignored in this mode. In 7-bit Master mode, the I2CxADB1 register is used to copy address data byte, including the R/W value, to the shift register.

#### 33.3.10.4 Master Mode (10-bit)

In 10-bit Master mode, the I2CxADB0 register stores the low address data byte value that will be copied to the shift register after the high address byte is shifted out. The I2CxADB1 register stores the high address byte value that will be copied to the shift register. It is up to the user to specify all eight of these bits, even though the I^2^C specification defines the upper five bits as a constant.

#### 33.3.10.5 Multi-Master Mode (7-bit only)

In Multi-Master mode, the device can be both master and slave depending on the sequence of events on the bus. If being addressed as a slave, the I2CxADB0 register stores the received matching slave address byte. If the device is trying to communicate as a master on the bus, the contents of the I2CxADB1 register are copied to the shift register for addressing a slave device.

#### 33.3.11 RECEIVE AND TRANSMIT BUFFER

The receive buffer holds one byte of data while another is shifted into the SDA pin. The user can access the buffer by software (or DMA) through the I2CxRXB register. When new data is loaded into the I2CxRXB register, the receive buffer full Status bit (RXBF) is set and reading the I2CxRXB register clears this bit.

If the user tries to read I2CxRXB when it is empty (i.e., RXBF = 0), receive read error bit (RXRE) is set and a NACK will be generated. The user must clear the error bit to resume normal operation.

The transmit buffer holds one byte of data while another can be shifted out through the SDA pin. The user can access the buffer by software (or DMA) through the I2CxTXB register. When the I2CxTXB does not contain any transmit data, the transmit buffer empty Status bit (TXBE) is set. At this point, the user can load another byte into the buffer.

If the user tries to write I2CxTXB when it is NOT empty (i.e., TXBE = 0), transmit write error flag bit (TXRE) is set and the new data is discarded. When TXRE is set, the user must clear this error condition to resume normal operation.

By setting the CLRBF bit in the I2CxSTAT1 register, the user can clear both receive and transmit buffers. CLRBF will also clear the I2CxRXIF and I2CxTXIF bits.

#### 33.3.12 CLOCK STRETCHING

When a slave device has not completed processing data, it can delay the transfer of more data through the process of clock stretching. An addressed slave device may hold the SCL clock line low after receiving or sending a bit, indicating that it is not yet ready to continue. The master will attempt to raise the SCL line in order to transfer the next bit, but will detect that the clock line has not yet been released. Since the SCL connection is open-drain, the slave has the ability to hold the line low until it is ready to continue communicating. Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data.
Clock stretching can be enabled or disabled by the clearing or setting of CSTRDIS (clock stretching disable) bit in the I2CxCON2 register. This bit is valid only in the Multi-Master and Slave modes of operation.

33.3.12.1 Clock Stretching for Buffer Operations

If enabled, clock stretching is forced during buffer read/write operations. For example, in Slave mode if RXBF = 1 (receive buffer full), the clock will be stretched after the seventh falling edge of SCL. The SCL line is released only after the user reads data from the receive buffer. This ensures that there is never a receive data overflow. In this situation, if clock stretching is disabled, the RXO bit in I2CxCON1 is set indicating a receive overflow. When set, the module will always respond with a NACK.

Similarly, when TXBE = 1 (transmit buffer empty) and I2CCNT! = 0, the clock is stretched after the 8th falling edge of SCL. The SCL line is released only after the user loads new data into the transmit buffer. This ensures that there is never a transmit underflow. In this situation, if clock stretching is disabled, the TXUF bit in I2CxCON1 is set indicating a transmit underflow. When set, the module will always respond with a NACK.

33.3.12.2 Clock Stretching for Other Slave Operations

There are three Interrupt and Hold bits that provide clock stretching in Slave mode. These bits can also be used in conjunction with the I2CxIE bit in PIRx register to generate system level interrupts.

- Incoming address match interrupt
  - Clock stretching after an incoming matching address byte is enabled by the Address Interrupt and Hold (ADRIE) bit of the I2CxPIE register. When ADRIE = 1, the CSTR bit is set and the SCL line is stretched following the 8th falling edge of SCL of a received matching address. This allows the user to read the received address from the I2CADBO/1 registers and selectively ACK/NACK based on the received address. Clock stretching from ADRIE is released by software clearing the CSTR bit.

- Data Write Interrupt
  - The data write interrupt and hold enable (WRIE) bit is used to enable clock stretching after a received data byte. When WRIE = 1, the CSTR bit is set, and the SCL line is stretched, following the 8th falling SCL edge for incoming slave data. This bit allows user software to selectively ACK/NACK each received data byte. Clock stretching from WRIE is released by software clearing the CSTR bit.

- Acknowledge status
  - The acknowledge status time interrupt and hold enable (ACKTIE) bit is used to enable clock stretching after the ACK phase of a transmission. This bit enables clock stretching for all address/data transactions; address, write, or read. Following the ACK, the slave hardware will set CSTR. Clock stretching from ACKTIE is released by software clearing the CSTR bit.

33.3.13 DATA BYTE COUNT

The I2CxCNT register is used to specify the number of bytes in a complete I2C packet. The value in this register will decrement every time a data byte is received or transmitted from the I2C module. The I2CxCNT register will not decrement past zero.

If a byte transfer causes the I2CxCNT register to decrement to zero, the Count Interrupt Flag bit (CNTIF) in I2CPIR is set. This flag bit is set on the 9th falling edge of SCL for transmit operations and can be more informative if the edge is specified.

The I2CxCNT register can be auto-loaded if the ACNT bit in the I2CxCON2 register is set. When ACNT bit is set, the data byte following the address byte is loaded into the I2CxCNT register.

Note 1: I2CxCNT decrements on the eighth (receive) or ninth (transmit) falling edge of SCL; writes during this bit time can corrupt the value.

2: If the block size of the message is greater than 255, the I2CxCNT register can be updated mid-message to prevent decrement to zero.

33.4 I2C Slave Mode

The I2C Slave mode operates in one of four modes selected in the Mode bits of I2CxCON0. The modes can be divided into 7- and 10-bit Addressing modes. 10-bit Addressing modes operate the same as 7-bit with some additional overhead for handling the larger addresses.

33.4.1 SLAVE ADDRESSING MODES

The I2CxADR/1/2/3 registers contain the Slave mode addresses. The first byte received after a Start or Restart condition is compared against the values stored in these registers. If the byte matches a value, it is loaded into the I2CADBO/1 registers. If the value does not match, there is no response from the module. The I2C module can be configured in the following slave configurations.
33.4.1.1 7-bit Addresses Mode
In this mode, the LSb of the received data byte is ignored when determining if there is an address match. All four I2CxADR registers are independently compared to the received address byte.

33.4.1.2 7-bit Addresses with Masking
In this mode, the value in I2CxADR0 is masked with the value in I2CxADR1 to determine if an address match occurred. A second address and mask are also compared from I2CxADR2/3. When Mode<2:0> = 001 or 111, the I2CxADR1/3 registers serve as the mask value for I2CxADR0/2. All seven bits of the address can be masked.

33.4.1.3 10-bit Addresses
In this mode, the values stored in I2CxADR0 and I2CxADR1 registers are used to create a 10-bit address. A second 10-bit compare address is formed from I2CxADR2 and I2CxADR3.

33.4.1.4 10-bit Address with Masking
In this mode, the I2CxADR0/1 registers are used to form a 10-bit address, and the I2CxADR2/3 registers are used to form a 10-bit mask for that address. When MODE<2:0> = 011, the I2CxADR2/3 registers serve as the mask value for the 10-bit address stored in I2CxADR0/1.

33.4.2 GENERAL CALL ADDRESS SUPPORT
The addressing procedure for the I2C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an ACK. The general call address is a reserved address in the I2C protocol, defined as address 0x00.

In order for the slave hardware to ACK this address, it must be enabled by setting the GCEN bit in the I2CxCON2 register. Setting one of the I2CxADR0/1/2/3 registers to 0x00 is not required. Figure 33-5 shows a General Call reception sequence.

If the ADRIE bit is set, the module will clock stretch after the eighth SCL pulse just like any other address match.

Note: General Call addressing is supported in only 7-bit Addressing modes.

Note: Even though 10-bit addressing calls out only ten bits used in the address comparison, all 15 address bits in I2CxADR0/1 are compared in these modes.

FIGURE 33-5: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE

Address is compared to General Call Address (I2CxADR0 = 0x00) after ACK, set interrupt

Clear by software

Matching address written to I2CxADB0
33.4.3 SLAVE OPERATION IN 7-BIT ADDRESSING MODE

The 8th bit in an address byte transmitted by the master is used to determine if the master wants to read from or write to the slave device. If set, it denotes that the master wants to read from the slave and if cleared it means the master wants to write to the slave device. If there is an address match, the R/W bit is copied to the R/W bit of the I2CSTAT0 register.

33.4.3.1 Slave Reception (7-bit Addressing Mode)

This section describes the sequence of events for the I2C module configured as an I2C slave in 7-bit Addressing mode and is receiving data. Figure 33-6, Figure 33-7, and Figure 33-8 are used as a visual reference for this description.

1. Master asserts Start condition (can also be a restart) on the bus. Start condition Interrupt Flag (SCIF) in I2CxPIR register is set.
2. If Start condition interrupt is enabled (SCIE bit is set), generic interrupt I2CxIF is set.
3. Master transmits eight bits – 7-bit address and R/W = 0.
4. Received address is compared with the values in I2CxADR0/I2CxADR1/I2CxADR2/I2CxADR3 registers. Refer to section Section 33.4.1 "Slave Addressing Modes" for slave addressing modes.
5. If address matches; SMA in I2CSTAT0 register is set, R/W is copied to R/W bit, D/A bit is cleared. If the address does not match; module becomes Idle.
6. The matched address data is loaded into I2CxADB0 and ADRIIF in I2CxPIR register is set.
7. If Address hold interrupt is enabled (ADRIE = 1), CSTR is set. I2CxIF is set. Slave software can read address from I2CxADB0 and set/clear ACKDT before releasing SCL.
8. If there are any previous error conditions (e.g., Receive buffer overflow or transmit buffer underflow errors), slave will force a NACK and the module becomes Idle.
9. ACKDT value is copied out to SDA for ACK pulse to be read by the master on the 9th SCL pulse.
10. If the receive buffer is full from the previous transaction (i.e., RXBF = 1 (I2CxRXIF = 1)), CSTR is set. Slave software must read data out of I2CxRB to resume communication.
11. Master sends 8th SCL pulse of the data byte. D/A bit is set, WRIF is set.
12. I2CxRB is loaded with new data, RXBF bit is set, I2CxRXIF is set.
13. If Data write interrupt and hold is enabled (WRIE = 1), CSTR is set, I2CxIF is set. Slave software can read data from I2CxRB and set/clear ACKDT before releasing SCL by clearing CSTR.
14. If I2CxCNT = 0, the ACKCNT value is output to the SDA; else, if I2CxCNT! = 0, the ACKDT value is used and the value of I2CxCNT is decremented.
15. The ACK value is copied out to SDA to be read by the master on the 9th SCL pulse.
16. If I2CxCNT = 0, CNTIF is set.
17. If a NACK was sent, NACKIF is set, module becomes idle.
18. If ACKTIE = 1, CSTR is set, I2CxIF is set. Slave software can read data from I2CxRB before releasing SCL by clearing CSTR.
19. Go to step 11.
FIGURE 33-6: I2C SLAVE, 7-BIT ADDRESS, RECEPTION (ACKTIE = 0, ADRIE = 0, WRIE = 0)
FIGURE 33-7: I2C SLAVE, 7-BIT ADDRESS, RECEPTION WITH I2CxCNT (ACKTIE = 1, ADRIE = 0, WRIE = 0)

Bus Master sends stop condition

From Slave to Master

SDA S
Receive Address
A7 A6 A5 A4 A3 A2 A1 R/W = 0 ACK D7 D6 D5 D4 D3 D2 D1 D0
Receive Data
ACK D7 D6 D5 D4 D3 D2 D1 D0
Receive Data
NACK P

CSTR
SCIF is set
ACKTIE = 0
ADRIE = 0
R/W copied from matching address
ACKTIE = 1
ADRIF is set

I2CxADB0
matching address copied to
I2CxADB0

I2CxCNT
0x02
0x2
0x01
0x00

Slave sends ACKCNT value for I2CxCNT = 0
CNTIF is set

RXBF
Data byte written to I2CxRXB
RXIF set
Software reads I2CxRXB clearing RXIF

Second data byte written to I2CxRXB
RXIF set

SCIF is set
Software clears CSTR
No CSTR for NACK

ACKTIE = 1
WRIE = 0
ACKTIE = 1
WRIE = 0

WRIF is set
ACKTIF is set
WRIF is set
ACKTIF is set

R/W = 0
ACK

A/D
R/W
ADRIF is set

WRIE = 0
ACKTIF is set
WRIE = 0
ACKTIF is set

SCIF is set
Software clears CSTR

ACKTIE = 1
WRIE = 0
ACKTIE = 1
WRIE = 0

WRIF is set
ACKTIF is set
WRIF is set
ACKTIF is set

SCIF is set
Software clears CSTR

ACKTIE = 1
WRIE = 0
ACKTIE = 1
WRIE = 0

WRIF is set
ACKTIF is set
WRIF is set
ACKTIF is set

SCIF is set
Software clears CSTR

ACKTIE = 1
WRIE = 0
ACKTIE = 1
WRIE = 0

WRIF is set
ACKTIF is set
WRIF is set
ACKTIF is set

SCIF is set
Software clears CSTR

ACKTIE = 1
WRIE = 0
ACKTIE = 1
WRIE = 0

WRIF is set
ACKTIF is set
WRIF is set
ACKTIF is set

SCIF is set
Software clears CSTR

ACKTIE = 1
WRIE = 0
ACKTIE = 1
WRIE = 0

WRIF is set
ACKTIF is set
WRIF is set
ACKTIF is set

SCIF is set
Software clears CSTR

ACKTIE = 1
WRIE = 0
ACKTIE = 1
WRIE = 0

WRIF is set
ACKTIF is set
WRIF is set
ACKTIF is set

SCIF is set
Software clears CSTR

ACKTIE = 1
WRIE = 0
ACKTIE = 1
WRIE = 0

WRIF is set
ACKTIF is set
WRIF is set
ACKTIF is set

SCIF is set
Software clears CSTR

ACKTIE = 1
WRIE = 0
ACKTIE = 1
WRIE = 0

WRIF is set
ACKTIF is set
WRIF is set
ACKTIF is set

SCIF is set
Software clears CSTR
FIGURE 33-8: \( ^2 \text{C SLAVE, 7-BIT ADDRESS, RECEPTION NO I2CxBNT} \) (ACKTIE = 0, ADRIE = 1, WRIE = 1)

- Master Releases SDA to slave for ACK sequence
- Clock is held low until CSTR is set to '1'
- CSTR cleared software, SCL is released
- Slave software sets ACKDT
- WRIF is set
- NACKIF is set
- Master sends stop condition

- Receiving Address R/W = 0
- Receiving Data
- ACK
- D7 D6 D5 D4 D3 D2 D1 D0
- ACK
- D7 D6 D5 D4 D3 D2 D1 D0
- NACK

- Matching address written to I2CxADB0
- Software reads I2CxADB0
- Software clears ACKDT
- ACKTIF is set
- Slave software sets ACKDT
- ACKT cleared by hardware on 8th falling edge of SCL
- ACKTIF is set

- CSTR is set by hardware
- WRIF is set
- NACKIF is set

- Matching address written to I2CxADB0
- Software reads data from I2CxADB0
- Clearing I2CxADBF

- CSTR cleared software, SCL is released
- WRIF is set
- NACKIF is set

- Data byte written to I2CxADBF
- Second data byte to I2CxADBF
- Software reads data from I2CxADBF
- Clearing I2CxADBF

- ACKTIF is set
- Slave software sets ACKDT
- ACKT cleared by hardware in 9th rising edge of SCL
- ACKTIF is set

- I2CxCBIF is set
- Software reads data from I2CxCBIF
- Clearing I2CxCBIF

- RXBF
33.4.3.2Slave Transmission (7-bit Addressing Mode)

This section describes the sequence of events for the I²C module configured as an I²C slave in 7-bit Addressing mode and is transmitting data. Figure 33-9 and Figure 33-10 are used as a visual reference for this description.

1. Master asserts Start condition (can also be a restart) on the bus. Start condition Interrupt Flag (SCIF) in I2CxPIR register is set.
2. If Start condition interrupt is enabled (SCIE bit is set), generic interrupt I2CxIF is set.
3. Master transmits eight bits – 7-bit address and R/W = 1.
4. Received address is compared with the values in I2CxADR0/I2CxADR1/I2CxADR2/I2CxADR3 registers. Refer to Section 33.4.1 “Slave Addressing Modes” for Slave Addressing modes.
5. If address matches; SMA in I2CxSTAT0 register is set, R/W is copied to R/W bit, D/A bit is cleared. If the address does not match; module becomes idle.
6. The matched address data is loaded into I2CxADB0 and ADRIF in I2CxPIR register is set.
7. If Address hold interrupt is enabled (ADRIE = 1), CSTR is set. I2CxIF is set. Slave software can read address from I2CxADB0 and set/clear ACKDT before releasing SCL. SCL line can be released by clearing CSTR.
8. If the transmit buffer is empty from the previous transaction, i.e., TXBE = 1 and I2CxCNT!= 0 (I2CxTXIF = 1), CSTR is set. Slave software must load data into I2CXTXB to release SCL. I2CxCNT decrements after the byte is loaded into the shift register.
9. Slave hardware waits for 9th SCL pulse with ACK data from master.
10. If I2CxCNT = 0, CNTIF is set.
11. If the Acknowledge interrupt and hold is enabled (ACKTIE = 1), CSTR is set, I2CxIF is set.
12. Slave software can change the value of ACKDT before releasing SCL by clearing CSTR.
13. Master sends eight SCL pulses to clock out data or asserts a Stop condition to end the transaction.
FIGURE 33-9: I2C SLAVE, 7-BIT ADDRESS, TRANSMISSION

Slave Transmitting Data

Master Releases SDA
Slave sends ACK

Master sends ACK
Slave Transmitting Data

Master sends NACK

Master sends NACK
stop condition

SDA

S

A7 A6 A5 A4 A3 A2 A1

D7 D6 D5 D4 D3 D2 D1 D0

D7 D6 D5 D4 D3 D2 D1 D0

ACKSTAT

ACKTIE = 1

SDA

S

A7 A6 A5 A4 A3 A2 A1

D7 D6 D5 D4 D3 D2 D1 D0

D7 D6 D5 D4 D3 D2 D1 D0

CSTR

SCIF is set
ADRIF is set
Software write to I2CxB, clears CSTR

R/W

SDA

S

A7 A6 A5 A4 A3 A2 A1

D7 D6 D5 D4 D3 D2 D1 D0

D7 D6 D5 D4 D3 D2 D1 D0

ACKSTAT

ACKTIE = 0

R/W copied from matching address

D/A

SDA

S

A7 A6 A5 A4 A3 A2 A1

D7 D6 D5 D4 D3 D2 D1 D0

D7 D6 D5 D4 D3 D2 D1 D0

I2CxCNT

Software writes I2CxCNT

0x02

0x01

0x00

TXBE

TXIF is set for read address when TXBE = 1
value in I2CxCNT is ignored
Software write to I2CxB, clears CSTR
MSb is of I2CxB copied to SDA
Data byte 1 loaded from I2CxB to shifter
TXIF set

Software writes I2CxB
MSb is of I2CxB copied to SDA
Data byte 2 loaded from I2CxB to shifter
TXIF NOT set

NACKIF is set

PCIF is set

TXIF NOT set

No new TX data on I2CxCNT = 0 (shifter loaded 8'b1111 1111)

Master Releases SDA
Slave sends ACK

ACKTIE = 0

TXIF is set

Software write to I2CxB, clears CSTR
MSb is of I2CxB copied to SDA
Data byte 1 loaded from I2CxB to shifter
TXIF set

ACKTIF is set

SCIF is set

PCIF is set

TXIF NOT set

PCIF is set

TXIF NOT set

No new TX data on I2CxCNT = 0 (shifter loaded 8'b1111 1111)
**FIGURE 33-10: I²C SLAVE, 7-BIT ADDRESS, TRANSMISSION (NO CLOCK STRETCHING)**

- **SDA**
  - A7 A6 A5 A4 A3 A2 A1
  - Master Releases SDA
  - Slave sends ACK
  - Master sends ACK
  - Slave Transmitting Data
  - Slave Transmitting Data
  - Master sends ACK
  - Master sends NACK (stop condition)

- **SCL**
  - D7 D6 D5 D4 D3 D2 D1 D0

- **CSTR**
  - SCIF is set
  - ADRIE = 0
  - ACKTIE = 0
  - PCIF is set

- **R/W**
  - R/W copied from matching address
  - ADRIF is set
  - ACKTIF is set
  - ACKTIF is set

- **D/A**
  - matching address copy to I²CxADB0

- **ACKSTAT**
  - Master’s ACK copied to ACKSTAT
  - NACKIF is set

- **I²CxCNT**
  - 0x02
  - 0x01
  - 0x00

- **TXBE**
  - Before Start, software loads one byte in I²CxTXB
  - MSb is of I²CxTXB copied to SDA
  - Data byte 1 loaded from I²CxTXB to shifter
  - TXIF set
  - Software writes I²CxTXB
  - MSb is of I²CxTXB copied to SDA
  - Data byte 2 loaded from I²CxTXB to shifter
  - I²CXTXIF NOT set
  - No new TX data on I²CxCNT = 0
    - (shifter loaded 8'b1111 1111)
  - I²CxtXIF NOT set
33.4.3.3 Slave operation in 10-bit Addressing Mode

In 10-bit Addressing mode, the first received byte is compared to the binary value of '11110A9A80'. A9 and A8 are the two MSb of the 10-bit address. The first byte is compared with the value in I2CxADR1 and I2CxADR3 registers. After the high byte is acknowledged, the low address byte is clocked in and all eight bits are compared to the low address value in the I2CxADR0 and I2CxADR2 registers. A high and low address match as a write request is required at the start of all 10-bit addressing communication. To initiate a read, the master needs to issue a Restart once the slave is addressed and clock in the high address with the R/W bit set. The slave hardware will then acknowledge the read request and prepare to clock out data. The SMA (slave active) bit is set only when both the high and low address bytes match.

Note: All seven bits of the received high address are compared to the values in the I2CxADR1 and I2CxADR3 registers. The five-bit '11110' high address format is not enforced by module hardware. It is up to the user to configure these bits correctly.

33.4.3.4 Slave Reception (10-bit Addressing Mode)

This section describes the sequence of events for the I2C module configured as an I2C slave in 10-bit Addressing mode and is receiving data. Figure 33-11 is used as a visual reference for this description.

1. Master asserts Start condition (can also be a restart) on the bus. Start condition Interrupt Flag (SCIF) in I2CxPIR register is set. If Start condition interrupt is enabled (SCIE bit is set), generic interrupt I2CxIF is set.
2. Master transmits high address byte with R/W = 0.
3. The received high address is compared with the values in I2CxADR1 and I2CxADR3 registers.
4. If high address matches; R/W is copied to R/W bit, D/A bit is cleared, high address data is copied to I2CxADB1. If the address does not match; module becomes idle.
5. If Address hold interrupt is enabled (ADRIE = 1), CSTR is set. I2CxIF is set.
6. Slave software can read high address from I2CxADB1 and set/clear ACKDT before releasing SCL.
7. ACKDT value is copied out to SDA for ACK pulse. SCL line is released by clearing CSTR.
8. Master sends ninth SCL pulse for ACK.
9. Slave can force a NACK at this point due to previous error not being cleared. E.g. Receive buffer overflow or transmit buffer underflow errors. In these cases the slave hardware forces a NACK and the module becomes Idle.
10. Master transmits low address data byte
11. If the low address matches; SMA is set, ADRIF is set, R/W is copied to R/W bit, D/A bit is cleared, low address data is copied to I2CxADB0, and ACTDT is copied to SDA. If the address does not match; module becomes Idle.
12. If address hold interrupt is enabled, the CSTR bit is set as mentioned in step 6. Slave software can read low address byte from I2CxADB0 register and change ACKDT value before releasing SCL.
13. Master sends ninth SCL pulse for ACK.
14. If the Acknowledge interrupt and hold is enabled (ACKTIE = 1), CSTR is set, I2CxIF is set.
15. Slave software can read address from I2CxADB0 and I2CxADB1 registers and change the value of ACKDT before releasing SCL by clearing CSTR.
16. Master sends first seven SCL pulses of the data byte or a Stop condition (in the case of NACK).
17. If Stop condition; PCIF in I2CxPIR register is set, module becomes Idle.
18. If the receive buffer is full from the previous transaction i.e. RXBF = 1 (I2CxRXIF = 1), CSTR is set. Slave software must read data out of I2CxRXB to resume communication.
19. Master sends eighth SCL pulse of the data byte. D/A bit is set, WRIF is set. I2CxRXB is loaded with new data, RXBF bit is set.
20. If Data write interrupt and hold is enabled (WRIE = 1), CSTR is set, I2CxIF is set. Slave software can read data from I2CxRB and set/clear ACKDT before releasing SCL by clearing CSTR.
21. If I2CxCNT = 0, the ACKCNT value is output to the SDA; else, the ACKDT value is used and the value of I2CxCNT is decremented.
22. Master sends SCL pulse for ACK.
23. If I2CxCNT = 0, CNTIF is set.
24. If the response was a NACK; NACKIF is set, module becomes idle.
25. If ACKTIE = 1, CSTR is set, I2CxIF is set. Slave software can read data from I2CxRXB clearing RXBF; before releasing SCL by clearing CSTR.
26. Go to step 16.
FIGURE 33-11: \( \text{I}^2\text{C} \text{ SLAVE, 10-BIT ADDRESS, RECEPTION WITH STOP (ADB = 1)} \)

- **SDA**: S
- **SCL**: 1
- **ADRIE = 0**: R/W copied from matching address, ADRIF is set
- **SMA**: R/W = 0 from I2CxADB[0]
- **RXBF**: I2CxRXIF is set, Software reads address from I2CxRXB, Clearing I2CxRXIF

1. **Receive Data**
2. **Receive Low Address**
3. **Receive High Address**
4. **High Address copied to I2CxRXB**
5. **Low Address copied to I2CxRXB**
6. **ACKTIF NOT set for high address /w**
7. **ACKTIF is set**
8. **ACKTIE = 0**
9. **PCIF is set**
10. **SCIF is set**
11. **ADRIF is set**
12. **ADRIE = 0**
13. **ACKTIF is set**
14. **ACKTIF is set**
15. **SMA set only after full address match**
16. **Hardware clears SMA**
33.4.3.5 Slave Transmission (10-bit Addressing Mode)

This section describes the sequence of events for the \( I^2\!C \) module configured as an \( I^2\!C \) slave in 10-bit Addressing mode and is transmitting data. Figure 33-12 is used as a visual reference for this description.

1. Master asserts Start condition (can also be a restart) on the bus. Start condition Interrupt Flag (SCIF) in \( I^2\!C \)XPIR register is set. If Start condition interrupt is enabled (SCIE bit is set), generic interrupt \( I^2\!C \)IF is set.
2. Master transmits high address byte with R/W = 0.
3. The received high address is compared with the values in \( I^2\!C \)xADR1 and \( I^2\!C \)xADR3 registers.
4. If high address matches; R/W is copied to R/W bit, D/A bit is cleared, high address data is copied to \( I^2\!C \)xADB1. If the address does not match; module becomes Idle.
5. If Address hold interrupt is enabled (ADRIE = 1), CSTR is set. \( I^2\!C \)IF is set.
6. Slave software can read high address from \( I^2\!C \)xADB1 and set/clear ACKDT before releasing SCL.
7. ACKDT value is copied out to SDA for ACK pulse. SCL line is released by clearing CSTR.
8. Master sends ninth SCL pulse for ACK.
9. Slave can force a NACK at this point due to previous error not being cleared. E.g. Receive buffer overflow or transmit buffer underflow errors. In these cases the slave hardware forces a NACK and the module becomes Idle.
10. Master transmits low address data byte.
11. If the low address matches; SMA is set, adrIF is set, R/W is copied to R/W bit, D/A bit is cleared, low address data is copied to \( I^2\!C \)xADB0, and ACTDT is copied to SDA. If the address does not match; module becomes Idle.
12. If address hold interrupt is enabled, the CSTR bit is set as mentioned in step 6. Slave software can read low address byte from \( I^2\!C \)xADB0 register and change ACKDT value before releasing SCL.
13. Master sends 9th SCL pulse for ACK.
14. If the Acknowledge interrupt and hold is enabled (ACKTIE = 1), CSTR is set, \( I^2\!C \)IF is set.
15. Slave software can read address from \( I^2\!C \)xADB0 and \( I^2\!C \)xADB1 registers and change the value of ACKDT before releasing SCL by clearing CSTR.
16. Master asserts Restart condition (cannot be Start) on the bus. Restart Condition Interrupt Flag (RSCIF) is set. If the Restart Condition Interrupt is enabled, generic interrupt \( I^2\!C \)IF is set.
17. Master transmits high address byte with R/W = 1.
FIGURE 33-12:  I2C SLAVE, 10-BIT ADDRESS, TRANSMISSION

Master sends start event

S

1 1 1 1 0 A9 A8

ACK

A7 A6 A5 A4 A3 A2 A1 A0

ACK

Master sends restart event

Sr

1 1 1 0 A9 A8

D7 D6 D5 D4 D3 D2 D1 D0

Transmit data loaded from I2CxB to TX shift reg

ACK

S

R/W = 0

High Address copied to I2CxADB1[7:0]

Low Address copied to I2CxADB0[7:0]

R/W = 1

High Address copied to I2CxADB1[7:0]

R/W copied from matching address

ADRIF is set

ACKTIE NOT set for high address /w

D/A

matching address R/W value copied

R/W

RSIF is set

SCIF is set

SMA

Hardware clears SMA

CSTR

Full matching address

PCIF is set

R/W copied from matching address

ADRIF is set

ACKTIE is set

ACKTIE is set

ACKTIE is set

TXBE

I2CxTXIF is set

Software loads I2CxB

I2CxCNT

0x00

0x00

Software loads I2CxCNT

Master sends stop event

Master sends NACK
33.5 \( \textit{I}^2\text{C} \) Master Mode

Master mode is enabled by setting and clearing the appropriate Mode<2:0> bits in I2CxCON and then by setting the I2CEN bit. Master mode of operation is supported by interrupt generation on buffer full (RXIF), buffer empty (TXIF), and the detection of the Start, Restart, and Stop conditions. The Stop (P), Restart (RS) and Start (S) bits are cleared from a Reset or when the \( \textit{I}^2\text{C} \) module is disabled. Control of the \( \textit{I}^2\text{C} \) bus is asserted when the BFRE bit of I2CSTAT0 is set.

33.5.1 \( \textit{I}^2\text{C} \) MASTER MODE OPERATION

The master device generates all of the serial clock pulses and the Start, Restart, and Stop conditions. A transfer is ended with a Stop condition or with a Restart condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the \( \textit{I}^2\text{C} \) bus will not be released, and MMA bit will stay set signifying that the master module is still active.

The steps to initiate a transaction depends on the setting of the address buffer disable bit (ABD) of the I2CxCON2 register.

- **ABD = 0** (Address buffers are enabled)
  
  In this case, the master module will use the address stored in the address buffer registers (I2CxADBO/1) to initiate communication with a slave device. User software needs to set the Start bit (S) in the I2CxCON0 register to start communication. This is valid for both 7-bit and 10-bit Addressing modes.

- **ABD = 1** (Address buffers are disabled)
  
  In this case, the slave address is transmitted through the transmit buffer and the contents of the address buffers are ignored. User software needs to write the slave address to the transmit buffer (I2CxTXB) to initiate communication. Writing to the Start bit is ignored in this mode. This is valid for both 7-bit and 10-bit Addressing modes.

33.5.1.1 Master Transmitter

In Master Transmitter mode, the first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/W) bit. In the case of master transmitter, the R/W bit will be logic ‘0’. Serial data is transmitted eight bits at a time. After each byte is transmitted, an Acknowledge bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

33.5.1.2 Master Receiver

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/W bit. In this case, the R/W bit will be logic ‘1’. Thus, the first byte transmitted is a 7-bit slave address followed by a ‘1’ to indicate the receive bit. Serial data is received via SDA, while SCL outputs the serial clock. Serial data is received eight bits at a time.

After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions indicate the beginning and end of the transmission.

33.5.2 MASTER CLOCK SOURCE AND ARBITRATION

The \( \textit{I}^2\text{C} \) module clock source is selected by the I2CxCLK register. The \( \textit{I}^2\text{C} \) clock provides the SCL output clock for Master mode and is used by the Bus Free timer. The \( \textit{I}^2\text{C} \) clock can be sourced from several peripherals.

33.5.3 BUS FREE TIME

In Master modes, the BFRE bit of the I2CSTAT0 register gives an indication of the bus idle status. The master hardware cannot assert a Start condition until this bit is set by the hardware. This prevents the master from colliding with other masters that may already be talking on the bus. The BFRET<1:0> bits of I2CxCON1 allow selection of 8 to 64 pulses of the \( \textit{I}^2\text{C} \) clock input before asserting the BFRE bit. The BFRET bits are used to ensure that the \( \textit{I}^2\text{C} \) module always follows the minimum Stop Hold Time. The \( \textit{I}^2\text{C} \) timing requirements are listed in the electrical specifications chapter.

\textbf{Note:} \( \textit{I}^2\text{C} \) clock is not required to have a 50% duty cycle.

33.5.4 MASTER CLOCK TIMING

The clock generation in the \( \textit{I}^2\text{C} \) module can be configured using the Fast Mode Enable (FME) bit of the I2CxCON2 register. This bit controls the number of times the SCL pin is sampled before the master hardware drives it.

33.5.4.1 Clock Timing with FME = 0

One Tscl, consists of five clocks of the \( \textit{I}^2\text{C} \) clock input. The first clock is used to drive SCL low, the third releases SCL high. The fourth and fifth clocks are used to detect if the SCL pin is, in fact, high or being stretched by a slave.

If a slave is clock stretching, the hardware waits; checking SCL on each successive \( \textit{I}^2\text{C} \) clock, proceeding only after detecting SCL high. **Figure 33-13** shows the clock synthesis timing when FME = 0.
33.5.4.2 Clock Timing with FME = 1

One TSCL, consists of four clocks of the I2C clock input. The first clock is used to drive SCL low, the third releases SCL high, and the fourth is used to detect if the clock is, in fact, high or being stretched by a slave.

If a slave is clock stretching, the hardware waits; checking SCL on each successive I2C clock, proceeding only after detecting SCL high. Figure 33-14 shows the clock synthesis timing when FME = 1.
33.5.5 I²C MASTER MODE START CONDITION TIMING

The user can initiate a Start condition by either writing to the Start bit (S) of the I2CxCON0 register or by writing to the I2CxTXB register based on the ABD bit setting. Master hardware waits for BFRE = 1, before asserting the Start condition. The action of the SDA being driven low while SCL is high is the Start condition, causing the SCIF bit to be set. One TSCL later the SCL is asserted low, ending the start sequence. Figure 33-15 shows the Start condition timing.

**FIGURE 33-15: START CONDITION TIMING**

33.5.6 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition occurs when the Start bit of the I2CxCON0 register is set and the master module is waiting from a Restart clock stretch event (RSEN = 1 and I2CxCNT = 0).

When the Start bit is set, the SDA pin is released high for TSCL/2. Then the SCL pin is released floated high for TSCL/2. If the SDA pin is detected low, bus collision flag (BCLIF) is set and the master goes idle. If SDA is detected high, the SDA pin will be pulled low (Start condition) for TSCL. Last, SCL is asserted low and I2CxADB0/1 is loaded into the shift register. As soon as a Restart condition is detected on the SDA and SCL pins, the RSCIF bit is set. Figure 33-16 shows the timings for repeated Start Condition.
33.5.7 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled automatically following an address/data byte transmission. The SCL pin is pulled low and the contents of the Acknowledge Data bits (ACKDT/ACKCNT) are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The master then waits one clock period (TSCl) and the SCL pin is released high. When the SCL pin is sampled high (clock arbitration), the master counts another TSCl. The SCL pin is then pulled low. Figure 33-17 shows the timings for Acknowledge sequence.

33.5.8 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of receive/transmit when I2CxCNT = 0. After the last byte of a receive/transmit sequence, the SCL line is held low. The master asserts the SDA line low. The SCL pin is then released high TSCl/2 later and is detected high. The SDA pin is then released. When the SDA pin transitions high while SCL is high, the PCIF bit of the I2CxIF register is set. Figure 33-18 shows the timings for a Stop condition.
33.5.9 MASTER TRANSMISSION IN 7-BIT ADDRESSING MODE

This section describes the sequence of events for the I²C module configured as an I²C master in 7-bit Addressing mode and is transmitting data. Figure 33-19 is used as a visual reference for this description.

1. If ABD = 0; i.e., Address buffers are enabled

Master software loads number of bytes to be transmitted in one sequence in I2CxCNT, slave address in I2CxADB1 with R/W = 0 and the first byte of data in I2CxTXB. Master software has to set the Start (S) bit to initiate communication.

   If ABD = 1; i.e., Address buffers are disabled

Master software loads the number of bytes to be transmitted in one sequence in I2CxCNT and the slave address with R/W = 0 into the I2CxTXB register. Writing to the I2CxTXB will assert the start condition on the bus and sets the S bit. Software writes to the S bit are ignored in this case.

2. Master hardware waits for BFRE bit to be set; then shifts out start and address.

3. If the transmit buffer is empty (i.e., TXBE = 1) and I2CxCNT! = 0, the I2Ctxtxf and MDR bits are set and the clock is stretched on the 8th falling SCL edge. Clock can be started by loading the next data byte to I2Ctxtxb register.

4. Master sends out the 9th SCL pulse for ACK.

5. If the master hardware receives ACK from slave device, it loads the next byte from the transmit buffer (I2Ctxtxb) into the shift register and the value of I2CxCNT register is decremented.

6. If a NACK was received, master hardware asserts Stop or Restart

7. If ABD = 0; i.e., Address buffers are enabled

If I2CxCNT = 0, Master hardware sends Stop or sets MDR if RSEN = 1 and waits for the software to set the Start bit again to issue a restart condition.

If ABD = 1; i.e., Address buffers are disabled

If I2CxCNT = 0, Master hardware sends Stop or sets MDR if RSEN = 1 and waits for the software to write the new address to the I2Ctxtxb register. Software writes to the S bit are ignored in this case.

8. Master hardware outputs data on SDA.

9. If TXBE = 1 and I2CxCNT! = 0, I2Ctxtxf and MDR bits are set and the clock is stretched on 8th falling SCL edge. The user can release the clock by writing the next data byte to I2Ctxtxb register.

10. Master hardware clocks in ACK from slave, and loads the next data byte from I2Ctxtxb to the shift register. The value of I2CxCNT is decremented.

**FIGURE 33-19: I²C MASTER, 7-BIT ADDRESS, TRANSMISSION WITH STOP**

- **SDA**
  - A7 A6 A5 A4 A3 A2 A1
  - Address copied from I²CxADB1[7:1]

- **SCL**
  - 2 3 4 5 6 7 8 9

- **MMA**
  - Software sets START to start transmission
  - SCIF is set

- **ACKSTAT**
  - 0x01

- **I²CxCNT**
  - 0x02
  - 0x01
  - 0x00
  - CNTIF is set
  - I²CxCNT = 0
  - RSEN = 0, master sends Stop

- **TXBE**
  - Before Start, software loads one byte in I²C𝕏TXB
  - MSb is of I²C𝕏TXB copied to SDA
  - Data byte loaded from I²C𝕏TXB to shifter
  - I²C𝕏TXF is set

  - Software writes I²C𝕏TXB
  - MSb is of I²C𝕏TXB copied to SDA
  - Second data byte loaded from I²C𝕏TXB to shifter
  - I²C𝕏TXF NOT set

  - No new TX data on I²CxCNT = 0
  - (shifter loaded 8'b1111 1111)
  - I²C𝕏TXF NOT set
33.5.10 MASTER RECEPTION IN 7-BIT ADDRESSING MODE

This section describes the sequence of events for the \( \text{I}^2\text{C} \) module configured as an \( \text{I}^2\text{C} \) master in 7-bit Addressing mode and is receiving data. Figure 33-20 is used as a visual reference for this description.

1. Master software loads slave address in \( \text{I2CxADB1} \) with \( \text{R/W} \) bit = d and number of bytes to be received in one sequence in \( \text{I2CxCNT} \) register.
2. Master hardware waits for \( \text{BFRE} \) bit to be set; then shifts out start and address with \( \text{R/W} = 1 \).
3. Master sends out the 9\textsuperscript{th} SCL pulse for ACK, master hardware clocks in ACK from slave
4. If \( \text{ABD} = 0 \); i.e., Address buffers are enabled
   - If NACK, master hardware sends Stop or sets MDR (if \( \text{RSEN} = 1 \)) and waits for user software to write to S bit for restart.
   - If \( \text{ABD} = 1 \); i.e., Address buffers are disabled
   - If NACK, master hardware sends Stop or sets MDR (if \( \text{RSEN} = 1 \)) and waits for user software to load the new address into \( \text{I2CxTXB} \). Software writes to the S bit are ignored in this case.
5. If ACK, master hardware receives 7 bits of data into the shift register.
6. If the receive buffer is full (i.e., \( \text{RXBF} = 1 \)), clock is stretched on 7\textsuperscript{th} falling SCL edge.
7. Master software must read previous data out of \( \text{I2CxRXB} \) to clear \( \text{RXBF} \).
8. Master hardware receives 8\textsuperscript{th} bit of data into the shift register and loads it into \( \text{I2CxRXB} \), sets \( \text{I2CxRXIF} \) and \( \text{RXBF} \) bits. \( \text{I2CxCNT} \) is decremented.
9. If \( \text{I2CxCNT}! = 0 \), master hardware clocks out \( \text{ACKDT} \) as ACK value to slave. If \( \text{I2CxCNT} = 0 \), master hardware clocks out \( \text{ACKCNT} \) as ACK value to slave. It is up to the user to set the values of \( \text{ACKDT} \) and \( \text{ACKCNT} \) correctly. If the user does not set \( \text{ACKCNT} \) to '1', the master hardware will never send a NACK when \( \text{I2CxCNT} \) becomes zero. Since a NACK was not seen on the bus, the master hardware will also not assert a Stop condition.
FIGURE 33-20: \(^2\text{C MASTER, 7-BIT ADDRESS, RECEPTION}\)

- Slave Sends ACK
  - R/W = 1 from I2CxADB1[0]
- Master sends ACK
- Slave Transmitting Data
- Slave Sends ACK
- Master sends ACK
- Slave Transmitting Data
- Master sends NACK
  - RSEN = 0; Master sends stop condition
- Slave Address copied from I2CxADB1[7:1]
- Software sets START to start transmission
- Hardware clears MMA
- SCIF is set
- PCIF is set
- Master's ACK copied from ACKDT
- NACK on CNT= 0
  - NACKIF is set
- Software reads data from I2CxRXB
- I2CxRXIF is set
  - Software reads I2CxRXB
- Software reads data from I2CxRXB
33.5.11 MASTER TRANSMISSION IN 10-BIT ADDRESSING MODE

This section describes the sequence of events for the I\(^2\)C module configured as an I\(^2\)C master in 10-bit Addressing mode and is transmitting data. Figure 33-21 is used as a visual reference for this description.

1. If ABD = 0; i.e., Address buffers are enabled
   Master software loads number of bytes to be transmitted in one sequence in I2CxCNT, high address byte of slave address in I2CxADB1 with R/W = 0, low address byte in I2CxADB0 and the first byte of data in I2CxTXB. Master software has to set the Start (S) bit to initiate communication.

2. Master hardware waits for BFRE bit to be set; then shifts out the start and high address and waits for acknowledge.

3. If NACK, master hardware sends Stop.

4. If ABD = 0; i.e., Address buffer are enabled
   If ACK, master hardware sends the low address byte from I2CxADB0.

5. If TXBE = 1 and I2CxCNT! = 0, I2CxTXIF and MDR bits are set. Clock is stretched on 8th falling SCL edge till master software writes next data byte to I2CxTXB.

6. Master hardware sends ninth SCL pulse for ACK from slave and loads the shift register from I2CxTXB. I2CxCNT is decremented.

7. If slave sends a NACK, master hardware sends Stop and ends transmission.

8. If slave sends an ACK, master hardware outputs data in the shift register on SDA. I2CxCNT value is checked on the 8th falling SCL edge. If I2CxCNT = 0; master hardware sends 9th SCL pulse for ACK and CNTIF is set.

9. If I2CxCNT! = 0; go to step 5.
FIGURE 33-21: i²C MASTER, 10-BIT ADDRESS, TRANSMISSION WITH STOP

SDA

1 1 1 1 0 A9 A8

S

ACK

A7 A6 A5 A4 A3 A2 A1 A0

ACK

D7 D6 D5 D4 D3 D2 D1 D0

ACK

Transmitting Data

High Address copied from I2CxADB1[7:1]

Low Address copied from I2CxADB0[7:0]

From Slave to Master

MMA

Software sets START to start transmission

SCIF is set

Hardware clears MMA

PCIF is set

ACKSTAT

0x01

I2CxNT

0x01

0x00

CNTIF is set

I2CxNT = 0

Master sends Stop

TXBE

Before Start, software loads one byte in I2CxTXB

I2CxTXIF NOT set

Data byte loaded from I2CxTXB to shifter

No new TX data on I2CxCNT = 0 (shifter loaded 8'b1111 1111)

I2CxTXIF NOT set
33.5.12 MASTER RECEPTION IN 10-BIT ADDRESSING MODE

This section describes the sequence of events for the \textit{I^2C} module configured as an \textit{I^2C} master in 10-bit Addressing mode and is receiving data. Figure 33-22 is used as a visual reference for this description.

1. Master software loads high address byte in I2CxADB1 and low address byte in I2CxADB0 for write and sets restart enable (RSTEN) bit.
2. Master software sets START bit.
3. Master hardware waits for BFRE bit to be set; then shifts out start, high address and waits for acknowledge.
4. If slave responds with a NACK, master hardware sends Stop and ends communication.
5. If slave responds with ACK, master hardware shifts out the low address.
6. If the transmit buffer empty flag (TXBE) is set and I2CxCNT! = 0, the clock is stretched on 8th falling SCL edge. Allowing master software writes next data to I2CxTXB.
7. Master hardware sends 9th SCL pulse for ACK from slave and loads the shift register from I2CxTXB.
8. If slave responds with a NACK, master hardware sends Stop and ends communication.
9. If slave responds with an ACK and I2CxCNT = 0, master hardware sets MDR bit, go to Step 11.
10. If slave responds with an ACK and I2CxCNT! = 0, master hardware outputs data in shift register on SDA and waits for ACK from slave. Go to step 4.
11. Master software loads I2CxADB0 for read, and I2CCNT with the number of bytes to be received in the current transaction.
12. Master software sets Start bit.
13. Master hardware shifts out Restart and high address with R/W = 1.
14. Master sends out 9th SCL pulse for ACK from slave.
15. If slave responds with a NACK, master hardware sends Stop or sets MDR (RSEN bit).
16. If slave responds with an ACK, master hardware shifts 7 bits of data into the shift register from the slave.
17. If the receive buffer full flag (RXBF) is set, clock is stretched on seventh falling SCL edge.
18. Master software can clear clock stretching by reading the previous data in the receive buffer.
19. Master hardware shifts 8th bit of data into the shift register from slave and loads it into I2CxRXB.
20. Master software reads data from I2CxRXB register.
21. If I2CxCNT! = 0, master hardware clocks out ACKDT as ACK value to slave.
22. If I2CxCNT = 0, master hardware clocks out ACKCNT as ACK value to slave.
23. Go to step 4.
FIGURE 33-22: I2C MASTER, 10-BIT ADDRESS, RECEPTION (USING RSTEN BIT)
33.6 I²C Multi-Master Mode

In Multi-Master mode, the bus-free (BFRE) bit allows the master to determine when the bus is free. Control of the I²C bus may be taken when the BFRE bit of the I2CxSTAT0 register is set. Interrupt generation on the detection of a slave address match, ADRIE; causes a clock stretch and allows user software to respond to the master being addressed as a slave device. The Slave Active (SMA) bit is set for a matching received slave address.

Clock arbitration occurs when the master, during any receive, transmit or Restart/Stop condition, releases the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the SCL line is monitored to see if the pin is actually sampled high.

In master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed by hardware with the result placed in the BCLIF bit. MSTACK is cleared when BCLIF is set. The states where arbitration can be lost are:
- Address Transfer
- Data Transfer (master write)
- Repeated Start Condition
- Acknowledge Condition

33.6.1 MULTI-MASTER MODE BUS COLLISION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a ‘1’ on SDA, by letting SDA float high and another master asserts a ‘0’. When the SCL pin floats high, data is stable. If the expected data on SDA is a ‘1’ and the data sampled on the SDA pin is ‘0’, then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLIF and reset the I²C bus to its Idle state. Refer to Figure 33-23 for a detailed timing diagram.

Note: In this mode, the slave hardware has priority over the master hardware. Master mode communication can only be initiated when the SMA = 0.

If transmission was in progress when the bus collision occurred, the SDA and SCL lines are released. If a Repeated Start, Stop or Acknowledge was in progress when the bus collision occurred, the action is aborted; the SDA and SCL lines are released. The BCLIF condition must be cleared by software to allow an ACK to be shifted out on the bus again, until then the module will always respond with a NACK. Refer to Figure 33-24 for a detailed timing diagram of a transaction in Multi-Master mode.
FIGURE 33-24: I2C MULTI-MASTER, 7-BIT ADDRESS, WRITE (ADRIE = 1, WRIE = 0)

- **SDA**
  - Address copied from I2CxADB1

- **SCL**
  - If RX shift register matches I2CxADR:
    - Received Address and RW copied to I2CxADB0[7:0]

- **CSTR**
  - User must use ADRIE bit to interrupt on slave address match
  - CSTR cleared by software

- **SMA**
  - MMA
    - Software sets START
    - Master loses arbitration of address
    - BCLIF is set, hardware clears MMA
    - Continues to clock in slave address

- **MMA**
  - Software sets START

- **ACKDT**
  - ACKDT cleared by software
  - User must clear BCLIF to send ACK

- **I2CxCNT**
  - Software updates I2CxCNT for Slave receive message
  - 0x00
  - 0x01
  - 0x02

- **RXBF**
  - I2C RXIF is set
  - Software reads data from I2C RXB

- **ACK**
  - Received Data
  -ACK

- Another Master clocks ACK and begins sending data
- Other Master sends stop condition

- **RXBF**
  - I2C RXIF is set
  - Software reads I2C RXB
33.7 Register Definitions: I2C Control

This section defines all the registers associated with the control and status of the I2C bus.

REGISTER 33-1: I2CxCON0: I2C CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W/HC/HS-0</th>
<th>R/C/HS/HC-0</th>
<th>R-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN(1,2)</td>
<td>RSEN</td>
<td>S</td>
<td>CSTR(3)</td>
<td>MDR</td>
<td>MODE &lt;2:0&gt;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **1** = Bit is set
- **0** = Bit is cleared

**bit 7**
- **EN**: I2C Module Enable bit
  - **1** = Enables the I2C module
  - **0** = Disables the I2C module.

**bit 6**
- **RSEN**: Restart Enable bit (Only mode<2:0> = 1xx)
  - **1** = When (I2CCNT = 0 or ACKSTAT = 1), on 9th falling SCL sets MDR.
  - **0** = When (I2CCNT = 0 or ACKSTAT = 1), on 9th falling SCL; master shifts out a Stop condition

**bit 5**
- **S**: Master Start/Restart bit (Only Mode<2:0> = 1xx)
  - When MMA = 0
    - **1** = Set by user set of START bit or write to I2CTXB, waits for BFRE = 1 to begin with a Start
    - **0** = Cleared by hardware after sending Start
  - When (MMA = 1 & MDR = 1 & pause_for_Restart)
    - **1** = Set by user set of START bit or write to I2CTXB, resumes communication with a Restart
    - **0** = Cleared by hardware after sending Restart
  - Else - Writes to I2CTXB or set has no effect on Start bit

**bit 4**
- **CSTR**: Slave Clock Stretching bit (3)
  - **1** = Clock is held low (clock stretching)
  - **0** = Enable clocking, SCL control is released

- **SMA = 1 and RXBF = 1(6)**
  - Set by hardware on 7th falling SCL edge
  - User must read byte I2CRXB to release SCL

- **SMA = 1 and TXBE = 1 and I2CCNT!= 0**
  - Set by hardware on 8th falling SCL edge
  - User must write byte to I2CTXB to release SCL

when **ADRIE is set (4)**
- Set by hardware on 8th falling SCL edge of matching received address
  - User must clear CSTR to release SCL

- **SMA = 1 & WRIE = 1**
  - Set by hardware on 8th falling SCL edge of received data byte
  - User must clear CSTR to release SCL

- **SMA = 1 & ACKTIE = 1**
  - Set by hardware on 9th falling SCL edge
  - User must clear CSTR to release SCL
bit 3  MDR: Master Data Request (Master pause)
1 = Master state machine pauses until data is read/written to proceed (SCL is output held low)
0 = Master clocking of data is enabled.

MMA = 1 & RXBF = 1
pause_for_rx - Set by hardware on 7th falling SCL edge
- User must read from I2CRXB to release SCL

MMA = 1 & TXBE = 1 & I2CCNT!= 0
pause_for_tx - Set by hardware on 8th falling SCL edge
- User must write to I2CTXB to release SCL

ADB = 1
- I2CCNT is ignored for the high and low address in 10-bit mode

pause_for_restart - Set by hardware on 9th falling SCL edge
RSEN = 1 & MMA = 1 && I2CCNT = 0 || ACKSTAT = 1
- User must set START or write to I2CTXB to release SCL and shift Restart onto bus

bit 2-0  MODE<2:0>: I2C Mode Select bits
111 = I2C Multi-Master mode (SMBus 2.0 Host), (5)
Works as both mode<2:0> = 001 and mode<2:0> = 100
110 = I2C Multi-Master mode (SMBus 2.0 Host), (5)
Works as both mode<2:0> = 000 and mode<2:0> = 100
101 = I2C Master mode, 10-bit address
100 = I2C Master mode, 7-bit address
011 = I2C Slave mode, one 10-bit address with masking
010 = I2C Slave mode, two 10-bit address
001 = I2C Slave mode, two 7-bit address with masking
000 = I2C Slave mode, four 7-bit address

Note 1: SDA and SCL pins must be configured for open-drain with internal or external pull-up
2: SDA and SCL pins must be selected as both input and output in PPS
3: CSTR can be set by more than one hardware source, all sources must be addressed by user software before the SCL line is released. CSTR is a module Status bit, and does not show the true bus state.
4: SMA is set on the same SCL edge as CSTR for a matching received address
5: In this mode, ADRIE should be set, this allows an interrupt to clear the BCLIF condition and allow the ACK of matching address.
6: In 10-bit Slave mode, when ADB = 1, CSTR will set when the high address has not been read out of I2CxRXB before the low address is shifted in.
### REGISTER 33-2: I2CxCON1: I2C CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R-0</th>
<th>U-0</th>
<th>R/W/HS-0</th>
<th>R/W/HS-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACKCNT(2)</td>
<td>ACKDT(1,2)</td>
<td>ACKSTAT</td>
<td>ACKT</td>
<td>—</td>
<td>RXO</td>
<td>TXU</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **u = Bit is unchanged**
- **x = Bit is unknown**
- **-n/n = Value at POR and BOR/Value at all other Resets**
- **'1' = Bit is set**
- **'0' = Bit is cleared**
- **HS = Hardware set**
- **HC = Hardware clear**

#### bit 7
- **ACKCNT**: Acknowledge End of Count bit(2)
  - Acknowledge value transmitted after received data, when I2CCNT = 0
  - 1 = Not Acknowledge (copied to SDA output)
  - 0 = Acknowledge (copied to SDA output)

#### bit 6
- **ACKDT**: Acknowledge Data bit(1,2)
  - Acknowledge value transmitted after matching address
  - Acknowledge value transmitted after received data, when I2CCNT! = 0
  - 1 = Not Acknowledge (copied to SDA output)
  - 0 = Acknowledge (copied to SDA output)

#### bit 5
- **ACKSTAT**: Acknowledge Status bit (Transmission only)
  - 1 = Acknowledge was not received for most recent transmission
  - 0 = Acknowledge was received for most recent transmission

#### bit 4
- **ACKT**: Acknowledge Time Status bit
  - 1 = Indicates the I2C bus is in an Acknowledge sequence, set on 8th falling edge of SCL clock
  - 0 = Not in Acknowledge sequence, cleared on 9th rising edge of SCL

#### bit 3
- **Unimplemented**: Read as ‘1’b0

#### bit 2
- **RXO**: Receive Overflow Status bit (MODE<2:0> = 0xx & 11x)
  - This bit can only be set when CSD= 1
  - 1 = Set when SMA = 1, and a master clocks in data when RXBF = 1
  - 0 = No slave overflow condition

#### bit 1
- **TXU**: Transmit Underflow Status bit (MODE<2:0> = 0xx & 11x)
  - This bit can only be set when CSTRDIS = 1
  - 1 = Set when SMA = 1, and a master clocks out data when TXBE = 1
  - 0 = No slave underflow condition

#### bit 0
- **CSD**: Clock Stretching Disable bit (MODE<2:0> = 0xx & 11x)
  - 1 = When SMA = 1, the CSTR bit will never be set
  - 0 = Slave clock stretching proceeds normally

**Note 1:** Software writes to ACKDT bit must be followed by a minimum SDA data-setup time before clearing CSTR.

**Note 2:** NACK may still be generated by I2C hardware when bus errors are indicated in the I2CxSTAT1 or I2CxERR registers.
REGISTER 33-3:  I2CxCON2: I2C CONTROL REGISTER 2

<table>
<thead>
<tr>
<th></th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACNT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GCEN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FME</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SDAHT&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BFRET&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- HS = Hardware set
- HC = Hardware clear

bit 7  **ACNT**: Auto-Load I2C Count Register Enable bit
1 = The first received or transmitted byte after the address, is automatically loaded into the I2CCNT register. The I2CCNT register is loaded at the same time as the value is moved to/from the shifter. ACKDT is used to determine the ACK/NACK value for the address bytes and first data byte of a received message. This prevents a I2CCNT<NACK> from being sent for the byte that would update the I2CCNT register.
0 = Auto-load of I2CCNT disabled

bit 6  **GCEN**: General Call Address Enable bit (MODE<2:0> = 00x & 11x)
1 = General call address, 0x00, causes address match event
0 = General call address disabled

bit 5  **FME**: Fast Mode Enable bit
1 = SCL is sampled high only once before driving SCL low. (F_SCL = FCLK/4)
0 = SCL is sampled high twice before driving SCL low. (F_SCL = FCLK/5)

bit 4  **ADB**: Address Data Buffer Disable bit
1 = Received address data is loaded into both the I2CADB and I2CRXB
   Transmitted address data is loaded from the I2CTXB
0 = Received address data is loaded only into the I2CADB
   Transmitted address data is loaded from the I2CADB0/1 registers.

bit 3-2  **SDAHT<1:0>**: SDA Hold Time Selection bits
11 = Reserved
10 = Minimum of 30 ns hold time on SDA after the falling edge of SCL
01 = Minimum of 100 ns hold time on SDA after the falling edge of SCL
00 = Minimum of 300 ns hold time on SDA after the falling edge of SCL

bit 1-0  **BFRET<1:0>**: Bus Free Time Selection bits
11 = 64 I2C Clock pulses
10 = 32 I2C Clock pulses
01 = 16 I2C Clock pulses
00 = 8 I2C Clock pulses
REGISTER 33-4: I2CxCLK: I2C CLOCK SELECTION REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CLK&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7-0

**Unimplemented:** Read as '0'

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared
- HS = Hardware set
- HC = Hardware clear

<table>
<thead>
<tr>
<th>CLK&lt;3:0&gt;</th>
<th>I2Cx Clock Selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>1010-1111</td>
<td>Reserved</td>
</tr>
<tr>
<td>1001</td>
<td>SMT1 overflow</td>
</tr>
<tr>
<td>1000</td>
<td>TMR6 post scaled output</td>
</tr>
<tr>
<td>0111</td>
<td>TMR4 post scaled output</td>
</tr>
<tr>
<td>0110</td>
<td>TMR2 post scaled output</td>
</tr>
<tr>
<td>0101</td>
<td>TMR0 overflow</td>
</tr>
<tr>
<td>0100</td>
<td>Clock Reference output</td>
</tr>
<tr>
<td>0011</td>
<td>MFINTOSC (500 kHz)</td>
</tr>
<tr>
<td>0010</td>
<td>HFINTOSC</td>
</tr>
<tr>
<td>0001</td>
<td>Fosc</td>
</tr>
<tr>
<td>0000</td>
<td>Fosc/4</td>
</tr>
</tbody>
</table>
## REGISTER 33-5: I2CxBTO: I²C BUS TIMEOUT SELECTION REGISTER

| bit 7-3 | Unimplemented: Read as '0' |
| bit 2-0 | BTO<2:0>: I²C Bus Timeout Selection bits |
| BTO<2:0> | I²Cx Bus Timeout Selection |
| — | — |
| 111 | CLC4OUT |
| 110 | CLC3OUT |
| 101 | CLC2OUT |
| 100 | CLC1OUT |
| 011 | TMR6 post scaled output |
| 010 | TMR4 post scaled output |
| 001 | TMR2 post scaled output |
| 000 | Reserved |

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **HS** = Hardware set
- **HC** = Hardware clear
## REGISTER 33-6: I2CSTAT0: I²C STATUS REGISTER 0

| Bit 7 | BFRE: Bus Free Status bit<br>
|---|---
| R  = Readable bit | W  = Writable bit | U  = Unimplemented bit, read as '0'
| u  = Bit is unchanged | x  = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets
| '1' = Bit is set | '0' = Bit is cleared | HS = Hardware set | HC = Hardware clear |
| bit 6 | SMA: Slave Module Active Status bit<br>
| 1 = Set after the 8th falling SCL edge of a received matching 7-bit slave address<br>Set after the 8th falling SCL edge of a received matching 10-bit slave low address<br>Set after the 8th falling SCL edge of a received matching 10-bit slave high w/ read address, only after a previous matching high and low w/ write. | 1 = Indicates the I²C bus is Idle<br>Both SCL and SDA have been high for time-out selected by I2CCON2<BFRET<1:0>> bits. I2CCCLK must select a valid clock source for this bit to function. | 0 = Bus not Idle<br>(When no I2CCCLK is selected, this bit remains clear) |
| bit 5 | MMA: Master Module Active Status bit<br>
| 1 = Master Mode state machine is active<br>Set when master state machine asserts a Start on bus | 1 = Indicates the last matching received (high) address was a Read request<br>0 = Indicates the last matching received (high) address was a Write |
| 0 = Master state machine is Idle<br>Cleared when BCLIF is set<br>Cleared when Stop is shifted out by master.<br>Cleared for BTOIF condition, after the master successfully shifts out a Stop condition. | 0 = Indicates the last byte received or transmitted was data<br>0 = Indicates the last byte received or transmitted was an address |
| bit 4 | R: Read Information bit<br>
| 1 = Indicates the last matching received (high) address was a Read request<br>0 = Indicates the last matching received (high) address was a Write |
| bit 3 | D: Data bit<br>
| 1 = Indicates the last byte received or transmitted was data<br>0 = Indicates the last byte received or transmitted was an address |
| bit 2-0 | Unimplemented: Read as 1'b0 |

### Note 1:
This bit holds the R bit information following the last received address match. Addresses transmitted by the master or appearing on the bus without a match do not affect this bit.

### Note 2:
Clock requests and input from I2CxCLK register are disabled in Slave modes.

### Note 3:
Software must use the EN bit to force master or slave hardware to Idle.
**REGISTER 33-7: I2CxSTAT1: I2C STATUS REGISTER 1**

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXWE(2)</td>
<td>Unimplemented</td>
<td>TXBE(1, 3)</td>
<td>Unimplemented</td>
<td>RXRE(2)</td>
<td>CLRBF</td>
<td>Unimplemented</td>
<td>RXBF(1, 3)</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **’1’** = Bit is set
- **’0’** = Bit is cleared
- **HS** = Hardware set
- **HC** = Hardware clear

**bit 7**
- **TXWE**: Transmit Write Error Status bit
  - 1 = A new byte of data was written to I2CTXB when it was full (Must be cleared by software)
  - 0 = No transmit write error

**bit 6**
- **Unimplemented**: Read as ‘0’

**bit 5**
- **TXBE**: Transmit Buffer Empty Status bit
  - 1 = I2CTXB is empty (Cleared by writing the I2CTXB register)
  - 0 = I2CTXB is full

**bit 4**
- **Unimplemented**: Read as ‘0’

**bit 3**
- **RXRE**: Receive Read Error Status bit
  - 1 = A byte of data was read from I2CRXB when it was empty. (Must be cleared by software)
  - 0 = No receive overflow

**bit 2**
- **CLRBF**: Clear Buffer bit
  - Setting this bit clears/empties the receive and transmit buffers, causing reset of RXBF and TXBE.
  - Setting this bit clears the RXIF and TXIF interrupt flags.
  - This bit is set-only special function, and always reads ‘0’

**bit 1**
- **Unimplemented**: Read as ‘0’

**bit 0**
- **RXBF**: Receive Buffer Full Status bit
  - 1 = I2CRXB has received new data ( Cleared by reading the I2CRXB register)
  - 0 = I2CRXB is empty

**Note 1:** The bits are held in Reset when I2CEN = 0.
- **2:** Will cause NACK to be sent for slave address and master/slave data read bytes.
- **3:** Used as triggers for DMA operation.
**REGISTER 33-8: I2CxERR: I²C ERROR REGISTER**

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>BTOIF(1,2)</td>
<td>BCLIF(1)</td>
<td>NACKIF(1)</td>
<td>—</td>
<td>BTOIE</td>
<td>BCLIE</td>
<td>NACKIE</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **1** = Bit is set
- **0** = Bit is cleared
- **HS** = Hardware set
- **HC** = Hardware clear

**bit 7**

*Unimplemented: Read as '0'*

**bit 6**

**BTOIF:** Bus Time-Out Interrupt Flag bit(1,2)

- **1** = Bus Timeout occurred
- **0** = No bus timeout

**bit 5**

**BCLIF:** Bus Collision Detect Interrupt Flag bit(1)

- **1** = Bus collision detected (On the rising edge of SCL input, SDA output is high and input is sampled low)
  - Slave and Master mode the module immediately goes Idle
  - Multi-Master mode attempts to match slave addresses, and/or goes Idle
- **0** = No bus collision detected

**bit 4**

**NACKIF:** NACK Detect Interrupt Flag bit(1)

- **1** = When (SMA = 1 || MMA = 1) and a NACK is detected on the bus
  - NACKIF is also set when any of the TXWRE, RXRDE, TXUF, RXOVR bits are set.
- **0** = No NACK/Error detected
  - NACKIF is not set by the NACK send for non-matching slave addresses

**bit 3**

*Unimplemented: Read as '0'*

**bit 2**

**BTOIE:** Bus Time-Out Interrupt Enable bit

- **1** = Enable interrupt on bus time out
- **0** = Bus Tim-out not enabled

**bit 1**

**BCLIE:** Bus Collision Detect Interrupt Enable bit

- **1** = Enable interrupt on bus collision
- **0** = Bus collision interrupts are disabled

**bit 0**

**NACKIE:** NACK Detect Interrupt Enable bit

- **1** = Enable interrupt on NACKIF
- **0** = NACKIF interrupt is disabled

**Note 1:**

Enabled error interrupt flags are OR’d to produce the PIRx<I2CEIF> bit.

**2:**

User software must select the Bus Time-out Source in the I2CBTO register.
REGISTER 33-9: I2CxCNT: I²C BYTE COUNT REGISTER

<table>
<thead>
<tr>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNT&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'

u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set  '0' = Bit is cleared  HS = Hardware set  HC = Hardware clear

bit 7-0  CNT<7:0>: I²C Byte Count Register bits

If receiving data,

decremented 8th SCL edge, when a new data byte is loaded into I2CxRXB

If transmitting data,

decremented 9th SCL edge, when a new data byte is moved from I2CxTXB

CNTIF flag is set on 9th falling SCL edge, when I2CxCNT = 0. (Byte count cannot decrement past '0')

Note 1: It is recommended to write this register only when the module is IDLE (MMA = 0, SMA = 0) or when clock stretching (CSTR = 1 || MDR = 1).
## REGISTER 33-10: I2CxPIR: I2CxIF INTERRUPT FLAG REGISTER

<table>
<thead>
<tr>
<th>R/W/HS-0</th>
<th>R/W/HS-0</th>
<th>U-0</th>
<th>R/W/HS-0</th>
<th>R/W/HS-0</th>
<th>R/W/HS-0</th>
<th>R/W/HS-0</th>
<th>R/W/HS-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNTIF</td>
<td>ACKTIF</td>
<td>---</td>
<td>WRIF</td>
<td>ADRIF</td>
<td>PCIF</td>
<td>RSCIF</td>
<td>SCIF</td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **HS** = Hardware set
- **HC** = Hardware clear

#### bit 7  CNTIF: Byte Count Interrupt Flag bit
- **1** = When I2CCNT = 0, set by the 9th falling edge of SCL.
- **0** = I2CCNT condition has not occurred.

#### bit 6  ACKTIF: Acknowledge Status Time Interrupt Flag bit \(^{(2)}\) (MODE<2:0> = 0xx OR 11x)
- **1** = Set by the 9th falling edge of SCL for any byte when addressed as a slave
- **0** = Acknowledge condition not detected.

#### bit 5  Unimplemented: Read as '0'

#### bit 4  WRIF: Data Write Interrupt Flag bit (MODE<2:0> = 0xx OR 11x)
- **1** = Set the 8th falling edge of SCL for a received data byte.
- **0** = Data Write condition not detected

#### bit 3  ADRIF: Address Interrupt Flag bit (MODE<2:0> = 0xx OR 11x)
- **1** = Set the 8th falling edge of SCL for a matching received (high/low) address byte
- **0** = Address condition not detected

#### bit 2  PCIF: Stop Condition Interrupt Flag
- **1** = Set on detection of Stop condition
- **0** = No Stop condition detected

#### bit 1  RSCIF: Restart Condition Interrupt Flag
- **1** = Set on detection of Restart condition
- **0** = No Restart condition detected

#### bit 0  SCIF: Start Condition Interrupt Flag
- **1** = Set on detection of Start condition
- **0** = No Start condition detected

### Note:
1. Enabled interrupt flags are OR’d to produce the PIRx<I2CxIF> bit.
2. ACKTIF is not set by a matching, 10-bit, high address byte with the R/W bit clear. It is only set after the matching low address byte is shifted in.
REGISTER 33-11: I2CxPIE: I2CxIE INTERRUPT AND HOLD ENABLE REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNTIE</td>
<td>ACKTIE</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- '0' = Bit is cleared
- '1' = Bit is set
- -n/n = Value at POR and BOR/Value at all other Resets
- HS = Hardware set
- HC = Hardware clear

bit 7  CNTIE: Byte Count Interrupt Enable bit
       1 = When CNTIF is set
       0 = Byte count interrupts are disabled

bit 6  ACKTIE: Acknowledge Interrupt and Hold Enable bit
       1 = When ACKTIF is set
           - If ACK is generated, CSTR is also set.
           - If NACK is generated, CSTR is unchanged
       0 = Acknowledge holding and interrupt is disabled

bit 5  Unimplemented: Read as '0'

bit 4  WRIE: Data Write Interrupt and Hold Enable bit
       1 = When WRIF is set; CSTR is set
       0 = Data Write holding and interrupt is disabled

bit 3  ADRIE: Address Interrupt and Hold Enable bit
       1 = When ADRIF is set; CSTR is set
       0 = Address holding and interrupt is disabled

bit 2  PCIE: Stop Condition Interrupt Enable bit
       1 = Enable interrupt on detection of Stop condition
       0 = Stop detection interrupts are disabled

bit 1  RSCIE: Restart Condition Interrupt Enable bit
       1 = Enable interrupt on detection of Restart condition
       0 = Start detection interrupts are disabled

bit 0  SCIE: Start Condition Interrupt Enable bit
       1 = Enable interrupt on detection of Start condition
       0 = Start detection interrupts are disabled

Note 1: Enabled interrupt flags are OR'd to produce the PIRx<I2CxlF> bit.
## REGISTER 33-12: I2CxADR0: I2C ADDRESS 0 REGISTER

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADR7</td>
<td>ADR6</td>
<td>ADR5</td>
<td>ADR4</td>
<td>ADR3</td>
<td>ADR2</td>
<td>ADR1</td>
<td>ADR0</td>
</tr>
</tbody>
</table>

### Legend:

- **R** = Readable bit
- **W** =Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **1** = Bit is set
- **0** = Bit is cleared
- **HS** = Hardware set
- **HC** = Hardware clear

**bit 7-0**

- **ADR<7-0>:** Address 1 bits
- **MODE<2:0> = 00x | 11x - 7-bit Slave/Multi-Master Modes**
  - **ADR0<7:1>:** 7-bit Slave Address
  - **ADR0<0>:** Unused in this mode; bit state is a “don’t care”
- **MODE<2:0> = 01x - 10-bit Slave Modes**
  - **ADR0<7:0>:** Eight Least Significant bits of 10-bit address 0
## REGISTER 33-13: I2CxADR1: I²C ADDRESS 1 REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADR14</td>
<td>ADR13</td>
<td>ADR12</td>
<td>ADR11</td>
<td>ADR10</td>
<td>ADR9</td>
<td>ADR8</td>
<td>—</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>U-0</td>
</tr>
<tr>
<td>ADR7</td>
<td>ADR6</td>
<td>ADR5</td>
<td>ADR4</td>
<td>ADR3</td>
<td>ADR2</td>
<td>ADR1</td>
<td>—</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **HS** = Hardware set
- **HC** = Hardware clear
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-1**: ADR[7-1]: Address or Divider bits

- **MODE<2:0> = 000**: 7-bit Slave/Multi-Master Modes
  - **ADR<7:1>**: 7-bit Slave Address
  - **ADR<0>**: Unused in this mode; bit state is a "don't care"

- **MODE<2:0> = 001**: 7-bit Slave/Multi-Master modes w/Masking
  - **MSK0<7:1>**: 7-bit Slave Address
  - **MSK0<0>**: Unused in this mode; bit state is a "don't care"

- **MODE<2:0> = 01x**: 10-bit Slave Modes
  - **ADR<14-10>**: Bit pattern sent by master is fixed by I²C specification and must be equal to '11110'. However, these bit values are compared by hardware to the received data to determine a match. It is up to the user to set these bits as '11110'.
  - **ADR<9-8>**: Two Most Significant bits of 10-bit address

**bit 0**: Unimplemented: Read as '0'.
REGISTER 33-14: I2CxADR2: I2C ADDRESS 2 REGISTER

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADR7</td>
<td>ADR6</td>
<td>ADR5</td>
<td>ADR4</td>
<td>ADR3</td>
<td>ADR2</td>
<td>ADR1</td>
<td>ADR0</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **HS** = Hardware set
- **HC** = Hardware clear

bit 7-0  
**ADR<7-0>: Address 2 bits**

- **MODE<2:0> = 000** - 7-bit Slave/Multi-Master Modes
- **MODE<2:0> = 110** - 7-bit Slave Address

- **MODE<2:0> = 001** - 7-bit Slave/Multi-Master Modes with Masking
- **MODE<2:0> = 111** - 7-bit Slave Address

- **MODE<2:0> = 010** - 10-Bit Slave Mode
- **MODE<2:0> = 010** - 8-Bit Least Significant bits of second 10-bit address

- **MODE<2:0> = 011** - 10-Bit Slave Mode with Masking
- **MODE<2:0> = 011** - 10-Bit Slave Mode with Masking

**MSK0<7-0>:** The received address byte is masked, then compared to I2CxADR0
**REGISTER 33-15: I2CXADR3: I²C ADDRESS 3 REGISTER**

<table>
<thead>
<tr>
<th>Bit 15</th>
<th>Bit 8</th>
<th>Bit 7</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
<tr>
<td>ADR14</td>
<td>ADR13</td>
<td>ADR12</td>
<td>ADR11</td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
<tr>
<td>ADR10</td>
<td>ADR9</td>
<td>ADR8</td>
<td>U-0</td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
<tr>
<td>ADR7</td>
<td>ADR6</td>
<td>ADR5</td>
<td>ADR4</td>
</tr>
<tr>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
<tr>
<td>ADR3</td>
<td>ADR2</td>
<td>ADR1</td>
<td>U-0</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared
- HS = Hardware set
- HC = Hardware clear

**bit 7-0**

**ADR<7-0>: Address 3 bits**

**MODE<2:0> = 000** - 7-bit Slave/Multi-Master Modes
- **ADR<7:1>:** 7-bit Slave Address
- **ADR<0>:** Unused in this mode; bit state is a "don't care"

**MODE<2:0> = 001** - 7-bit Slave/Multi-Master Mode with Masking
- **MSK1<7:1>:** 7-bit Slave Address
- **MSK1<0>:** Unused in this mode; bit state is a "don't care"

**MODE<2:0> = 010** - 10-Bit Slave Mode
- **ADR<14-10>:** Bit pattern sent by master is fixed by I²C specification and must be equal to '11110'. However, these bit values are compared by hardware to the received data to determine a match. It is up to the user to set these bits as '11110'
- **ADR<9-8>:** Two Most Significant bits of 10-bit address

**MODE<2:0> = 011** - 10-Bit Slave Mode with Masking
- **MSK0<14-8>:** The received address byte, bit n, is compared to I2CxADR0 to detect I²C address match
REGISTER 33-16: I2CxADB0: I2C ADDRESS DATA BUFFER 0 REGISTER(1)

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>Mode&lt;2:0&gt;</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADB&lt;7:1&gt;</td>
<td>Address Data byte</td>
<td>Received matching 7-bit slave address data</td>
</tr>
<tr>
<td>R/W: Read/not-Write Data bit</td>
<td>Received read/write value from 7-bit address byte</td>
<td></td>
</tr>
<tr>
<td>MODE&lt;2:0&gt; = 00x</td>
<td>Address Data byte</td>
<td>Received matching lower eight bits of 10-bit slave address data</td>
</tr>
<tr>
<td>MODE&lt;2:0&gt; = 01x</td>
<td>Address Data byte</td>
<td>Received matching 7-bit slave address</td>
</tr>
<tr>
<td>R/W: Read/not-Write Data bit</td>
<td>Received read/write value received 7-bit slave address byte</td>
<td></td>
</tr>
<tr>
<td>MODE&lt;2:0&gt; = 100</td>
<td>Unused in this mode; bit state is a “don’t care”</td>
<td></td>
</tr>
<tr>
<td>MODE&lt;2:0&gt; = 101</td>
<td>Address Data byte</td>
<td>Low 10-bit address value copied to transmit shift register</td>
</tr>
<tr>
<td>MODE&lt;2:0&gt; = 11x</td>
<td>Address Data byte</td>
<td>Received matching 7-bit slave address</td>
</tr>
<tr>
<td>R/W: Read/not-Write Data bit</td>
<td>Received read/write value received 7-bit slave address byte</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** This register is read only except in master, 10-bit Address mode (MODE<2:0> = 101).
REGISTER 33-17: I2CxADB1: I²C ADDRESS DATA BUFFER 1 REGISTER(1)

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>MODE&lt;2:0&gt; = 00x</th>
<th>R/W: Read/not-Write Data bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unused in this mode; bit state is a “don’t care”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MODE&lt;2:0&gt; = 01x</td>
<td>ADB&lt;7:1&gt;: 10-bit Address High byte</td>
<td></td>
</tr>
<tr>
<td>Received matching 10-bit high address data</td>
<td>R/W: Read/not-Write Data bit</td>
<td></td>
</tr>
<tr>
<td>Received read/write value from matching 10-bit high address</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MODE&lt;2:0&gt; = 100</td>
<td>ADB&lt;7:1&gt;: Address Data byte</td>
<td></td>
</tr>
<tr>
<td>7-bit address value copied to transmit shift register</td>
<td>R/W: Read/not-Write Data bit</td>
<td></td>
</tr>
<tr>
<td>Read/write value copied to transmit shift register</td>
<td>Master hardware uses this bit to produce read versus write operations</td>
<td></td>
</tr>
<tr>
<td>MODE&lt;2:0&gt; = 101</td>
<td>ADB&lt;7:1&gt;: 10-bit Address High Data byte</td>
<td></td>
</tr>
<tr>
<td>10-bit high address value copied to transmit shift register</td>
<td>R/W: Read/not-Write Data bit</td>
<td></td>
</tr>
<tr>
<td>Read/write value copied to transmit shift register</td>
<td>Master hardware uses this bit to produce read versus write operations</td>
<td></td>
</tr>
<tr>
<td>MODE&lt;2:0&gt; = 11x</td>
<td>ADB&lt;7:1&gt;: Address Data byte</td>
<td></td>
</tr>
<tr>
<td>7-bit address value copied to transmit shift register</td>
<td>R/W: Read/not-Write Data bit</td>
<td></td>
</tr>
<tr>
<td>Read/write value copied to transmit shift register</td>
<td>Master hardware uses this bit to produce read versus write operations</td>
<td></td>
</tr>
<tr>
<td>Note 1: This register is read only in slave, 7-bit Addressing modes (MODE&lt;2:0&gt; = 0xx)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
u = Bit is unchanged
x = Bit is unknown
-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set
‘0’ = Bit is cleared
HS = Hardware set
HC = Hardware clear

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
u = Bit is unchanged
x = Bit is unknown
-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set
‘0’ = Bit is cleared
HS = Hardware set
HC = Hardware clear
### TABLE 33-18: SUMMARY OF REGISTERS FOR I2C 8-BIT MACRO

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2CxBTO</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>BTO&lt;2:0&gt;</td>
</tr>
<tr>
<td>I2CxCLK</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CLK&lt;2:0&gt;</td>
</tr>
<tr>
<td>I2CxPIE</td>
<td>CNTIE</td>
<td>ACKTIE</td>
<td>—</td>
<td>WRIE</td>
<td>ADRIE</td>
<td>PCIE</td>
<td>RSCIE</td>
<td>SCIE</td>
<td>573</td>
</tr>
<tr>
<td>I2CxPIR</td>
<td>CNTIF</td>
<td>ACKTIF</td>
<td>—</td>
<td>WRIF</td>
<td>ADRIF</td>
<td>PCIF</td>
<td>RSCIF</td>
<td>SCIF</td>
<td>566</td>
</tr>
<tr>
<td>I2CxERR</td>
<td>—</td>
<td>BTOIF</td>
<td>BCLIF</td>
<td>NACKIF</td>
<td>—</td>
<td>BTOIE</td>
<td>BCLIE</td>
<td>NACKIE</td>
<td>572</td>
</tr>
<tr>
<td>I2CxSTAT0</td>
<td>BFRE</td>
<td>SMA</td>
<td>MMA</td>
<td>R</td>
<td>D</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>570</td>
</tr>
<tr>
<td>I2CxSTAT1</td>
<td>TXWE</td>
<td>—</td>
<td>TXBE</td>
<td>—</td>
<td>RXRE</td>
<td>CLRBF</td>
<td>—</td>
<td>RXBF</td>
<td>569</td>
</tr>
<tr>
<td>I2CxCON0</td>
<td>EN</td>
<td>RSEN</td>
<td>S</td>
<td>CSTR</td>
<td>MDR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>568</td>
</tr>
<tr>
<td>I2CxCON1</td>
<td>ACKCNT</td>
<td>ACKDT</td>
<td>ACKSTAT</td>
<td>ACKT</td>
<td>—</td>
<td>RXOV</td>
<td>TXU</td>
<td>CSD</td>
<td>564</td>
</tr>
<tr>
<td>I2CxCON2</td>
<td>ACNT</td>
<td>GCEN</td>
<td>FME</td>
<td>ADB</td>
<td>SDAHT&lt;3:2&gt;</td>
<td>—</td>
<td>BFRET&lt;1:0&gt;</td>
<td>565</td>
<td></td>
</tr>
<tr>
<td>I2CxADR0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>574</td>
</tr>
<tr>
<td>I2CxADR1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>575</td>
</tr>
<tr>
<td>I2CxADR2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>576</td>
</tr>
<tr>
<td>I2CxADR3</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>577</td>
</tr>
<tr>
<td>I2CxADB0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>578</td>
</tr>
<tr>
<td>I2CxADB1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>579</td>
</tr>
<tr>
<td>I2CxCNT</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>571</td>
</tr>
<tr>
<td>I2CxRXB</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>570</td>
</tr>
<tr>
<td>I2CxTXB</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>572</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented, read as ‘0’. Shaded cells are unused by the I2C module.
34.0 CAN MODULE

This family of devices contain a Controller Area Network (CAN) module. The CAN module is fully backwards-compatible with the CAN and ECAN modules found in older PIC18 devices.

The Controller Area Network (CAN) module is a serial interface which is useful for communicating with other peripherals or microcontroller devices. This interface, or protocol, was designed to allow communications within noisy environments.

The CAN module is a communication controller, implementing the CAN 2.0A or B protocol as defined in the BOSCH specification. The module will support CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system; however, the CAN specification is not covered within this data sheet. Refer to the BOSCH CAN specification for further details.

The module features are as follows:

- Implementation of the CAN protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
- DeviceNet™ data bytes filter support
- Standard and extended data frames
- 0-8 bytes data length
- Programmable bit rate up to 1 Mbit/sec
- Fully backward compatible with CAN modules on older PIC18 devices
- Three modes of operation:
  - Mode 0 – Legacy mode
  - Mode 1 – Enhanced Legacy mode with DeviceNet support
  - Mode 2 – FIFO mode with DeviceNet support
- Support for remote frames with automated handling
- Double-buffered receiver with two prioritized received message storage buffers
- Six buffers programmable as RX and TX message buffers
- 16 full (standard/extended identifier) acceptance filters that can be linked to one of four masks
- Two full acceptance filter masks that can be assigned to any filter
- One full acceptance filter that can be used as either an acceptance filter or acceptance filter mask
- Three dedicated transmit buffers with application specified prioritization and abort capability
- Programmable wake-up functionality with integrated low-pass filter
- Programmable Loopback mode supports self-test operation
- Signaling via interrupt capabilities for all CAN receiver and transmitter error states
- Programmable clock source
- Programmable link to timer module for time-stamping and network synchronization
- Low-power Sleep mode

34.1 Module Overview

The CAN bus module consists of a protocol engine and message buffering and control. The CAN protocol engine automatically handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors and then matched against filters to see if it should be received and stored in one of the two receive registers.

The CAN module supports the following frame types:

- Standard Data Frame
- Extended Data Frame
- Remote Frame
- Error Frame
- Overload Frame Reception

The CANRX input pin is selected with the CANRXPPS register. The CANTX output pin is selected with each pin's RxyPPS register.

Note: The CANRX pin defaults to pin RB3, but the CANTX has no default location and must be assigned to a pin before CAN transmissions can occur.

In Normal mode, the user must ensure that the appropriate TRIS bit for CANRX is set and the appropriate TRIS bit for CANTX is cleared. In addition, the appropriate ANSEL bit for CANRX must be cleared to disable the analog input buffer.

Note: Unlike older Microchip devices with CAN functionality, the CAN pins can be mapped to pins with analog functionality. Ensure that the analog functionality on the CANRX pin is disabled, or the CAN module will not properly function.

34.1.1 MODULE FUNCTIONALITY

The CAN bus module consists of a protocol engine, message buffering and control (see Figure 34-1). The protocol engine can best be understood by defining the types of data frames to be transmitted and received by the module.

The following sequence illustrates the necessary initialization steps before the CAN module can be used to transmit or receive a message. Steps can be added or removed depending on the requirements of the application.

1. Use the CANRXPPS and appropriate RxyPPS registers to map the CANRX and CANTX functions to the desired pins of the device.
2. Initialize LAT, TRIS and ANSEL bits for the selected CANRX and CANTX pins.
3. Ensure that the CAN module is in Configuration mode.
4. Select CAN Functional mode.
5. Set up the Baud Rate registers.
6. Set up the Filter and Mask registers.
7. Set the CAN module to Normal mode or any other mode required by the application logic.
FIGURE 34-1:  CAN BUFFERS AND PROTOCOL ENGINE BLOCK DIAGRAM

BUFFERS

MESSAGE BUFFERS

Acceptance Filters
(RXF0-RXF05)  
MODE 0

Acceptance Filters
(RXF06-RXF15)  
MODE 1, 2

Message Queue Control

Transmit Byte Sequencer

Acceptance Filters
(RXF0-RXF05)

Acceptance Filters
(RXF06-RXF15)

RXF15

RXF06

RXF05

RXF04

RXF03

RXF02

RXF01

RXF00

RXF0

Acceptance Mask

RXM0

Acceptance Mask

RXM1

MAB

Receive Byte

Transmit Byte Sequencer

Transmission Option

Transmit Option

Transmit Buffers

Receive Buffers

Message Queue Control

Transmit Byte Sequencer

Receive Byte Sequencer

Transmit Logic

Receive Logic

Transmit Error Counter

Receive Error Counter

Protocol Finite State Machine

Bit Timing Logic

Clock Generator

Configuration Registers

16 - 4 to 1 MUXs

VCC

RXF0

Validate Identifier

Data Field

Acceptance Mask

RXM0

RXM1
34.2 CAN Modes of Operation

The CAN module has six main modes of operation:

- Configuration mode
- Disable/Sleep mode
- Normal Operation mode
- Listen Only mode
- Loopback mode
- Error Recognition mode

All modes, except Error Recognition, are requested by setting the REQOP bits (CANCON<7:5>). Error Recognition mode is requested through the RXM bits of the Receive Buffer register(s). Entry into a mode is acknowledged by monitoring the OPMODE bits.

When changing modes, the mode will not actually change until all pending message transmissions are complete. Because of this, the user must verify that the device has actually changed into the requested mode before further operations are executed.

Note: The module may fail to change modes from Configuration mode if the CANRX and CANTX pins are not externally connected to a CAN transceiver. If connection to a transceiver is not desired for the particular use case or application (for example, transitioning to Loopback mode for development/debugging), the CANRX pin must be externally tied to VDD through a 10k pull-up resistor.

34.2.1 CONFIGURATION MODE

The CAN module has to be initialized before the activation. This is only possible if the module is in the Configuration mode. The Configuration mode is requested by setting the REQOP<2:0> bits to 0b100. Only when the Status bits OPMODE<2:0> are equal to 0b100, can the initialization be performed. Afterwards, the Configuration registers, the acceptance mask registers and the acceptance filter registers can be written.

Configuration mode protects the user from accidentally violating the CAN protocol through programming errors, as all registers which control the configuration of the module can not be modified while the module is online. The CAN module will not enter the Configuration mode while a transmission or reception is taking place. The following registers can only be modified in Configuration mode:

- Configuration Registers
- Functional Mode Selection Registers
- Bit Timing Registers
- Identifier Acceptance Filter Registers
- Identifier Acceptance Mask Registers
- Filter and Mask Control Registers
- Mask Selection Registers

In the Configuration mode, the module will not transmit or receive. The error counters are cleared and the interrupt flags remain unchanged. The programmer will have access to Configuration registers that are access restricted in other modes. I/O pins will revert to normal I/O functions.

34.2.2 DISABLE/SLEEP MODE

When the REQOP<2:0> bits are set to '001', the module will enter Disable/Sleep mode. This mode is similar to disabling other peripheral modules by turning off the module enables. This causes the module internal clock to stop unless the module is active (i.e., receiving or transmitting a message). If the module is active, the module will wait for 11 recessive bits on the CAN bus, detect that condition as an Idle bus, then accept the module Disable/Sleep command. OPMODE<2:0> = 001 indicates whether the module successfully went into the module Disable/Sleep mode. In Disable/Sleep mode, the module will not transmit or receive. The module has the ability to set the WAKIF bit due to bus activity. However, any pending interrupts will remain and the error counters will retain their value.

The WAKIF interrupt is the only module interrupt that is still active in the Disable/Sleep mode. If the WAKDIS is cleared and WAKIE is set, the processor will receive an interrupt whenever the module detects a recessive to dominant transition. On wake-up, the module will automatically be set to the previous mode of operation. For example, if the module was switched from Normal to Disable/Sleep mode on bus activity wake-up, the module will automatically enter into Normal mode and the first message that caused the module to wake-up is lost. The module will not generate any error frame. Firmware logic must detect this condition and make sure that retransmission is requested. If the processor receives a wake-up interrupt while it is sleeping, more than one message may get lost. The actual number of messages lost would depend on the processor oscillator start-up time and incoming message bit rate.

The CANTX pin will stay in the recessive state while the module is in Disable/Sleep mode.

34.2.3 NORMAL MODE

This is the standard operating mode of the CAN module. In this mode, the device actively monitors all bus messages and generates Acknowledge bits, error frames, etc. This is also the only mode in which the CAN module will transmit messages over the CAN bus. The Normal mode is activated by clearing the mode request bits in the CANCON register.
34.2.4 LISTEN ONLY MODE

Listen Only mode provides a means for the CAN module to receive all messages, including messages with errors. This mode can be used for bus monitor applications or for detecting the baud rate in ‘hot plugging’ situations. For auto-baud detection, it is necessary that there are at least two other nodes which are communicating with each other. The baud rate can be detected empirically by testing different values until valid messages are received. The Listen Only mode is a silent mode, meaning no messages will be transmitted while in this state, including error flags or Acknowledge signals. In Listen Only mode, both valid and invalid messages will be received, regardless of RXMn bit settings. The filters and masks can still be used to allow only particular valid messages to be loaded into the Receive registers, or the filter masks can be set to all zeros to allow a message with any identifier to pass. All invalid messages will be received in this mode, regardless of filters and masks or RXMn Receive Buffer mode bits. The error counters are reset and deactivated in this state. The Listen Only mode is activated by setting the mode request bits in the CANCON register to 0b011.

34.2.5 LOOPBACK MODE

This mode will allow internal transmission of messages from the transmit buffers to the receive buffers without actually transmitting messages on the CAN bus. This mode can be used in system development and testing. In this mode, the ACK bit is ignored and the device will allow incoming messages from itself, just as if they were coming from another node. The Loopback mode is a silent mode, meaning no messages will be transmitted while in this state, including error flags or Acknowledge signals. The TXCAN pin will revert to port I/O while the device is in this mode. The filters and masks can be used to allow only particular messages to be loaded into the receive registers. The masks can be set to all zeros to provide a message that accepts all messages. The Loopback mode is activated by setting the mode request bits in the CANCON register to 0b010.

34.2.6 ERROR RECOGNITION MODE

The module can be set to ignore all errors and receive any message. In functional Mode 0, the Error Recognition mode is activated by setting the RXM<1:0> bits in the RXBnCON registers to ‘11’. In this mode, the data which is in the message assembly buffer until the error time, is copied in the receive buffer and can be read via the CPU interface.

34.3 CAN Module Functional Modes

In addition to CAN modes of operation, the CAN module offers a total of three functional modes. Each of these modes are identified as Mode 0, Mode 1 and Mode 2.

34.3.1 MODE 0 – LEGACY MODE

Mode 0 is designed to be fully compatible with CAN modules used in PIC18CXX8 and PIC18FXX8 devices. This is the default mode of operation on all Reset conditions. As a result, module code written for the PIC18XX8 CAN module may be used on the CAN module with only very minor code changes.

The following is the list of resources available in Mode 0:

- Three transmit buffers: TXB0, TXB1 and TXB2
- Two receive buffers: RXB0 and RXB1
- Two acceptance masks, one for each receive buffer: RXM0, RXM1
- Six acceptance filters, 2 for RXB0 and 4 for RXB1: RXF0, RXF1, RXF2, RXF3, RXF4, RXF5

34.3.2 MODE 1 – ENHANCED LEGACY MODE

Mode 1 is similar to Mode 0, with the exception that more resources are available in Mode 1. There are 16 acceptance filters and two acceptance mask registers. Acceptance Filter 15 can be used as either an acceptance filter or an acceptance mask register. In addition to three transmit and two receive buffers, there are six more message buffers. One or more of these additional buffers can be programmed as transmit or receive buffers. These additional buffers can also be programmed to automatically handle RTR messages.

Fourteen of sixteen acceptance filter registers can be dynamically associated to any receive buffer and acceptance mask register. One can use this capability to associate more than one filter to any one buffer. When a receive buffer is programmed to use standard identifier messages, part of the full acceptance filter register can be used as a data byte filter. The length of the data byte filter is programmable from 0 to 18 bits. This functionality simplifies implementation of high-level protocols, such as the DeviceNet™ protocol.

The following is the list of resources available in Mode 1:

- Three transmit buffers: TXB0, TXB1 and TXB2
- Two receive buffers: RXB0 and RXB1
- Six buffers programmable as TX or RX: B0-B5
- Automatic RTR handling on B0-B5
- Sixteen dynamically assigned acceptance filters: RXF0-RXF15
- Two dedicated acceptance mask registers; RXF15 programmable as third mask: RXM0-RXM1, RXF15
- Programmable data filter on standard identifier
34.3.3 MODE 2 – ENHANCED FIFO MODE

In Mode 2, two or more receive buffers are used to form the receive FIFO (first in, first out) buffer. There is no one-to-one relationship between the receive buffer and acceptance filter registers. Any filter that is enabled and linked to any FIFO receive buffer can generate acceptance and cause FIFO to be updated.

FIFO length is user-programmable, from 2-8 buffers deep. FIFO length is determined by the very first programmable buffer that is configured as a transmit buffer. For example, if Buffer 2 (B2) is programmed as a transmit buffer, FIFO consists of RXB0, RXB1, B0 and B1, creating a FIFO length of four. If all programmable buffers are configured as receive buffers, FIFO will have the maximum length of eight.

The following is the list of resources available in Mode 2:

- Three transmit buffers: TXB0, TXB1 and TXB2
- Two receive buffers: RXB0 and RXB1
- Six buffers programmable as TX or RX; receive buffers form FIFO: B0-B5
- Automatic RTR handling on B0-B5
- Sixteen acceptance filters: RXF0-RXF15
- Two dedicated acceptance mask registers; RXF15 programmable as third mask: RXM0-RXM1, RXF15
- Programmable data filter on standard identifier messages: SDFLC, useful for DeviceNet protocol

34.4 CAN Message Buffers

34.4.1 DEDICATED TRANSMIT BUFFERS

The CAN module implements three dedicated transmit buffers – TXB0, TXB1 and TXB2. Each of these buffers occupies 14 bytes of SRAM and are mapped into the SFR memory map. These are the only transmit buffers available in Mode 0. Mode 1 and 2 may access these and other additional buffers.

Each transmit buffer contains one Control register (TXBnCON), four Identifier registers (TXBnSIDL, TXBnSIDH, TXBnEIDL, TXBnEIDH), one Data Length Count register (TXBnDLC) and eight Data Byte registers (TXBnDm).

34.4.2 DEDICATED RECEIVE BUFFERS

The CAN module implements two dedicated receive buffers: RXB0 and RXB1. Each of these buffers occupies 14 bytes of SRAM and are mapped into SFR memory map. These are the only receive buffers available in Mode 0. Mode 1 and 2 may access these and other additional buffers.

Each receive buffer contains one Control register (RXBnCON), four Identifier registers (RXBnSIDL, RXBnSIDH, RXBnEIDL, RXBnEIDH), one Data Length Count register (RXBnDLC) and eight Data Byte registers (RXBnDm).

34.4.3 PROGRAMMABLE TRANSMIT/RECEIVE BUFFERS

The CAN module implements six non-dedicated buffers: B0-B5. These buffers are individually programmable as either transmit or receive buffers. These buffers are available only in Mode 1 and 2. As with dedicated transmit and receive buffers, each of these programmable buffers occupies 14 bytes of SRAM and are mapped into SFR memory map.

Each buffer contains one Control register (BnCON), four Identifier registers (BnSIDL, BnSIDH, BnEIDL, BnEIDH), one Data Length Count register (BnDLC) and eight Data Byte registers (BnDm). Each of these registers contains two sets of control bits. Depending on whether the buffer is configured as transmit or receive, one would use the corresponding control bit set. By default, all buffers are configured as receive buffers. Each buffer can be individually configured as a transmit or receive buffer by setting the corresponding TXENn bit in the BSEL0 register.

When configured as transmit buffers, user firmware may access transmit buffers in any order similar to accessing dedicated transmit buffers. In receive configuration with Mode 1 enabled, user firmware may also access receive buffers in any order required. But in Mode 2, all receive buffers are combined to form a single FIFO. Actual FIFO length is programmable by user firmware. Access to FIFO must be done through the FIFO Pointer bits (FP<4:0>) in the CANCON register. It must be noted that there is no hardware protection against out of order FIFO reads.

34.4.4 PROGRAMMABLE AUTO-RTR BUFFERS

In Mode 1 and 2, any of six programmable transmit/receive buffers may be programmed to automatically respond to predefined RTR messages without user firmware intervention. Automatic RTR handling is enabled by setting the TX2EN bit in the BSEL0 register and the RTREN bit in the BnCON register. After this setup, when an RTR request is received, the TXREQ bit is automatically set and the current buffer content is automatically queued for transmission as a RTR
response. As with all transmit buffers, once the TXREQ bit is set, buffer registers become read-only and any writes to them will be ignored.
The following outlines the steps required to automatically handle RTR messages:

1. Set buffer to Transmit mode by setting the TXnEN bit to '1' in the BSEL0 register.
2. At least one acceptance filter must be associated with this buffer and preloaded with the expected RTR identifier.
3. Bit, RTREN in the BnCON register, must be set to '1'.
4. Buffer must be preloaded with the data to be sent as a RTR response.

Normally, user firmware will keep buffer data registers up to date. If firmware attempts to update the buffer while an automatic RTR response is in the process of transmission, all writes to buffers are ignored.

### 34.5 CAN Message Transmission

#### 34.5.1 INITIATING TRANSMISSION

For the MCU to have write access to the message buffer, the TXREQ bit must be clear, indicating that the message buffer is clear of any pending message to be transmitted. At a minimum, the SIDH, SIDL and DLC registers must be loaded. If data bytes are present in the message, the Data registers must also be loaded. If the message is to use extended identifiers, the EIDH:EIDL registers must also be loaded and the EXIDE bit set.

To initiate message transmission, the TXREQ bit must be set for each buffer to be transmitted. When TXREQ is set, the TXABT, TXLARB and TXERR bits will be cleared. To successfully complete the transmission, there must be at least one node with matching baud rate on the network.

Setting the TXREQ bit does not initiate a message transmission; it merely flags a message buffer as ready for transmission. Transmission will start when the device detects that the bus is available. The device will then begin transmission of the highest priority message that is ready.

When the transmission has completed successfully, the TXREQ bit will be cleared, the TXBnIF bit will be set and an interrupt will be generated if the TXBnIE bit is set.

If the message transmission fails, the TXREQ will remain set, indicating that the message is still pending for transmission and one of the following condition flags will be set. If the message started to transmit but encountered an error condition, the TXERR and the IRXIF bits will be set and an interrupt will be generated. If the message lost arbitration, the TXLARB bit will be set.

#### 34.5.2 ABORTING TRANSMISSION

The MCU can request to abort a message by clearing the TXREQ bit associated with the corresponding message buffer (TXBnCON<3> or BnCON<3>). Setting the ABAT bit (CANCON<4>) will request an abort of all pending messages. If the message has not yet started transmission, or if the message started but is interrupted by loss of arbitration or an error, the abort will be processed. The abort is indicated when the module sets the TXABT bit for the corresponding buffer (TXBnCON<6> or BnCON<6>). If the message has started to transmit, it will attempt to transmit the current message fully. If the current message is transmitted fully and is not lost to arbitration or an error, the TXABT bit will not be set because the message was transmitted successfully. Likewise, if a message is being transmitted during an abort request and the message is lost to arbitration or an error, the TXABT bit will be set, indicating that the message was successfully aborted.

Once an abort is requested by setting the ABAT or TXABT bits, it cannot be cleared to cancel the abort request. Only CAN module hardware or a POR condition can clear it.

#### 34.5.3 TRANSMIT PRIORITY

Transmit priority is a prioritization within the ECAN module of the pending transmittable messages. This is independent from, and not related to, any prioritization implicit in the message arbitration scheme built into the CAN protocol. Prior to sending the Start-of-Frame (SOF), the priority of all buffers that are queued for transmission is compared. The transmit buffer with the highest priority will be sent first. If two buffers have the same priority setting, the buffer with the highest buffer number will be sent first. There are four levels of transmit priority. If the TXP bits for a particular message buffer are set to '11', that buffer has the highest possible priority. If the TXP bits for a particular message buffer are set to '00', that buffer has the lowest possible priority.
34.6 Message Reception

34.6.1 RECEIVING A MESSAGE

Of all receive buffers, the MAB is always committed to receiving the next message from the bus. The MCU can access one buffer while the other buffer is available for message reception or holding a previously received message.

The entire contents of the MAB are moved into the receive buffer once a message is accepted. This means that regardless of the type of identifier (standard or extended) and the number of data bytes received, the entire receive buffer is overwritten with the MAB contents. Therefore, the contents of all registers in the buffer must be assumed to have been modified when any message is received.

When a message is moved into either of the receive buffers, the associated RXFUL bit is set. This bit must be cleared by the MCU when it has completed processing the message in the buffer in order to allow a new message to be received into the buffer. This bit provides a positive lockout to ensure that the firmware has finished with the message before the module attempts to load a new message into the receive buffer. If the receive interrupt is enabled, an interrupt will be generated to indicate that a valid message has been received.

Once a message is loaded into any matching buffer, user firmware may determine exactly what filter caused this reception by checking the filter hit bits in the RXBnSIDL or BnSIDL register. In Mode 0, FILHIT<2:0> of RXBnSIDL serve as filter hit bits. In Mode 1 and 2, FILHIT<4:0> bits of BnSIDL serve as filter hit bits. The same registers also indicate whether the current message is an RTR frame or not. A received message is considered a standard identifier message if the EXID/EXIDE bit in the RXBnSIDL or the BnSIDL register is cleared. Conversely, a set EXID bit indicates an extended identifier message. If the received message is a standard identifier message, user firmware needs to read the SIDL and SIDH registers. In the case of an extended identifier message, firmware should read the SIDL, SIDH, EIDL and EIDH registers. If the RXBnDLC or BnDLC register contain non-zero data count, user firmware should also read the corresponding number of data bytes by accessing the RXBnDm or the BnDm registers. When a received message is an RTR, and if the current buffer is not configured for automatic RTR handling, user firmware must take appropriate action and respond manually.

Each receive buffer contains RXM bits to set special Receive modes. In Mode 0, RXM<1:0> bits in RXBnCON define a total of four Receive modes. In Mode 1 and 2, RXM1 bit, in combination with the EXID mask and filter bit, define the same four receive modes. Normally, these bits are set to ‘00’ to enable reception of all valid messages as determined by the appropriate acceptance filters. In this case, the determination of whether or not to receive standard or extended messages is determined by the EXIDE bit in the acceptance filter register. In Mode 0, if the RXM bits are set to ‘01’ or ‘10’, the receiver will accept only messages with standard or extended identifiers, respectively. If an acceptance filter has the EXIDE bit set, such that it does not correspond with the RXM mode, that acceptance filter is rendered useless. In Mode 1 and 2, setting EXID in the SIDL Mask register will ensure that only standard or extended identifiers are received. These two modes of RXM bits can be used in systems where it is known that only standard or extended messages will be on the bus. If the RXM bits are set to ‘11’ (RXM1 = 1 in Mode 1 and 2), the buffer will receive all
messages regardless of the values of the acceptance filters. Also, if a message has an error before the end of frame, that portion of the message assembled in the MAB before the error frame will be loaded into the buffer. This mode may serve as a valuable debugging tool for a given CAN network. It should not be used in an actual system environment as the actual system will always have some bus errors and all nodes on the bus are expected to ignore them.

In Mode 1 and 2, when a programmable buffer is configured as a transmit buffer and one or more acceptance filters are associated with it, all incoming messages matching this acceptance filter criteria will be discarded. To avoid this scenario, user firmware must make sure that there are no acceptance filters associated with a buffer configured as a transmit buffer.

34.6.2 RECEIVE PRIORITY

When in Mode 0, RXB0 is the higher priority buffer and has two message acceptance filters associated with it. RXB1 is the lower priority buffer and has four acceptance filters associated with it. The lower number of acceptance filters makes the match on RXB0 more restrictive and implies a higher priority for that buffer. Additionally, the RXB0CON register can be configured such that if RXB0 contains a valid message and another valid message is received, an overflow error will not occur and the new message will be moved into RXB1 regardless of the acceptance criteria of RXB1. There are also two programmable acceptance filter masks available, one for each receive buffer (see Section 34.4 “CAN Message Buffers”).

In Mode 1 and 2, there are a total of 16 acceptance filters available and each can be dynamically assigned to any of the receive buffers. A buffer with a lower number has higher priority. Given this, if an incoming message matches with two or more receive buffer acceptance criteria, the buffer with the lower number will be loaded with that message.

34.6.3 ENHANCED FIFO MODE

When configured for Mode 2, two of the dedicated receive buffers in combination with one or more programmable transmit/receive buffers, are used to create a maximum of an eight buffers deep FIFO buffer. In this mode, there is no direct correlation between filters and receive buffer registers. Any filter that has been enabled can generate an acceptance. When a message has been accepted, it is stored in the next available receive buffer register and an internal Write Pointer is incremented. The FIFO can be a maximum of eight buffers deep. The entire FIFO must consist of contiguous receive buffers. The FIFO head begins at RXB0 buffer and its tail spans toward B5. The maximum length of the FIFO is limited by the presence or absence of the first transmit buffer starting from B0. If a buffer is configured as a transmit buffer, the FIFO length is reduced accordingly. For instance, if B3 is configured as a transmit buffer, the actual FIFO will consist of RXB0, RXB1, B0, B1 and B2, a total of five buffers. If B0 is configured as a transmit buffer, the FIFO length will be two. If none of the programmable buffers are configured as a transmit buffer, the FIFO will be eight buffers deep. A system that requires more transmit buffers should try to locate transmit buffers at the very end of B0-B5 buffers to maximize available FIFO length.

When a message is received in FIFO mode, the Interrupt Flag Code bits (EICODE<4:0>) in the CANSTAT register will have a value of ‘10000’, indicating the FIFO has received a message. FIFO Pointer bits, FP<3:0> in the CANCON register, point to the buffer that contains data not yet read. The FIFO Pointer bits, in this sense, serve as the FIFO Read Pointer. The user should use the FP bits and read corresponding buffer data. When receive data is no longer needed, the RXFUL bit in the current buffer must be cleared, causing FP<3:0> to be updated by the module.

To determine whether FIFO is empty or not, the user may use the FP<3:0> bits to access the RXFUL bit in the current buffer. If RXFUL is cleared, the FIFO is considered to be empty. If it is set, the FIFO may contain one or more messages. In Mode 2, the module also provides a bit called FIFO High Water Mark (FIFOWM) in the ECANCON register. This bit can be used to cause an interrupt whenever the FIFO contains only one or four empty buffers. The FIFO high water mark interrupt can serve as an early warning to a full FIFO condition.

34.6.4 TIME-STAMPING

The CAN module can be programmed to generate a time-stamp for every message that is received. When enabled, the module generates a capture signal for the CCP modules, which in turn captures the value of Timer1, Timer3 or Timer5. This value can be used as the message time-stamp.

To use the time-stamp capability, set the CTS<3:0> bits of the appropriate CCPxCAP register to ‘1000’ to configure the CCP module capture input to the CAN_rx_timestamp signal.

In addition, the CAN_rx_timestamp can be chosen as a signal input for the Signal Measurement Timer, which can be used for a variety of other timing applications.
34.7 Message Acceptance Filters and Masks

The message acceptance filters and masks are used to determine if a message in the Message Assembly Buffer should be loaded into any of the receive buffers. Once a valid message has been received into the MAB, the identifier fields of the message are compared to the filter values. If there is a match, that message will be loaded into the appropriate receive buffer. The filter masks are used to determine which bits in the identifier are examined with the filters. A truth table is shown below in Table 34-1 that indicates how each bit in the identifier is compared to the masks and filters to determine if a message should be loaded into a receive buffer. The mask essentially determines which bits to apply the acceptance filters to. If any mask bit is set to a zero, then that bit will automatically be accepted regardless of the filter bit.

### Table 34-1: Filter/Mask Truth Table

<table>
<thead>
<tr>
<th>Mask bit n</th>
<th>Filter bit n</th>
<th>Message Identifier bit n001</th>
<th>Accept or Reject bit n</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>x</td>
<td>x</td>
<td>Accept</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Accept</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Reject</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Reject</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Accept</td>
</tr>
</tbody>
</table>

Legend:  x = don’t care

In Mode 0, acceptance filters, RXF0 and RXF1, and filter mask, RXM0, are associated with RXB0. Filters, RXF2, RXF3, RXF4 and RXF5, and mask, RXM1, are associated with RXB1.

In Mode 1 and 2, there are an additional ten acceptance filters, RXF6-RXF15, creating a total of 16 available filters. RXF15 can be used either as an acceptance filter or acceptance mask register. Each of these acceptance filters can be individually enabled or disabled by setting or clearing the RXFENn bit in the RXFCONn register. Any of these 16 acceptance filters can be dynamically associated with any of the receive buffers. Actual association is made by setting the appropriate bits in the RXFBCONn register. Each RXFBCONn register contains a nibble for each filter. This nibble can be used to associate a specific filter to any of available receive buffers. User firmware may associate more than one filter to any one specific receive buffer.

In addition to dynamic filter to buffer association, in Mode 1 and 2, each filter can also be dynamically associated to available Acceptance Mask registers. The FILn_m bits in the MSELn register can be used to link a specific acceptance filter to an acceptance mask register. As with filter to buffer association, one can also associate more than one mask to a specific acceptance filter.

When a filter matches and a message is loaded into the receive buffer, the filter number that enabled the message reception is loaded into the FILHIT bit(s). In Mode 0 for RXB1, the RXB1CON register contains the FILHIT<2:0> bits. They are coded as follows:

- 101 = Acceptance Filter 5 (RXF5)
- 100 = Acceptance Filter 4 (RXF4)
- 011 = Acceptance Filter 3 (RXF3)
- 010 = Acceptance Filter 2 (RXF2)
- 001 = Acceptance Filter 1 (RXF1)
- 000 = Acceptance Filter 0 (RXF0)

The coding of the RXB0DBEN bit enables these three bits to be used similarly to the FILHIT bits and to distinguish a hit on filter, RXF0 and RXF1, in either RXB0 or after a rollover into RXB1.

- 111 = Acceptance Filter 1 (RXF1)
- 110 = Acceptance Filter 0 (RXF0)
- 001 = Acceptance Filter 1 (RXF1)
- 000 = Acceptance Filter 0 (RXF0)

If the RXB0DBEN bit is clear, there are six codes corresponding to the six filters. If the RXB0DBEN bit is set, there are six codes corresponding to the six filters, plus two additional codes corresponding to RXF0 and RXF1 filters, that rollover into RXB1.

In Mode 1 and 2, each buffer control register contains five bits of filter hit bits (FILHIT<4:0>). A binary value of ‘0’ indicates a hit from RXF0 and 15 indicates RXF15. If more than one acceptance filter matches, the FILHIT bits will encode the binary value of the lowest numbered filter that matched. In other words, if filter RXF2 and filter RXF4 match, FILHIT will be loaded with the value for RXF2. This essentially prioritizes the acceptance filters with a lower number filter having higher priority. Messages are compared to filters in ascending order of filter number.

The mask and filter registers can only be modified when the CAN module is in Configuration mode.

The coding of the RXB0DBEN bit enables three bits to be used similarly to the FILHIT bits and to distinguish a hit on filter, RXF0 and RXF1, in either RXB0 or after a rollover into RXB1.
34.8 Baud Rate Setting

All nodes on a given CAN bus must have the same nominal bit rate. The CAN protocol uses Non-Return-to-Zero (NRZ) coding which does not encode a clock within the data stream. Therefore, the receive clock must be recovered by the receiving nodes and synchronized to the transmitter’s clock.

As oscillators and transmission time may vary from node to node, the receiver must have some type of Phase Lock Loop (PLL) synchronized to data transmission edges to synchronize and maintain the receiver clock. Since the data is NRZ coded, it is necessary to include bit stuffing to ensure that an edge occurs at least every six bit times to maintain the Digital Phase Lock Loop (DPLL) synchronization.

The bit timing of the CAN module is implemented using a DPLL that is configured to synchronize to the incoming data and provides the nominal timing for the transmitted data. The DPLL breaks each bit time into multiple segments made up of minimal periods of time called the Time Quanta (TQ).

Bus timing functions executed within the bit time frame, such as synchronization to the local oscillator, network transmission delay compensation and sample point positioning, are defined by the programmable bit timing logic of the DPLL.

All devices on the CAN bus must use the same bit rate. However, all devices are not required to have the same master oscillator clock frequency. For the different clock frequencies of the individual devices, the bit rate has to be adjusted by appropriately setting the baud rate prescaler and number of time quanta in each segment.

The “Nominal Bit Rate” is the number of bits transmitted per second, assuming an ideal transmitter with an ideal oscillator, in the absence of resynchronization. The nominal bit rate is defined to be a maximum of 1 Mb/s.

The “Nominal Bit Time” is defined as:

EQUATION 34-1: NOMINAL BIT TIME

\[ T_{\text{bit}} = 1/\text{Nominal Bit Rate} \]

The Nominal Bit Time can be thought of as being divided into separate, non-overlapping time segments. These segments (Figure 34-4) include:

- Synchronization Segment (Sync_Seg)
- Propagation Time Segment (Prop_Seg)
- Phase Buffer Segment 1 (Phase_Seg1)
- Phase Buffer Segment 2 (Phase_Seg2)

The time segments (and thus, the Nominal Bit Time) are, in turn, made up of integer units of time called Time Quanta or TQ (see Figure 34-4). By definition, the Nominal Bit Time is programmable from a minimum of 8 TQ to a maximum of 25 TQ. Also by definition, the minimum Nominal Bit Time is 1 \( \mu \)s, corresponding to a maximum 1 Mb/s rate. The actual duration is given by the following relationship:

EQUATION 34-2: NOMINAL BIT TIME DURATION

\[ \text{Nominal Bit Time} = T_Q \times (\text{Sync}_\text{Seg} + \text{Prop}_\text{Seg} + \text{Phase}_\text{Seg1} + \text{Phase}_\text{Seg2}) \]
The Time Quantum is a fixed unit derived from the oscillator period. It is also defined by the programmable baud rate prescaler, with integer values from 1 to 64, in addition to a fixed divide-by-two for clock generation. Mathematically, this is:

**EQUATION 34-3: TIME QUANTUM**

\[
T_Q (\mu s) = \frac{(2 \times (BRP + 1))}{F_{OSC} (MHz)}
\]

or

\[
T_Q (\mu s) = (2 \times (BRP + 1)) \times T_{OSC} (\mu s)
\]

where \( F_{OSC} \) is the clock frequency, \( T_{OSC} \) is the corresponding oscillator period and \( BRP \) is an integer (0 through 63) represented by the binary values of BRGCON1<5:0>. The equation above refers to the effective clock frequency used by the microcontroller. If, for example, a 10 MHz crystal in HS mode is used, then \( F_{OSC} = 10 \text{ MHz} \) and \( T_{OSC} = 100 \text{ ns} \). If the same 10 MHz crystal is used in HS-PLL mode, then the effective frequency is \( F_{OSC} = 40 \text{ MHz} \) and \( T_{OSC} = 25 \text{ ns} \).

**FIGURE 34-4: BIT TIME PARTITIONING**

34.8.1 EXTERNAL CLOCK, INTERNAL CLOCK AND MEASURABLE JITTER IN HS-PLL BASED OSCILLATORS

The microcontroller clock frequency generated from a PLL circuit is subject to a jitter, also defined as Phase Jitter or Phase Skew. For its PIC18 Enhanced microcontrollers, Microchip specifies phase jitter \( (P_{jitter}) \) as being 2% (Gaussian distribution, within three standard deviations, see Parameter PLL04 in Table 45-9) and Total Jitter \( (T_{jitter}) \) as being \( 2 \times P_{jitter} \).

The CAN protocol uses a bit-stuffing technique that inserts a bit of a given polarity following five bits with the opposite polarity. This gives a total of ten bits transmitted without resynchronization (compensation for jitter or phase error).

Given the random nature of the added jitter error, it can be shown that the total error caused by the jitter tends to cancel itself over time. For a period of ten bits, it is necessary to add only two jitter intervals to correct for jitter induced error: one interval in the beginning of the 10-bit period and another at the end. The overall effect is shown in Figure 34-5.
Once these considerations are taken into account, it is possible to show that the relation between the jitter and the total frequency error can be defined as:

**EQUATION 34-4: JITTER AND TOTAL FREQUENCY ERROR**

\[
\Delta f = \frac{T_{\text{jitter}}}{10 \times \text{NBT}} = \frac{2 \times P_{\text{jitter}}}{10 \times \text{NBT}}
\]

where jitter is expressed in terms of time and NBT is the Nominal Bit Time.

For example, assume a CAN bit rate of 125 Kb/s, which gives an NBT of 8 µs. For a 16 MHz clock generated from a 4x PLL, the jitter at this clock frequency is:

**EQUATION 34-5: 16 MHz CLOCK FROM 4x PLL JITTER:**

\[
2\% \times \frac{1}{16 \text{ MHz}} = \frac{0.02}{16 \times 10^6} = 1.25 \text{ ns}
\]

and resultant frequency error is:

**EQUATION 34-6: RESULTANT FREQUENCY ERROR:**

\[
\frac{2 \times (1.25 \times 10^{-9})}{10 \times (8 \times 10^{-6})} = 3.125 \times 10^{-5} = 0.0031\%
\]

Table 34-2 shows the relation between the clock generated by the PLL and the frequency error from jitter (measured jitter-induced error of 2%, Gaussian distribution, within three standard deviations), as a percentage of the nominal clock frequency.

This is clearly smaller than the expected drift of a crystal oscillator, typically specified at 100 ppm or 0.01%. If we add jitter to oscillator drift, we have a total frequency drift of 0.0132%. The total oscillator frequency errors for common clock frequencies and bit rates, including both drift and jitter, are shown in Table 34-3.

**TABLE 34-2: FREQUENCY ERROR FROM JITTER AT VARIOUS PLL GENERATED CLOCK SPEEDS**

<table>
<thead>
<tr>
<th>PLL Output</th>
<th>$P_{\text{jitter}}$</th>
<th>$T_{\text{jitter}}$</th>
<th>Frequency Error at Various Nominal Bit Times (Bit Rates)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>8 µs (125 Kb/s)</td>
</tr>
<tr>
<td>40 MHz</td>
<td>0.5 ns</td>
<td>1 ns</td>
<td>0.00125%</td>
</tr>
<tr>
<td>24 MHz</td>
<td>0.83 ns</td>
<td>1.67 ns</td>
<td>0.00209%</td>
</tr>
<tr>
<td>16 MHz</td>
<td>1.25 ns</td>
<td>2.5 ns</td>
<td>0.00313%</td>
</tr>
</tbody>
</table>
34.8.2 TIME QUANTA
As already mentioned, the Time Quanta is a fixed unit derived from the oscillator period and baud rate prescaler. Its relationship to TBIT and the Nominal Bit Rate is shown in Example 34-1.

EXAMPLE 34-1: CALCULATING TQ, NOMINAL BIT RATE AND NOMINAL BIT TIME

\[
T_Q (\mu s) = \frac{2 \times (B\text{RP} + 1)}{F_{OSC} (MHz)} \\
T_{\text{BIT}} (\mu s) = T_Q (\mu s) \times \text{number of } T_Q \text{ per bit interval} \\
\text{Nominal Bit Rate (bits/s)} = \frac{1}{T_{\text{BIT}}} \\
\text{This frequency (FOSC) refers to the effective frequency used. If, for example, a 10 MHz external signal is used along with a PLL, then the effective frequency will be 4 x 10 MHz which equals 40 MHz.}
\]

**CASE 1:**
For FOSC = 16 MHz, B\text{RP}<5:0> = 00h and Nominal Bit Time = 8 TQ:

\[
T_Q = \frac{2 \times 1}{16} = 0.125 \mu s (125 \text{ ns}) \\
T_{\text{BIT}} = 8 \times 0.125 = 1 \mu s (10^{-6} \text{ s}) \\
\text{Nominal Bit Rate} = 1/10^{-6} = 10^6 \text{ bits/s (1 Mb/s)}
\]

**CASE 2:**
For FOSC = 20 MHz, B\text{RP}<5:0> = 01h and Nominal Bit Time = 8 TQ:

\[
T_Q = \frac{2 \times 2}{20} = 0.2 \mu s (200 \text{ ns}) \\
T_{\text{BIT}} = 8 \times 0.2 = 1.6 \mu s (1.6 \times 10^{-6} \text{ s}) \\
\text{Nominal Bit Rate} = 1/1.6 \times 10^{-6} = 625,000 \text{ bits/s (625 Kbps)}
\]

**CASE 3:**
For FOSC = 25 MHz, B\text{RP}<5:0> = 3Fh and Nominal Bit Time = 25 TQ:

The frequencies of the oscillators in the different nodes must be coordinated in order to provide a system wide specified Nominal Bit Time. This means that all oscillators must have a Tosc that is an integral divisor of T0. It should also be noted that although the number of T0 is programmable from 4 to 25, the usable minimum is 8 T0. There is no assurance that a bit time of less than 8 T0 in length will operate correctly.

34.8.3 SYNCHRONIZATION SEGMENT
This part of the bit time is used to synchronize the various CAN nodes on the bus. The edge of the input signal is expected to occur during the sync segment. The duration is 1 TQ.

34.8.4 PROPAGATION SEGMENT
This part of the bit time is used to compensate for physical delay times within the network. These delay times consist of the signal propagation time on the bus line and the internal delay time of the nodes. The length of the propagation segment can be programmed from 1 TQ to 8 TQ by setting the PRSEG<2:0> bits.

34.8.5 PHASE BUFFER SEGMENTS
The phase buffer segments are used to optimally locate the sampling point of the received bit within the Nominal Bit Time. The sampling point occurs between Phase Segment 1 and Phase Segment 2. These segments can be lengthened or shortened by the resynchronization process. The end of Phase Segment 1 determines the sampling point within a bit time. Phase Segment 1 is programmable from 1 TQ to 8 TQ in duration. Phase Segment 2 provides a delay before the next transmitted data transition and is also programmable from 1 TQ to 8 TQ in duration. However, due to IPT requirements, the actual minimum length of Phase Segment 2 is 2 TQ, or it may be defined to be equal to the greater of Phase Segment 1 or the Information Processing Time (IPT). The sampling point should be as late as possible or approximately 80% of the bit time.

34.8.6 SAMPLE POINT
The sample point is the point of time at which the bus level is read and the value of the received bit is determined. The sampling point occurs at the end of Phase Segment 1. If the bit timing is slow and contains many T0, it is possible to specify multiple sampling of the bus line at the sample point. The value of the received bit is determined to be the value of the majority decision of three values. The three samples are taken at the sample point and twice before, with a time of T0/2 between each sample.
### 34.8.7 INFORMATION PROCESSING TIME

The Information Processing Time (IPT) is the time segment starting at the sample point that is reserved for calculation of the subsequent bit level. The CAN specification defines this time to be less than or equal to 2 TQ. The ECAN module defines this time to be 2 TQ. Thus, Phase Segment 2 must be at least 2 TQ long.

### 34.8.8 CLOCK SELECTION

The CLKSEL bit of the CIOCON register allows for selection between two CAN input clocks. When CLKSEL = 0 (default), the CAN clock (fosc in the equations above) will be the same as the system clock. When CLKSEL = 1, the CAN clock will be the clock selected by the FEXTOSC Configuration bit, regardless of the system clock. This allows for the core of the device to be clocked by a PLL at 64 MHz (16 MHz HS crystal+4xPLL) while keeping the CAN clocked by the base 16 MHz HS crystal without the PLL, for example.

**Note:** If CLKSEL = 1, the system clock must be greater than or equal to the FEXTOSC selected clock. Having a slower system clock than the CAN clock will lead to unexpected behavior. The Information Processing Time (IPT) is the time segment starting at the sample point that is reserved for calculation of the subsequent bit level. The CAN specification defines this time to be less than or equal to 2 TQ. The CAN module defines this time to be 2 TQ. Thus, Phase Segment 2 must be at least 2 TQ long.

### 34.9 Synchronization

To compensate for phase shifts between the oscillator frequencies of each of the nodes on the bus, each CAN controller must be able to synchronize to the relevant signal edge of the incoming signal. When an edge in the transmitted data is detected, the logic will compare the location of the edge to the expected time (Sync_Seg). The circuit will then adjust the values of Phase Segment 1 and Phase Segment 2 as necessary. There are two mechanisms used for synchronization.

#### 34.9.1 HARD SYNCHRONIZATION

Hard synchronization is only done when there is a recessive to dominant edge during a bus Idle condition, indicating the start of a message. After hard synchronization, the bit time counters are restarted with Sync_Seg. Hard synchronization forces the edge, which has occurred to lie within the synchronization segment of the restarted bit time. Due to the rules of synchronization, if a hard synchronization occurs, there will not be a resynchronization within that bit time.

#### 34.9.2 RESYNCHRONIZATION

As a result of resynchronization, Phase Segment 1 may be lengthened or Phase Segment 2 may be shortened. The amount of lengthening or shortening of the phase buffer segments has an upper bound given by the Synchronization Jump Width (SJW). The value of the SJW will be added to Phase Segment 1 (see Figure 34-6) or subtracted from Phase Segment 2 (see Figure 34-7). The SJW is programmable between 1 TQ and 4 TQ.

Clocking information will only be derived from recessive to dominant transitions. The property, that only a fixed maximum number of successive bits have the same value, ensures resynchronization to the bit stream during a frame.

The phase error of an edge is given by the position of the edge relative to Sync_Seg, measured in TQ. The phase error is defined in magnitude of TQ as follows:

- $e = 0$ if the edge lies within Sync_Seg.
- $e > 0$ if the edge lies before the sample point.
- $e < 0$ if the edge lies after the sample point of the previous bit.

If the magnitude of the phase error is less than, or equal to, the programmed value of the Synchronization Jump Width, the effect of a resynchronization is the same as that of a hard synchronization.

If the magnitude of the phase error is larger than the Synchronization Jump Width and if the phase error is positive, then Phase Segment 1 is lengthened by an amount equal to the Synchronization Jump Width.

If the magnitude of the phase error is larger than the resynchronization jump width and if the phase error is negative, then Phase Segment 2 is shortened by an amount equal to the Synchronization Jump Width.

#### 34.9.3 SYNCHRONIZATION RULES

- Only one synchronization within one bit time is allowed.
- An edge will be used for synchronization only if the value detected at the previous sample point (previously read bus value) differs from the bus value immediately after the edge.
- All other recessive to dominant edges fulfilling rules 1 and 2 will be used for resynchronization, with the exception that a node transmitting a dominant bit will not perform a resynchronization as a result of a recessive to dominant edge with a positive phase error.

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**Note:** If CLKSEL = 1, the system clock must be greater than or equal to the FEXTOSC selected clock. Having a slower system clock than the CAN clock will lead to unexpected behavior.
34.10 Programming Time Segments

Some requirements for programming of the time segments:

- Prop_Seg + Phase_Seg 1 ≥ Phase_Seg 2
- Phase_Seg 2 ≥ Sync Jump Width.

For example, assume that a 125 kHz CAN baud rate is desired, using 20 MHz for FOSC. With a Tosc of 50 ns, a baud rate prescaler value of 04h gives a TQ of 500 ns. To obtain a Nominal Bit Rate of 125 kHz, the Nominal Bit Time must be 8 µs or 16 TQ.

Using 1 TQ for the Sync_Seg, 2 TQ for the Prop_Seg and 7 TQ for Phase Segment 1 would place the sample point at 10 TQ after the transition. This leaves 6 TQ for Phase Segment 2.

By the rules above, the Sync Jump Width could be the maximum of 4 TQ. However, normally a large SJW is only necessary when the clock generation of the different nodes is inaccurate or unstable, such as using ceramic resonators. Typically, an SJW of 1 is enough.

34.11 Oscillator Tolerance

As a rule of thumb, the bit timing requirements allow ceramic resonators to be used in applications with transmission rates of up to 125 Kbit/sec. For the full bus speed range of the CAN protocol, a quartz oscillator is required. Refer to ISO11898-1 for oscillator tolerance requirements.

34.12 Bit Timing Configuration Registers

The Baud Rate Control registers (BRGCON1, BRGCON2, BRGCON3) control the bit timing for the CAN bus interface. These registers can only be modified when the CAN module is in Configuration mode.

34.12.1 BRGCON1

The BRP bits control the baud rate prescaler. The SJW<1:0> bits select the synchronization jump width in terms of multiples of TQ.
34.12.2  BRGCON2
The PRSEG bits set the length of the propagation segment in terms of Tq. The SEG1PH bits set the length of Phase Segment 1 in Tq. The SAM bit controls how many times the RXCAN pin is sampled. Setting this bit to a '1' causes the bus to be sampled three times: twice at Tq/2 before the sample point and once at the normal sample point (which is at the end of Phase Segment 1). The value of the bus is determined to be the value read during at least two of the samples. If the SAM bit is set to a '0', then the RXCAN pin is sampled only once at the sample point. The SEG2PHTS bit controls how the length of Phase Segment 2 is determined. If this bit is set to a '1', then the length of Phase Segment 2 is determined by the SEG2PH bits of BRGCON3. If the SEG2PHTS bit is set to a '0', then the length of Phase Segment 2 is the greater of Phase Segment 1 and the information processing time (which is fixed at 2 Tq for the ECAN module).

34.12.3  BRGCON3
The PHSEG2<2:0> bits set the length (in Tq) of Phase Segment 2 if the SEG2PHTS bit is set to a '1'. If the SEG2PHTS bit is set to a '0', then the PHSEG2<2:0> bits have no effect.

34.13  Error Detection
The CAN protocol provides sophisticated error detection mechanisms. The following errors can be detected.

34.13.1  CRC ERROR
With the Cyclic Redundancy Check (CRC), the transmitter calculates special check bits for the bit sequence, from the start of a frame until the end of the data field. This CRC sequence is transmitted in the CRC field. The receiving node also calculates the CRC sequence using the same formula and performs a comparison to the received sequence. If a mismatch is detected, a CRC error has occurred and an error frame is generated. The message is repeated.

34.13.2  ACKNOWLEDGE ERROR
In the Acknowledge field of a message, the transmitter checks if the Acknowledge slot (which was sent out as a recessive bit) contains a dominant bit. If not, no other node has received the frame correctly. An Acknowledge error has occurred, an error frame is generated and the message will have to be repeated.

34.13.3  FORM ERROR
If a node detects a dominant bit in one of the four segments, including End-of-Frame (EOF), interframe space, Acknowledge delimiter or CRC delimiter, then a form error has occurred and an error frame is generated. The message is repeated.

34.13.4  BIT ERROR
A bit error occurs if a transmitter sends a dominant bit and detects a recessive bit, or if it sends a recessive bit and detects a dominant bit, when monitoring the actual bus level and comparing it to the just transmitted bit. In the case where the transmitter sends a recessive bit and a dominant bit is detected during the arbitration field and the Acknowledge slot, no bit error is generated because normal arbitration is occurring.

34.13.5  STUFF BIT ERROR
If, between the Start-of-Frame (SOF) and the CRC delimiter, six consecutive bits with the same polarity are detected, the bit stuffing rule has been violated. A stuff bit error occurs and an error frame is generated. The message is repeated.

34.13.6  ERROR STATES
Detected errors are made public to all other nodes via error frames. The transmission of the erroneous message is aborted and the frame is repeated as soon as possible. Furthermore, each CAN node is in one of the three error states; “error-active”, “error-passive” or “bus-off”, according to the value of the internal error counters. The error-active state is the usual state where the bus node can transmit messages and activate error frames (made of dominant bits) without any restrictions. In the error-passive state, messages and passive error frames (made of recessive bits) may be transmitted. The bus-off state makes it temporarily impossible for the node to participate in the bus communication. During this state, messages can neither be received nor transmitted.

34.13.7  ERROR MODES AND ERROR COUNTERS
The CAN module contains two error counters: the Receive Error Counter (RXERRCNT) and the Transmit Error Counter (TXERRCNT). The values of both counters can be read by the MCU. These counters are incremented or decremented in accordance with the CAN bus specification.

The CAN module is error-active if both error counters are below the error-passive limit of 128. They are error-passive if at least one of the error counters equals or exceeds 128. They go to bus-off if the transmit error counter equals or exceeds the bus-off limit of 256. The devices remain in this state until the bus-off recovery sequence is finished. The bus-off recovery sequence consists of 128 occurrences of 11 consecutive recessive bits (see Figure 34-8). Note that the CAN module, after going bus-off, will recover back to error-active without any intervention by the MCU if the bus remains Idle for 128 x 11 bit times. If this is not desired, the error Interrupt Service Routine should address this. The current Error mode of the CAN module can be read by the MCU via the COMSTAT register.
Additionally, there is an Error State Warning flag bit, EWARN, which is set if at least one of the error counters equals or exceeds the error warning limit of 96. EWARN is reset if both error counters are less than the error warning limit.

**FIGURE 34-8: ERROR MODES STATE DIAGRAM**
34.14 CAN Interrupts

The module has several sources of interrupts. Each of these interrupts can be individually enabled or disabled. The PIR5 register contains interrupt flags. The PIE5 register contains the enables for the eight main interrupts. A special set of read-only bits in the CANSTAT register, the ICODE bits, can be used in combination with a jump table for efficient handling of interrupts.

All interrupts have one source, with the exception of the error interrupt and buffer interrupts in Mode 1 and 2. Any of the error interrupt sources can set the error interrupt flag. The source of the error interrupt can be determined by reading the Communication Status register, COMSTAT. In Mode 1 and 2, there are two interrupt enable/disable and flag bits – one for all transmit buffers and the other for all receive buffers.

The interrupts can be broken up into two categories: receive and transmit interrupts.

The receive related interrupts are:
- Receive Interrupts
- Wake-up Interrupt
- Receiver Overrun Interrupt
- Receiver Warning Interrupt
- Receiver Error-Passive Interrupt

The transmit related interrupts are:
- Transmit Interrupts
- Transmitter Warning Interrupt
- Transmitter Error-Passive Interrupt
- Bus-Off Interrupt

34.14.1 INTERRUPT CODE BITS

To simplify the interrupt handling process in user firmware, the ECAN module encodes a special set of bits. In Mode 0, these bits are ICODE<3:1> in the CANSTAT register. In Mode 1 and 2, these bits are EICODE<4:0> in the CANSTAT register. Interrupts are internally prioritized such that the higher priority interrupts are assigned lower values. Once the highest priority interrupt condition has been cleared, the code for the next highest priority interrupt that is pending (if any) will be reflected by the ICODE bits (see Table 34-4). Note that only those interrupt sources that have their associated interrupt enable bit set will be reflected in the ICODE bits.

In Mode 2, when a receive message interrupt occurs, the EICODE bits will always consist of ‘10000’. User firmware may use FIFO Pointer bits to actually access the next available buffer.

34.14.2 TRANSMIT INTERRUPT

When the transmit interrupt is enabled, an interrupt will be generated when the associated transmit buffer becomes empty and is ready to be loaded with a new message. In Mode 0, there are separate interrupt enable/disable and flag bits for each of the three dedicated transmit buffers. The TXBnIF bit will be set to indicate the source of the interrupt. The interrupt is cleared by the MCU, resetting the TXBnIF bit to a ‘0’. In Mode 1 and 2, all transmit buffers share one interrupt enable/disable bit and one flag bit. In Mode 1 and 2, TXBnIE in PIE5 and TXBnIF in PIR5 indicate when a transmit buffer has completed transmission of its message. TXBnIF, TXBnIE and TXBnIP in PIR5, PIE5 and IPR5, respectively, are not used in Mode 1 and 2. Individual transmit buffer interrupts can be enabled or disabled by setting or clearing TXBnIE and B0IE register bits. When a shared interrupt occurs, user firmware must poll the TXREQ bit of all transmit buffers to detect the source of interrupt.

34.14.3 RECEIVE INTERRUPT

When the receive interrupt is enabled, an interrupt will be generated when a message has been successfully received and loaded into the associated receive buffer. This interrupt is activated immediately after receiving the End-of-Frame (EOF) field.

In Mode 0, the RXBnIF bit is set to indicate the source of the interrupt. The interrupt is cleared by the MCU, resetting the RXBnIF bit to a ‘0’.

In Mode 1 and 2, all receive buffers share RXBnIE, RXBnIF and RXBnIP in PIE5, PIR5 and IPR5, respectively. Individual receive buffer interrupts can be controlled by the TXBnIE and BIE0 registers. In Mode 1, when a shared receive interrupt occurs, user firmware must poll the RXFUL bit of each receive buffer to detect the source of interrupt. In Mode 2, a receive interrupt indicates that the new message is loaded into FIFO. FIFO can be read by using FIFO Pointer bits, FP.
34.14.4 MESSAGE ERROR INTERRUPT

When an error occurs during transmission or reception of a message, the message error flag, IRXIF, will be set and if the IRXIE bit is set, an interrupt will be generated. This is intended to be used to facilitate baud rate determination when used in conjunction with Listen Only mode.

34.14.5 BUS ACTIVITY WAKE-UP INTERRUPT

When the ECAN module is in Sleep mode and the bus activity wake-up interrupt is enabled, an interrupt will be generated and the WAKIF bit will be set when activity is detected on the CAN bus. This interrupt causes the MCU to exit Sleep mode. The interrupt is reset by the MCU, clearing the WAKIF bit.

34.14.6 ERROR INTERRUPT

When the CAN module error interrupt (ERRIE in PIE5) is enabled, an interrupt is generated if an overflow condition occurs, or if the error state of the transmitter or receiver has changed. The error flags in COMSTAT will indicate one of the following conditions.

34.14.6.1 Receiver Overflow

An overflow condition occurs when the MAB has assembled a valid received message (the message meets the criteria of the acceptance filters) and the receive buffer associated with the filter is not available for loading of a new message. The associated RXBnOVFL bit in the COMSTAT register will be set to indicate the overflow condition. This bit must be cleared by the MCU. In mode 0, RXB0 and RXB1 have separate overflow bits. In modes 1 and 2, there is one shared bit that indicates a receive buffer has overflowed, but each buffer must be checked individually.

34.14.6.2 Receiver Warning

The receive error counter has reached the MCU warning limit of 96. This is indicated by the RXWARN bit of the COMSTAT register.

34.14.6.3 Transmitter Warning

The transmit error counter has reached the MCU warning limit of 96. This is indicated by the TXWARN bit of the COMSTAT register.

34.14.6.4 Receiver Bus Passive

This will occur when the device has gone to the error-passive state because the receive error counter is greater or equal to 128. This is indicated by the RXBP bit of the COMSTAT register.

34.14.6.5 Transmitter Bus Passive

This will occur when the device has gone to the error-passive state because the transmit error counter is greater or equal to 128. This is indicated by the TXBP bit of the COMSTAT register.

34.14.6.6 Bus-Off

The transmit error counter has exceeded 255 and the device has gone to bus-off state. This is indicated by the TXBO bit of the COMSTAT register.

**TABLE 34-4: VALUES FOR ICODE<2:0>**

<table>
<thead>
<tr>
<th>ICODE&lt;2:0&gt;</th>
<th>Interrupt</th>
<th>Boolean Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>None</td>
<td>ERR•WAK•TX0•TX1•TX2•RX0•RX1</td>
</tr>
<tr>
<td>001</td>
<td>Error</td>
<td>ERR</td>
</tr>
<tr>
<td>010</td>
<td>TXB2</td>
<td>ERR•TX0•TX1•TX2</td>
</tr>
<tr>
<td>011</td>
<td>TXB1</td>
<td>ERR•TX0•TX1</td>
</tr>
<tr>
<td>100</td>
<td>TXB0</td>
<td>ERR•TX0</td>
</tr>
<tr>
<td>101</td>
<td>RXB1</td>
<td>ERR•TX0•TX1•TX2•RX0•RX1</td>
</tr>
<tr>
<td>110</td>
<td>RXB0</td>
<td>ERR•TX0•TX1•TX2•RX0</td>
</tr>
<tr>
<td>111</td>
<td>Wake on Interrupt</td>
<td>ERR•TX0•TX1•TX2•RX0•RX1•WAK</td>
</tr>
</tbody>
</table>

**Legend:**

ERR = ERRIF * ERRIE
RX0 = RXB0IF * RXB0IE
TX0 = TXB0IF * TXB0IE
RX1 = RXB1IF * RXB1IE
TX1 = TXB1IF * TXB1IE
WAK = WAKIF * WAKIE
TX2 = TXB2IF * TXB2IE
34.15 CAN Module Registers

| Note: | Not all CAN registers are available in the Access Bank. |

There are many control and data registers associated with the CAN module. For convenience, their descriptions have been grouped into the following sections:

- Control and Status Registers
- Dedicated Transmit Buffer Registers
- Dedicated Receive Buffer Registers
- Programmable TX/RX and Auto RTR Buffers
- Baud Rate Control Registers
- I/O Control Register
- Interrupt Status and Control Registers

Detailed descriptions of each register and their usage are described in the following sections.

34.15.1 CAN CONTROL AND STATUS REGISTERS

The registers described in this section control the overall operation of the CAN module and show its operational status.
REGISTER 34-1: CANCON: CAN CONTROL REGISTER

<table>
<thead>
<tr>
<th>Mode 0</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/S-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>REQP2</td>
<td>REQP1</td>
<td>REQP0</td>
<td>ABAT</td>
<td>WIN2</td>
<td>WIN1</td>
<td>WIN0</td>
<td>—</td>
</tr>
<tr>
<td>Mode 1</td>
<td>R/W-1</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/S-0</td>
<td>U0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td></td>
<td>REQP2</td>
<td>REQP1</td>
<td>REQP0</td>
<td>ABAT</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Mode 2</td>
<td>R/W-1</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/S-0</td>
<td>R-0</td>
<td>R-0</td>
<td>R-0</td>
<td>R-0</td>
</tr>
<tr>
<td></td>
<td>REQP2</td>
<td>REQP1</td>
<td>REQP0</td>
<td>ABAT</td>
<td>FP3</td>
<td>FP2</td>
<td>FP1</td>
<td>FP0</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- S = Settable bit
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 7-5  REQP<2:0>: Request CAN Operation Mode bits
1xx = Requests Configuration mode
011 = Requests Listen Only mode
010 = Requests Loopback mode
001 = Disabled/Sleep mode
000 = Requests Normal mode

bit 4  ABAT: Abort All Pending Transmissions bit
1 = Abort all pending transmissions (in all transmit buffers)(1)
0 = Transmissions proceeding as normal

bit 3-1  Mode 0:
WIN<2:0>: Window Address bits
These bits select which of the CAN buffers to switch into the Access Bank area. This allows access to the
buffer registers from any data memory bank. After a frame has caused an interrupt, the ICODE<3:0> bits
can be copied to the WIN<2:0> bits to select the correct buffer. See Example 34-2 for a code example.
111 = Receive Buffer 0
110 = Receive Buffer 0
101 = Receive Buffer 1
100 = Transmit Buffer 0
011 = Transmit Buffer 1
010 = Transmit Buffer 2
001 = Receive Buffer 0
000 = Receive Buffer 0

bit 0  Mode 0:
Unimplemented: Read as ‘0’

bit 4-0  Mode 1:
Unimplemented: Read as ‘0’

Mode 2:
FP<3:0>: FIFO Read Pointer bits
These bits point to the message buffer to be read.
0000 = Receive Message Buffer 0
0001 = Receive Message Buffer 1
0010 = Receive Message Buffer 2
0011 = Receive Message Buffer 3
0100 = Receive Message Buffer 4
0101 = Receive Message Buffer 5
0110 = Receive Message Buffer 6
0111 = Receive Message Buffer 7
1000:1111 Reserved

Note 1: This bit will clear when all transmissions are aborted.
## REGISTER 34-2: CANSTAT: CAN STATUS REGISTER

<table>
<thead>
<tr>
<th>Mode</th>
<th>R-1</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mode 1,2</td>
<td>R-1</td>
<td>R-0</td>
<td>R-0</td>
<td>R-0</td>
<td>R-0</td>
<td>R-0</td>
<td>R-0</td>
<td>R-0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**bit 7-5**: OPCODE<2:0>: Operation Mode Status bits\(^{(1)}\)

<table>
<thead>
<tr>
<th>Mode</th>
<th>000</th>
<th>001</th>
<th>010</th>
<th>011</th>
<th>100</th>
<th>101</th>
<th>110</th>
<th>111</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**bit 4**: Mode 0:
- Unimplemented: Read as ‘0’

**bit 3, 4-0**: Mode 0:
- ICODE<2:0>: Interrupt Code bits

When an interrupt occurs, a prioritized coded interrupt value will be present in these bits. This code indicates the source of the interrupt. By copying ICODE<3:1> to WIN<3:0> (Mode 0) or EICODE<4:0> to EWIN<4:0> (Mode 1 and 2), it is possible to select the correct buffer to map into the Access Bank area. See Example 34-2 for a code example. To simplify the description, the following table lists all five bits.

<table>
<thead>
<tr>
<th>Mode 0</th>
<th>Mode 1</th>
<th>Mode 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>No interrupt</td>
<td>00000</td>
<td>00000</td>
</tr>
<tr>
<td>CAN bus error interrupt</td>
<td>00010</td>
<td>00010</td>
</tr>
<tr>
<td>TXB2 interrupt</td>
<td>00100</td>
<td>00100</td>
</tr>
<tr>
<td>TXB1 interrupt</td>
<td>00110</td>
<td>00110</td>
</tr>
<tr>
<td>TXB0 interrupt</td>
<td>01000</td>
<td>01000</td>
</tr>
<tr>
<td>RXB1 interrupt</td>
<td>01010</td>
<td>10001</td>
</tr>
<tr>
<td>RXB0 interrupt</td>
<td>01100</td>
<td>10000</td>
</tr>
<tr>
<td>Wake-up interrupt</td>
<td>01110</td>
<td>01110</td>
</tr>
<tr>
<td>RXB0 interrupt</td>
<td>-----</td>
<td>10000</td>
</tr>
<tr>
<td>RXB1 interrupt</td>
<td>-----</td>
<td>10001</td>
</tr>
<tr>
<td>RX/TX B0 interrupt</td>
<td>-----</td>
<td>10010</td>
</tr>
<tr>
<td>RX/TX B1 interrupt</td>
<td>-----</td>
<td>10011</td>
</tr>
<tr>
<td>RX/TX B2 interrupt</td>
<td>-----</td>
<td>10100</td>
</tr>
<tr>
<td>RX/TX B3 interrupt</td>
<td>-----</td>
<td>10101</td>
</tr>
<tr>
<td>RX/TX B4 interrupt</td>
<td>-----</td>
<td>10110</td>
</tr>
<tr>
<td>RX/TX B5 interrupt</td>
<td>-----</td>
<td>10111</td>
</tr>
</tbody>
</table>

**bit 0**: Mode 0:
- Unimplemented: Read as ‘0’

**bit 4-0**: Mode 1, 2:
- EICODE<4:0>: Interrupt Code bits

See ICODE<3:1> above.

**Note 1**: To achieve maximum power saving and/or able to wake-up on CAN bus activity, switch the CAN module in Disable/Sleep mode before putting the device to Sleep.

**Note 2**: If the buffer is configured as a receiver, the EICODE bits will contain ‘10000’ upon interrupt.
EXAMPLE 34-2:  CHANGING TO CONFIGURATION MODE

; Request Configuration mode.
MOVLW B'10000000' ; Set to Configuration Mode.
MOVWF CANCON

; A request to switch to Configuration mode may not be immediately honored.
; Module will wait for CAN bus to be idle before switching to Configuration Mode.
; Request for other modes such as Loopback, Disable etc. may be honored immediately.
; It is always good practice to wait and verify before continuing.
ConfigWait:
    MOVF CANSTAT, W ; Read current mode state.
    ANDLW B'10000000' ; Interested in OPMODE bits only.
    TSTFSZ WREG ; Is it Configuration mode yet?
    BRA ConfigWait ; No. Continue to wait...

; Module is in Configuration mode now.
; Modify configuration registers as required.
; Switch back to Normal mode to be able to communicate.

EXAMPLE 34-3:  WIN AND ICODE BITS USAGE IN INTERRUPT SERVICE ROUTINE TO ACCESS TX/RX BUFFERS

; Save application required context.
; Poll interrupt flags and determine source of interrupt
; This was found to be CAN interrupt
; TempCANCON and TempCANSTAT are variables defined in Access Bank low
    MOVF TempCANSTAT, W ; Retrieve ICODE bits
    ANDLW B'00001110'
    ADDWF PCL, F ; Perform computed GOTO
    BRA NoInterrupt ; 000 = No interrupt
    BRA ErrorInterrupt ; 001 = Error interrupt
    BRA TXB2Interrupt ; 010 = TXB2 interrupt
    BRA TXB1Interrupt ; 011 = TXB1 interrupt
    BRA RXB0Interrupt ; 100 = RXB0 interrupt
    BRA RXB1Interrupt ; 101 = RXB1 interrupt
    BRA RXB0Interrupt ; 110 = RXB0 interrupt
    BRA WakeupInterrupt ; 111 = Wake-up on interrupt

WakeupInterrupt
    BCF PIR3, WAKIF ; Clear the interrupt flag
    ; User code to handle wake-up procedure
    ;
    ; Continue checking for other interrupt source or return from here
    ...

NoInterrupt
    ; PC should never vector here. User may
    ; place a trap such as infinite loop or pin/port
    ; indication to catch this error.
EXAMPLE 34-2: WIN AND ICODE BITS USAGE IN INTERRUPT SERVICE ROUTINE TO ACCESS TX/RX BUFFERS (CONTINUED)

```assembly
ErrorInterrupt
    BCF PIR3, ERRIF ; Clear the interrupt flag
    ... ; Handle error.
    RETFIE

TXB2Interrupt
    BCF PIR3, TXB2IF ; Clear the interrupt flag
    GOTO AccessBuffer

TXB1Interrupt
    BCF PIR3, TXB1IF ; Clear the interrupt flag
    GOTO AccessBuffer

TXB0Interrupt
    BCF PIR3, TXB0IF ; Clear the interrupt flag
    GOTO AccessBuffer

RXB1Interrupt
    BCF PIR3, RXB1IF ; Clear the interrupt flag
    GOTO AccessBuffer

RXB0Interrupt
    BCF PIR3, RXB0IF ; Clear the interrupt flag
    GOTO AccessBuffer

AccessBuffer ; This is either TX or RX interrupt
    ; Copy CANSTAT.ICODE bits to CANCON.WIN bits
    MOVF TempCANCON, W ; Clear CANCON.WIN bits before copying
    ; new ones.
    ANDLW B'11110001' ; Use previously saved CANCON value to
    ; make sure same value.
    MOVWF TempCANCON
    MOVF TempCANSTAT, W ; Retrieve ICODE bits
    ANDLW B'00001110' ; Use previously saved CANSTAT value
    ; to make sure same value.
    IORWF TempCANCON ; Copy ICODE bits to WIN bits.
    MOVFF TempCANCON, CANCON ; Copy the result to actual CANCON
    ; Access current buffer...
    ; User code
    ; Restore CANCON.WIN bits
    MOVF CANCON, W ; Preserve current non WIN bits
    ANDLW B'11110001'
    IORWF TempCANCON ; Restore original WIN bits
    ; Do not need to restore CANSTAT - it is read-only register.
    ; Return from interrupt or check for another module interrupt source
```
**REGISTER 34-3: ECANCON: ENHANCED CAN CONTROL REGISTER**

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDSEL1(1)</td>
<td>MDSEL0(1)</td>
<td>FIFOWM(2)</td>
<td>EWIN4</td>
<td>EWIN3</td>
<td>EWIN2</td>
<td>EWIN1</td>
<td>EWIN0</td>
</tr>
</tbody>
</table>

**Legend:**

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**bit 7-6**

**MDSEL<1:0>: Mode Select bits(1)**

- 00 = Legacy mode (Mode 0, default)
- 01 = Enhanced Legacy mode (Mode 1)
- 10 = Enhanced FIFO mode (Mode 2)
- 11 = Reserved

**bit 5**

**FIFOWM: FIFO High Water Mark bit(2)**

- 1 = Will cause FIFO interrupt when one receive buffer remains
- 0 = Will cause FIFO interrupt when four receive buffers remain(3)

**bit 4-0**

**EWIN<4:0>: Enhanced Window Address bits**

These bits map the group of 16 banked CAN SFRs into Access Bank addresses, 0F60-0F6Dh. The exact group of registers to map is determined by the binary value of these bits.

- **Mode 0:**
  - **Unimplemented:** Read as ‘0’
- **Mode 1, 2:**
  - 00000 = Acceptance Filters 0, 1, 2 and BRGCON2, 3
  - 00001 = Acceptance Filters 3, 4, 5 and BRGCON1, CIOCON
  - 00010 = Acceptance Filter Masks, Error and Interrupt Control
  - 00011 = Transmit Buffer 0
  - 00100 = Transmit Buffer 1
  - 00101 = Transmit Buffer 2
  - 00110 = Acceptance Filters 6, 7, 8
  - 00111 = Acceptance Filters 9, 10, 11
  - 01000 = Acceptance Filters 12, 13, 14
  - 01001 = Acceptance Filter 15
  - 01010-01110 = Reserved
  - 01111 = RXINT0, RXINT1
  - 10000 = Receive Buffer 0
  - 10001 = Receive Buffer 1
  - 10010 = TX/RX Buffer 0
  - 10011 = TX/RX Buffer 1
  - 10100 = TX/RX Buffer 2
  - 10101 = TX/RX Buffer 3
  - 10110 = TX/RX Buffer 4
  - 10111 = TX/RX Buffer 5
  - 11000-11111 = Reserved

**Note 1:** These bits can only be changed in Configuration mode. See Register 34-1 to change to Configuration mode.

**2:** This bit is used in Mode 2 only.

**3:** If FIFO is configured to contain four or less buffers, then the FIFO interrupt will trigger.
### REGISTER 34-4: COMSTAT: COMMUNICATION STATUS REGISTER

<table>
<thead>
<tr>
<th>Mode 0</th>
<th>R/C-0</th>
<th>R/C-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXB0OVFL</td>
<td>RXB1OVFL</td>
<td>TXBO</td>
<td>TXBP</td>
<td>RXBP</td>
<td>TXWARN</td>
<td>RXWARN</td>
<td>EWARN</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Mode 1</th>
<th>R/C-0</th>
<th>R/C-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>RXBnOVFL</td>
<td>TXBO</td>
<td>TXBP</td>
<td>RXBP</td>
<td>TXWARN</td>
<td>RXWARN</td>
<td>EWARN</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Mode 2</th>
<th>R/C-0</th>
<th>R/C-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIFOEMPTY</td>
<td>RXBnOVFL</td>
<td>TXBO</td>
<td>TXBP</td>
<td>RXBP</td>
<td>TXWARN</td>
<td>RXWARN</td>
<td>EWARN</td>
<td></td>
</tr>
</tbody>
</table>

#### Legend:
- **C**: Clearable bit
- **R**: Readable bit
- **W**: Writable bit
- **U**: Unimplemented bit, read as ‘0’
- **-n**: Value at POR
- **‘1’**: Bit is set
- **‘0’**: Bit is cleared
- **x**: Bit is unknown

#### bit 7
- **Mode 0**: RXB0OVFL: Receive Buffer 0 Overflow bit
  - 1 = Receive Buffer 0 has overflowed
  - 0 = Receive Buffer 0 has not overflowed
- **Mode 1**: Unimplemented: Read as ‘0’
- **Mode 2**: FIFOEMPTY: FIFO Not Empty bit
  - 1 = Receive FIFO is not empty
  - 0 = Receive FIFO is empty

#### bit 6
- **Mode 0**: RXB1OVFL: Receive Buffer 1 Overflow bit
  - 1 = Receive Buffer 1 has overflowed
  - 0 = Receive Buffer 1 has not overflowed
- **Mode 1, 2**: RXBnOVFL: Receive Buffer n Overflow bit
  - 1 = Receive Buffer n has overflowed
  - 0 = Receive Buffer n has not overflowed

#### bit 5
- TXBO: Transmitter Bus-Off bit
  - 1 = Transmit error counter > 255
  - 0 = Transmit error counter ≤ 255

#### bit 4
- TXBP: Transmitter Bus Passive bit
  - 1 = Transmit error counter > 127
  - 0 = Transmit error counter ≤ 127

#### bit 3
- RXBP: Receiver Bus Passive bit
  - 1 = Receive error counter > 127
  - 0 = Receive error counter ≤ 127

#### bit 2
- TXWARN: Transmitter Warning bit
  - 1 = Transmit error counter > 95
  - 0 = Transmit error counter ≤ 95

#### bit 1
- RXWARN: Receiver Warning bit
  - 1 = 127 ≥ Receive error counter > 95
  - 0 = Receive error counter ≤ 95

#### bit 0
- EWARN: Error Warning bit
  - This bit is a flag of the RXWARN and TXWARN bits.
  - 1 = The RXWARN or the TXWARN bits are set
  - 0 = Neither the RXWARN or the TXWARN bits are set
34.15.2 DEDICATED CAN TRANSMIT BUFFER REGISTERS

This section describes the dedicated CAN Transmit Buffer registers and their associated control registers.

REGISTER 34-5: TXBnCON: TRANSMIT BUFFER n CONTROL REGISTERS [0 ≤ n ≤ 2]

<table>
<thead>
<tr>
<th>RC-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXBIF</td>
<td>TXABT</td>
<td>TXLRARB</td>
<td>TXERR</td>
<td>TXREQ</td>
<td>TXPRI1</td>
<td>TXPRI0</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- C = Clearable bit
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 7  **TXBIF**: Transmit Buffer Interrupt Flag bit
- 1 = Transmit buffer has completed transmission of a message and may be reloaded
- 0 = Transmit buffer has not completed transmission of a message

bit 6  **TXABT**: Transmission Aborted Status bit
- 1 = Message was aborted
- 0 = Message was not aborted

bit 5  **TXLRARB**: Transmission Lost Arbitration Status bit
- 1 = Message lost arbitration while being sent
- 0 = Message did not lose arbitration while being sent

bit 4  **TXERR**: Transmission Error Detected Status bit
- 1 = A bus error occurred while the message was being sent
- 0 = A bus error did not occur while the message was being sent

bit 3  **TXREQ**: Transmit Request Status bit
- 1 = Requests sending a message; clears the TXABT, TXLRARB and TXERR bits
- 0 = Automatically cleared when the message is successfully sent

bit 2  **Unimplemented**: Read as ‘0’

bit 1-0  **TXPRI<1:0>**: Transmit Priority bits
- 11 = Priority Level 3 (highest priority)
- 10 = Priority Level 2
- 01 = Priority Level 1
- 00 = Priority Level 0 (lowest priority)

Note:
1: This bit is automatically cleared when TXREQ is set.
2: While TXREQ is set, Transmit Buffer registers remain read-only. Clearing this bit in software while the bit is set will request a message abort.
3: These bits define the order in which transmit buffers will be transferred. They do not alter the CAN message identifier.
**REGISTER 34-6: TXBnSIDH: TRANSMIT BUFFER ‘n’ STANDARD IDENTIFIER REGISTERS, HIGH BYTE [0 ≤ n ≤ 2]**

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>SID10</td>
<td>SID9</td>
<td>SID8</td>
<td>SID7</td>
<td>SID6</td>
<td>SID5</td>
<td>SID4</td>
<td>SID3</td>
</tr>
</tbody>
</table>

Legend:

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 7-0  
\( \text{SID<10:3>}: \) Standard Identifier bits (if EXIDE (TXBnSIDL<3>) = 0)  
Extended Identifier bits, EID<28:21> (if EXIDE = 1).

**REGISTER 34-7: TXBnSIDL: TRANSMIT BUFFER ‘n’ STANDARD IDENTIFIER REGISTERS, LOW BYTE [0 ≤ n ≤ 2]**

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>U-0</th>
<th>R/W-x</th>
<th>U-0</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>SID2</td>
<td>SID1</td>
<td>SID0</td>
<td>—</td>
<td>EXIDE</td>
<td>—</td>
<td>EID17</td>
<td>EID16</td>
</tr>
</tbody>
</table>

Legend:

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 7-5  
\( \text{SID<2:0>}: \) Standard Identifier bits (if EXIDE (TXBnSIDL<3>) = 0)  
Extended Identifier bits, EID<20:18> (if EXIDE = 1).

bit 4  
Unimplemented: Read as ‘0’

bit 3  
EXIDE: Extended Identifier Enable bit

- 1 = Message will transmit extended ID, SID<10:0> become EID<28:18>
- 0 = Message will transmit standard ID, EID<17:0> are ignored

bit 2  
Unimplemented: Read as ‘0’

bit 1-0  
EID<17:16>: Extended Identifier bits

**REGISTER 34-8: TXBnEIDH: TRANSMIT BUFFER ‘n’ EXTENDED IDENTIFIER REGISTERS, HIGH BYTE [0 ≤ n ≤ 2]**

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>EID15</td>
<td>EID14</td>
<td>EID13</td>
<td>EID12</td>
<td>EID11</td>
<td>EID10</td>
<td>EID9</td>
<td>EID8</td>
</tr>
</tbody>
</table>

Legend:

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 7-0  
\( \text{EID<15:8>}: \) Extended Identifier bits (not used when transmitting standard identifier message)
REGISTER 34-9:  TXBnEIDL: TRANSMIT BUFFER 'n' EXTENDED IDENTIFIER REGISTERS, LOW BYTE [0 ≤ n ≤ 2]

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>EID7</td>
<td>EID6</td>
<td>EID5</td>
<td>EID4</td>
<td>EID3</td>
<td>EID2</td>
<td>EID1</td>
<td>EID0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'

- n = Value at POR  
1 = Bit is set  
0 = Bit is cleared  
x = Bit is unknown

bit 7-0  
EID<7:0>: Extended Identifier bits (not used when transmitting standard identifier message)

REGISTER 34-10:  TXBnDm: TRANSMIT BUFFER 'n' DATA FIELD BYTE 'm' REGISTERS  
[0 ≤ n ≤ 2, 0 ≤ m ≤ 7]

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXBnDm7</td>
<td>TXBnDm6</td>
<td>TXBnDm5</td>
<td>TXBnDm4</td>
<td>TXBnDm3</td>
<td>TXBnDm2</td>
<td>TXBnDm1</td>
<td>TXBnDm0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'

- n = Value at POR  
1 = Bit is set  
0 = Bit is cleared  
x = Bit is unknown

bit 7-0  
TXBnDm<7:0>: Transmit Buffer n Data Field Byte m bits (where 0 ≤ n < 3 and 0 ≤ m < 8)
Each transmit buffer has an array of registers. For example, Transmit Buffer 0 has 7 registers: TXB0D0 to TXB0D7.
 REGISTER 34-11: TXBnDLC: TRANSMIT BUFFER ‘n’ DATA LENGTH CODE REGISTERS [0 ≤ n ≤ 2]

<table>
<thead>
<tr>
<th></th>
<th>U-0</th>
<th>R/W-x</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>—</td>
<td>TXRTR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DLC3</td>
<td>DLC2</td>
<td>DLC1</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown

bit 7
   **Unimplemented**: Read as ‘0’

bit 6
   **TXRTR**: Transmit Remote Frame Transmission Request bit
   1 = Transmitted message will have the TXRTR bit set
   0 = Transmitted message will have the TXRTR bit cleared

bit 5-4
   **Unimplemented**: Read as ‘0’

bit 3-0
   **DLC<3:0>**: Data Length Code bits
   1111 = Reserved
   1110 = Reserved
   1101 = Reserved
   1100 = Reserved
   1011 = Reserved
   1010 = Reserved
   1001 = Reserved
   1000 = Data length = 8 bytes
   0111 = Data length = 7 bytes
   0110 = Data length = 6 bytes
   0101 = Data length = 5 bytes
   0100 = Data length = 4 bytes
   0011 = Data length = 3 bytes
   0010 = Data length = 2 bytes
   0001 = Data length = 1 bytes
   0000 = Data length = 0 bytes

 REGISTER 34-12: TXERRCNT: TRANSMIT ERROR COUNT REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEC7</td>
<td>TEC6</td>
<td>TEC5</td>
<td>TEC4</td>
<td>TEC3</td>
<td>TEC2</td>
<td>TEC1</td>
<td>TEC0</td>
<td></td>
</tr>
</tbody>
</table>

bit 7
	**TEC<7:0>**: Transmit Error Counter bits

This register contains a value which is derived from the rate at which errors occur. When the error count overflows, the bus-off state occurs. When the bus has 128 occurrences of 11 consecutive recessive bits, the counter value is cleared.
EXAMPLE 34-3: TRANSMITTING A CAN MESSAGE USING BANKED METHOD

; Need to transmit Standard Identifier message 123h using TXB0 buffer.
; To successfully transmit, CAN module must be either in Normal or Loopback mode.
; TXB0 buffer is not in access bank. And since we want banked method, we need to make sure
; that correct bank is selected.
BANKSEL TXB0CON ; One BANKSEL in beginning will make sure that we are
; in correct bank for rest of the buffer access.

; Now load transmit data into TXB0 buffer.
MOVLW MY_DATA_BYTE1 ; Load first data byte into buffer
MOVWF TXB0D0 ; Compiler will automatically set “BANKED” bit
; Load rest of data bytes - up to 8 bytes into TXB0 buffer.
...
; Load message identifier
MOVLW 60H ; Load SID2:SID0, EXIDE = 0
MOVWF TXB0SIDL
MOVLW 24H ; Load SID10:SID3
MOVWF TXB0SIDH
; No need to load TXB0EIDL:TXB0EIDH, as we are transmitting Standard Identifier Message only.

; Now that all data bytes are loaded, mark it for transmission.
MOVLW B’00001000’ ; Normal priority; Request transmission
MOVWF TXB0CON

; If required, wait for message to get transmitted
BTFSC TXB0CON, TXREQ ; Is it transmitted?
BRA $-2 ; No. Continue to wait...

; Message is transmitted.
EXAMPLE 34-4: TRANSMITTING A CAN MESSAGE USING WIN BITS

; Need to transmit Standard Identifier message 123h using TXB0 buffer.
; To successfully transmit, CAN module must be either in Normal or Loopback mode.
; TXB0 buffer is not in access bank. Use WIN bits to map it to RXB0 area.
MOVF CANCON, W ; WIN bits are in lower 4 bits only. Read CANCON register to preserve all other bits. If operation mode is already known, there is no need to preserve other bits.
ANDLW B’11110000’ ; Clear WIN bits.
IORLW B’00001000’ ; Select Transmit Buffer 0
MOVWF CANCON ; Apply the changes.
; Now TXB0 is mapped in place of RXB0. All future access to RXB0 registers will actually yield TXB0 register values.

; Load transmit data into TXB0 buffer.
MOVLW MY_DATA_BYTE1 ; Load first data byte into buffer
MOVWF RXB0D0 ; Access TXB0D0 via RXB0D0 address.
; Load rest of the data bytes - up to 8 bytes into “TXB0” buffer using RXB0 registers.
...
; Load message identifier
MOVLW 60H ; Load SID2:SID0, EXIDE = 0
MOVWF RXB0SIDL
MOVLW 24H ; Load SID10:SID3
MOVWF RXB0SIDH
; No need to load RXB0EIDL:RXB0EIDH, as we are transmitting Standard Identifier Message only.

; Now that all data bytes are loaded, mark it for transmission.
MOVLW B’00000100’ ; Normal priority; Request transmission
MOVWF RXB0CON

; If required, wait for message to get transmitted
BTFSC RXB0CON, TXREQ ; Is it transmitted?
BRA $-2 ; No. Continue to wait...

; Message is transmitted.
; If required, reset the WIN bits to default state.
34.15.3  DEDICATED CAN RECEIVE BUFFER REGISTERS

This section shows the dedicated CAN Receive Buffer registers with their associated control registers.

REGISTER 34-13: RXB0CON: RECEIVE BUFFER 0 CONTROL REGISTER

<table>
<thead>
<tr>
<th>Mode 0</th>
<th>R/C-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>R-0</th>
<th>R/W-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RXFUL (1)</td>
<td>RXM1</td>
<td>RXM0</td>
<td></td>
<td>RXRTRRO</td>
<td>RXB0DBEN</td>
<td>JTOFF (2)</td>
<td>FILHIT0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Mode 1,2</th>
<th>R/C-0</th>
<th>R/W-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RXFUL (1)</td>
<td>RXM1</td>
<td>RTRRO</td>
<td>FILHITF4</td>
<td>FILHIT3</td>
<td>FILHIT2</td>
<td>FILHIT1</td>
<td>FILHIT0</td>
</tr>
</tbody>
</table>

Legend:
- **C** = Clearable bit
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

bit 7  **RXFUL**: Receive Full Status bit (1)
- 1 = Receive buffer contains a received message
- 0 = Receive buffer is open to receive a new message

bit 6,6-5  **Mode 0**: RXM<1:0>: Receive Buffer Mode bit 1 (combines with RXM0 to form RXM<1:0> bits, see bit 5)
- 11 = Receive all messages (including those with errors); filter criteria is ignored
- 10 = Receive only valid messages with extended identifier; EXIDEN in RXFnSIDL must be ‘1’
- 01 = Receive only valid messages with standard identifier; EXIDEN in RXFnSIDL must be ‘0’
- 00 = Receive all valid messages as per the EXIDEN bit in the RXFnSIDL register

**Mode 1, 2**: RXM1: Receive Buffer Mode bit 1
- 1 = Receive all messages (including those with errors); acceptance filters are ignored
- 0 = Receive all valid messages as per acceptance filters

bit 5  **Mode 0**: RXM0: Receive Buffer Mode bit 0 (combines with RXM1 to form RXM<1:0>bits, see bit 6)

**Mode 1, 2**: RTRRO: Remote Transmission Request bit for Received Message (read-only)
- 1 = A remote transmission request is received
- 0 = A remote transmission request is not received

bit 4  **Mode 0**: Unimplemented: Read as ‘0’

**Mode 1, 2**: FILHIT<4:0>: Filter Hit bit 4
This bit combines with other bits to form filter acceptance bits<4:0>.

bit 3  **Mode 0**: RXRTRRO: Remote Transmission Request bit for Received Message (read-only)
- 1 = A remote transmission request is received
- 0 = A remote transmission request is not received

**Mode 1, 2**: FILHIT<4:0>: Filter Hit bit 3
This bit combines with other bits to form filter acceptance bits<4:0>.

**Note 1**: This bit is set by the CAN module upon receiving a message and must be cleared by software after the buffer is read. As long as RXFUL is set, no new message will be loaded and the buffer will be considered full. After clearing the RXFUL flag, the PIR5 bit, RXB0IF, can be cleared. If RXB0IF is cleared, but RXFUL is not cleared, then RXB0IF is set again.

**Note 2**: This bit allows the same filter jump table for both RXB0CON and RXB1CON.
REGISTER 34-13: RXB0CON: RECEIVE BUFFER 0 CONTROL REGISTER (CONTINUED)

bit 2  
- **Mode 0:**
  - **RB0DBEN:** Receive Buffer 0 Double-Buffer Enable bit
    - 1 = Receive Buffer 0 overflow will write to Receive Buffer 1
    - 0 = No Receive Buffer 0 overflow to Receive Buffer 1
  
- **Mode 1, 2:**
  - **FILHIT<4:0>:** Filter Hit bit 2
    This bit combines with other bits to form filter acceptance bits<4:0>.

bit 1  
- **Mode 0:**
  - **JTOFF:** Jump Table Offset bit (read-only copy of RXB0DBEN)[2]
    - 1 = Allows jump table offset between 6 and 7
    - 0 = Allows jump table offset between 1 and 0
  
- **Mode 1, 2:**
  - **FILHIT<4:0>:** Filter Hit bit 1
    This bit combines with other bits to form filter acceptance bits<4:0>.

bit 0  
- **Mode 0:**
  - **FILHIT0:** Filter Hit bit 0
    This bit indicates which acceptance filter enabled the message reception into Receive Buffer 0.
    - 1 = Acceptance Filter 1 (RXF1)
    - 0 = Acceptance Filter 0 (RXF0)
  
- **Mode 1, 2:**
  - **FILHIT<4:0>:** Filter Hit bit 0
    This bit, in combination with FILHIT<4:1>, indicates which acceptance filter enabled the message reception into this receive buffer.
    - 01111 = Acceptance Filter 15 (RXF15)
    - 01110 = Acceptance Filter 14 (RXF14)
    - ...
    - 00000 = Acceptance Filter 0 (RXF0)

Note 1:  
This bit is set by the CAN module upon receiving a message and must be cleared by software after the buffer is read. As long as RXFUL is set, no new message will be loaded and the buffer will be considered full. After clearing the RXFUL flag, the PIR5 bit, RXB0IF, can be cleared. If RXB0IF is cleared, but RXFUL is not cleared, then RXB0IF is set again.

2:  
This bit allows the same filter jump table for both RXB0CON and RXB1CON.
**REGISTER 34-14: RXB1CON: RECEIVE BUFFER 1 CONTROL REGISTER**

<table>
<thead>
<tr>
<th>Mode 0</th>
<th>R/C-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>R-0</th>
<th>R/W-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RXFUL (1)</td>
<td>RXM1</td>
<td>RXM0</td>
<td>—</td>
<td>RXRTRRO</td>
<td>FILHIT2</td>
<td>FILHIT1</td>
<td>FILHIT0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Mode 1, 2</th>
<th>R/C-0</th>
<th>R/W-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RXFUL (1)</td>
<td>RXM1</td>
<td>RTRRO</td>
<td>FILHIT4</td>
<td>FILHIT3</td>
<td>FILHIT2</td>
<td>FILHIT1</td>
<td>FILHIT0</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **C** = Clearable bit
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **x** = Bit is unknown

**bit 7**
- **RXFUL**: Receive Full Status bit
  - 1 = Receive buffer contains a received message
  - 0 = Receive buffer is open to receive a new message

**bit 6-5, 6**
- Mode 0:
  - **RXM<1:0>**: Receive Buffer Mode bit 1 (combines with RXM0 to form RXM<1:0> bits, see bit 5)
    - 11 = Receive all messages (including those with errors); filter criteria is ignored
    - 10 = Receive only valid messages with extended identifier; EXIDEN in RXFnSIDL must be ‘1’
    - 01 = Receive only valid messages with standard identifier, EXIDEN in RXFnSIDL must be ‘0’
    - 00 = Receive all valid messages as per EXIDEN bit in RXFnSIDL register
  - Mode 1, 2:
    - **RXM1**: Receive Buffer Mode bit
      - 1 = Receive all messages (including those with errors); acceptance filters are ignored
      - 0 = Receive all valid messages as per acceptance filters

**bit 5**
- Mode 0:
  - **RXM<1:0>**: Receive Buffer Mode bit 0 (combines with RXM1 to form RXM<1:0> bits, see bit 6)
  - Mode 1, 2:
    - **RTRRO**: Remote Transmission Request bit for Received Message (read-only)
      - 1 = A remote transmission request is received
      - 0 = A remote transmission request is not received

**bit 4**
- Mode 0:
  - **FILHIT24**: Filter Hit bit 4
  - Mode 1, 2:
    - **FILHIT<4:0>**: Filter Hit bit 4
      - This bit combines with other bits to form the filter acceptance bits<4:0>.

**bit 3**
- Mode 0:
  - **RXRTRRO**: Remote Transmission Request bit for Received Message (read-only)
    - 1 = A remote transmission request is received
    - 0 = A remote transmission request is not received
  - Mode 1, 2:
    - **FILHIT<4:0>**: Filter Hit bit 3
      - This bit combines with other bits to form the filter acceptance bits<4:0>.

**Note 1**: This bit is set by the CAN module upon receiving a message and must be cleared by software after the buffer is read. As long as RXFUL is set, no new message will be loaded and the buffer will be considered full.
REGISTER 34-14: RXB1CON: RECEIVE BUFFER 1 CONTROL REGISTER (CONTINUED)

bit 2-0  Mode 0:
FILHIT<2:0> : Filter Hit bits
These bits indicate which acceptance filter enabled the last message reception into Receive Buffer 1.
111 = Reserved
110 = Reserved
101 = Acceptance Filter 5 (RXF5)
100 = Acceptance Filter 4 (RXF4)
011 = Acceptance Filter 3 (RXF3)
010 = Acceptance Filter 2 (RXF2)
001 = Acceptance Filter 1 (RXF1), only possible when RXB0DBEN bit is set
000 = Acceptance Filter 0 (RXF0), only possible when RXB0DBEN bit is set

Mode 1, 2:
FILHIT<4:0> : Filter Hit bits<2:0>
These bits, in combination with FILHIT<4:3>, indicate which acceptance filter enabled the message reception into this receive buffer.
01111 = Acceptance Filter 15 (RXF15)
01110 = Acceptance Filter 14 (RXF14)
...
00000 = Acceptance Filter 0 (RXF0)

Note 1: This bit is set by the CAN module upon receiving a message and must be cleared by software after the buffer is read. As long as RXFUL is set, no new message will be loaded and the buffer will be considered full.

REGISTER 34-15: RXBnSIDH: RECEIVE BUFFER ‘n’ STANDARD IDENTIFIER REGISTERS, HIGH BYTE [0 ≤ n ≤ 1]

<table>
<thead>
<tr>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>SID10</td>
<td>SID9</td>
<td>SID8</td>
<td>SID7</td>
<td>SID6</td>
<td>SID5</td>
<td>SID4</td>
<td>SID3</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit   W = Writable bit   U = Unimplemented bit, read as ‘0’
-n = Value at POR   ‘1’ = Bit is set   ‘0’ = Bit is cleared   x = Bit is unknown

bit 7-0  SID<10:3>: Standard Identifier bits (if EXID (RXBnSIDL<3>) = 0)
Extended Identifier bits, EID<28:21> (if EXID = 1).
REGISTER 34-16: RXBnSIDL: RECEIVE BUFFER ‘n’ STANDARD IDENTIFIER REGISTERS, LOW BYTE [0 ≤ n ≤ 1]

<table>
<thead>
<tr>
<th></th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>U-0</th>
<th>R-x</th>
<th>R-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>SID2</td>
<td>SID1</td>
<td>SID0</td>
<td>SRR</td>
<td>EXID</td>
<td>—</td>
<td>EID17</td>
<td>EID16</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

- n = Value at POR

| bit | SID<2:0> | Extended Identifier bits, EID<20:18> (if EXID = 1)
|-----|----------|------------------------------------------------------------------
| 7-5 | Standard Identifier bits (if EXID = 0)                           

- bit 7-5 SID<2:0>: Standard Identifier bits (if EXID = 0)
- Extended Identifier bits, EID<20:18> (if EXID = 1).

- bit 4:SRR: Substitute Remote Request bit

- bit 3:EXID: Extended Identifier bit
- 1 = Received message is an extended data frame, SID<10:0> are EID<28:18>
- 0 = Received message is a standard data frame

- bit 2:Unimplemented: Read as ‘0’

- bit 1-0:EID<17:16>: Extended Identifier bits

REGISTER 34-17: RXBnEIDH: RECEIVE BUFFER ‘n’ EXTENDED IDENTIFIER REGISTERS, HIGH BYTE [0 ≤ n ≤ 1]

<table>
<thead>
<tr>
<th></th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>EID15</td>
<td>EID14</td>
<td>EID13</td>
<td>EID12</td>
<td>EID11</td>
<td>EID10</td>
<td>EID9</td>
<td>EID8</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

- n = Value at POR

<table>
<thead>
<tr>
<th>bit</th>
<th>EID&lt;15:8&gt;: Extended Identifier bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td></td>
</tr>
</tbody>
</table>

REGISTER 34-18: RXBnEIDL: RECEIVE BUFFER ‘n’ EXTENDED IDENTIFIER REGISTERS, LOW BYTE [0 ≤ n ≤ 1]

<table>
<thead>
<tr>
<th></th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>EID7</td>
<td>EID6</td>
<td>EID5</td>
<td>EID4</td>
<td>EID3</td>
<td>EID2</td>
<td>EID1</td>
<td>EID0</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

- n = Value at POR

<table>
<thead>
<tr>
<th>bit</th>
<th>EID&lt;7:0&gt;: Extended Identifier bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td></td>
</tr>
</tbody>
</table>
REGISTER 34-19: RXBnDLC: RECEIVE BUFFER ‘n’ DATA LENGTH CODE REGISTERS [0 ≤ n ≤ 1]

<table>
<thead>
<tr>
<th>U-0</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>RXRTR</td>
<td>RB1</td>
<td>RB0</td>
<td>DLC3</td>
<td>DLC2</td>
<td>DLC1</td>
<td>DLC0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’  
-n = Value at POR  
‘1’ = Bit is set  
‘0’ = Bit is cleared  
x = Bit is unknown

bit 7  
**Unimplemented**: Read as ‘0’

bit 6  
**RXRTR**: Receiver Remote Transmission Request bit  
1 = Remote transfer request  
0 = No remote transfer request

bit 5  
**RB1**: Reserved bit 1  
Reserved by CAN Spec and read as ‘0’.

bit 4  
**RB0**: Reserved bit 0  
Reserved by CAN Spec and read as ‘0’.

bit 3-0  
**DLC<3:0>:** Data Length Code bits  
1111 = Invalid  
1110 = Invalid  
1101 = Invalid  
1100 = Invalid  
1011 = Invalid  
1010 = Invalid  
1001 = Invalid  
1000 = Data length = 8 bytes  
0111 = Data length = 7 bytes  
0110 = Data length = 6 bytes  
0101 = Data length = 5 bytes  
0100 = Data length = 4 bytes  
0011 = Data length = 3 bytes  
0010 = Data length = 2 bytes  
0001 = Data length = 1 byte  
0000 = Data length = 0 bytes

REGISTER 34-20: RXBnDm: RECEIVE BUFFER ‘n’ DATA FIELD BYTE ‘m’ REGISTERS  
[0 ≤ n ≤ 1, 0 ≤ m ≤ 7]

<table>
<thead>
<tr>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXBnDm7</td>
<td>RXBnDm6</td>
<td>RXBnDm5</td>
<td>RXBnDm4</td>
<td>RXBnDm3</td>
<td>RXBnDm2</td>
<td>RXBnDm1</td>
<td>RXBnDm0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’  
-n = Value at POR  
‘1’ = Bit is set  
‘0’ = Bit is cleared  
x = Bit is unknown

bit 7-0  
**RXBnDm<7:0>:** Receive Buffer n Data Field Byte m bits (where 0 ≤ n < 1 and 0 < m ≤ 7)  
Each receive buffer has an array of registers. For example, Receive Buffer 0 has eight registers: RXB0D0 to RXB0D7.
EXAMPLE 34-5: READING A CAN MESSAGE

; Need to read a pending message from RXB0 buffer.
; To receive any message, filter, mask and RXM1:RXM0 bits in RXB0CON registers must be
; programmed correctly.
;
; Make sure that there is a message pending in RXB0.
BTFSS RXB0CON, RXFUL ; Does RXB0 contain a message?
BRA NoMessage ; No. Handle this situation...
;
; We have verified that a message is pending in RXB0 buffer.
; If this buffer can receive both Standard or Extended Identifier messages,
; identify type of message received.
BTFSS RXB0IDL, EXID ; Is this Extended Identifier?
BRA StandardMessage ; No. This is Standard Identifier message.
; Yes. This is Extended Identifier message.
;
; Read all 29-bits of Extended Identifier message.
...
;
; Now read all data bytes
MOVFF RXB0DO, MY_DATA_BYTE1
...
;
; Once entire message is read, mark the RXB0 that it is read and no longer FULL.
BCF RXB0CON, RXFUL ; This will allow CAN Module to load new messages
; into this buffer.
...
34.15.3.1 Programmable TX/RX and Auto-RTR Buffers

The ECAN module contains six message buffers that can be programmed as transmit or receive buffers. Any of these buffers can also be programmed to automatically handle RTR messages.

**Note:** These registers are not used in Mode 0.

**REGISTER 34-22: BnCON: TX/RX BUFFER 'n' CONTROL REGISTERS IN RECEIVE MODE**

\[0 \leq n \leq 5, \text{TXnEN} (\text{BSEL0}<n>) = 0\]  

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
<th>R-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXFUL</td>
<td>RXM1</td>
<td>RXRTRRO</td>
<td>FILHIT4</td>
<td>FILHIT3</td>
<td>FILHIT2</td>
<td>FILHIT1</td>
<td>FILHIT0</td>
</tr>
</tbody>
</table>

**Legend:**

- \(R\) = Readable bit
- \(W\) = Writable bit
- \(U\) = Unimplemented bit, read as ‘0’
- \(-n\) = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- \(x\) = Bit is unknown

bit 7 **RXFUL:** Receive Full Status bit\(^{(2)}\)

- 1 = Receive buffer contains a received message
- 0 = Receive buffer is open to receive a new message

bit 6 **RXM1:** Receive Buffer Mode bit

- 1 = Receive all messages including partial and invalid (acceptance filters are ignored)
- 0 = Receive all valid messages as per acceptance filters

bit 5 **RXRTRRO:** Read-Only Remote Transmission Request for Received Message bit

- 1 = Received message is a remote transmission request
- 0 = Received message is not a remote transmission request

bit 4-0 **FILHIT<4:0>:** Filter Hit bits

These bits indicate which acceptance filter enabled the last message reception into this buffer.

- \(01111\) = Acceptance Filter 15 (RXF15)
- \(01110\) = Acceptance Filter 14 (RXF14)
- \(\ldots\)
- \(00001\) = Acceptance Filter 1 (RXF1)
- \(00000\) = Acceptance Filter 0 (RXF0)

**Note 1:** These registers are available in Mode 1 and 2 only.

**Note 2:** This bit is set by the CAN module upon receiving a message and must be cleared by software after the buffer is read. As long as RXFUL is set, no new message will be loaded and the buffer will be considered full.
**REGISTER 34-23: BnCON: TX/RX BUFFER ‘n’ CONTROL REGISTERS IN TRANSMIT MODE**

\[0 \leq n \leq 5, \text{TXnEN (BSEL0}<n>) = 1^{(1)}\]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value at POR</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>TXBIF: Transmit Buffer Interrupt Flag bit(^{(3)})</td>
<td>‘1’ =</td>
<td>A message was successfully transmitted</td>
</tr>
<tr>
<td></td>
<td></td>
<td>‘0’ =</td>
<td>No message was transmitted</td>
</tr>
<tr>
<td>6</td>
<td>TXABT: Transmission Aborted Status bit(^{(3)})</td>
<td>‘1’ =</td>
<td>Message was aborted</td>
</tr>
<tr>
<td></td>
<td></td>
<td>‘0’ =</td>
<td>Message was not aborted</td>
</tr>
<tr>
<td>5</td>
<td>TXLARB: Transmission Lost Arbitration Status bit(^{(3)})</td>
<td>‘1’ =</td>
<td>Message lost arbitration while being sent</td>
</tr>
<tr>
<td></td>
<td></td>
<td>‘0’ =</td>
<td>Message did not lose arbitration while being sent</td>
</tr>
<tr>
<td>4</td>
<td>TXERR: Transmission Error Detected Status bit(^{(3)})</td>
<td>‘1’ =</td>
<td>A bus error occurred while the message was being sent</td>
</tr>
<tr>
<td></td>
<td></td>
<td>‘0’ =</td>
<td>A bus error did not occur while the message was being sent</td>
</tr>
<tr>
<td>3</td>
<td>TXREQ: Transmit Request Status bit(^{(2,4)})</td>
<td>‘1’ =</td>
<td>Requests sending a message; clears the TXABT, TXLARB and TXERR bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>‘0’ =</td>
<td>Automatically cleared when the message is successfully sent</td>
</tr>
<tr>
<td>2</td>
<td>RTREN: Automatic Remote Transmission Request Enable bit</td>
<td>‘1’ =</td>
<td>When a remote transmission request is received, TXREQ will be</td>
</tr>
<tr>
<td></td>
<td></td>
<td>‘0’ =</td>
<td>automatically set when the message is successfully sent</td>
</tr>
<tr>
<td>1-0</td>
<td>TXPRI&lt;1:0&gt;: Transmit Priority bits(^{(5)})</td>
<td>‘11’ =</td>
<td>Priority Level 3 (highest priority)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>‘10’ =</td>
<td>Priority Level 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>‘01’ =</td>
<td>Priority Level 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>‘00’ =</td>
<td>Priority Level 0 (lowest priority)</td>
</tr>
</tbody>
</table>

**Note 1:** These registers are available in Mode 1 and 2 only.

**2:** Clearing this bit in software while the bit is set will request a message abort.

**3:** This bit is automatically cleared when TXREQ is set.

**4:** While TXREQ is set or a transmission is in progress, Transmit Buffer registers remain read-only.

**5:** These bits set the order in which the Transmit Buffer register will be transferred. They do not alter the CAN message identifier.
**REGISTER 34-24: BnSIDH: TX/RX BUFFER 'n' STANDARD IDENTIFIER REGISTERS, HIGH BYTE IN RECEIVE MODE [0 ≤ n ≤ 5, TXnEN (BSEL0<n>) = 0]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>SID10</th>
<th>SID9</th>
<th>SID8</th>
<th>SID7</th>
<th>SID6</th>
<th>SID5</th>
<th>SID4</th>
<th>SID3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R-x</td>
<td>R-x</td>
<td>R-x</td>
<td>R-x</td>
<td>R-x</td>
<td>R-x</td>
<td>R-x</td>
<td>R-x</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**Note 1:** These registers are available in Mode 1 and 2 only.

**REGISTER 34-25: BnSIDH: TX/RX BUFFER 'n' STANDARD IDENTIFIER REGISTERS, HIGH BYTE IN TRANSMIT MODE [0 ≤ n ≤ 5, TXnEN (BSEL0<n>) = 1]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>SID10</th>
<th>SID9</th>
<th>SID8</th>
<th>SID7</th>
<th>SID6</th>
<th>SID5</th>
<th>SID4</th>
<th>SID3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R/W-x</td>
<td>R/W-x</td>
<td>R/W-x</td>
<td>R/W-x</td>
<td>R/W-x</td>
<td>R/W-x</td>
<td>R/W-x</td>
<td>R/W-x</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**Note 1:** These registers are available in Mode 1 and 2 only.
REGISTER 34-26: BnSIDL: TX/RX BUFFER ‘n’ STANDARD IDENTIFIER REGISTERS,
LOW BYTE IN RECEIVE MODE \[0 \leq n \leq 5, \text{TXnEN (BSEL0}<n\text{>) = 0}\]¹

| bit 7-5 | SID<2:0>: Standard Identifier bits (if EXID = 0)  
Extended Identifier bits, EID<20:18> (if EXID = 1). |
| bit 4  | SRR: Substitute Remote Transmission Request bit  
This bit is always ‘1’ when EXID = 1 or equal to the value of RXRTRRO (BnCON<5>) when EXID = 0. |
| bit 3  | EXIDE: Extended Identifier Enable bit  
1 = Received message is an extended identifier frame (SID<10:0> are EID<28:18>)  
0 = Received message is a standard identifier frame |
| bit 2  | Unimplemented: Read as ‘0’ |
| bit 1-0 | EID<17:16>: Extended Identifier bits |

Note 1: These registers are available in Mode 1 and 2 only.

REGISTER 34-27: BnSIDL: TX/RX BUFFER ‘n’ STANDARD IDENTIFIER REGISTERS,
LOW BYTE IN TRANSMIT MODE \[0 \leq n \leq 5, \text{TXnEN (BSEL0}<n\text{>) = 1}\]¹

| bit 7-5 | SID<2:0>: Standard Identifier bits (if EXID = 0)  
Extended Identifier bits, EID<20:18> (if EXID = 1). |
| bit 4  | Unimplemented: Read as ‘0’ |
| bit 3  | EXIDE: Extended Identifier Enable bit  
1 = Message will transmit extended ID, SID<10:0> bits become EID<28:18>  
0 = Received will transmit standard ID, EID<17:0> are ignored |
| bit 2  | Unimplemented: Read as ‘0’ |
| bit 1-0 | EID<17:16>: Extended Identifier bits |

Note 1: These registers are available in Mode 1 and 2 only.
REGISTER 34-28: BnEIDH: TX/RX BUFFER 'n' EXTENDED IDENTIFIER REGISTERS, HIGH BYTE IN RECEIVE MODE [0 ≤ n ≤ 5, TXnEN (BSEL0<n>) = 0](1)

<table>
<thead>
<tr>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>EID15</td>
<td>EID14</td>
<td>EID13</td>
<td>EID12</td>
<td>EID11</td>
<td>EID10</td>
<td>EID9</td>
<td>EID8</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

bit 7-0  EID<15:8>: Extended Identifier bits

Note 1: These registers are available in Mode 1 and 2 only.

REGISTER 34-29: BnEIDH: TX/RX BUFFER 'n' EXTENDED IDENTIFIER REGISTERS, HIGH BYTE IN TRANSMIT MODE [0 ≤ n ≤ 5, TXnEN (BSEL0<n>) = 1](1)

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>EID15</td>
<td>EID14</td>
<td>EID13</td>
<td>EID12</td>
<td>EID11</td>
<td>EID10</td>
<td>EID9</td>
<td>EID8</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

bit 7-0  EID<15:8>: Extended Identifier bits

Note 1: These registers are available in Mode 1 and 2 only.

REGISTER 34-30: BnEIDL: TX/RX BUFFER 'n' EXTENDED IDENTIFIER REGISTERS, LOW BYTE IN RECEIVE MODE [0 ≤ n ≤ 5, TXnEN (BSEL<n>) = 0](1)

<table>
<thead>
<tr>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>EID7</td>
<td>EID6</td>
<td>EID5</td>
<td>EID4</td>
<td>EID3</td>
<td>EID2</td>
<td>EID1</td>
<td>EID0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

bit 7-0  EID<7:0>: Extended Identifier bits

Note 1: These registers are available in Mode 1 and 2 only.
REGISTER 34-31: BnEIDL: TX/RX BUFFER ‘n’ EXTENDED IDENTIFIER REGISTERS, LOW BYTE IN RECEIVE MODE \(0 \leq n \leq 5\), TXnEN (BSEL<\(n\>) = 1\)

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>EID7</td>
<td>EID6</td>
<td>EID5</td>
<td>FEID4</td>
<td>EID3</td>
<td>EID2</td>
<td>EID1</td>
<td>EID0</td>
</tr>
</tbody>
</table>

Legend:
- \(R\) = Readable bit
- \(W\) = Writable bit
- \(U\) = Unimplemented bit, read as ‘0’
- \(-n\) = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- \(x\) = Bit is unknown

Note 1: These registers are available in Mode 1 and 2 only.

REGISTER 34-32: BnDm: TX/RX BUFFER ‘n’ DATA FIELD BYTE ‘m’ REGISTERS IN RECEIVE MODE \(0 \leq n \leq 5\), 0 \(\leq m \leq 7\), TXnEN (BSEL<\(n\>) = 0\)

<table>
<thead>
<tr>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>BnDm7</td>
<td>BnDm6</td>
<td>BnDm5</td>
<td>BnDm4</td>
<td>BnDm3</td>
<td>BnDm2</td>
<td>BnDm1</td>
<td>BnDm0</td>
</tr>
</tbody>
</table>

Legend:
- \(R\) = Readable bit
- \(W\) = Writable bit
- \(U\) = Unimplemented bit, read as ‘0’
- \(-n\) = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- \(x\) = Bit is unknown

Note 1: These registers are available in Mode 1 and 2 only.

REGISTER 34-33: BnDm: TX/RX BUFFER ‘n’ DATA FIELD BYTE ‘m’ REGISTERS IN TRANSMIT MODE \(0 \leq n \leq 5\), 0 \(\leq m \leq 7\), TXnEN (BSEL<\(n\>) = 1\)

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>BnDm7</td>
<td>BnDm6</td>
<td>BnDm5</td>
<td>BnDm4</td>
<td>BnDm3</td>
<td>BnDm2</td>
<td>BnDm1</td>
<td>BnDm0</td>
</tr>
</tbody>
</table>

Legend:
- \(R\) = Readable bit
- \(W\) = Writable bit
- \(U\) = Unimplemented bit, read as ‘0’
- \(-n\) = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- \(x\) = Bit is unknown

Note 1: These registers are available in Mode 1 and 2 only.

\(n\) = Bit 7-0
\(EID<7:0>:\) Extended Identifier bits

\(m\) = Bit 7-0
\(BnDm<7:0>:\) Receive Buffer \(n\) Data Field Byte \(m\) bits (where \(0 \leq n < 3\) and \(0 < m < 8\))

\(m\) = Bit 7-0
\(BnDm<7:0>:\) Transmit Buffer \(n\) Data Field Byte \(m\) bits (where \(0 \leq n < 3\) and \(0 < m < 8\))
## REGISTER 34-34: BnDLC: TX/RX BUFFER ‘n’ DATA LENGTH CODE REGISTERS IN RECEIVE MODE

\[0 \leq n \leq 5, \text{TXnEN (BSEL<n>) = 0}^{(1)}\]

<table>
<thead>
<tr>
<th>U-0</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>RXRTR</td>
<td>RB1</td>
<td>RB0</td>
<td>DLC3</td>
<td>DLC2</td>
<td>DLC1</td>
<td>DLC0</td>
</tr>
</tbody>
</table>

### Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- *x* = Bit is unknown

**bit 7**: Unimplemented: Read as ‘0’

**bit 6**: RXRTR: Receiver Remote Transmission Request bit

- 1 = This is a remote transmission request
- 0 = This is not a remote transmission request

**bit 5**: RB1: Reserved bit 1

- Reserved by CAN Spec and read as ‘0’.

**bit 4**: RB0: Reserved bit 0

- Reserved by CAN Spec and read as ‘0’.

**bit 3-0**: DLC<3:0>: Data Length Code bits

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>Reserved</td>
</tr>
<tr>
<td>1110</td>
<td>Reserved</td>
</tr>
<tr>
<td>1101</td>
<td>Reserved</td>
</tr>
<tr>
<td>1100</td>
<td>Reserved</td>
</tr>
<tr>
<td>1011</td>
<td>Reserved</td>
</tr>
<tr>
<td>1010</td>
<td>Reserved</td>
</tr>
<tr>
<td>1001</td>
<td>Reserved</td>
</tr>
<tr>
<td>1000</td>
<td>Data length = 8 bytes</td>
</tr>
<tr>
<td>0111</td>
<td>Data length = 7 bytes</td>
</tr>
<tr>
<td>0110</td>
<td>Data length = 6 bytes</td>
</tr>
<tr>
<td>0101</td>
<td>Data length = 5 bytes</td>
</tr>
<tr>
<td>0100</td>
<td>Data length = 4 bytes</td>
</tr>
<tr>
<td>0011</td>
<td>Data length = 3 bytes</td>
</tr>
<tr>
<td>0010</td>
<td>Data length = 2 bytes</td>
</tr>
<tr>
<td>0001</td>
<td>Data length = 1 byte</td>
</tr>
<tr>
<td>0000</td>
<td>Data length = 0 bytes</td>
</tr>
</tbody>
</table>

**Note 1**: These registers are available in Mode 1 and 2 only.
REGISTER 34-35: BnDLC: TX/RX BUFFER ‘n’ DATA LENGTH CODE REGISTERS IN TRANSMIT MODE

[0 ≤ n ≤ 5, TXnEN (BSEL<n>) = 1(1)]

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/W-x</th>
<th>U-0</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>TXRTR</td>
<td>—</td>
<td>—</td>
<td>DLC3</td>
<td>DLC2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>DLC1</td>
<td>DLC0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown

bit 7 Unimplemented: Read as ‘0’
bit 6 TXRTR: Transmitter Remote Transmission Request bit
1 = Transmitted message will have the RTR bit set
0 = Transmitted message will have the RTR bit cleared
bit 5-4 Unimplemented: Read as ‘0’
bit 3-0 DLC<3:0>: Data Length Code bits
1111-1001 = Reserved
1000 = Data length = 8 bytes
0111 = Data length = 7 bytes
0110 = Data length = 6 bytes
0101 = Data length = 5 bytes
0100 = Data length = 4 bytes
0011 = Data length = 3 bytes
0010 = Data length = 2 bytes
0001 = Data length = 1 byte
0000 = Data length = 0 bytes

Note 1: These registers are available in Mode 1 and 2 only.

REGISTER 34-36: BSEL0: BUFFER SELECT REGISTER 0(1)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>B5TXEN</td>
<td>B4TXEN</td>
<td>B3TXEN</td>
<td>B2TXEN</td>
<td>B1TXEN</td>
<td>B0TXEN</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown

bit 7-2 B<5:0>TXEN: Buffer 5 to Buffer 0 Transmit Enable bits
1 = Buffer is configured in Transmit mode
0 = Buffer is configured in Receive mode
bit 1-0 Unimplemented: Read as ‘0’

Note 1: These registers are available in Mode 1 and 2 only.
34.15.3.2 Message Acceptance Filters and Masks

This section describes the message acceptance filters and masks for the CAN receive buffers.

**REGISTER 34-37: RXFnSIDH: RECEIVE ACCEPTANCE FILTER 'n' STANDARD IDENTIFIER FILTER REGISTERS, HIGH BYTE \(0 \leq n \leq 15\)**

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>SID10</td>
<td>SID9</td>
<td>SID8</td>
<td>SID7</td>
<td>SID6</td>
<td>SID5</td>
<td>SID4</td>
<td>SID3</td>
</tr>
</tbody>
</table>

Legend:
- \(R\) = Readable bit
- \(W\) = Writable bit
- \(U\) = Unimplemented bit, read as ‘0’
- \(-n\) = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared \(x\) = Bit is unknown

bit 7-0 \(\text{SID}<10:3>\): Standard Identifier Filter bits (if EXIDEN = 0)
Extended Identifier Filter bits, \(\text{EID}<28:21>\) (if EXIDEN = 1).

**Note 1:** Registers, RXF6SIDH:RXF15SIDH, are available in Mode 1 and 2 only.

**REGISTER 34-38: RXFnSIDL: RECEIVE ACCEPTANCE FILTER 'n' STANDARD IDENTIFIER FILTER REGISTERS, LOW BYTE \(0 \leq n \leq 15\)**

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>U-0</th>
<th>R/W-x</th>
<th>U-0</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>SID2</td>
<td>SID1</td>
<td>SID0</td>
<td>—</td>
<td>EXIDEN(^{(4)})</td>
<td>—</td>
<td>EID17</td>
<td>EID16</td>
</tr>
</tbody>
</table>

Legend:
- \(R\) = Readable bit
- \(W\) = Writable bit
- \(U\) = Unimplemented bit, read as ‘0’
- \(-n\) = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared \(x\) = Bit is unknown

bit 7-5 \(\text{SID}<2:0>\): Standard Identifier Filter bits (if EXIDEN = 0)
Extended Identifier Filter bits, \(\text{EID}<20:18>\) (if EXIDEN = 1).

bit 4 Unimplemented: Read as ‘0’

bit 3 \(\text{EXIDEN}\): Extended Identifier Filter Enable bit\(^{(2)}\)
1 = Filter will only accept extended ID messages
0 = Filter will only accept standard ID messages

bit 2 Unimplemented: Read as ‘0’

bit 1-0 \(\text{EID}<17:16>\): Extended Identifier Filter bits

**Note 1:** Registers, RXF6SIDL:RXF15SIDL, are available in Mode 1 and 2 only.

**2:** In Mode 0, this bit must be set/cleared as required, irrespective of corresponding mask register value.
**REGISTER 34-39: RXFnEIDH: RECEIVE ACCEPTANCE FILTER ‘n’ EXTENDED IDENTIFIER REGISTERS, HIGH BYTE [0 ≤ n ≤ 15]**

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>EID15</td>
<td>EID14</td>
<td>EID13</td>
<td>EID12</td>
<td>EID11</td>
<td>EID10</td>
<td>EID9</td>
<td>EID8</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**bit 7-0**  
**EID<15:8>:** Extended Identifier Filter bits

**Note 1:** Registers, RXF6EIDH:RXF15EIDH, are available in Mode 1 and 2 only.

---

**REGISTER 34-40: RXFnEIDL: RECEIVE ACCEPTANCE FILTER ‘n’ EXTENDED IDENTIFIER REGISTERS, LOW BYTE [0 ≤ n ≤ 15]**

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>EID7</td>
<td>EID6</td>
<td>EID5</td>
<td>EID4</td>
<td>EID3</td>
<td>EID2</td>
<td>EID1</td>
<td>EID0</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**bit 7-0**  
**EID<7:0>:** Extended Identifier Filter bits

**Note 1:** Registers, RXF6EIDL:RXF15EIDL, are available in Mode 1 and 2 only.

---

**REGISTER 34-41: RXMnSIDH: RECEIVE ACCEPTANCE MASK ‘n’ STANDARD IDENTIFIER MASK REGISTERS, HIGH BYTE [0 ≤ n ≤ 1]**

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>SID10</td>
<td>SID9</td>
<td>SID8</td>
<td>SID7</td>
<td>SID6</td>
<td>SID5</td>
<td>SID4</td>
<td>SID3</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**bit 7-0**  
**SID<10:3>:** Standard Identifier Mask bits or Extended Identifier Mask bits (EID<28:21>)
REGISTER 34-42: RXMnSIDL: RECEIVE ACCEPTANCE MASK ‘n’ STANDARD IDENTIFIER MASK REGISTERS, LOW BYTE [0 ≤ n ≤ 1]

<table>
<thead>
<tr>
<th>Bit</th>
<th>SID2</th>
<th>SID1</th>
<th>SID0</th>
<th>EXIDEN(1)</th>
<th>—</th>
<th>EID17</th>
<th>EID16</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown

bit 7-5    SID<2:0>: Standard Identifier Mask bits or Extended Identifier Mask bits (EID<20:18>)
bit 4    Unimplemented: Read as ‘0’
bit 3    Mode 0:
          Unimplemented: Read as ‘0’
          Mode 1, 2:
          EXIDEN: Extended Identifier Filter Enable Mask bit(1)
          1 = Messages selected by the EXIDEN bit in RXFnSIDL will be accepted
          0 = Both standard and extended identifier messages will be accepted
bit 2    Unimplemented: Read as ‘0’
bit 1-0    EID<17:16>: Extended Identifier Mask bits

Note 1: This bit is available in Mode 1 and 2 only.

REGISTER 34-43: RXMnEIDH: RECEIVE ACCEPTANCE MASK ‘n’ EXTENDED IDENTIFIER MASK REGISTERS, HIGH BYTE [0 ≤ n ≤ 1]

<table>
<thead>
<tr>
<th>Bit</th>
<th>EID15</th>
<th>EID14</th>
<th>EID13</th>
<th>EID12</th>
<th>EID11</th>
<th>EID10</th>
<th>EID9</th>
<th>EID8</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown

bit 7-0    EID<15:8>: Extended Identifier Mask bits
## REGISTER 34-44: RXMnEIDL: RECEIVE ACCEPTANCE MASK ‘n’ EXTENDED IDENTIFIER MASK REGISTERS, LOW BYTE [0 ≤ n ≤ 1]

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>EID7</td>
<td>EID6</td>
<td>EID5</td>
<td>EID4</td>
<td>EID3</td>
<td>EID2</td>
<td>EID1</td>
<td>EID0</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- ‘-n’ = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**bit 7-0**  
**EID<7:0>:** Extended Identifier Mask bits

## REGISTER 34-45: RXFCONn: RECEIVE FILTER CONTROL REGISTER ‘n’ [0 ≤ n ≤ 1]

### RXFCON0

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXF7EN</td>
<td>RXF6EN</td>
<td>RXF5EN</td>
<td>RXF4EN</td>
<td>RXF3EN</td>
<td>RXF2EN</td>
<td>RXF1EN</td>
<td>RXF0EN</td>
</tr>
</tbody>
</table>

### RXFCON1

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXF15EN</td>
<td>RXF14EN</td>
<td>RXF13EN</td>
<td>RXF12EN</td>
<td>RXF11EN</td>
<td>RXF10EN</td>
<td>RXF9EN</td>
<td>RXF8EN</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- ‘-n’ = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**bit 7-0**  
**RXF<7:0>EN:** Receive Filter n Enable bits
- **0** = Filter is disabled
- **1** = Filter is enabled

**Note 1:** This register is available in Mode 1 and 2 only.

**Note:** Register 34-46 through Register 34-51 are writable in Configuration mode only.
REGISTER 34-46: SDFLC: STANDARD DATA BYTES FILTER LENGTH COUNT REGISTER(1)

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>FLC4</td>
<td>FLC3</td>
<td>FLC2</td>
<td>FLC1</td>
<td>FLC0</td>
</tr>
</tbody>
</table>

bit 7                  bit 0

Legend:
R = Readable bit       W = Writable bit       U = Unimplemented bit, read as '0'
-n = Value at POR      ‘1’ = Bit is set      ‘0’ = Bit is cleared
x = Bit is unknown

bit 7-5                  Unimplemented: Read as ‘0’
bit 4-0                  FLC<4:0>: Filter Length Count bits

Mode 0:
Not used; forced to ‘00000’.

Mode 1, 2:
00000 to 10010 = 0  18 bits are available for standard data byte filter. Actual number of bits used depends on the DLC<3:0> bits (RXBnDLC<3:0> or BnDLC<3:0> if configured as RX buffer) of the message being received.

If DLC<3:0> = 0000  No bits will be compared with incoming data bits.
If DLC<3:0> = 0001  Up to 8 data bits of RXFnEID<7:0>, as determined by FLC<2:0>, will be compared with the corresponding number of data bits of the incoming message.
If DLC<3:0> = 0010  Up to 16 data bits of RXFnEID<15:0>, as determined by FLC<3:0>, will be compared with the corresponding number of data bits of the incoming message.
If DLC<3:0> = 0011  Up to 18 data bits of RXFnEID<17:0>, as determined by FLC<4:0>, will be compared with the corresponding number of data bits of the incoming message.

Note 1: This register is available in Mode 1 and 2 only.
### REGISTER 34-47: RXFBCONn: RECEIVE FILTER BUFFER CONTROL REGISTER 'n'(1)

<table>
<thead>
<tr>
<th>RXFBCON0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>F1BP_3</td>
<td>F1BP_2</td>
<td>F1BP_1</td>
<td>F1BP_0</td>
<td>F0BP_3</td>
<td>F0BP_2</td>
<td>F0BP_1</td>
<td>F0BP_0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RXFBCON1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>F3BP_3</td>
<td>F3BP_2</td>
<td>F3BP_1</td>
<td>F3BP_0</td>
<td>F2BP_3</td>
<td>F2BP_2</td>
<td>F2BP_1</td>
<td>F2BP_0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RXFBCON2</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>F5BP_3</td>
<td>F5BP_2</td>
<td>F5BP_1</td>
<td>F5BP_0</td>
<td>F4BP_3</td>
<td>F4BP_2</td>
<td>F4BP_1</td>
<td>F4BP_0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RXFBCON3</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>F7BP_3</td>
<td>F7BP_2</td>
<td>F7BP_1</td>
<td>F7BP_0</td>
<td>F6BP_3</td>
<td>F6BP_2</td>
<td>F6BP_1</td>
<td>F6BP_0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RXFBCON4</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>F9BP_3</td>
<td>F9BP_2</td>
<td>F9BP_1</td>
<td>F9BP_0</td>
<td>F8BP_3</td>
<td>F8BP_2</td>
<td>F8BP_1</td>
<td>F8BP_0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RXFBCON5</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>F11BP_3</td>
<td>F11BP_2</td>
<td>F11BP_1</td>
<td>F10BP_0</td>
<td>F10BP_3</td>
<td>F10BP_2</td>
<td>F10BP_1</td>
<td>F10BP_0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RXFBCON6</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>F13BP_3</td>
<td>F13BP_2</td>
<td>F13BP_1</td>
<td>F12BP_0</td>
<td>F12BP_3</td>
<td>F12BP_2</td>
<td>F12BP_1</td>
<td>F12BP_0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RXFBCON7</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>F15BP_3</td>
<td>F15BP_2</td>
<td>F15BP_1</td>
<td>F14BP_0</td>
<td>F14BP_3</td>
<td>F14BP_2</td>
<td>F14BP_1</td>
<td>F14BP_0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**bit 7-0 F<15:2>BP_<3:0>: Filter n Buffer PointerNibble bits**

- 0000 = Filter n is associated with RXB0
- 0001 = Filter n is associated with RXB1
- 0010 = Filter n is associated with B0
- 0011 = Filter n is associated with B1
- ...
- 0111 = Filter n is associated with B5
- 1111–1000 = Reserved

**Note 1:** This register is available in Mode 1 and 2 only.
REGISTER 34-48: MSEL0: MASK SELECT REGISTER 0(1)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIL3_1</td>
<td>FIL3_0</td>
<td>FIL2_1</td>
<td>FIL2_0</td>
<td>FIL1_1</td>
<td>FIL1_0</td>
<td>FIL0_1</td>
<td>FIL0_0</td>
</tr>
</tbody>
</table>

bit 7-6  **FIL3_<1:0>:** Filter 3 Select bits 1 and 0
11 = No mask
10 = Filter 15
01 = Acceptance Mask 1
00 = Acceptance Mask 0

bit 5-4  **FIL2_<1:0>:** Filter 2 Select bits 1 and 0
11 = No mask
10 = Filter 15
01 = Acceptance Mask 1
00 = Acceptance Mask 0

bit 3-2  **FIL1_<1:0>:** Filter 1 Select bits 1 and 0
11 = No mask
10 = Filter 15
01 = Acceptance Mask 1
00 = Acceptance Mask 0

bit 1-0  **FIL0_<1:0>:** Filter 0 Select bits 1 and 0
11 = No mask
10 = Filter 15
01 = Acceptance Mask 1
00 = Acceptance Mask 0

**Note 1:** This register is available in Mode 1 and 2 only.

---

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown
### REGISTER 34-49: MSEL1: MASK SELECT REGISTER 1(1)

<table>
<thead>
<tr>
<th>Bit 7-6</th>
<th>FIL7_&lt;1:0&gt;</th>
<th>Bit 5-4</th>
<th>FIL6_&lt;1:0&gt;</th>
<th>Bit 3-2</th>
<th>FIL5_&lt;1:0&gt;</th>
<th>Bit 1-0</th>
<th>FIL4_&lt;1:0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0</td>
<td>FIL7_1</td>
<td>R/W-0</td>
<td>FIL6_1</td>
<td>R/W-0</td>
<td>FIL5_1</td>
<td>R/W-0</td>
<td>FIL4_1</td>
</tr>
<tr>
<td>R/W-0</td>
<td>FIL7_0</td>
<td>R/W-0</td>
<td>FIL6_0</td>
<td>R/W-0</td>
<td>FIL5_0</td>
<td>R/W-0</td>
<td>FIL4_0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

- **bit 7-6**
  - FIL7_<1:0>: Filter 7 Select bits 1 and 0
    - 11 = No mask
    - 10 = Filter 15
    - 01 = Acceptance Mask 1
    - 00 = Acceptance Mask 0

- **bit 5-4**
  - FIL6_<1:0>: Filter 6 Select bits 1 and 0
    - 11 = No mask
    - 10 = Filter 15
    - 01 = Acceptance Mask 1
    - 00 = Acceptance Mask 0

- **bit 3-2**
  - FIL5_<1:0>: Filter 5 Select bits 1 and 0
    - 11 = No mask
    - 10 = Filter 15
    - 01 = Acceptance Mask 1
    - 00 = Acceptance Mask 0

- **bit 1-0**
  - FIL4_<1:0>: Filter 4 Select bits 1 and 0
    - 11 = No mask
    - 10 = Filter 15
    - 01 = Acceptance Mask 1
    - 00 = Acceptance Mask 0

**Note 1:** This register is available in Mode 1 and 2 only.
**REGISTER 34-50: MSEL2: MASK SELECT REGISTER 2**(1)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value at POR</th>
<th>Mode 1</th>
<th>Mode 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6</td>
<td>FIL11_1:FIL11_0: Filter 11 Select bits 1 and 0</td>
<td>11 = No mask</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 = Filter 15</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>01 = Acceptance Mask 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>00 = Acceptance Mask 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5-4</td>
<td>FIL10_1:FIL10_0: Filter 10 Select bits 1 and 0</td>
<td>11 = No mask</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 = Filter 15</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>01 = Acceptance Mask 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>00 = Acceptance Mask 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3-2</td>
<td>FIL9_1:FIL9_0: Filter 9 Select bits 1 and 0</td>
<td>11 = No mask</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 = Filter 15</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>01 = Acceptance Mask 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>00 = Acceptance Mask 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1-0</td>
<td>FIL8_1:FIL8_0: Filter 8 Select bits 1 and 0</td>
<td>11 = No mask</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 = Filter 15</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>01 = Acceptance Mask 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>00 = Acceptance Mask 0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** This register is available in Mode 1 and 2 only.
### REGISTER 34-51: MSEL3: MASK SELECT REGISTER 3(1)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value 1</th>
<th>Value 0</th>
<th>Value 00</th>
<th>Value 01</th>
<th>Value 10</th>
<th>Value 11</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6</td>
<td>FIL15_&lt;1:0&gt;</td>
<td>No mask</td>
<td>Filter 15</td>
<td>Acceptance Mask 1</td>
<td>Acceptance Mask 0</td>
<td>Filter 15</td>
<td>No mask</td>
</tr>
<tr>
<td>5-4</td>
<td>FIL14_&lt;1:0&gt;</td>
<td>No mask</td>
<td>Filter 15</td>
<td>Acceptance Mask 1</td>
<td>Acceptance Mask 0</td>
<td>Filter 15</td>
<td>No mask</td>
</tr>
<tr>
<td>3-2</td>
<td>FIL13_&lt;1:0&gt;</td>
<td>No mask</td>
<td>Filter 15</td>
<td>Acceptance Mask 1</td>
<td>Acceptance Mask 0</td>
<td>Filter 15</td>
<td>No mask</td>
</tr>
<tr>
<td>1-0</td>
<td>FIL12_&lt;1:0&gt;</td>
<td>No mask</td>
<td>Filter 15</td>
<td>Acceptance Mask 1</td>
<td>Acceptance Mask 0</td>
<td>Filter 15</td>
<td>No mask</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **-n** = Value at POR
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **x** = Bit is unknown

**Note 1:** This register is available in Mode 1 and 2 only.
34.15.4 CAN BAUD RATE REGISTERS

This section describes the CAN Baud Rate registers.

**Note:** These registers are writable in Configuration mode only.

### REGISTER 34-52: BRGCON1: BAUD RATE CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SJW1</td>
<td>SJW0</td>
<td>BRP5</td>
<td>BRP4</td>
<td>BRP3</td>
<td>BRP2</td>
<td>BRP1</td>
<td>BRP0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **-n** = Value at POR
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **x** = Bit is unknown

#### bit 7-6: **SJW<1:0>**
- Synchronized Jump Width bits
  - **11** = Synchronization jump width time = 4 x Tq
  - **10** = Synchronization jump width time = 3 x Tq
  - **01** = Synchronization jump width time = 2 x Tq
  - **00** = Synchronization jump width time = 1 x Tq

#### bit 5-0: **BRP<5:0>**
- Baud Rate Prescaler bits
  - **111111** = Tq = (2 x 64)/Fosc
  - **111110** = Tq = (2 x 63)/Fosc
    - ...
  - **000001** = Tq = (2 x 2)/Fosc
  - **000000** = Tq = (2 x 1)/Fosc
## REGISTER 34-53: BRGCON2: BAUD RATE CONTROL REGISTER 2

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEG2PHTS</td>
<td>SAM</td>
<td>SEG1PH2</td>
<td>SEG1PH1</td>
<td>SEG1PH0</td>
<td>PRSEG2</td>
<td>PRSEG1</td>
<td>PRSEG0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEG2PHTS: Phase Segment 2 Time Select bit</td>
</tr>
<tr>
<td>1 = Freely programmable</td>
</tr>
<tr>
<td>0 = Maximum of PHEG1 or Information Processing Time (IPT), whichever is greater</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 6</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAM: Sample of the CAN bus Line bit</td>
</tr>
<tr>
<td>1 = Bus line is sampled three times prior to the sample point</td>
</tr>
<tr>
<td>0 = Bus line is sampled once at the sample point</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 5-3</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEG1PH&lt;2:0&gt;: Phase Segment 1 bits</td>
</tr>
<tr>
<td>111 = Phase Segment 1 time = 8 x Tq</td>
</tr>
<tr>
<td>110 = Phase Segment 1 time = 7 x Tq</td>
</tr>
<tr>
<td>101 = Phase Segment 1 time = 6 x Tq</td>
</tr>
<tr>
<td>100 = Phase Segment 1 time = 5 x Tq</td>
</tr>
<tr>
<td>011 = Phase Segment 1 time = 4 x Tq</td>
</tr>
<tr>
<td>010 = Phase Segment 1 time = 3 x Tq</td>
</tr>
<tr>
<td>001 = Phase Segment 1 time = 2 x Tq</td>
</tr>
<tr>
<td>000 = Phase Segment 1 time = 1 x Tq</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 2-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRSEG&lt;2:0&gt;: Propagation Time Select bits</td>
</tr>
<tr>
<td>111 = Propagation time = 8 x Tq</td>
</tr>
<tr>
<td>110 = Propagation time = 7 x Tq</td>
</tr>
<tr>
<td>101 = Propagation time = 6 x Tq</td>
</tr>
<tr>
<td>100 = Propagation time = 5 x Tq</td>
</tr>
<tr>
<td>011 = Propagation time = 4 x Tq</td>
</tr>
<tr>
<td>010 = Propagation time = 3 x Tq</td>
</tr>
<tr>
<td>001 = Propagation time = 2 x Tq</td>
</tr>
<tr>
<td>000 = Propagation time = 1 x Tq</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown
REGISTER 34-54: BRGCON3: BAU D RATE CONTROL REGISTER 3

<table>
<thead>
<tr>
<th></th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>WAKDIS</td>
<td>WAKFIL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SEG2PH2(1)</td>
<td>SEG2PH1(1)</td>
<td>SEG2PH0(1)</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**bit 7**  
**WAKDIS**: Wake-up Disable bit  
1 = Disable CAN bus activity wake-up feature  
0 = Enable CAN bus activity wake-up feature

**bit 6**  
**WAKFIL**: Selects CAN bus Line Filter for Wake-up bit  
1 = Use CAN bus line filter for wake-up  
0 = CAN bus line filter is not used for wake-up

**bit 5-3**  
**Unimplemented**: Read as ‘0’

**bit 2-0**  
**SEG2PH<2:0>**: Phase Segment 2 Time Select bits(1)  
111 = Phase Segment 2 time = 8 x Tq  
110 = Phase Segment 2 time = 7 x Tq  
101 = Phase Segment 2 time = 6 x Tq  
100 = Phase Segment 2 time = 5 x Tq  
011 = Phase Segment 2 time = 4 x Tq  
010 = Phase Segment 2 time = 3 x Tq  
001 = Phase Segment 2 time = 2 x Tq  
000 = Phase Segment 2 time = 1 x Tq  

**Note 1**: These bits are ignored if SEG2PHTS bit (BRGCON2<7>) is ‘0’. 
34.15.5 CAN MODULE I/O CONTROL REGISTER

This register controls the operation of the CAN module’s I/O pins in relation to the rest of the microcontroller.

REGISTER 34-55: CIOCON: CAN I/O CONTROL REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX1SRC</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CLKSEL</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit 0</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**bit 7**  
**TX1SRC**: CAN_tx1 Signal Data Source bit
- **1** = CAN_tx1 signal will output the CAN clock
- **0** = CAN_tx1 signal will output CANTX

**bit 6-1**  
**Unimplemented**: Read as ‘0’

**bit 0**  
**CLKSEL**: CAN Clock Source Selection bit
- **1** = CAN clock is sourced by the clock selected by the FEXTOSC Configuration bit field, regardless of system clock(1)
- **0** = CAN clock is sourced from the system clock

**Note 1**: When **CLKSEL** = **1**, the clock supplied by FEXTOSC must be less than or equal to the system clock. If the CAN clock is greater than the system clock, unexpected behavior will occur.
34.15.6 CAN INTERRUPT REGISTERS

The registers in this section are the same as described in Section 9.0 “Interrupt Controller”. They are duplicated here for convenience.

REGISTER 34-56: PIR5: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 5

<table>
<thead>
<tr>
<th>Mode</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>IRXIF</td>
<td>WAKIF</td>
<td>ERRIF</td>
<td>TXB2IF</td>
<td>TXB1IF(1)</td>
<td>TXB0IF(1)</td>
<td>RXB1IF</td>
<td>RXB0IF</td>
</tr>
<tr>
<td>Mode 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mode 1,2</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td></td>
<td>IRXIF</td>
<td>WAKIF</td>
<td>ERRIF</td>
<td>TXBnIF</td>
<td>TXB1IF(1)</td>
<td>TXB0IF(1)</td>
<td>RXBnIF</td>
<td>FIFOWMIF</td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown

bit 7 IRXIF: CAN Bus Error Message Received Interrupt Flag bit
1 = An invalid message has occurred on the CAN bus
0 = No invalid message on the CAN bus

bit 6 WAKIF: CAN Bus Activity Wake-up Interrupt Flag bit
1 = Activity on the CAN bus has occurred
0 = No activity on the CAN bus

bit 5 ERRIF: CAN Module Error Interrupt Flag bit
1 = An error has occurred in the CAN module (multiple sources; refer to Section 34.14.6 “Error Interrupt”)
0 = No CAN module errors

bit 4 When CAN is in Mode 0:
TXB2IF: CAN Transmit Buffer 2 Interrupt Flag bit
1 = Transmit Buffer 2 has completed transmission of a message and may be reloaded
0 = Transmit Buffer 2 has not completed transmission of a message

When CAN is in Mode 1 or 2:

TXBnIF: Any Transmit Buffer Interrupt Flag bit(1)
1 = One or more transmit buffers have completed transmission of a message and may be reloaded
0 = No transmit buffer is ready for reload

bit 3 TXB1IF: CAN Transmit Buffer 1 Interrupt Flag bit(1)
1 = Transmit Buffer 1 has completed transmission of a message and may be reloaded
0 = Transmit Buffer 1 has not completed transmission of a message

bit 2 TXB0IF: CAN Transmit Buffer 0 Interrupt Flag bit(1)
1 = Transmit Buffer 0 has completed transmission of a message and may be reloaded
0 = Transmit Buffer 0 has not completed transmission of a message

bit 1 When CAN is in Mode 0:
RXB1IF: CAN Receive Buffer 1 Interrupt Flag bit
1 = Receive Buffer 1 has received a new message
0 = Receive Buffer 1 has not received a new message

When CAN is in Mode 1 or 2:

RXBnIF: Any Receive Buffer Interrupt Flag bit
1 = One or more receive buffers has received a new message
0 = No receive buffer has received a new message

bit 0 When CAN is in Mode 0:
RXB0IF: CAN Receive Buffer 0 Interrupt Flag bit
1 = Receive Buffer 0 has received a new message
0 = Receive Buffer 0 has not received a new message

When CAN is in Mode 1:

Unimplemented: Read as ‘0’

When CAN is in Mode 2:

FIFOWMIF: FIFO Watermark Interrupt Flag bit
1 = FIFO high watermark is reached
0 = FIFO high watermark is not reached

Note 1: In CAN Mode 1 and 2, these bits are forced to ‘0’.
**REGISTER 34-57: PIE5: PERIPHERAL INTERRUPT ENABLE REGISTER 5**

<table>
<thead>
<tr>
<th></th>
<th>Mode 0</th>
<th></th>
<th></th>
<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
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<td>R/W-0</td>
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<tr>
<td>IRXIE</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>WAKIE</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>ERRIE</td>
<td></td>
<td></td>
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<tr>
<td>TXB2IE</td>
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</tr>
<tr>
<td>TXB1IE</td>
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<td></td>
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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>RXB1IE</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RXB0IE</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Mode 1</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
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<td>R/W-0</td>
</tr>
<tr>
<td>IRXIE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WAKIE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ERRIE</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>txBnIE</td>
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<td></td>
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<td></td>
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<tr>
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<td></td>
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<tr>
<td>RXBnIE</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RXB1IE</td>
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<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RXB0IE</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit  
- **W** = Writable bit  
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR  
- ‘1’ = Bit is set  
- ‘0’ = Bit is cleared  
- **x** = Bit is unknown

**Legend:**
- **R** = Readable bit  
- **W** = Writable bit  
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR  
- ‘1’ = Bit is set  
- ‘0’ = Bit is cleared  
- **x** = Bit is unknown

**Legend:**
- **R** = Readable bit  
- **W** = Writable bit  
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR  
- ‘1’ = Bit is set  
- ‘0’ = Bit is cleared  
- **x** = Bit is unknown

**Legend:**
- **R** = Readable bit  
- **W** = Writable bit  
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR  
- ‘1’ = Bit is set  
- ‘0’ = Bit is cleared  
- **x** = Bit is unknown

| Bit | Description | Value at POR | Mode 0 |     | Mode 1 |     |     |     |     |     |     |     |     |     |     |
|-----|-------------|--------------|--------|-----|--------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 7   | IRXIE: CAN Bus Error Message Received Interrupt Enable bit | 0 | 1 | Enable invalid message received interrupt | 0 | Disable invalid message received interrupt | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 6   | WAKIE: CAN bus Activity Wake-up Interrupt Enable bit | 0 | 1 | Enable bus activity wake-up interrupt | 0 | Disable bus activity wake-up interrupt | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5   | ERRIE: CAN bus Error Interrupt Enable bit | 0 | 1 | Enable CAN module error interrupt | 0 | Disable CAN module error interrupt | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4   | When CAN is in Mode 0: | 0 | 1 | Enable Transmit Buffer 2 interrupt | 0 | Disable Transmit Buffer 2 interrupt | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3   | TXB2IE: CAN Transmit Buffer 2 Interrupt Enable bit | 0 | 1 | Enable Transmit Buffer 2 interrupt | 0 | Disable Transmit Buffer 2 interrupt | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2   | When CAN is in Mode 1 or 2: | 0 | 1 | Enable transmit buffer interrupt; individual interrupt is enabled by TXB1IE and BIE0 | 0 | Disable all transmit buffer interrupts | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1   | TXB1IE: CAN Transmit Buffer 1 Interrupt Enable bit | 0 | 1 | Enable Transmit Buffer 1 interrupt | 0 | Disable Transmit Buffer 1 interrupt | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0   | RXB0IE: CAN Transmit Buffer 0 Interrupt Enable bit | 0 | 1 | Enable Transmit Buffer 0 interrupt | 0 | Disable Transmit Buffer 0 interrupt | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Note 1:** In CAN Mode 1 and 2, these bits are forced to ‘0’.

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Preliminary  
DS40001943A-page 645
### REGISTER 34-58: IPR5: PERIPHERAL INTERRUPT PRIORITY REGISTER 5

<table>
<thead>
<tr>
<th>Mode 0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRXIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>WAKIP</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ERRIP</td>
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</tr>
<tr>
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</tr>
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</tr>
<tr>
<td>RXB0IP</td>
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<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Mode 1,2</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRXIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WAKIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ERRIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TXBnIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TXB1IP(1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RXBnIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FIFOWMIP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- ‘-n’ = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

#### bit 7
**IRXIP**: CAN Bus Error Message Received Interrupt Priority bit
- 1 = High priority
- 0 = Low priority

#### bit 6
**WAKIP**: CAN Bus Activity Wake-up Interrupt Priority bit
- 1 = High priority
- 0 = Low priority

#### bit 5
**ERRIP**: CAN Module Error Interrupt Priority bit
- 1 = High priority
- 0 = Low priority

#### bit 4
When CAN is in Mode 0:
**TXB2IP**: CAN Transmit Buffer 2 Interrupt Priority bit
- 1 = High priority
- 0 = Low priority

When CAN is in Mode 1 or 2:
**TXBnIP**: CAN Transmit Buffer Interrupt Priority bit
- 1 = High priority
- 0 = Low priority

#### bit 3
**TXB1IP**: CAN Transmit Buffer 1 Interrupt Priority bit(1)
- 1 = High priority
- 0 = Low priority

#### bit 2
**TXB0IP**: CAN Transmit Buffer 0 Interrupt Priority bit(1)
- 1 = High priority
- 0 = Low priority

#### bit 1
When CAN is in Mode 0:
**RXB1IP**: CAN Receive Buffer 1 Interrupt Priority bit
- 1 = High priority
- 0 = Low priority

When CAN is in Mode 1 or 2:
**RXBnIP**: CAN Receive Buffer Interrupts Priority bit
- 1 = High priority
- 0 = Low priority

#### Note 1:
In CAN Mode 1 and 2, these bits are forced to ‘0’.
REGISTER 34-58:  IPR5: PERIPHERAL INTERRUPT PRIORITY REGISTER 5 (CONTINUED)

bit 0  When CAN is in Mode 0:
   RXB0IP: CAN Receive Buffer 0 Interrupt Priority bit
   1 = High priority
   0 = Low priority
When CAN is in Mode 1:
   Unimplemented: Read as ‘0’
When CAN is in Mode 2:
   FIFOWMIP: FIFO Watermark Interrupt Priority bit
   1 = High priority
   0 = Low priority

Note 1:  In CAN Mode 1 and 2, these bits are forced to ‘0’.

REGISTER 34-59:  TXBIE: TRANSMIT BUFFERS INTERRUPT ENABLE REGISTER(1)

<table>
<thead>
<tr>
<th></th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

bit 7-5  Unimplemented: Read as ‘0’
bit 4-2  TXB2IE:TXB0IE: Transmit Buffer 2-0 Interrupt Enable bits(2)
   1 = Transmit buffer interrupt is enabled
   0 = Transmit buffer interrupt is disabled
bit 1-0  Unimplemented: Read as ‘0’

Note 1:  This register is available in Mode 1 and 2 only.
2:  TXBnIE in PIE5 register must be set to get an interrupt.
## REGISTER 34-60: BIE0: BUFFER INTERRUPT ENABLE REGISTER 0(1)

<table>
<thead>
<tr>
<th></th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>B5IE(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B4IE(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B3IE(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B2IE(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B1IE(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B0IE(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RXB1IE(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RXB0IE(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

- **bit 7-2**  
  - B<5:0>IE: Programmable Transmit/Receive Buffer 5-0 Interrupt Enable bits(2)
    - 1 = Interrupt is enabled
    - 0 = Interrupt is disabled

- **bit 1-0**  
  - RXB<1:0>IE: Dedicated Receive Buffer 1-0 Interrupt Enable bits(2)
    - 1 = Interrupt is enabled
    - 0 = Interrupt is disabled

**Note 1:** This register is available in Mode 1 and 2 only.

**2:** Either TXBnIE or RXBnIE, in the PIE5 register, must be set to get an interrupt.
35.0 FIXED VOLTAGE REFERENCE (FVR)

The Fixed Voltage Reference, or FVR, is a stable voltage reference, independent of VDD, with 1.024V, 2.048V or 4.096V selectable output levels. The output of the FVR can be configured to supply a reference voltage to the following:

- ADC input channel
- ADC positive reference
- Comparator input
- Digital-to-Analog Converter (DAC)

The FVR can be enabled by setting the EN bit of the FVRCON register.

Note: Fixed Voltage Reference output cannot exceed VDD.

35.1 Independent Gain Amplifiers

The output of the FVR, which is connected to the ADC, Comparators, and DAC, is routed through two independent programmable gain amplifiers. Each amplifier can be programmed for a gain of 1x, 2x or 4x, to produce the three possible voltage levels.

The ADFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the ADC module. Reference Section 37.0 “Analog-to-Digital Converter with Computation (ADC2) Module” for additional information.

The CDAFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the DAC and comparator module. Reference Section 38.0 “5-Bit Digital-to-Analog Converter (DAC) Module” and Section 39.0 “Comparator Module” for additional information.

35.2 FVR Stabilization Period

When the Fixed Voltage Reference module is enabled, it requires time for the reference and amplifier circuits to stabilize. Once the circuits stabilize and are ready for use, the RDY bit of the FVRCON register will be set.

FIGURE 35-1: VOLTAGE REFERENCE BLOCK DIAGRAM

![Voltage Reference Block Diagram](image-url)
35.3 Register Definitions: FVR Control

**REGISTER 35-1: FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER**

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>RDY</td>
<td>TSEN</td>
<td>TSRNG</td>
<td>CDAFVR&lt;1:0&gt;</td>
<td>ADFVR&lt;1:0&gt;</td>
<td></td>
<td></td>
<td>648</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **q** = Value depends on condition

**bit 7**

- **EN**: Fixed Voltage Reference Enable bit
  - 1 = Fixed Voltage Reference is enabled
  - 0 = Fixed Voltage Reference is disabled

**bit 6**

- **RDY**: Fixed Voltage Reference Ready Flag bit\(^{(1)}\)
  - 1 = Fixed Voltage Reference output is ready for use
  - 0 = Fixed Voltage Reference output is not ready or not enabled

**bit 5**

- **TSEN**: Temperature Indicator Enable bit\(^{(3)}\)
  - 1 = Temperature Indicator is enabled
  - 0 = Temperature Indicator is disabled

**bit 4**

- **TSRNG**: Temperature Indicator Range Selection bit\(^{(3)}\)
  - 1 = VOUT = 3VT (High Range)
  - 0 = VOUT = 2VT (Low Range)

**bit 3-2**

- **CDAFVR<1:0>**: Comparator FVR Buffer Gain Selection bits
  - 11 = FVR Buffer 1 Gain is 4x, (4.096V)\(^{(2)}\)
  - 10 = FVR Buffer 1 Gain is 2x, (2.048V)\(^{(2)}\)
  - 01 = FVR Buffer 1 Gain is 1x, (1.024V)
  - 00 = FVR Buffer 1 is off

**bit 1-0**

- **ADFVR<1:0>**: ADC FVR Buffer Gain Selection bit
  - 11 = FVR Buffer 2 Gain is 4x, (4.096V)\(^{(2)}\)
  - 10 = FVR Buffer 2 Gain is 2x, (2.048V)\(^{(2)}\)
  - 01 = FVR Buffer 2 Gain is 1x, (1.024V)
  - 00 = FVR Buffer 2 is off

**Note 1:** FVRRDY is always ‘1’.

**Note 2:** Fixed Voltage Reference output cannot exceed VDD.

**Note 3:** See Section 36.0 “Temperature Indicator Module” for additional information.

**TABLE 35-1: SUMMARY OF REGISTERS ASSOCIATED WITH FIXED VOLTAGE REFERENCE**

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>FVRCON</td>
<td>EN</td>
<td>RDY</td>
<td>TSEN</td>
<td>TSRNG</td>
<td>CDAFVR&lt;1:0&gt;</td>
<td>ADFVR&lt;1:0&gt;</td>
<td></td>
<td></td>
<td>648</td>
</tr>
</tbody>
</table>

**Legend:**

- **—** = Unimplemented location, read as ‘0’. Shaded cells are not used with the Fixed Voltage Reference.
36.0 TEMPERATURE INDICATOR MODULE

This family of devices is equipped with a temperature circuit designed to measure the operating temperature of the silicon die. The main purpose of the Temperature Indicator module is to provide temperature-dependent voltage that can be measured by the Analog-to-Digital Converter.

The circuit's range of operating temperature falls between -40°C and +125°C. The circuit may be used as a temperature threshold detector or a more accurate temperature indicator, depending on the level of calibration performed. A one-point calibration allows the circuit to indicate a temperature closely surrounding that point. A two-point calibration allows the circuit to sense the entire range of temperature more accurately.

36.1 Module Operation

The temperature indicator module consists of a temperature-sensing circuit that provides a voltage to the device ADC. The analog voltage output, VTSENSE, varies inversely to the device temperature. The output of the temperature indicator is referred to as VOUT.

Figure 36-1 shows a simplified block diagram of the temperature indicator module.

![Figure 36-1: Temperature Circuit Diagram](image)

The output of the circuit is measured using the internal Analog-to-Digital Converter. A channel is reserved for the temperature circuit output. Refer to Section 37.0 “Analog-to-Digital Converter with Computation (ADC2) Module” for detailed information.

The ON/OFF bit for the module is located in the FVRCON register. See Section 35.0 “Fixed Voltage Reference (FVR)” for more information. The circuit is enabled by setting the TSEN bit of the FVRCON register. When the module is disabled, the circuit draws no current.

The circuit operates in either High or Low range. Refer to Section 36.5 “Temperature Indicator Range” for more details on the range settings.

36.2 Estimation of Temperature

This section describes how the sensor voltage can be used to estimate the temperature of the module. To use the sensor, the output voltage, VTSENSE, is measured and the corresponding temperature is determined. Equation 36-1 provides an estimate for the die temperature based on the VTSENSE value.

**EQUATION 36-1: SENSOR TEMPERATURE**

\[ T_{SENSE} = V_{TSENSE} \times (-M_t) + T_{OFFSET} \]

Where:
- \( M_t = 1/M_v \), where \( M_v \) = sensor voltage sensitivity (V/°C).
- \( T_{OFFSET} \) is the temperature difference between the theoretical temperature and the actual temperature.
36.2.1 CALIBRATION

36.2.1.1 Single-Point Calibration
Single-point calibration is performed by application software using Equation 36-1 and the assumed Mt. A reading of VTSENSE at a known temperature is taken, and the theoretical temperature is calculated by temporarily setting TOFFSET = 0. Then TOFFSET is computed as the difference of the actual and calculated temperatures. Finally, TOFFSET is stored in nonvolatile memory within the device, and is applied to future readings to gain a more accurate measurement.

36.2.1.2 Higher-Order Calibration
If the application requires more precise temperature measurement, additional calibrations steps will be necessary. For these applications, two-point or three-point calibration is recommended.

Note 1: The TOFFSET value may be determined by the user with a temperature test.

2: Although the measurement range is -40°C to +125 °C, due to the variations in offset error, the single-point uncalibrated calculated TSENSE value may indicate a temperature from -140°C to +225°C, before the calibration offset is applied.

3: The User must take into consideration self-heating of the device at different clock frequencies and output pin loading. For package related characteristics information, refer to Table 45-6.

36.2.2 TEMPERATURE RESOLUTION
The resolution of the ADC reading, Ma (°C/count), depends on both the ADC resolution N and the reference voltage used for conversion, as shown in Equation 36-2. It is recommended to use the smallest VREF value, such as 2.048 FVR reference voltage, instead of VDD.

Note: Refer to Table 45-17 for FVR reference voltage accuracy.

EQUATION 36-2: TEMPERATURE RESOLUTION (°C/LSb)

\[
Ma = \frac{V_{\text{REF}}}{2^N} \times Mt
\]

\[
Ma = \frac{V_{\text{REF}}}{2^N \cdot Mv}
\]

Where:
Mv = sensor voltage sensitivity (V/°C)
VREF = Reference voltage of the ADC module (in Volts)
N = Resolution of the ADC

The typical Mv value for a single diode is approximately -1.267 to -1.32 mV/C.
The typical Mv value for a stack of two diodes (Low Range setting) is approximately -2.533 mV/C.
The typical Mv value for a stack of three diodes (High range setting) is approximately -3.8 mV/C.

36.3 ADC Acquisition Time
To ensure accurate temperature measurements, the user must wait a certain time for the ADC value to settle, after the ADC input multiplexer is connected to the temperature indicator output, before the conversion is performed.
36.4 Minimum Operating VDD

When the temperature circuit is operated in low range, the device may be operated at any operating voltage that is within specifications. When the temperature circuit is operated in High range, the device operating voltage, VDD, must be high enough to ensure that the temperature circuit is correctly biased.

Table 36-1 shows the recommended minimum VDD vs. Range setting.

Table 36-1: Recommended VDD vs. Range

<table>
<thead>
<tr>
<th>Min. VDD, TSRNG = 1 (High Range)</th>
<th>Min. VDD, TSRNG = 0 (Low Range)</th>
</tr>
</thead>
<tbody>
<tr>
<td>≥ 2.5</td>
<td>≥ 1.8</td>
</tr>
</tbody>
</table>

36.5 Temperature Indicator Range

The temperature indicator circuit operates in either high or low range. The high range, selected by setting the TSRNG bit of the FVRCON register, provides a wider output voltage. This provides more resolution over the temperature range. High range requires a higher-bias voltage to operate and thus, a higher VDD is needed. The low range is selected by clearing the TSRNG bit of the FVRCON register. The low range generates a lower sensor voltage and thus, a lower VDD voltage is needed to operate the circuit.

The output voltage of the sensor is the highest value at -40°C and the lowest value at +125°C.

- **High Range:** The high range is used in applications with the reference for the ADC, VREF = 2.048V. This range may not be suitable for battery-powered applications.
- **Low Range:** This mode is useful in applications in which the VDD is too low for high-range operation. The VDD in this mode can be as low as 1.8V. VDD must, however, be at least 0.5V higher than the maximum sensor voltage depending on the expected low operating temperature.

36.6 DIA Information

DIA data provide ADC readings at one operating temperature. DIA data is taken during factory testing and stored within the device. The 90°C reading alone allows single-point calibration as described in Section 36.2.1, Calibration, by solving Equation 36-1 for TOFFSET.

Refer to Section 5.7 “Device Information Area” for more information on the data stored in the DIA and how to access them.

Note: The lower temperature range (e.g., -40°C) will suffer in accuracy because temperature conversion must extrapolate below the reference points, amplifying any measurement errors.

Table 36-2: Summary of Registers Associated with the Temperature Indicator

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>FVRCON</td>
<td>EN</td>
<td>RDY</td>
<td>TSEN</td>
<td>TSRNG</td>
<td>CDAFVR&lt;1:0&gt;</td>
<td>ADFVR&lt;1:0&gt;</td>
<td></td>
<td></td>
<td>648</td>
</tr>
</tbody>
</table>

Legend: — = Unimplemented location, read as ‘0’. Shaded cells are unused by the temperature indicator module.
37.0 ANALOG-TO-DIGITAL CONVERTER WITH COMPUTATION (ADC²) MODULE

The Analog-to-Digital Converter with Computation (ADC²) allows conversion of an analog input signal to a 12-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 12-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESH:ADRESL register pair).

Additionally, the following features are provided within the ADC module:

- 13-bit Acquisition Timer
- Hardware Capacitive Voltage Divider (CVD) support:
  - 13-bit Precharge Timer
  - Adjustable sample and hold capacitor array
  - Guard ring digital output drive
- Automatic repeat and sequencing:
  - Automated double sample conversion for CVD
  - Two sets of result registers (Result and Previous result)
  - Auto-conversion trigger
  - Internal retrigger
- Computation features:
  - Averaging and Low-Pass Filter functions
  - Reference Comparison
  - 2-level Threshold Comparison
  - Selectable Interrupts

Figure 37-1 shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

The ADC can generate an interrupt upon completion of a conversion and upon threshold comparison. These interrupts can be used to wake up the device from Sleep.
FIGURE 37-1: ADC\(^2\) BLOCK DIAGRAM

- **Vref+ and Vref-**: Positive and negative reference inputs.
- **Enable**: Enables the ADC.
- **DACx_output**:输出DAC。
- **FVR_buffer1**: 电压参考缓冲器。
- **Temp Indicator**: 温度指示器。
- **PCH<5:0>**: 外部通道输入。
- **External Channel Inputs**: 外部通道输入。
- **Internal Channel Inputs**: 内部通道输入。
- **AN0, ANa, ANz**: 内部通道输入。
- **VSS**: 地。
- **VDD**: 电源。
- **VREF+ pin**: 电压参考+引脚。
- **VREF- pin**: 电压参考-引脚。
- **GO/DONE**: 完成。
- **Start**: 启动。
- **ADC Sample Circuit**: ADC取样电路。
- **ART<4:0>**: 自动转换触发。
- **ADON**: ADC使能。
- **Trigger Select**: 触发选择。
- **Trigger Sources**: 触发源。
- **12-bit Result**: 12位结果。
- **ADRESH, ADRESL**: 高16位和低16位。
- **CS**: 片选。
- **ADC Clock Select**: ADC时钟选择。
- **FRC**: 内部时钟。
- **Fosc/n**: Fosc分频。
- **Fosc**: 振荡器。
- **ADFM**: 16位过采样。
- **ADON**: ADC使能。
- **VSS**: 地。
37.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port configuration
- Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Result formatting
- Conversion Trigger Selection
- ADC Acquisition Time
- ADC Precharge Time
- Additional Sample and Hold Capacitor
- Single/Double Sample Conversion
- Guard Ring Outputs

37.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. Refer to Section 16.0 “I/O Ports” for more information.

37.1.2 CHANNEL SELECTION

There are several channel selections available:

- Eight PORTA pins (RA<7:0>)
- Eight PORTB pins (RB<7:0>)
- Eight PORTC pins (RC<7:0>)
- Temperature Indicator
- DAC output
- Fixed Voltage Reference (FVR)
- VSS (ground)

The ADPCH register determines which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion.

Refer to Section 37.2 “ADC Operation” for more information.

Note: Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

37.1.3 ADC VOLTAGE REFERENCE

The ADPREF<1:0> bits of the ADREF register provide control of the positive voltage reference. The positive voltage reference can be:

- VREF+ pin
- VDD
- FVR outputs

The ADNREF bit of the ADREF register provides control of the negative voltage reference. The negative voltage reference can be:

- VREF- pin
- VSS

See Section 35.0 “Fixed Voltage Reference (FVR)” for more details on the Fixed Voltage Reference.

37.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCLK register and the CS bits of the ADCON0 register. If Fosc is selected as the ADC clock, there is a prescaler available to divide the clock so that it meets the ADC clock period specification. The ADC clock source options are the following:

- F OSC/(2^n)(where n is from 1 to 128)
- FRC (dedicated RC oscillator)

The time to complete one bit conversion is defined as TAD. Refer Figure 37-2 for the complete timing details of the ADC conversion.

For correct conversion, the appropriate TAD specification must be met. Refer to Table 45-14 for more information. Table 37-1 gives examples of appropriate ADC clock selections.

Note 1: Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

2: The internal control logic of the ADC runs off of the clock selected by the CS bit of ADCON0. What this can mean is when the CS bit of ADCON0 is set to ‘1’ (ADC runs on FRC), there may be unexpected delays in operation when setting ADC control bits.
### TABLE 37-1: ADC CLOCK PERIOD (TAD) VS. DEVICE OPERATING FREQUENCIES(1,4)

<table>
<thead>
<tr>
<th>ADC Clock Period (TAD)</th>
<th>Device Frequency (Fosc)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC Clock Source CS&lt;5:0&gt;</td>
<td>64 MHz</td>
</tr>
<tr>
<td>Fosc/2 000000</td>
<td>31.25 ns(2)</td>
</tr>
<tr>
<td>Fosc/4 000001</td>
<td>62.5 ns(2)</td>
</tr>
<tr>
<td>Fosc/6 000010</td>
<td>125 ns(2)</td>
</tr>
<tr>
<td>Fosc/8 000011</td>
<td>187.5 ns(2)</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>Fosc/16 000111</td>
<td>250 ns(2)</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>Fosc/128 111111</td>
<td>2.0 µs</td>
</tr>
<tr>
<td>FRC</td>
<td>CS(ADCON0&lt;4&gt;) = 1</td>
</tr>
</tbody>
</table>

**Legend:** Shaded cells are outside of recommended range.

**Note:**
1: See TAD parameter for FRC source typical TAD value.
2: These values violate the required TAD time.
3: Outside the recommended TAD time.
4: The ADC clock period (TAD) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock Fosc. However, the FRC oscillator source must be used when conversions are to be performed with the device in Sleep mode.

### FIGURE 37-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES

<table>
<thead>
<tr>
<th>Precharge Time 1-8191 TCY (TPRE)</th>
<th>Acquisition/Sharing Time 1-8191 TCY (TACQ)</th>
<th>Conversion Time (Traditional Timing of ADC Conversion)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TCV=TCY-TAD</td>
<td>TAD11 TAD2 TAD3 TAD4 TAD5 TAD6 TAD7 TAD8 TAD9 TAD10 TAD11 TAD12 TAD13 2TCY</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TAD11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Conversion starts</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Holding capacitor CHOLD is disconnected from analog input (typically 100ns)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>External and Internal Channels are charged/discharged</td>
<td>External and Internal Channels share charge</td>
<td></td>
</tr>
<tr>
<td>If ADPRE ≠ 0</td>
<td>If ADACQ ≠ 0</td>
<td></td>
</tr>
<tr>
<td>Set GO bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>On the following cycle: ADRESH/ADRESL is loaded, GO bit is cleared, ADIF bit is set,</td>
</tr>
</tbody>
</table>

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37.1.5 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC Interrupt Flag is the ADIF bit in the PIR1 register. The ADC Interrupt Enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

**Note 1:** The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.

**Note 2:** The ADC operates during Sleep only when the FRC oscillator is selected.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake up from Sleep and resume in-line code execution, the ADIE bit of the PIEX register and the GIE bits of the INTCON0 register must both be set. If all these bits are set, the execution will switch to the Interrupt Service Routine.

37.1.6 RESULT FORMATTING

The 12-bit ADC conversion result can be supplied in two formats, left justified or right justified. The FM bits of the ADCON0 register controls the output format. Figure 37-3 shows the two output formats.

 Writes to the ADRES register pair are always right justified regardless of the selected format mode. Therefore, data read after writing to ADRES when $ADFRM0 = 0$ will be shifted left four places.

**FIGURE 37-3: 12-BIT ADC CONVERSION RESULT FORMAT**

![Diagram of ADC conversion result format](image-url)
37.2 ADC Operation

37.2.1 STARTING A CONVERSION
To enable the ADC module, the ON bit of the ADCON0 register must be set to a ‘1’. A conversion may be started by any of the following:

• Software setting the GO bit of ADCON0 to ‘1’
• An external trigger (selected by Register 37-3)
• A continuous-mode retrigger (see section Section 37.6.8 “Continuous Sampling mode”)

Note: The GO bit should not be set in the same instruction that turns on the ADC. Refer to Section 37.2.6 “ADC Conversion Procedure (Basic Mode)”.

37.2.2 COMPLETION OF A CONVERSION
When any individual conversion is complete, the value already in ADRES is written into PREV (if ADPSIS = 1) and the new conversion results appear in ADRES. When the conversion completes, the ADC module will:

• Clear the GO bit (unless the CONT bit of ADCON0 is set)
• Set the ADIF Interrupt Flag bit
• Set the ADMATH bit
• Update ACC

When ADDSEN = 0 then after every conversion, or when ADDSEN = 1 then after every other conversion, the following events occur:

• ERR is calculated
• ADTIF is set if ERR calculation meets threshold comparison

Importantly, filter and threshold computations occur after the conversion itself is complete. As such, interrupt handlers responding to ADIF should check ADTIF before reading filter and threshold results.

37.2.3 ADC OPERATION DURING SLEEP
The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC oscillator source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ON bit remains set.

37.2.4 EXTERNAL TRIGGER DURING SLEEP
If the external trigger is received during Sleep while ADC clock source is set to the FRC, ADC module will perform the conversion and set the ADIF bit upon completion.

If an external trigger is received when the ADC clock source is something other than FRC, the trigger will be recorded, but the conversion will not begin until the device exits Sleep.
37.2.5 AUTO-CONVERSION TRIGGER

The auto-conversion trigger allows periodic ADC measurements without software intervention. When a rising edge of the selected source occurs, the GO bit is set by hardware.

The auto-conversion trigger source is selected by the ADACT register.

Using the auto-conversion trigger does not assure proper ADC timing. It is the user’s responsibility to ensure that the ADC timing requirements are met. See Register 37-33 for auto-conversion sources.

37.2.6 ADC CONVERSION PROCEDURE (BASIC MODE)

This is an example procedure for using the ADC to perform an analog-to-digital conversion:

1. Configure Port:
   - Disable pin output driver (Refer to the TRISx register)
   - Configure pin as analog (Refer to the ANSELx register)

2. Configure the ADC module:
   - Select ADC conversion clock
   - Select voltage reference
   - Select ADC input channel
   - Precharge and acquisition
   - Turn on ADC module

3. Configure ADC interrupt (optional):
   - Clear ADC interrupt flag
   - Enable ADC interrupt
   - Enable global interrupt (GIEL bit)(1)

4. If ADACQ = 0, software must wait the required acquisition time(2).

5. Start conversion by setting the GO bit.

6. Wait for ADC conversion to complete by one of the following:
   - Polling the GO bit
   - Polling the ADIF bit
   - Waiting for the ADC interrupt (interrupts enabled)

7. Read ADC Result.

8. Clear the ADC interrupt flag (required if interrupt is enabled).

Note 1: The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

Example 37-1: ADC CONVERSION

```c
/*This code block configures the ADC for polling, VDD and VSS references, FRC oscillator and AN0 input. Conversion start & polling for completion are included.
*/
void main() {
    //System Initialize
    initializeSystem();

    //Setup ADC
    ADCON0bits.FM = 1; //right justify
    ADCON0bits.CS = 1; //FRC Clock
    ADPC = 0x00; //RA0 is Analog channel
    TRISAbits.TRISA0 = 1; //Set RA0 to input
    ANSELAbits.ANSELA0 = 1; //Set RA0 to analog
    ADCON0bits.ON = 1; //Turn ADC On

    while (1) {
        ADCON0bits.GO = 1; //Start conversion
        while (ADCON0bits.GO); //Wait for conversion done
        resultHigh = ADRESH; //Read result
        resultLow = ADRESL; //Read result
    }
}
```
37.3 ADC Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 37-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), refer to Figure 37-4. The maximum recommended impedance for analog sources is 10 kΩ. If the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an ADC acquisition must be completed before the conversion can be started. To calculate the minimum acquisition time, Equation 37-1 may be used. This equation assumes that 1/2 LSb error is used (4,096 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 37-1: ACQUISITION TIME EXAMPLE

Assumptions: Temperature = 50°C and external impedance of 10kΩ 5.0V VDD

\[ T_{ACQ} = \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \]
\[ = T_{AMP} + T_C + T_{COFF} \]
\[ = 2\mu s + T_C + [(\text{Temperature} - 25^\circ C)(0.05\mu s/\circ C)] \]

The value for TC can be approximated with the following equations:

\[ V_{APPLIED}\left(1 - \frac{1}{\left(2^n + 1\right)}\right) = V_{CHOLD} \quad ;[1] \text{VCHOLD charged to within 1/2 lsb} \]

\[ V_{APPLIED}\left(1 - e^{-\frac{T_C}{RC}}\right) = V_{CHOLD} \quad ;[2] \text{VCHOLD charge response to VAPPLIED} \]

\[ V_{APPLIED}\left(1 - e^{-\frac{T_C}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{\left(2^n + 1\right)}\right) \quad ;\text{combining [1] and [2]} \]

Note: Where \( n = \text{number of bits of the ADC} \).

Solving for TC:

\[ T_C = -CHOLD(R IC + RSS + RS) \ln(1/8191) \]
\[ = -28pF(1k\Omega + 7k\Omega + 10k\Omega) \ln(0.0001221) \]
\[ = 4.54\mu s \]

Therefore:

\[ T_{ACQ} = 2\mu s + 4.54\mu s + [(50^\circ C - 25^\circ C)(0.05\mu s/\circ C)] \]
\[ = 7.79\mu s \]

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.
FIGURE 37-4: ANALOG INPUT MODEL

Legend:
- **CHOLD** = Sample/Hold Capacitance
- **CPIN** = Input Capacitance
- **I LEAKAGE** = Leakage current at the pin due to various junctions
- **Ric** = Interconnect Resistance
- **RSS** = Resistance of Sampling Switch
- **SS** = Sampling Switch
- **VT** = Threshold Voltage

**Note 1:** Refer to Table 45-4 (parameter D340 and D341).

FIGURE 37-5: ADC TRANSFER FUNCTION

Legend:
- **REF-** = Analog Input Voltage
- **0.5 LSB**
- **1.5 LSB**
- **Zero-Scale Transition**
- **Full-Scale Transition**
- **ADC Output Code**
- **Full-Scale Range**
- **Analog Input Voltage**
- **REF+**
37.4 ADC Charge Pump

The ADC module has a dedicated charge pump which can be controlled through the ADCP register (Register 37-36). The primary purpose of the charge pump is to supply a constant voltage to the gates of transistor devices in the A/D converter, signal and reference input pass-gates, to prevent degradation of transistor performance at low operating voltage.

The charge pump can be enabled by setting the CPON bit in the ADC register. Once enabled, the pump will undergo a start-up time to stabilize the charge pump output. Once the output stabilizes and is ready for use, the CPRDY bit of the ADCP register will be set.

37.5 Capacitive Voltage Divider (CVD) Features

The ADC module contains several features that allow the user to perform a relative capacitance measurement on any ADC channel using the internal ADC sample and hold capacitance as a reference. This relative capacitance measurement can be used to implement capacitive touch or proximity sensing applications. Figure 37-6 shows the basic block diagram of the CVD portion of the ADC module.

FIGURE 37-6: HARDWARE CAPACITIVE VOLTAGE DIVIDER BLOCK DIAGRAM

![Diagram](image-url)
37.5.1 CVD OPERATION

A CVD operation begins with the ADC’s internal sample and hold capacitor \( (C_{\text{HOLD}}) \) being disconnected from the path which connects it to the external capacitive sensor node. While disconnected, \( C_{\text{HOLD}} \) is precharged to \( V_{\text{DD}} \) or \( V_{\text{SS}} \), while the path to the sensor node is precharged to the level opposite that of \( C_{\text{HOLD}} \). When the precharge phase is complete, the \( V_{\text{DD}}/V_{\text{SS}} \) precharge paths for the two nodes are shut off and \( C_{\text{HOLD}} \) and the path to the external sensor node are reconnected, at which time the acquisition phase of the CVD operation begins. During acquisition, a capacitive voltage divider is formed between the precharged \( C_{\text{HOLD}} \) and sensor nodes, which results in a final voltage level setting on \( C_{\text{HOLD}} \), which is determined by the capacitances and precharge levels of the two nodes. After acquisition, the ADC converts the voltage level on \( C_{\text{HOLD}} \). This process is then repeated with inverted precharge levels for both the \( C_{\text{HOLD}} \) and external sensor nodes. Figure 37-7 shows the waveform for two inverted CVD measurements, which is known as differential CVD measurement.

FIGURE 37-7: DIFFERENTIAL CVD MEASUREMENT WAVEFORM
37.5.2 PRECHARGE CONTROL

The precharge stage is an optional period of time that brings the external channel and internal sample and hold capacitor to known voltage levels. Precharge is enabled by writing a non-zero value to the PRE register. This stage is initiated when an ADC conversion begins, either from setting the GO bit, a special event trigger, or a conversion restart from the computation functionality. If the PRE register is cleared when an ADC conversion begins, this stage is skipped.

During the precharge time, CHOLD is disconnected from the outer portion of the sample path that leads to the external capacitive sensor and is connected to either VDD or VSS, depending on the value of the ADPPOL bit of ADCON1. At the same time, the port pin logic of the selected analog channel is overridden to drive a digital high or low out, in order to precharge the outer portion of the ADC’s sample path, which includes the external sensor. The output polarity of this override is also determined by the ADPPOL bit of ADCON1. The amount of time that this charging receives is controlled by the PRE register.

37.5.4 GUARD RING OUTPUTS

Note 1: The external charging overrides the TRIS setting of the respective I/O pin.

2: If there is a device attached to this pin, Precharge should not be used.

37.5.3 ACQUISITION CONTROL

The Acquisition stage is an optional time for the voltage on the internal sample and hold capacitor to charge or discharge from the selected analog channel. This acquisition time is controlled by the ADACQ register. If PRE = 0, acquisition starts at the beginning of conversion. When PRE = 1, the acquisition stage begins when precharge ends.

At the start of the acquisition stage, the port pin logic of the selected analog channel is overridden to turn off the digital high/low output drivers so they do not affect the final result of the charge averaging. Also, the selected ADC channel is connected to CHOLD. This allows charge averaging to proceed between the precharged channel and the CHOLD capacitor.

Note: When PRE = 0, acquisition time cannot be ‘0’. In this case, setting ADACQ to ‘0’ will set a maximum acquisition time (8191 ADC clock cycles). When precharge is disabled, setting ADACQ to ‘0’ will disable hardware acquisition time control.

Figure 37-8 shows a typical guard ring circuit. CGUARD represents the capacitance of the guard ring trace placed on the PCB board. The user selects values for RA and RB that will create a voltage profile on CGUARD, which will match the selected acquisition channel.

The purpose of the guard ring is to generate a signal in phase with the CVD sensing signal to minimize the effects of the parasitic capacitance on sensing electrodes. It also can be used as a mutual drive for mutual capacitive sensing. For more information about active guard and mutual drive, see Application Note AN1478, “mTouch™ Sensing Solution Acquisition Methods Capacitive Voltage Divider” (DS01478).

The ADC has two guard ring drive outputs, ADGRDA and ADGRDB. These outputs can be routed through PPS controls to I/O pins (see Section 17.0 “Peripheral Pin Select (PPS) Module” for details) and the polarity of these outputs are controlled by the ADGPOL and ADIPEN bits of ADCON1.

At the start of the first precharge stage, both outputs are set to match the ADGPOL bit of ADCON1. Once the acquisition stage begins, ADGRDA changes polarity, while ADGRDB remains unchanged. When performing a double sample conversion, setting the ADIPEN bit of ADCON1 causes both guard ring outputs to transition to the opposite polarity of ADGPOL at the start of the second precharge stage, and ADGRDA toggles again for the second acquisition. For more information on the timing of the guard ring output, refer to Figure 37-8 and Figure 37-9.
37.5.5 ADDITIONAL SAMPLE AND HOLD CAPACITANCE

Additional capacitance can be added in parallel with the internal sample and hold capacitor (CHOLD) by using the ADCAP register. This register selects a digitally programmable capacitance which is added to the ADC conversion bus, increasing the effective internal capacitance of the sample and hold capacitor in the ADC module. This is used to improve the match between internal and external capacitance for a better sensing performance. The additional capacitance does not affect analog performance of the ADC because it is not connected during conversion. See Figure 37-10.
37.6 Computation Operation

The ADC module hardware is equipped with post conversion computation features. These features provide data post-processing functions that can be operated on the ADC conversion result, including digital filtering/averaging and threshold comparison functions.

FIGURE 37-10: COMPUTATIONAL FEATURES SIMPLIFIED BLOCK DIAGRAM

The operation of the ADC computational features is controlled by ADMD <2:0> bits in the ADCON2 register.

The module can be operated in one of five modes:

- **Basic**: In this mode, ADC conversion occurs on single (ADDSEN = 0) or double (ADDSEN = 1) samples. ADIF is set after all the conversion are complete.

- **Accumulate**: With each trigger, the ADC conversion result is added to accumulator and CNT increments. ADIF is set after each conversion. ADTIF is set according to the calculation mode.

- **Average**: With each trigger, the ADC conversion result is added to the accumulator. When the RPT number of samples have been accumulated, a threshold test is performed. Upon the next trigger, the accumulator is cleared. For the subsequent tests, additional RPT samples are required to be accumulated.

- **Burst Average**: At the trigger, the accumulator is cleared. The ADC conversion results are then collected repetitively until RPT samples are accumulated and finally the threshold is tested.

- **Low-Pass Filter (LPF)**: With each trigger, the ADC conversion result is sent through a filter. When RPT samples have occurred, a threshold test is performed. Every trigger after that the ADC conversion result is sent through the filter and another threshold test is performed.

The five modes are summarized in Table 37-2 below.
### TABLE 37-2: COMPUTATION MODES

<table>
<thead>
<tr>
<th>Mode</th>
<th>ADMD</th>
<th>ACC and CNT</th>
<th>Bit Clear Conditions</th>
<th>Value after Trigger completion</th>
<th>Threshold Operations</th>
<th>Interrupt</th>
<th>ADAOV</th>
<th>FLTR</th>
<th>CNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic</td>
<td>0</td>
<td>ACC and CNT</td>
<td>ADACLR = 1</td>
<td>Unchanged</td>
<td>Unchanged</td>
<td>No</td>
<td>Every Sample</td>
<td>If threshold=true</td>
<td>N/A</td>
</tr>
<tr>
<td>Accumulate</td>
<td>1</td>
<td>ACC and CNT</td>
<td>ADACLR = 1</td>
<td>S + ACC or (S2-S1) + ACC</td>
<td>If (CNT=0xFF): CNT, otherwise: CNT+1</td>
<td>No</td>
<td>Every Sample</td>
<td>If threshold=true</td>
<td>ACC Overflow</td>
</tr>
<tr>
<td>Average</td>
<td>2</td>
<td>ACC and CNT</td>
<td>ADACLR = 1 or CNT&gt;=RPT at GO or retrigger</td>
<td>S + ACC or (S2-S1) + ACC</td>
<td>If (CNT=0xFF): CNT, otherwise: CNT+1</td>
<td>No</td>
<td>If CNT&gt;=RPT</td>
<td>If threshold=true</td>
<td>ACC Overflow</td>
</tr>
<tr>
<td>Burst Average</td>
<td>3</td>
<td>ACC and CNT</td>
<td>ADACLR = 1 or GO set or retrigger</td>
<td>Each repetition: same as Average End with sum of all samples</td>
<td>Each repetition: same as Average End with CNT=RPT</td>
<td>Repeat while CNT&lt;RPT</td>
<td>If CNT&gt;=RPT</td>
<td>If threshold=true</td>
<td>ACC Overflow</td>
</tr>
<tr>
<td>Low-pass Filter</td>
<td>4</td>
<td>ACC and CNT</td>
<td>ADACLR = 1</td>
<td>S+ACC-ACC/2ADCRS or (S2-S1)+ACC/2ADCRS</td>
<td>Count up, stop counting when CNT = 0xFF</td>
<td>No</td>
<td>If CNT&gt;=RPT</td>
<td>If threshold=true</td>
<td>ACC Overflow</td>
</tr>
</tbody>
</table>

**Note:** S1 and S2 are abbreviations for Sample 1 and Sample 2, respectively. When ADDSEN = 0, S1 = ADRES; When ADDSEN = 1, S1 = PREV and S2 = ADRES.
37.6.1 DIGITAL FILTER/AVERAGE

The digital filter/average module consists of an accumulator with data feedback options, and control logic to determine when threshold tests need to be applied. The accumulator is a 16-bit wide register which can be accessed through the ADACC:ADACCL register pair.

Upon each trigger event (the GO bit set or external event trigger), the ADC conversion result is added to the accumulator. If the accumulated result exceeds \(2^{(\text{accumulator width})} - 1 = 2^{18} = 262143\), the overflow bit ADAOV in the ADSTAT register is set.

The number of samples to be accumulated is determined by the RPT (A/D Repeat Setting) register. Each time a sample is added to the accumulator, the ADCNT register is incremented. Once RPT samples are accumulated (CNT = RPT), an Accumulator Clear command can be issued by the software by setting the ADACLR bit in the ADCON2 register. Setting the ADACLR bit will also clear the ADAOV (accumulator overflow) bit in the ADSTAT register, as well as the ADCNT register. The ADACLR bit is cleared by the hardware when accumulator clearing action is complete.

**Note:** When ADC is operating from FRC, five FRC clock cycles are required to execute the ACC clearing operation.

The ADCRS <2:0> bits in the ADCON2 register control the data shift on the accumulator result, which effectively divides the value in accumulator (ADACC:ADACCH:ADACCL) register pair. For the Accumulate mode of the digital filter, the shift provides a simple scaling operation. For the Average/Burst Average mode, the shift bits are used to determine the number of logical right shifts to be performed on the accumulated result. For the Low-pass Filter mode, the shift is an integral part of the filter, and determines the cut-off frequency of the filter. Table 37-3 shows the -3 dB cut-off frequency in \(\omega_T\) (radians) and the highest signal attenuation obtained by this filter at Nyquist frequency (\(\omega_T = \pi\)).

---

**TABLE 37-3: LOW-PASS FILTER -3 dB CUT-OFF FREQUENCY**

<table>
<thead>
<tr>
<th>ADCRS</th>
<th>(\omega_T) (radians) @ -3 dB Frequency</th>
<th>dB @ (F_{\text{Nyquist}}=1/(2T))</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.72</td>
<td>-9.5</td>
</tr>
<tr>
<td>2</td>
<td>0.284</td>
<td>-16.9</td>
</tr>
<tr>
<td>3</td>
<td>0.134</td>
<td>-23.5</td>
</tr>
<tr>
<td>4</td>
<td>0.065</td>
<td>-29.8</td>
</tr>
<tr>
<td>5</td>
<td>0.032</td>
<td>-36.0</td>
</tr>
<tr>
<td>6</td>
<td>0.016</td>
<td>-42.0</td>
</tr>
<tr>
<td>7</td>
<td>0.0078</td>
<td>-48.1</td>
</tr>
</tbody>
</table>

37.6.2 BASIC MODE

Basic mode (ADMD = 000) disables all additional computation features. In this mode, no accumulation occurs but threshold error comparison is performed. Double sampling, Continuous mode, and all CVD features are still available, but no features involving the digital filter/average features are used.

37.6.3 ACCUMULATE MODE

In Accumulate mode (ADMD = 001), after every conversion, the ADC result is added to the ADACC register. The ADACC register is right-shifted by the value of the ADCRS bits in the ADCON2 register. This right-shifted value is copied into the ADFLT register. The Formatting mode does not affect the right-justification of the ACC value. Upon each sample, CNT is also incremented, incrementing the number of samples accumulated. After each sample and accumulation, the ACC value has a threshold comparison performed on it (see Section 37.6.7 “Threshold Comparison”) and the ADTIF interrupt may trigger.

---

37.6.4 AVERAGE MODE

In Average mode (ADMD = 010), the ADACC registers accumulate with each ADC sample, much as in Accumulate mode, and the ADCNT register increments with each sample. The ADFLT register is also updated with the right-shifted value of the ADACC register. The value of the ADCRS bits governs the number of right shifts. However, in Average mode, the threshold comparison is performed upon CNT being greater than or equal to a user-defined RPT value. In this mode when RPT = \(2^{\text{CNT}}\), then the final accumulated value will be divided by number of samples, allowing for a threshold comparison operation on the average of all gathered samples.
37.6.5 BURST AVERAGE MODE

The Burst Average mode (ADMD = 011) acts the same as the Average mode in most respects. The one way it differs is that it continuously retriggers ADC sampling until the CNT value is greater than or equal to RPT, even if Continuous Sampling mode (see Section 37.6.8 “Continuous Sampling mode”) is not enabled. This allows for a threshold comparison on the average of a short burst of ADC samples.

37.6.6 LOW-PASS FILTER MODE

The Low-pass Filter mode (ADMD = 100) acts similarly to the Average mode in how it handles samples (accumulates samples until CNT value greater than or equal to RPT, then triggers threshold comparison), but instead of a simple average, it performs a low-pass filter operation on all of the samples, reducing the effect of high-frequency noise on the average, then performs a threshold comparison on the results. (see Table 37-2 for a more detailed description of the mathematical operation). In this mode, the ADCRS bits determine the cut-off frequency of the low-pass filter (as demonstrated by Table 37-3).

37.6.7 THRESHOLD COMPARISON

At the end of each computation:
- The conversion results are latched and held stable at the end-of-conversion.
- The error is calculated based on a difference calculation which is selected by the ADCALC<2:0> bits in the ADCON3 register. The value can be one of the following calculations (see Register 37-4 for more details):
  - The first derivative of single measurements
  - The CVD result in CVD mode
  - The current result vs. a setpoint
  - The current result vs. the filtered/average result
  - The first derivative of the filtered/average value
  - Filtered/average value vs. a setpoint
- The result of the calculation (ERR) is compared to the upper and lower thresholds, UTH<ADUTHH:ADUTHL> and LTH<ADLTHH:ADLTHL> registers, to set the ADUTHR and ADLTHR flag bits. The threshold logic is selected by ADTMD<2:0> bits in the ADCON3 register. The threshold trigger option can be one of the following:
  - Never interrupt
  - Error is less than lower threshold
  - Error is greater than or equal to lower threshold
  - Error is between thresholds (inclusive)
  - Error is outside of thresholds
  - Error is less than or equal to upper threshold
  - Error is greater than upper threshold
- Always interrupt regardless of threshold test results
- If the threshold condition is met, the threshold interrupt flag ADTIF is set.

**Note 1:** The threshold tests are signed operations.

**Note 2:** If ADAOV is set, a threshold interrupt is signaled.

37.6.8 CONTINUOUS SAMPLING MODE

Setting the CONT bit in the ADCON0 register automatically retriggers a new conversion cycle after updating the ADACC register. The GO bit remains set and retriggereing occurs automatically.

If ADSOI = 1, a threshold interrupt condition will clear GO and the conversions will stop.

37.6.9 DOUBLE SAMPLE CONVERSION

Double sampling is enabled by setting the ADDSEN bit of the ADCON1 register. When this bit is set, two conversions are required before the module will calculate threshold error (each conversion must still be triggered separately). The first conversion will set the ADMATH bit of the ADSTAT register and update ADACC, but will not calculate ERR or trigger ADTIF.

When the second conversion completes, the first value is transferred to PREV (depending on the setting of ADPSIS) and the value of the second conversion is placed into ADRES. Only upon the completion of the second conversion is ERR calculated and ADTIF triggered (depending on the value of ADCALC).
### 37.7 Register Definitions: ADC Control

**REGISTER 37-1: ADCON0: ADC CONTROL REGISTER 0**

<table>
<thead>
<tr>
<th>bit</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R/W/HC-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ON</td>
<td>CONT</td>
<td>—</td>
<td>CS</td>
<td>—</td>
<td>FM</td>
<td>—</td>
<td>GO</td>
</tr>
<tr>
<td>0</td>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **’1’** = Bit is set
- **’0’** = Bit is cleared
- **HC** = Bit is cleared by hardware

#### bit 7

**ON:** ADC Enable bit

- 1 = ADC is enabled
- 0 = ADC is disabled

#### bit 6

**CONT:** ADC Continuous Operation Enable bit

- 1 = GO is retriggered upon completion of each conversion trigger until ADTIF is set (if ADSOI is set) or until GO is cleared (regardless of the value of ADSOI)
- 0 = ADC is cleared upon completion of each conversion trigger

#### bit 5

**Unimplemented:** Read as '0'

#### bit 4

**CS:** ADC Clock Selection bit

- 1 = Clock supplied from FRC dedicated oscillator
- 0 = Clock supplied by Fosc, divided according to ADCLK register

#### bit 3

**Unimplemented:** Read as '0'

#### bit 2

**FM:** ADC results Format/alignment Selection

- 1 = ADRES and PREV data are right-justified
- 0 = ADRES and PREV data are left-justified, zero-filled

#### bit 1

**Unimplemented:** Read as '0'

#### bit 0

**GO:** ADC Conversion Status bit(1)

- 1 = ADC conversion cycle in progress. Setting this bit starts an ADC conversion cycle. The bit is cleared by hardware as determined by the CONT bit
- 0 = ADC conversion completed/not in progress

**Note 1:** This bit requires ON bit to be set.

**Note 2:** If cleared by software while a conversion is in progress, the results of the conversion up to this point will be transferred to ADRES and the state machine will be reset, but the ADIF interrupt flag bit will not be set; filter and threshold operations will not be performed.
REGISTER 37-2: ADCON1: ADC CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPOL</td>
<td>IPEN</td>
<td>GPOL</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>DSEN</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

bit 7  PPOL: Precharge Polarity bit
If PRE>0x00:

<table>
<thead>
<tr>
<th>PPOL</th>
<th>Action During 1st Precharge Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Connected to Vdd</td>
</tr>
<tr>
<td>0</td>
<td>Connected to Vss</td>
</tr>
</tbody>
</table>

Otherwise:
The bit is ignored

bit 6  IPEN: A/D Inverted Precharge Enable bit
If DSEN = 1
1 = The precharge and guard signals in the second conversion cycle are the opposite polarity of the first cycle
0 = Both Conversion cycles use the precharge and guards specified by ADPPOL and ADGPOL

Otherwise:
The bit is ignored

bit 5  GPOL: Guard Ring Polarity Selection bit
1 = ADC guard Ring outputs start as digital high during Precharge stage
0 = ADC guard Ring outputs start as digital low during Precharge stage

bit 4-1  Unimplemented: Read as ‘0’

bit 0  DSEN: Double-sample enable bit
1 = Two conversions are performed on each trigger. Data from the first conversion appears in PREV
0 = One conversion is performed for each trigger
## REGISTER 37-3: ADCON2: ADC CONTROL REGISTER 2

<table>
<thead>
<tr>
<th>PSIS</th>
<th>CRS&lt;2:0&gt;</th>
<th>ACLR</th>
<th>MD&lt;2:0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets

- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **HC** = Bit is cleared by hardware

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’

**Legend:**

- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets

**Legend:**

- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

**Legend:**

- **HC** = Bit is cleared by hardware

**Legend:**

- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets

**Legend:**

- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

**Legend:**

- **HC** = Bit is cleared by hardware

---

**bit 7**

**PSIS:** ADC Previous Sample Input Select bits

- **0** = PREV is the RES value at start-of-conversion
- **1** = PREV is the FLTR value at start-of-conversion

---

**bit 6-4**

**CRS<2:0>:** ADC Accumulated Calculation Right Shift Select bits

- If ADMD = **100**:
  - Low-pass filter time constant is $2^{ADCRS}$, filter gain is 1:1
- If ADMD = **001**, **010**, or **011**:
  - The accumulated value is right-shifted by CRS (divided by $2^{ADCRS}$) \(^{1,2}\)
- Otherwise:
  - Bits are ignored

---

**bit 3**

**ACLR:** A/D Accumulator Clear Command bit\(^{(3)}\)

- **1** = ACC, AOV and CNT registers are cleared
- **0** = Clearing action is complete (or not started)

---

**bit 2-0**

**MD<2:0>:** ADC Operating Mode Selection bits\(^{(4)}\)

- **111-101** = Reserved
- **100** = Low-pass Filter mode
- **011** = Burst Average mode
- **010** = Average mode
- **001** = Accumulate mode
- **000** = Basic mode

---

**Note 1:** To correctly calculate an average, the number of samples (set in RPT) must be $2^{ADCRS}$.

**Note 2:** ADCRS = **3'b111** is a reserved option.

**Note 3:** This bit is cleared by hardware when the accumulator operation is complete; depending on oscillator selections, the delay may be many instructions.

**Note 4:** See Table 37-2 for Full mode descriptions.
REGISTER 37-4: ADCON3: ADC CONTROL REGISTER 3

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6-4</th>
<th>CALC&lt;2:0&gt;</th>
<th>SOI</th>
<th>TMD&lt;2:0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>U</td>
<td>CALC&lt;2:0&gt;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **HC** = Bit is cleared by hardware

**bit 7**: Unimplemented: Read as ‘0’

**bit 6-4**: CALC<2:0>: ADC Error Calculation Mode Select bits

<table>
<thead>
<tr>
<th>CALC</th>
<th>DSEN = 0 Single-Sample Mode</th>
<th>DSEN = 1 CVD Double-Sample Mode(1)</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>111</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>110</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>101</td>
<td>FLTR-STPT</td>
<td>FLTR-STPT</td>
<td>Average/filtered value vs. setpoint</td>
</tr>
<tr>
<td>100</td>
<td>PREV-FLTR</td>
<td>PREV-FLTR</td>
<td>First derivative of filtered value(3) (negative)</td>
</tr>
<tr>
<td>011</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>010</td>
<td>RES-FLTR</td>
<td>(RES-PREV)-FLTR</td>
<td>Actual result vs. averaged/filtered value</td>
</tr>
<tr>
<td>001</td>
<td>RES-STPT</td>
<td>(RES-PREV)-STPT</td>
<td>Actual result vs.setpoint</td>
</tr>
<tr>
<td>000</td>
<td>RES-PREV</td>
<td>RES-PREV</td>
<td>First derivative of single measurement(2)</td>
</tr>
</tbody>
</table>

**bit 3**: SOI: ADC Stop-on-Interrupt bit

If **CONT = 1**:  
1 = GO is cleared when the threshold conditions are met, otherwise the conversion is retriggered  
0 = GO is not cleared by hardware, must be cleared by software to stop retriggers

**bit 2-0**: TMD<2:0>: Threshold Interrupt Mode Select bits

| 111   | Interrupt regardless of threshold test results |
| 110   | Interrupt if ERR>UTH             |
| 101   | Interrupt if ERR<UTH             |
| 100   | Interrupt if ERR<UTH or ERR>UTH  |
| 011   | Interrupt if ERR>UTH and ERR<UTH |
| 010   | Interrupt if ERR>LTH             |
| 001   | Interrupt if ERR<LTH             |
| 000   | Never interrupt                  |

**Note 1**: When PSIS = 0, the value of (RES-PREV) is the value of (S2-S1) from Table 37-2.

**2**: When PSIS = 0

**3**: When PSIS = 1.
REGISTER 37-5: ADSTAT: ADC STATUS REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>AOV</td>
<td>UTHR</td>
<td>LTHR</td>
<td>MATH</td>
<td>Unimplemented</td>
<td>STAT&lt;2:0&gt;</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets

- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- HS/HC = Bit is set/cleared by hardware

Legend:
- AOV: ADC Accumulator Overflow bit
  - 1 = ADC accumulator or ERR calculation have overflowed
  - 0 = ADC accumulator and ERR calculation have not overflowed

- UTHR: ADC Module Greater-than Upper Threshold Flag bit
  - 1 = ERR > UTH
  - 0 = ERR ≤ UTH

- LTHR: ADC Module Less-than Lower Threshold Flag bit
  - 1 = ERR < LTH
  - 0 = ERR ≥ LTH

- MATH: ADC Module Computation Status bit
  - 1 = Registers ACC, FLTR, UTH, LTH and the AOV bit are updating or have already updated
  - 0 = Associated registers/bits have not changed since this bit was last cleared

- Unimplemented: Read as ‘0’

- STAT<2:0>: ADC Module Cycle Multistage Status bits(1)
  - 111 = ADC module is in 2nd conversion stage
  - 110 = ADC module is in 2nd acquisition stage
  - 101 = ADC module is in 2nd precharge stage
  - 100 = Not used
  - 011 = ADC module is in 1st conversion stage
  - 010 = ADC module is in 1st acquisition stage
  - 001 = ADC module is in 1st precharge stage
  - 000 = ADC module is not converting

Note 1: If CS = 1, and FOSC<FRC, these bits may be invalid.
### REGISTER 37-6:  ADCLK: ADC CLOCK SELECTION REGISTER

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>---</td>
<td>---</td>
<td>---------</td>
<td>---------</td>
<td>---------</td>
<td>---------</td>
<td>---------</td>
<td>---------</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>CS&lt;5:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

- **bit 7-6:** Unimplemented: Read as ‘0’
- **bit 5-0:** CS<5:0>: ADC Conversion Clock Select bits
  - 111111 = Fosc/128
  - 111110 = Fosc/126
  - 111101 = Fosc/124
  - ...
  - 000000 = Fosc/2

### REGISTER 37-7:  ADREF: ADC REFERENCE SELECTION REGISTER

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---------</td>
<td>---------</td>
<td>---------</td>
<td>---------</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>NREF</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>PREF&lt;1:0&gt;</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

- **bit 7-5:** Unimplemented: Read as ‘0’
- **bit 4:** NREF: ADC Negative Voltage Reference Selection bit
  - 1 = VREF- is connected to external VREF-
  - 0 = VREF- is connected to VSS
- **bit 3-2:** Unimplemented: Read as ‘0’
- **bit 1-0:** PREF: ADC Positive Voltage Reference Selection bits
  - 11 = VREF+ is connected to internal Fixed Voltage Reference (FVR) module
  - 10 = VREF+ is connected to external VREF+
  - 01 = Reserved
  - 00 = VREF+ is connected to VDD
**REGISTER 37-8: ADPCH: ADC POSITIVE CHANNEL SELECTION REGISTER**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ADPCH&lt;5:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- \( \text{R} = \) Readable bit
- \( \text{W} = \) Writable bit
- \( \text{U} = \) Unimplemented bit, read as ‘0’
- \( u = \) Bit is unchanged
- \( x = \) Bit is unknown
- \( -n/n = \) Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7-6**
- Unimplemented: Read as ‘0’

**bit 5-0**
- ADPCH<5:0>: ADC Positive Input Channel Selection bits

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>111111</td>
<td>Fixed Voltage Reference (FVR)(^{(2)})</td>
</tr>
<tr>
<td>111110</td>
<td>DAC1 output(^{(1)})</td>
</tr>
<tr>
<td>111101</td>
<td>Temperature Indicator(^{(3)})</td>
</tr>
<tr>
<td>111100</td>
<td>AVss (Analog Ground)</td>
</tr>
<tr>
<td>111011</td>
<td>Reserved. No channel connected.</td>
</tr>
<tr>
<td>010111</td>
<td>ANC7</td>
</tr>
<tr>
<td>010110</td>
<td>ANC6</td>
</tr>
<tr>
<td>010101</td>
<td>ANC5</td>
</tr>
<tr>
<td>010100</td>
<td>ANC4</td>
</tr>
<tr>
<td>010011</td>
<td>ANC3</td>
</tr>
<tr>
<td>010010</td>
<td>ANC2</td>
</tr>
<tr>
<td>010001</td>
<td>ANC1</td>
</tr>
<tr>
<td>010000</td>
<td>ANC0</td>
</tr>
<tr>
<td>001111</td>
<td>ANB7</td>
</tr>
<tr>
<td>001110</td>
<td>ANB6</td>
</tr>
<tr>
<td>001101</td>
<td>ANB5</td>
</tr>
<tr>
<td>001100</td>
<td>ANB4</td>
</tr>
<tr>
<td>001011</td>
<td>ANB3</td>
</tr>
<tr>
<td>001010</td>
<td>ANB2</td>
</tr>
<tr>
<td>001001</td>
<td>ANB1</td>
</tr>
<tr>
<td>001000</td>
<td>ANB0</td>
</tr>
<tr>
<td>000111</td>
<td>ANA7</td>
</tr>
<tr>
<td>000110</td>
<td>ANA6</td>
</tr>
<tr>
<td>000101</td>
<td>ANA5</td>
</tr>
<tr>
<td>000100</td>
<td>ANA4</td>
</tr>
<tr>
<td>000011</td>
<td>ANA3</td>
</tr>
<tr>
<td>000010</td>
<td>ANA2</td>
</tr>
<tr>
<td>000001</td>
<td>ANA1</td>
</tr>
<tr>
<td>000000</td>
<td>ANA0</td>
</tr>
</tbody>
</table>

**Note**
1. See Section 38.0 “5-Bit Digital-to-Analog Converter (DAC) Module” for more information.
2. See Section 35.0 “Fixed Voltage Reference (FVR)” for more information.
3. See Section 36.0 “Temperature Indicator Module” for more information.
REGISTER 37-9: ADPREL: ADC PRECHARGE TIME CONTROL REGISTER (LOW BYTE)

<table>
<thead>
<tr>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>0/0</td>
<td>0/0</td>
<td>0/0</td>
<td>0/0</td>
<td>0/0</td>
<td>0/0</td>
<td>0/0</td>
<td>0/0</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- n/n = Value at POR and BOR/Value at all other Resets

**PRE<7:0>: Precharge Time Select bits**
- See Table 37-4.

REGISTER 37-10: ADPREH: ADC PRECHARGE TIME CONTROL REGISTER (HIGH BYTE)

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0/0</td>
<td>0/0</td>
<td>0/0</td>
<td>0/0</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- n/n = Value at POR and BOR/Value at all other Resets

**Unimplemented:** Read as ‘0’

**PRE<12:8>: Precharge Time Select bits**
- See Table 37-4.

**Note:** If PRE is not equal to ‘0’, then ADACQ = b’00000000 means Acquisition time is 256 clocks of the selected ADC clock.

**TABLE 37-4: PRECHARGE TIME**

<table>
<thead>
<tr>
<th>ADPRE</th>
<th>Precharge time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1111 1111 1111</td>
<td>8191 clocks of the selected ADC clock</td>
</tr>
<tr>
<td>1 1111 1111 1110</td>
<td>8190 clocks of the selected ADC clock</td>
</tr>
<tr>
<td>1 1111 1111 1101</td>
<td>8189 clocks of the selected ADC clock</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0 0000 0000 0010</td>
<td>2 clocks of the selected ADC clock</td>
</tr>
<tr>
<td>0 0000 0000 0001</td>
<td>1 clock of the selected ADC clock</td>
</tr>
<tr>
<td>0 0000 0000 0000</td>
<td>Not included in the data conversion cycle</td>
</tr>
</tbody>
</table>
REGISTER 37-11:  ADACQL: ADC ACQUISITION TIME CONTROL REGISTER (LOW BYTE)

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ACQ<7:0>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared

bit 7-0  ACQ<7:0>: Acquisition (charge share time) Select bits
See Table .

REGISTER 37-12:  ADACQH: ADC ACQUISITION TIME CONTROL REGISTER (HIGH BYTE)

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

— — — ACQ<12:8>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared

bit 7-5  Unimplemented: Read as ‘0’
bit 4-0  ACQ<12:8>: Acquisition (charge share time) Select bits
See Table .

TABLE 37-5:  ACQUISITION TIME

<table>
<thead>
<tr>
<th>ADACQ</th>
<th>Acquisition time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1111 1111 1111</td>
<td>8191 clocks of the selected ADC clock</td>
</tr>
<tr>
<td>1 1111 1111 1110</td>
<td>8190 clocks of the selected ADC clock</td>
</tr>
<tr>
<td>1 1111 1111 1101</td>
<td>8189 clocks of the selected ADC clock</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0 0000 0000 0010</td>
<td>2 clocks of the selected ADC clock</td>
</tr>
<tr>
<td>0 0000 0000 0001</td>
<td>1 clock of the selected ADC clock</td>
</tr>
<tr>
<td>0 0000 0000 0000</td>
<td>Not included in the data conversion cycle(1)</td>
</tr>
</tbody>
</table>

Note 1:  If ADPRE is not equal to ‘0’, then ADACQ = 0b0_0000_0000_0000 means Acquisition time is 8192 clocks of the selected ADC clock.
**REGISTER 37-13: ADCAP: ADC ADDITIONAL SAMPLE CAPACITOR SELECTION REGISTER**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ADCAP&lt;4:0&gt;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7-5**  **Unimplemented:** Read as ‘0’

**bit 4-0**  **ADCAP<4:0>: ADC Additional Sample Capacitor Selection bits**

11111 = 31 pF
11110 = 30 pF
11101 = 29 pF

00011 = 3 pF
00010 = 2 pF
00001 = 1 pF
00000 = No additional capacitance

**REGISTER 37-14: ADRPT: ADC REPEAT SETTING REGISTER**

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RPT&lt;7:0&gt;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7-0**  **RPT<7:0>: ADC Repeat Threshold bits**

Counts the number of times that the ADC has been triggered and is used along with CNT to determine when the error threshold is checked when the computation is Low-pass Filter, Burst Average, or Average modes. See Table 37-2 for more details.
**REGISTER 37-15: ADCNT: ADC REPEAT COUNTER REGISTER**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Legend</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>CNT&lt;7:0&gt;</td>
<td>R = Readable bit, W = Writable bit, U = Unimplemented bit, read as ‘0’, u = Bit is unchanged, x = Bit is unknown, ‘1’ = Bit is set, ‘0’ = Bit is cleared</td>
</tr>
</tbody>
</table>

bit 7-0 **CNT<7:0>:** ADC Repeat Count bits

Determines the number of times that the ADC is triggered before the threshold is checked when the computation is Low-pass Filter, Burst Average, or Average modes. See Table 37-2 for more details.

**REGISTER 37-16: ADFLTRH: ADC FILTER HIGH BYTE REGISTER**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Legend</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>FLTR&lt;15:8&gt;</td>
<td>R = Readable bit, W = Writable bit, U = Unimplemented bit, read as ‘0’, u = Bit is unchanged, x = Bit is unknown, ‘1’ = Bit is set, ‘0’ = Bit is cleared</td>
</tr>
</tbody>
</table>

bit 7-0 **FLTR<15:8>:** ADC Filter Output Most Significant bits

In Accumulate, Average, and Burst Average mode, this is equal to ACC right shifted by the ADCRS bits of ADCON2. In LPF mode, this is the output of the Low-pass Filter.

**REGISTER 37-17: ADFLTRL: ADC FILTER LOW BYTE REGISTER**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Legend</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>FLTR&lt;7:0&gt;</td>
<td>R = Readable bit, W = Writable bit, U = Unimplemented bit, read as ‘0’, u = Bit is unchanged, x = Bit is unknown, ‘1’ = Bit is set, ‘0’ = Bit is cleared</td>
</tr>
</tbody>
</table>

bit 7-0 **FLTR<7:0>:** ADC Filter Output Least Significant bits

In Accumulate, Average, and Burst Average mode, this is equal to ACC right shifted by the ADCRS bits of ADCON2. In LPF mode, this is the output of the Low-pass Filter.
REGISTER 37-18: ADRESH: ADC RESULT REGISTER HIGH, FM = 0

<table>
<thead>
<tr>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADRES&lt;11:4&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| bit 7 | bit 0 |

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared

bit 7-0  ADRES<11:4>: ADC Result Register bits
Upper eight bits of 12-bit conversion result.

REGISTER 37-19: ADRESL: ADC RESULT REGISTER LOW, FM = 0

<table>
<thead>
<tr>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADRES&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| bit 7 | bit 0 |

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared

bit 7-4  ADRES<3:0>: ADC Result Register bits. Lower four bits of 12-bit conversion result.
bit 3-0  Reserved
REGISTER 37-20: ADRESH: ADC RESULT REGISTER HIGH, FM = 1

<table>
<thead>
<tr>
<th></th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

ADRES<11:8>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- n/n = Value at POR and BOR/Value at all other Resets

bit 7-4 
Reserved

bit 3-0 
**ADRES<11:8>:** ADC Sample Result bits. Upper four bits of 12-bit conversion result.

REGISTER 37-21: ADRESL: ADC RESULT REGISTER LOW, FM = 1

<table>
<thead>
<tr>
<th></th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

ADRES<7:0>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- n/n = Value at POR and BOR/Value at all other Resets

bit 7-0 
**ADRES<7:0>:** ADC Result Register bits. Lower eight bits of 12-bit conversion result.
REGISTER 37-22: ADPREVH: ADC PREVIOUS RESULT REGISTER

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th>PREV&lt;15:8&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>R-x</td>
<td>R-x</td>
</tr>
<tr>
<td>R-x</td>
<td>R-x</td>
</tr>
<tr>
<td>R-x</td>
<td>R-x</td>
</tr>
<tr>
<td>R-x</td>
<td>R-x</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ’1’ = Bit is set
- ’0’ = Bit is cleared

bit 7-0  PREV<15:8>: Previous ADC Results bits
- If ADPSIS = 1:
  - Upper byte of FLTR at the start of current ADC conversion
- If ADPSIS = 0:
  - Upper bits of ADRES at the start of current ADC conversion

Note 1: If ADPSIS = 0, ADPREVH and ADPREVL are formatted the same way as ADRES is, depending on the FM bit.

REGISTER 37-23: ADPREVL: ADC PREVIOUS RESULT REGISTER

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th>PREV&lt;7:0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>R-x</td>
<td>R-x</td>
</tr>
<tr>
<td>R-x</td>
<td>R-x</td>
</tr>
<tr>
<td>R-x</td>
<td>R-x</td>
</tr>
<tr>
<td>R-x</td>
<td>R-x</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ’1’ = Bit is set
- ’0’ = Bit is cleared

bit 7-0  PREV<7:0>: Previous ADC Results bits
- If ADPSIS = 1:
  - Lower byte of FLTR at the start of current ADC conversion
- If ADPSIS = 0:
  - Lower bits of ADRES at the start of current ADC conversion

Note 1: If ADPSIS = 0, ADPREVH and ADPREVL are formatted the same way as ADRES is, depending on the FM bit.
REGISTER 37-24: ADACCU: ADC ACCUMULATOR REGISTER UPPER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
</tr>
<tr>
<td>bit 7-2</td>
<td>Unimplemented: Read as ‘0’</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 1-0</td>
<td>ACC&lt;17:16&gt;: ADC Accumulator MSB. Upper two bits of accumulator value. See Table 37-2 for more details.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- **R**: Readable bit
- **W**: Writable bit
- **U**: Unimplemented bit, read as ‘0’
- **u**: Bit is unchanged
- **x**: Bit is unknown
- **-n/n**: Value at POR and BOR/Value at all other Resets
- **‘1’**: Bit is set
- **‘0’**: Bit is cleared

REGISTER 37-25: ADACCH: ADC ACCUMULATOR REGISTER HIGH

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>ACC&lt;15:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7-0</td>
<td>ACC&lt;15:8&gt;: ADC Accumulator middle bits. Middle eight bits of accumulator value. See Table 37-2 for more details.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- **R**: Readable bit
- **W**: Writable bit
- **U**: Unimplemented bit, read as ‘0’
- **u**: Bit is unchanged
- **x**: Bit is unknown
- **-n/n**: Value at POR and BOR/Value at all other Resets
- **‘1’**: Bit is set
- **‘0’**: Bit is cleared

REGISTER 37-26: ADACCL: ADC ACCUMULATOR REGISTER LOW

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>R/W-x/x</td>
<td>ACC&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7-0</td>
<td>ACC&lt;7:0&gt;: ADC Accumulator LSB. Lower eight bits of accumulator value. See Table 37-2 for more details.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- **R**: Readable bit
- **W**: Writable bit
- **U**: Unimplemented bit, read as ‘0’
- **u**: Bit is unchanged
- **x**: Bit is unknown
- **-n/n**: Value at POR and BOR/Value at all other Resets
- **‘1’**: Bit is set
- **‘0’**: Bit is cleared
## REGISTER 37-27: ADSTPTH: ADC THRESHOLD SETPOINT REGISTER HIGH

<table>
<thead>
<tr>
<th>Bit</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>STPT&lt;15:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

**bit 7-0 STPT<15:8>:** ADC Threshold Setpoint MSB. Upper byte of ADC threshold setpoint, depending on ADCALC, may be used to determine ERR, see Register 37-29 for more details.

## REGISTER 37-28: ADSTPTL: ADC THRESHOLD SETPOINT REGISTER LOW

<table>
<thead>
<tr>
<th>Bit</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>STPT&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

**bit 7-0 STPT<7:0>:** ADC Threshold Setpoint LSB. Lower byte of ADC threshold setpoint, depending on ADCALC, may be used to determine ERR, see Register 37-30 for more details.
REGISTER 37-29: ADERRH: ADC SETPOINT ERROR REGISTER HIGH

<table>
<thead>
<tr>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**ERR<15:8>**
- Bit 7-0: ADC Setpoint Error MSB. Upper byte of ADC Setpoint Error. Setpoint Error calculation is determined by CALC bits of ADCON3, see Register 37-4 for more details.

REGISTER 37-30: ADERRL: ADC SETPOINT ERROR LOW BYTE REGISTER

<table>
<thead>
<tr>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**ERR<7:0>**
- Bit 7-0: ADC Setpoint Error LSB. Lower byte of ADC Setpoint Error calculation is determined by CALC bits of ADCON3, see Register 37-4 for more details.

REGISTER 37-31: ADLTHH: ADC LOWER THRESHOLD HIGH BYTE REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**LTH<15:8>**
- Bit 7-0: ADC Lower Threshold MSB. LTH and UTH are compared with ERR to set the ADUTHR and ADLTHR bits of ADSTAT. Depending on the setting of ADTMD, an interrupt may be triggered by the results of this comparison.
REGISTER 37-32: **ADLTHL**: ADC LOWER THRESHOLD LOW BYTE REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTH&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7-0** **LTH<7:0>:** ADC Lower Threshold LSB. LTH and UTH are compared with ERR to set the ADUTHR and ADLTHR bits of ADSTAT. Depending on the setting of ADTMD, an interrupt may be triggered by the results of this comparison.

REGISTER 37-33: **ADUTHH**: ADC UPPER THRESHOLD HIGH BYTE REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>UTH&lt;15:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7-0** **UTH<15:8>:** ADC Upper Threshold MSB. LTH and UTH are compared with ERR to set the ADUTHR and ADLTHR bits of ADSTAT. Depending on the setting of ADTMD, an interrupt may be triggered by the results of this comparison.

REGISTER 37-34: **ADUTHL**: ADC UPPER THRESHOLD LOW BYTE REGISTER

<table>
<thead>
<tr>
<th></th>
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<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>UTH&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7-0** **UTH<7:0>:** ADC Upper Threshold LSB. LTH and UTH are compared with ERR to set the ADUTHR and ADLTHR bits of ADSTAT. Depending on the setting of ADTMD, an interrupt may be triggered by the results of this comparison.
## REGISTER 37-35: ADACT: ADC AUTO-CONVERSION TRIGGER CONTROL REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ACT&lt;4:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-5**

Unimplemented: Read as ‘0’

**bit 4-0**

**ADACT<4:0>: Auto-Conversion Trigger Select Bits**

| 11111 | Reserved, do not use |
| 11110 | Reserved, do not use |
| 11101 | Software write to ADPCH |
| 11100 | Reserved, do not use |
| 11011 | Software read of ADRESH |
| 11010 | Software read of ADERRH |
| 11001 | CLC4_out |
| 11000 | CLC3_out |
| 10111 | CLC2_out |
| 10110 | CLC1_out |
| 10101 | Logical OR of all Interrupt-on-Change Interrupt Flags |
| 10100 | CMP2_out |
| 10111 | CMP1_out |
| 10101 | NCO1_out |
| 10100 | PWM8_out |
| 10001 | PWM7_out |
| 01111 | PWM6_out |
| 01110 | PWM5_out |
| 01101 | CCP4_trigger |
| 01100 | CCP3_trigger |
| 01111 | CCP2_trigger |
| 01110 | CCP1_trigger |
| 01001 | SMT1_trigger |
| 01000 | TMR6_postscaled |
| 00111 | TMR5_overflow |
| 00110 | TMR4_postscaled |
| 00101 | TMR3_overflow |
| 00100 | TMR2_postscaled |
| 00011 | TMR1_overflow |
| 00010 | TMR0_overflow |
| 00001 | Pin selected by ADACTPPS |
| 00000 | External Trigger Disabled |
### REGISTER 37-36: ADCP: ADC CHARGE PUMP CONTROL REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPON</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CPRDY</td>
</tr>
</tbody>
</table>

#### bit 7 CPON: Charge Pump On Control bit
- **1** = Charge Pump On when requested by the ADC
- **0** = Charge Pump Off

#### bit 6-1 Unimplemented: Read as ‘0’

#### bit 0 CPRDY: Charge Pump Ready Status bit
- **1** = Charge Pump is ready
- **0** = Charge Pump is not ready (or never started)

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **HS** = Hardware set
## TABLE 37-6: SUMMARY OF REGISTERS ASSOCIATED WITH ADC

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADCON0</td>
<td>ON</td>
<td>CONT</td>
<td>—</td>
<td>CS</td>
<td>—</td>
<td>FM</td>
<td>—</td>
<td>GO</td>
<td>669</td>
</tr>
<tr>
<td>ADCON1</td>
<td>ADPPOL</td>
<td>ADIPEN</td>
<td>ADGPOL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ADDSEN</td>
<td>670</td>
</tr>
<tr>
<td>ADCON2</td>
<td>ADPSIS</td>
<td>ADCRS&lt;2:0&gt;</td>
<td>ADACL&lt;2:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>MD&lt;2:0&gt;</td>
<td>671</td>
</tr>
<tr>
<td>ADCON3</td>
<td>—</td>
<td>ADcalc&lt;2:0&gt;</td>
<td>ADsoi&lt;2:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ADTMD&lt;2:0&gt;</td>
<td>672</td>
</tr>
<tr>
<td>ADSTAT</td>
<td>ADAOV</td>
<td>ADUTHR</td>
<td>ADLTHR</td>
<td>ADMATH</td>
<td>—</td>
<td>ADSTAT&lt;3:0&gt;</td>
<td>—</td>
<td>—</td>
<td>673</td>
</tr>
<tr>
<td>ADCLK</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CS&lt;5:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>674</td>
</tr>
<tr>
<td>ADREF</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ADNREF</td>
<td>—</td>
<td>—</td>
<td>ADREF&lt;1:0&gt;</td>
<td>674</td>
</tr>
<tr>
<td>ADPCH</td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>ADPCH&lt;5:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>675</td>
</tr>
<tr>
<td>ADPREL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>676</td>
</tr>
<tr>
<td>ADPREH</td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>PRE&lt;12:8&gt;</td>
<td>—</td>
<td>—</td>
<td>676</td>
</tr>
<tr>
<td>ADACQL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ACQ&lt;7:0&gt;</td>
<td>—</td>
<td>—</td>
<td>677</td>
</tr>
<tr>
<td>ADCAP</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ADCAP&lt;4:0&gt;</td>
<td>678</td>
</tr>
<tr>
<td>ADRPT</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>RPT&lt;7:0&gt;</td>
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<td>—</td>
<td>678</td>
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<tr>
<td>ADCNT</td>
<td>—</td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>CNT&lt;7:0&gt;</td>
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</tr>
<tr>
<td>ADFLTRH</td>
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<td>—</td>
<td>—</td>
<td>FLTR&lt;7:0&gt;</td>
<td>—</td>
<td>—</td>
<td>679</td>
</tr>
<tr>
<td>ADLTHH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>LTH&lt;15:8&gt;</td>
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<td>—</td>
<td>679</td>
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<td>ADRESL</td>
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<td>—</td>
<td>—</td>
<td>ADRESH&lt;7:0&gt;</td>
<td>—</td>
<td>—</td>
<td>680, 681</td>
</tr>
<tr>
<td>ADRESH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ADRESH&lt;7:0&gt;</td>
<td>—</td>
<td>—</td>
<td>680, 681</td>
</tr>
<tr>
<td>ADPREVLH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>PREV&lt;15:8&gt;</td>
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<td>—</td>
<td>682</td>
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<td>ADACCL</td>
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<td>—</td>
<td>ACC&lt;15:8&gt;</td>
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<td>—</td>
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<tr>
<td>ADACC</td>
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<td>—</td>
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<td>ACC&lt;7:0&gt;</td>
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<td>—</td>
<td>683</td>
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<tr>
<td>ADSTH</td>
<td>—</td>
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<td>—</td>
<td>ACC&lt;17:16&gt;</td>
<td>683</td>
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<tr>
<td>ADSTTH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>STPT&lt;7:0&gt;</td>
<td>—</td>
<td>—</td>
<td>684</td>
</tr>
<tr>
<td>ADERRL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ERR&lt;7:0&gt;</td>
<td>—</td>
<td>—</td>
<td>684</td>
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<tr>
<td>ADERRH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ERR&lt;15:8&gt;</td>
<td>—</td>
<td>—</td>
<td>685</td>
</tr>
<tr>
<td>ADLTH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>LTH&lt;15:8&gt;</td>
<td>—</td>
<td>—</td>
<td>685</td>
</tr>
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<td>ADUTH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>UTH&lt;15:8&gt;</td>
<td>—</td>
<td>—</td>
<td>686</td>
</tr>
<tr>
<td>ADULTH</td>
<td>—</td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>UTH&lt;7:0&gt;</td>
<td>—</td>
<td>—</td>
<td>686</td>
</tr>
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<td>—</td>
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<td>—</td>
<td>ERR&lt;15:8&gt;</td>
<td>—</td>
<td>—</td>
<td>686</td>
</tr>
<tr>
<td>ADAC</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>685</td>
</tr>
<tr>
<td>ADACP</td>
<td>CPON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>688</td>
</tr>
</tbody>
</table>

**Legend:**  
- = unimplemented read as ‘0’. Shaded cells are not used for the ADC module.
38.0 5-BIT DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 32 selectable output levels.

The positive input source (VSOURCE+) of the DAC can be connected to:
- FVR Buffer
- External VREF+ pin
- VDD supply voltage

The negative input source (VSOURCE-) of the DAC can be connected to:
- External VREF- pin
- Vss

The output of the DAC (DAC1_output) can be selected as a reference voltage to the following:
- Comparator positive input
- ADC input channel
- DAC1OUT1 pin
- DAC1OUT2 pin

The Digital-to-Analog Converter (DAC) can be enabled by setting the EN bit of the DAC1CON0 register.

FIGURE 38-1: DIGITAL-TO-ANALOG CONVERTER BLOCK DIAGRAM

Note 1: The unbuffered DACx_output is provided on the DACxOUT pin(s).
38.1 Output Voltage Selection
The DAC has 32 voltage level ranges. The 32 levels are set with the DATA<4:0> bits of the DAC1CON1 register.
The DAC output voltage can be determined by using Equation 38-1.

38.2 Ratiometric Output Level
The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.
The value of the individual resistors within the ladder can be found in Table 45-16.

38.3 DAC Voltage Reference Output
The unbuffered DAC voltage can be output to the DAC1OUTn pin(s) by setting the respective DACOEn bit(s) of the DAC1CON0 register. Selecting the DAC reference voltage for output on either DAC1OUTn pin automatically overrides the digital output buffer, the weak pull-up and digital input threshold detector functions of that pin.

EQUATION 38-1: DAC OUTPUT VOLTAGE

\[
\text{IF DACEN} = 1 \\
\text{DACx_output} = \left( (V_{REF^+} - V_{REF^-}) \times \frac{\text{DATA}[4:0]}{2^5} \right) + V_{REF^-}
\]

Note: See the DAC1CON0 register for the available VSOURCE+ and VSOURCE- selections.
38.6 Register Definitions: DAC Control

Long bit name prefixes for the DAC peripheral is shown below. Refer to Section 1.3.2.2 “Long Bit Names” for more information.

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Bit Name Prefix</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC1</td>
<td>DAC1</td>
</tr>
</tbody>
</table>

**REGISTER 38-1: DAC1CON0: DAC CONTROL REGISTER**

<table>
<thead>
<tr>
<th>R/R-0/0</th>
<th>U-0</th>
<th>R/R-0/0</th>
<th>R/R-0/0</th>
<th>R/R-0/0</th>
<th>U-0</th>
<th>R/R-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>—</td>
<td>OE1</td>
<td>OE2</td>
<td>PSS&lt;1:0&gt;</td>
<td>—</td>
<td>NSS</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3-2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td></td>
<td></td>
<td></td>
<td>PSS&lt;1:0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>u</td>
<td>x</td>
<td>u</td>
<td>x</td>
<td>u</td>
<td>x</td>
<td>u</td>
</tr>
</tbody>
</table>

**Legend:**

R = Readable bit   W = Writable bit   U = Unimplemented bit, read as '0'
u = Bit is unchanged   x = Bit is unknown   -n/n = Value at POR and BOR/Value at all other Resets

1 = DAC is enabled   0 = DAC is disabled

1 = DAC voltage level is output on the DAC1OUT1 pin   0 = DAC voltage level is disconnected from the DAC1OUT1 pin

1 = DAC voltage level is output on the DAC1OUT2 pin   0 = DAC voltage level is disconnected from the DAC1OUT2 pin

11 = Reserved   10 = FVR buffer 2   01 = VREF+   00 = VDD

1 = VREF-   0 = VSS

**Note 1:** DAC1OUTx output pins are still active.
REGISTER 38-2:  DAC1CON1: DAC DATA REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DATA&lt;4:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

bit 7-5  **Unimplemented:** Read as ‘0’
bit 4-0  DATA<4:0>: Data Input Register for DAC bits

TABLE 38-1:  SUMMARY OF REGISTERS ASSOCIATED WITH THE DAC MODULE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC1CON0</td>
<td>EN</td>
<td>—</td>
<td>OE1</td>
<td>OE2</td>
<td>PSS&lt;1:0&gt;</td>
<td>—</td>
<td>NSS</td>
<td></td>
<td>692</td>
</tr>
<tr>
<td>DAC1CON1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DATA&lt;4:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>693</td>
</tr>
</tbody>
</table>

**Legend:**  — = Unimplemented location, read as ‘0’. Shaded cells are not used with the DAC module.
39.0 COMPARATOR MODULE

Note: The PIC18(L)F25/26K83 devices have two comparators. Therefore, all information in this section refers to both C1 and C2.

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution.

The analog comparator module includes the following features:
• Programmable input selection
• Programmable output polarity
• Rising/falling output edge interrupts

39.1 Comparator Overview

A single comparator is shown in Figure 39-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

FIGURE 39-1: SINGLE COMPARATOR

Note: The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.
FIGURE 39-2: COMPARATOR MODULE SIMPLIFIED BLOCK DIAGRAM

Note 1: When CxON = 0, all multiplexer inputs are disconnected and the Comparator will produce a '0' at the output.
39.2 Comparator Control

Each comparator has two control registers: CMxCON0 and CMxCON1.

The CMxCON0 register (see Register 39-1) contains Control and Status bits for the following:

- Enable
- Output
- Output polarity
- Hysteresis enable
- Timer1 output synchronization

The CMxCON1 register (see Register 39-2) contains Control bits for the following:

- Interrupt on positive/negative edge enables

The CMxPCH and CMxNCH registers are used to select the positive and negative input channels, respectively.

39.2.1 COMPARATOR ENABLE

Setting the EN bit of the CMxCON0 register enables the comparator for operation. Clearing the EN bit disables the comparator resulting in minimum current consumption.

39.2.2 COMPARATOR OUTPUT

The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the CxOUT bit of the CMOUT register.

The comparator output can also be routed to an external pin through the RxyPPS register (Register 17-2). The corresponding TRIS bit must be clear to enable the pin as an output.

39.2.3 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the POL bit of the CMxCON0 register. Clearing the POL bit results in a noninverted output.

Table 39-1 shows the output state versus input conditions, including polarity control.

<table>
<thead>
<tr>
<th>TABLE 39-1: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Condition</td>
</tr>
<tr>
<td>-----------------</td>
</tr>
<tr>
<td>CxVN &gt; CxVP</td>
</tr>
<tr>
<td>CxVN &lt; CxVP</td>
</tr>
<tr>
<td>CxVN &gt; CxVP</td>
</tr>
<tr>
<td>CxVN &lt; CxVP</td>
</tr>
</tbody>
</table>

Note 1: The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.
39.3 Comparator Hysteresis

A selectable amount of separation voltage can be added to the input pins of each comparator to provide a hysteresis function to the overall operation. Hysteresis is enabled by setting the HYS bit of the CMxCON0 register.

See Comparator Specifications in Table 45-15 for more information.

39.3.1 COMPARATOR OUTPUT SYNCHRONIZATION

The output from a comparator can be synchronized with Timer1 by setting the SYNC bit of the CMxCON0 register.

Once enabled, the comparator output is latched on the falling edge of the Timer1 source clock. If a prescaler is used, the CxOUT bit is synchronized with the timer, so that the software sees no ambiguity due to timing. See the Comparator Block Diagram (Figure 39-2) and the Timer1 Block Diagram (Figure 21-1) for more information.

39.4 Comparator Interrupt

An interrupt can be generated for every rising or falling edge of the comparator output.

When either edge detector is triggered and its associated enable bit is set (INTP and/or INTN bits of the CMxCON1 register), the Corresponding Interrupt Flag bit (CxIF bit of the respective PIR register) will be set.

To enable the interrupt, you must set the following bits:

- EN bit of the CMxCON0 register
- CxE bit of the respective PIE register
- INTP bit of the CMxCON1 register (for a rising edge detection)
- INTN bit of the CMxCON1 register (for a falling edge detection)
- GIE bit of the INTCON0 register

The associated interrupt flag bit, CxIF bit of the respective PIR register, must be cleared in software. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

Note: Although a comparator is disabled, an interrupt can be generated by changing the output polarity with the POL bit of the CMxCON0 register, or by switching the comparator on or off with the EN bit of the CMxCON0 register.

39.5 Comparator Positive Input Selection

Configuring the PCH<2:0> bits of the CMxPCH register directs an internal voltage reference or an analog pin to the non-inverting input of the comparator:

- CxIN0+, CxIN1+ analog pin
- DAC output
- FVR (Fixed Voltage Reference)
- VSS (Ground)

See Section 35.0 “Fixed Voltage Reference (FVR)” for more information on the Fixed Voltage Reference module.

See Section 38.0 “5-Bit Digital-to-Analog Converter (DAC) Module” for more information on the DAC input signal.

Any time the comparator is disabled (EN = 0), all comparator inputs are disabled.

39.6 Comparator Negative Input Selection

The NCH<2:0> bits of the CMxNCH register direct an analog input pin and internal reference voltage or analog ground to the inverting input of the comparator:

- CxIN0-, CxIN1-, CxIN2-, CxIN3- analog pin
- FVR (Fixed Voltage Reference)
- Analog Ground

Note: To use CxINy+ and CxINy- pins as analog input, the appropriate bits must be set in the ANSEL register and the corresponding TRIS bits must also be set to disable the output drivers.
39.7 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in Table 45-15 and Table 45-17 for more details.

39.8 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 39-3. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of 10 kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

Note 1: When reading a PORT register, all pins configured as analog inputs will read as a ‘0’. Pins configured as digital inputs will convert as an analog input, according to the input specification.

2: Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

Note 1: See Section 45.0 “Electrical Specifications”.

FIGURE 39-3: ANALOG INPUT MODEL
39.9 CWG1 Auto-Shutdown Source

The output of the comparator module can be used as an auto-shutdown source for the CWG1 module. When the output of the comparator is active and the corresponding WGASxE is enabled, the CWG operation will be suspended immediately (see Section 26.10.1.2 “External Input Source”).

39.10 ADC Auto-Trigger Source

The output of the comparator module can be used to trigger an ADC conversion. When the ADACT register is set to trigger on a comparator output, an ADC conversion will trigger when the Comparator output goes high.

39.11 TMR2/4/6 Reset

The output of the comparator module can be used to reset Timer2. When the TxERS register is appropriately set, the timer will reset when the Comparator output goes high.

39.12 Operation in Sleep Mode

The comparator module can operate during Sleep. The comparator clock source is based on the Timer1 clock source. If the Timer1 clock source is either the system clock (Fosc) or the instruction clock (Fosc/4), Timer1 will not operate during Sleep, and synchronized comparator outputs will not operate.

A comparator interrupt will wake the device from Sleep. The CxIE bits of the respective PIE register must be set to enable comparator interrupts.
39.13 Register Definitions: Comparator Control

Long bit name prefixes for the Comparators are shown in Table 39-2. Refer to Section 1.3.2.2 “Long Bit Names” for more information.

TABLE 39-2:

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Bit Name Prefix</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>C1</td>
</tr>
<tr>
<td>C2</td>
<td>C2</td>
</tr>
</tbody>
</table>

REGISTER 39-1: CMxCON0: COMPARATOR x CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R-0/0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-1</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>OUT</td>
<td>—</td>
<td>POL</td>
<td>—</td>
<td>—</td>
<td>HYS</td>
<td>SYNC</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 7
EN: Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled and consumes no active power

bit 6
OUT: Comparator Output bit
If POL = 0 (noninverted polarity):
1 = CxVP > CxVN
0 = CxVP < CxVN
If POL = 1 (inverted polarity):
1 = CxVP < CxVN
0 = CxVP > CxVN

bit 5
Unimplemented: Read as ‘0’

bit 4
POL: Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 3
Unimplemented: Read as ‘0’

bit 2
Unimplemented: Read as ‘1’

bit 1
HYS: Comparator Hysteresis Enable bit
1 = Comparator hysteresis enabled
0 = Comparator hysteresis disabled

bit 0
SYNC: Comparator Output Synchronous Mode bit
1 = Comparator output to Timer1/3/5 and I/O pin is synchronous to changes on Timer1 clock source.
0 = Comparator output to Timer1/3/5 and I/O pin is asynchronous
Output updated on the falling edge of Timer1/3/5 clock source.
REGISTER 39-2: CMxCON1: COMPARATOR x CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>bit 7-2 Unimplemented: Read as '0'</th>
<th>bit 1 INTP: Comparator Interrupt on Positive-Going Edge Enable bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 = The CxIF interrupt flag will be set upon a positive-going edge of the CxOUT bit</td>
<td></td>
</tr>
<tr>
<td>0 = No interrupt flag will be set on a positive-going edge of the CxOUT bit</td>
<td></td>
</tr>
</tbody>
</table>

bit 0 INTN: Comparator Interrupt on Negative-Going Edge Enable bit
1 = The CxIF interrupt flag will be set upon a negative-going edge of the CxOUT bit
0 = No interrupt flag will be set on a negative-going edge of the CxOUT bit

REGISTER 39-3: CMxNCH: COMPARATOR x INVERTING CHANNEL SELECT REGISTER

<table>
<thead>
<tr>
<th>bit 7-3 Unimplemented: Read as '0'</th>
<th>bit 2-0 NCH&lt;2:0&gt;: Comparator Inverting Input Channel Select bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>111 = Vss</td>
<td></td>
</tr>
<tr>
<td>110 = FVR_Buffer2</td>
<td></td>
</tr>
<tr>
<td>101 = NCH not connected</td>
<td></td>
</tr>
<tr>
<td>100 = NCH not connected</td>
<td></td>
</tr>
<tr>
<td>011 = CxIN3-</td>
<td></td>
</tr>
<tr>
<td>010 = CxIN2-</td>
<td></td>
</tr>
<tr>
<td>001 = CxIN1-</td>
<td></td>
</tr>
<tr>
<td>000 = CxIN0-</td>
<td></td>
</tr>
</tbody>
</table>
**REGISTER 39-4: CMxPCH: COMPARATOR x NON-INVERTING CHANNEL SELECT REGISTER**

<table>
<thead>
<tr>
<th></th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PCH&lt;2:0&gt;</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

- **bit 7** Unimplemented: Read as ‘0’
- **bit 2-0** PCH<2:0>: Comparator Non-Inverting Input Channel Select bits
  - 111 = Vss
  - 110 = FVR_Buffer2
  - 101 = DAC_Output
  - 100 = PCH not connected
  - 011 = PCH not connected
  - 010 = PCH not connected
  - 001 = CxIN1+
  - 000 = CxIN0+

**REGISTER 39-5: CMOUT: COMPARATOR OUTPUT REGISTER**

<table>
<thead>
<tr>
<th></th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R-0/0</th>
<th>R-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>C2OUT</td>
<td>C1OUT</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

- **bit 7-2** Unimplemented: Read as ‘0’
- **bit 1** C2OUT: Mirror copy of C2OUT bit
- **bit 0** C1OUT: Mirror copy of C1OUT bit

**TABLE 39-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARATOR MODULE**

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Reset Values on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMxCON0</td>
<td>EN</td>
<td>OUT</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>HYS</td>
<td>SYNC 700</td>
</tr>
<tr>
<td>CMxCON1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>INTP</td>
<td>INTN 701</td>
</tr>
<tr>
<td>CMxNCH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>NCH&lt;2:0&gt;</td>
<td>701</td>
</tr>
<tr>
<td>CMxPCH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>PCH&lt;2:0&gt;</td>
<td>702</td>
</tr>
<tr>
<td>CMOUT</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>C2OUT C1OUT 702</td>
</tr>
</tbody>
</table>

**Legend:**
- — = unimplemented, read as ‘0’. Shaded cells are unused by the comparator module.
40.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

The PIC18(L)F25/26K83 family of devices has a High/Low-Voltage Detect module (HLVD). This is a programmable circuit that sets both a device voltage trip point and the direction of change from that point (positive going, negative going or both). If the device experiences an excursion past the trip point in that direction, an interrupt flag is set. If the interrupt is enabled, the program execution branches to the interrupt vector address and the software responds to the interrupt.

Complete control of the HLVD module is provided through the HLVDCON0 and HLVDCON1 register. This allows the circuitry to be "turned off" by the user under software control, which minimizes the current consumption for the device.

The module’s block diagram is shown in Figure 40-1.

Since the HLVD can be software enabled through the EN bit, setting and clearing the enable bit does not produce a false HLVD event glitch. Each time the HLVD module is enabled, the circuitry requires some time to stabilize. The RDY bit (HLVDCON0<4>) is a read-only bit used to indicate when the band gap reference voltages are stable.

The module can only generate an interrupt after the module is turned ON and the band gap reference voltages are ready.

The INTH and INTL bits determine the overall operation of the module. When INTH is set, the module monitors for rises in VDD above the trip point set by the HLVDCON1 register. When INTL is set, the module monitors for drops in VDD below the trip point set by the HLVDCON1 register. When both the INTH and INTL bits are set, any changes above or below the trip point set by the HLVDCON1 register can be monitored.

The OUT bit can be read to determine if the voltage is greater than or less than the voltage level selected by the HLVDCON1 register.
40.1 Operation

When the HLVD module is enabled, a comparator uses an internally generated voltage reference as the set point. The set point is compared with the trip point, where each node in the resistor divider represents a trip point voltage. The "trip point" voltage is the voltage level at which the device detects a high or low-voltage event, depending on the configuration of the module.

When the supply voltage is equal to the trip point, the voltage tapped off of the resistor array is equal to the internal reference voltage generated by the voltage reference module. The comparator then generates an interrupt signal by setting the HLVDIF bit.

The trip point voltage is software programmable to any of SEL<3:0> bits (HLVDCON1<3:0>).

FIGURE 40-1: HLVD MODULE BLOCK DIAGRAM
40.2 HLVD Setup

To set up the HLVD module:

1. Select the desired HLVD trip point by writing the value to the SEL<3:0> bits of the HLVDCON1 register.
2. Depending on the application to detect high-voltage peaks or low-voltage drops or both, set the INTH or INTL bit appropriately.
3. Enable the HLVD module by setting the EN bit.
4. Clear the HLVD interrupt flag (PIR2 register), which may have been set from a previous interrupt.
5. If interrupts are desired, enable the HLVD interrupt by setting the HLVDIE in the PIE2 register and GIE bits.

Note: Before changing any module settings (INTH, INTL, SEL<3:0>), first disable the module (EN = 0), make the changes and re-enable the module. This prevents the generation of false HLVD events.

40.3 Current Consumption

When the module is enabled, the HLVD comparator and voltage divider are enabled and consume static current. The total current consumption, when enabled, is specified in electrical specification Parameter D206 (Table 45-3).

Depending on the application, the HLVD module does not need to operate constantly. To reduce current requirements, the HLVD circuitry may only need to be enabled for short periods where the voltage is checked. After such a check, the module could be disabled.

40.4 HLVD Start-up Time

The internal reference voltage of the HLVD module, specified in electrical specification (Table 45-17), may be used by other internal circuitry, such as the programmable Brown-out Reset. If the HLVD or other circuits using the voltage reference are disabled to lower the device's current consumption, the reference voltage circuit will require time to become stable before a low or high-voltage condition can be reliably detected. This start-up time, TFVRST, is an interval that is independent of device clock speed. It is specified in electrical specification (Table 45-17).

The HLVD interrupt flag is not enabled until TFVRST has expired and a stable reference voltage is reached. For this reason, brief excursions beyond the set point may not be detected during this interval (see Figure 40-2 or Figure 40-3).
FIGURE 40-2: LOW-VOLTAGE DETECT OPERATION (INTL = 1)

CASE 1:
- VDD
- HLVDIF
- Enable HLVD
- RDY

HLVDIF may not be Set

Band Gap Reference Voltage is Stable

CASE 2:
- VDD
- HLVDIF
- Enable HLVD
- RDY

Band Gap Reference Voltage is Stable

HLVDIF Cleared in Software,
HLVDIF Remains Set since HLVD Condition still Exists
In many applications, it is desirable to detect a drop below, or rise above, a particular voltage threshold. For example, the HLVD module could be periodically enabled to detect Universal Serial Bus (USB) attach or detach. This assumes the device is powered by a lower voltage source than the USB when detached. An attach would indicate a High-Voltage Detect from, for example, 3.3V to 5V (the voltage on USB) and vice versa for a detach. This feature could save a design a few extra components and an attach signal (input pin).

For general battery applications, Figure 40-4 shows a possible voltage curve. Over time, the device voltage decreases. When the device voltage reaches voltage, $V_A$, the HLVD logic generates an interrupt at time, $T_A$. The interrupt could cause the execution of an Interrupt Service Routine (ISR), which would allow the application to perform “housekeeping tasks” and a controlled shutdown before the device voltage exits the valid operating range at $T_B$. This would give the application a time window, represented by the difference between $T_A$ and $T_B$, to safely exit.
40.6 Operation During Sleep

When enabled, the HLVD circuitry continues to operate during Sleep. If the device voltage crosses the trip point, the HLVDIF bit will be set and the device will wake up from Sleep. Device execution will continue from the interrupt vector address if interrupts have been globally enabled.

40.7 Operation During Idle and Doze Modes

In both Idle and Doze modes, the module is active and events are generated if peripheral is enabled.

40.8 Operation During Freeze

When in Freeze mode, no new event or interrupt can be generated. The state of the LRDY bit is frozen. Register reads and writes through the CPU interface are allowed.

40.9 Effects of a Reset

A device Reset forces all registers to their Reset state. This forces the HLVD module to be turned off.
40.10 Register Definitions: HLVD Control

Long bit name prefixes for the HLVD peripheral is shown in Table 40-1. Refer to Section 1.3.2.2 “Long Bit Names” for more information.

**TABLE 40-1:**

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Bit Name Prefix</th>
</tr>
</thead>
<tbody>
<tr>
<td>HLVD</td>
<td>HLVD</td>
</tr>
</tbody>
</table>

**REGISTER 40-1: HLVDCON0: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER 0**

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R-x</th>
<th>R-x</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>—</td>
<td>OUT</td>
<td>RDY</td>
<td>—</td>
<td>—</td>
<td>INTH</td>
<td>INTL</td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’  
-n = Value at POR  
‘1’ = Bit is set  
‘0’ = Bit is cleared  
x = Bit is unknown

bit 7  
EN: High/Low-voltage Detect Power Enable bit  
1 = Enables HLVD, powers up HLVD circuit and supporting reference circuitry  
0 = Disables HLVD, powers down HLVD and supporting circuitry

bit 6  
Unimplemented: Read as ‘0’

bit 5  
OUT: HLVD Comparator Output bit  
1 = Voltage \( \leq \) selected detection limit (HLVDL<3:0>)  
0 = Voltage \( \geq \) selected detection limit (HLVDL<3:0>)

bit 4  
RDY: Band Gap Reference Voltages Stable Status Flag bit  
1 = Indicates HLVD Module is ready and output is stable  
0 = Indicates HLVD Module is not ready

bit 3-2  
Unimplemented: Read as ‘0’

bit 1  
INTH: HLVD Positive going (High Voltage) Interrupt Enable  
1 = HLVDIF will be set when voltage \( \geq \) selected detection limit (SEL<3:0>)  
0 = HLVDIF will not be set

bit 0  
INTL: HLVD Negative going (Low Voltage) Interrupt Enable  
1 = HLVDIF will be set when voltage \( \leq \) selected detection limit (SEL<3:0>)  
0 = HLVDIF will not be set
REGISTER 40-2:  HLVDCON1: LOW-VOLTAGE DETECT CONTROL REGISTER 1

<table>
<thead>
<tr>
<th></th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/u</th>
<th>R/W-0/u</th>
<th>R/W-0/u</th>
<th>R/W-0/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEL&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit    W = Writable bit    U = Unimplemented bit, read as ‘0’
-n = Value at POR    ‘1’ = Bit is set    ‘0’ = Bit is cleared    u = Bit is unchanged

bit 7-4        Unimplemented: Read as ‘0’
bit 3-0        SEL<3:0>: High/Low Voltage Detection Limit Selection bits

<table>
<thead>
<tr>
<th>SEL&lt;3:0&gt;</th>
<th>Typical Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>Reserved</td>
</tr>
<tr>
<td>1110</td>
<td>4.65V</td>
</tr>
<tr>
<td>1101</td>
<td>4.35V</td>
</tr>
<tr>
<td>1100</td>
<td>4.20V</td>
</tr>
<tr>
<td>1011</td>
<td>4.00V</td>
</tr>
<tr>
<td>1010</td>
<td>3.75V</td>
</tr>
<tr>
<td>1001</td>
<td>3.60V</td>
</tr>
<tr>
<td>1000</td>
<td>3.35V</td>
</tr>
<tr>
<td>0111</td>
<td>3.15V</td>
</tr>
<tr>
<td>0110</td>
<td>2.90V</td>
</tr>
<tr>
<td>0101</td>
<td>2.75V</td>
</tr>
<tr>
<td>0100</td>
<td>2.60V</td>
</tr>
<tr>
<td>0011</td>
<td>2.50V</td>
</tr>
<tr>
<td>0010</td>
<td>2.25V</td>
</tr>
<tr>
<td>0001</td>
<td>2.10V</td>
</tr>
<tr>
<td>0000</td>
<td>1.90V</td>
</tr>
</tbody>
</table>

TABLE 40-2: SUMMARY OF REGISTERS ASSOCIATED WITH HIGH/LOW-VOLTAGE DETECT MODULE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>HLVDCON0</td>
<td>EN</td>
<td>—</td>
<td>OUT</td>
<td>RDY</td>
<td>—</td>
<td>—</td>
<td>INTH</td>
<td>INTL</td>
<td>709</td>
</tr>
<tr>
<td>HLVDCON1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SEL&lt;3:0&gt;</td>
<td></td>
<td>710</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented, read as ‘0’. Shaded cells are unused by the HLVD module.
41.0 IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

ICSP™ programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process, allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP™ programming:

- ICSPCLK
- ICSPDAT
- MCLR/VPP
- VDD
- VSS

In Program/Verify mode the program memory, User IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input. For more information on ICSP™ refer to the “PIC18(L)F25/26K82 Memory Programming Specification” (DS40000000).

41.1 High-Voltage Programming Entry Mode

The device is placed into High-Voltage Programming Entry mode by holding the ICSPCLK and ICSPDAT pins low then raising the voltage on MCLR/VPP to Vih.

41.2 Low-Voltage Programming Entry Mode

The Low-Voltage Programming Entry mode allows the PIC® Flash MCUs to be programmed using Vdd only, without high voltage. When the LVP bit of Configuration Words is set to ‘1’, the low-voltage ICSP™ programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to ‘0’.

Entry into the Low-Voltage Programming Entry mode requires the following steps:

1. MCLR is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

Once the key sequence is complete, MCLR must be held at VIL for as long as Program/Verify mode is to be maintained.

If low-voltage programming is enabled (LVP = 1), the MCLR Reset function is automatically enabled and cannot be disabled. See Section 6.5 “MCLR” for more information.

The LVP bit can only be reprogrammed to ‘0’ by using the High-Voltage Programming mode.

41.3 Common Programming Interfaces

Connection to a target device is typically done through an ICSP™ header. A commonly found connector on development tools is the RJ-11 in the 6P6C (6-pin, 6-connector) configuration. See Figure 41-1.

FIGURE 41-1: ICD RJ-11 STYLE CONNECTOR INTERFACE

Another connector often found in use with the PICkit™ programmers is a standard 6-pin header with 0.1 inch spacing. Refer to Figure 41-2.

For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices such as resistors, diodes, or even jumpers. See Figure 41-3 for more information.
FIGURE 41-2: PICkit™ PROGRAMMER STYLE CONNECTOR INTERFACE

<table>
<thead>
<tr>
<th>Pin Description*</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 = VPP/MCLR</td>
</tr>
<tr>
<td>2 = VDD Target</td>
</tr>
<tr>
<td>3 = VSS (ground)</td>
</tr>
<tr>
<td>4 = ICSPDAT</td>
</tr>
<tr>
<td>5 = ICSPCLK</td>
</tr>
<tr>
<td>6 = No Connect</td>
</tr>
</tbody>
</table>

* The 6-pin header (0.100" spacing) accepts 0.025" square pins.

FIGURE 41-3: TYPICAL CONNECTION FOR ICSP™ PROGRAMMING

External Programming Signals

Device to be Programmed

VDD

MCLR/VPP

VSS

ICSPDAT

ICSPCLK

To Normal Connections

* Isolation devices (as required).
42.0 INSTRUCTION SET SUMMARY

PIC18(L)F25/26K83 devices incorporate the standard set of PIC18 core instructions, as well as an extended set of instructions, for the optimization of code that is recursive or that utilizes a software stack. The extended set is discussed later in this section.

42.1 Standard Instruction Set

The standard PIC18 instruction set adds many enhancements to the previous PIC® MCU instruction sets, while maintaining an easy migration from these PIC® MCU instruction sets. Most instructions are a single program memory word (16 bits), but there are four instructions that require two-program memory locations and two that require three-program memory locations.

Each single-word instruction is a 16-bit word divided into an opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into four basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal** operations
- **Control** operations

The PIC18 instruction set summary in Table 42-3 lists byte-oriented, bit-oriented, literal and control operations. Table 42-1 shows the opcode field descriptions.

Most **byte-oriented** instructions have three operands:

1. The file register (specified by ‘f’)
2. The destination of the result (specified by ‘d’)
3. The accessed memory (specified by ‘a’)

The file register designator ‘f’ specifies which file register is to be used by the instruction. The destination designator ‘d’ specifies where the result of the operation is to be placed. If ‘d’ is zero, the result is placed in the WREG register. If ‘d’ is one, the result is placed in the file register specified in the instruction.

All **bit-oriented** instructions have three operands:

1. The file register (specified by ‘f’)
2. The bit in the file register (specified by ‘b’)
3. The accessed memory (specified by ‘a’)

The bit field designator ‘b’ selects the number of the bit affected by the operation, while the file register designator ‘f’ represents the number of the file in which the bit is located.

The literal instructions may use some of the following operands:

- A literal value to be loaded into a file register (specified by ‘k’)
- The desired FSR register to load the literal value into (specified by ‘f’)
- No operand required (specified by ‘—’)

The control instructions may use some of the following operands:

- A program memory address (specified by ‘n’)
- The mode of the CALL or RETURN instructions (specified by ‘s’)
- The mode of the table read and table write instructions (specified by ‘m’)
- No operand required (specified by ‘—’)

All instructions are a single word, except for four double-word instructions. These instructions were made double-word to contain the required information in 32 bits. In the second word, the four MSbs are ‘1’s. If this second word is executed as an instruction (by itself), it will execute as a NOP.

All single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the Program Counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles, with the additional instruction cycle(s) executed as a NOP.

The double-word instructions execute in two instruction cycles.

One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true, or the Program Counter is changed as a result of an instruction, the instruction execution time is 2 μs. Two-word branch instructions (if true) would take 3 μs.

Figure 42-1 shows the general formats that the instructions can have. All examples use the convention ‘nnh’ to represent a hexadecimal number.

The Instruction Set Summary, shown in Table 42-3, lists the standard instructions recognized by the Microchip Assembler (MPASM™).

Section 42.1.1 “Standard Instruction Set” provides a description of each instruction.
### TABLE 42-1: OPCODE FIELD DESCRIPTIONS

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>RAM access bit&lt;br&gt;&lt;br&gt; a = 0: RAM location in Access RAM (BSR register is ignored)&lt;br&gt; a = 1: RAM bank is specified by BSR register</td>
</tr>
<tr>
<td>ACCESS</td>
<td>ACCESS = 0: RAM access bit symbol</td>
</tr>
<tr>
<td>BANKED</td>
<td>BANKED = 1: RAM access bit symbol</td>
</tr>
<tr>
<td>bbb</td>
<td>Bit address within an 8-bit file register (0 to 7)</td>
</tr>
<tr>
<td>BSR</td>
<td>Bank Select Register. Used to select the current RAM bank.</td>
</tr>
<tr>
<td>d</td>
<td>Destination select bit;&lt;br&gt; d = 0: store result in WREG,&lt;br&gt; d = 1: store result in file register f.</td>
</tr>
<tr>
<td>dest</td>
<td>Destination either the WREG register or the specified register file location</td>
</tr>
<tr>
<td>f</td>
<td>8-bit Register file address (00h to FFh)</td>
</tr>
<tr>
<td>fn</td>
<td>FSR Number (0 to 2)</td>
</tr>
<tr>
<td>fs</td>
<td>12-bit Register file address (000h to FFFh). This is the source address.</td>
</tr>
<tr>
<td>fd</td>
<td>12-bit Register file address (000h to FFFh). This is the destination address.</td>
</tr>
<tr>
<td>zs</td>
<td>7-bit literal offset for FSR2 to used as register file address (000h to FFFh). This is the source address.</td>
</tr>
<tr>
<td>zd</td>
<td>7-bit literal offset for FSR2 to used as register file address (000h to FFFh). This is the destination address.</td>
</tr>
<tr>
<td>k</td>
<td>Literal field, constant data or label (may be a 6-bit, 8-bit, 12-bit or a 20-bit value)</td>
</tr>
<tr>
<td>label</td>
<td>Label name</td>
</tr>
<tr>
<td>mm</td>
<td>The mode of the TBLPTR register for the Table Read and Table Write instructions&lt;br&gt;&lt;br&gt; Only used with Table Read and Table Write instructions:&lt;br&gt;&lt;br&gt; * No Change to register (such as TBLPTR with Table reads and writes)&lt;br&gt; *+ Post-Increment register (such as TBLPTR with Table reads and writes)&lt;br&gt; <em>- Post-Decrement register (such as TBLPTR with Table reads and writes)&lt;br&gt; +</em> Pre-Increment register (such as TBLPTR with Table reads and writes)</td>
</tr>
<tr>
<td>n</td>
<td>The relative address (2's complement number) for relative branch instructions, or the direct address for Call/Branch and Return instructions</td>
</tr>
<tr>
<td>PRODH</td>
<td>Product of Multiply high byte</td>
</tr>
<tr>
<td>PRODL</td>
<td>Product of Multiply low byte</td>
</tr>
<tr>
<td>s</td>
<td>Fast Call / Return mode select bit.&lt;br&gt; s = 0: do not update into/from shadow registers&lt;br&gt; s = 1: certain registers loaded into/from shadow registers (Fast mode)</td>
</tr>
<tr>
<td>u</td>
<td>Unused or Unchanged</td>
</tr>
<tr>
<td>w</td>
<td>W = 0: Destination select bit symbol</td>
</tr>
<tr>
<td>WREG</td>
<td>Working register (accumulator)</td>
</tr>
<tr>
<td>x</td>
<td>Don’t care (0 or 1)&lt;br&gt;&lt;br&gt; The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.</td>
</tr>
<tr>
<td>TBLPTR</td>
<td>21-bit Table Pointer (points to a Program Memory location)</td>
</tr>
<tr>
<td>TABLAT</td>
<td>8-bit Table Latch</td>
</tr>
<tr>
<td>TOS</td>
<td>Top-of-Stack</td>
</tr>
<tr>
<td>PC</td>
<td>Program Counter</td>
</tr>
<tr>
<td>PCL</td>
<td>Program Counter Low Byte</td>
</tr>
<tr>
<td>PCH</td>
<td>Program Counter High Byte</td>
</tr>
<tr>
<td>PCLATH</td>
<td>Program Counter High Byte Latch</td>
</tr>
<tr>
<td>PCLATU</td>
<td>Program Counter Upper Byte Latch</td>
</tr>
<tr>
<td>GIE</td>
<td>Global Interrupt Enable bit</td>
</tr>
<tr>
<td>WDT</td>
<td>Watchdog Timer</td>
</tr>
<tr>
<td>TO</td>
<td>Time-out bit</td>
</tr>
<tr>
<td>FD</td>
<td>Power-down bit</td>
</tr>
<tr>
<td>C, DC, Z, OV, N</td>
<td>ALU Status bits Carry, Digit Carry, Zero, Overflow, Negative</td>
</tr>
<tr>
<td>l</td>
<td>Optional</td>
</tr>
<tr>
<td>i</td>
<td>Contents</td>
</tr>
<tr>
<td>→</td>
<td>Assigned to</td>
</tr>
</tbody>
</table>
TABLE 42-1: OPCODE FIELD DESCRIPTIONS (CONTINUED)

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; &gt;</td>
<td>Register bit field</td>
</tr>
<tr>
<td>a</td>
<td>In the set of</td>
</tr>
<tr>
<td>italic</td>
<td>User defined term (font is courier)</td>
</tr>
</tbody>
</table>

FIGURE 42-1: General Format for Instructions (1/2)

**Byte-oriented** file register operations

<table>
<thead>
<tr>
<th>15</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>opcode</td>
<td>d</td>
<td>a</td>
<td>f (FILE #)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- d = 0 for result destination to be WREG register
- d = 1 for result destination to be file register (f)
- a = 0 to force Access Bank
- a = 1 for BSR to select bank
- f = 8-bit file register address

**Example Instruction**

```
ADDWF MYREG, W, B
```

**Byte to Byte** move operations (2-word)

<table>
<thead>
<tr>
<th>15</th>
<th>12</th>
<th>11</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>opcode</td>
<td>f (Source FILE #)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>15</th>
<th>12</th>
<th>11</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>f (Destination FILE #)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- f = 12-bit file register address

**Example Instruction**

```
MOVFF MYREG1, MYREG2
```

**Byte to Byte** move operations (3-word)

<table>
<thead>
<tr>
<th>15</th>
<th>12</th>
<th>11</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>opcode</td>
<td>FILE #</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>15</th>
<th>12</th>
<th>11</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>FILE #</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>15</th>
<th>12</th>
<th>11</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>FILE #</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bit-oriented** file register operations

<table>
<thead>
<tr>
<th>15</th>
<th>12</th>
<th>11</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>opcode</td>
<td>b (BIT #)</td>
<td>a</td>
<td>f (FILE #)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- b = 3-bit position of bit in file register (f)
- a = 0 to force Access Bank
- a = 1 for BSR to select bank
- f = 8-bit file register address

**Example Instruction**

```
BSF MYREG, bit, B
```

**Literal** operations

<table>
<thead>
<tr>
<th>15</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>opcode</td>
<td>k (literal)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- k = 8-bit immediate value

**Example Instruction**

```
MOVLW 7Fh
```
### FIGURE 42-2: General Format for Instructions (2/2)

#### Control operations

**CALL, GOTO and Branch operations**

<table>
<thead>
<tr>
<th>15</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPCODE</td>
<td>n&lt;7:0&gt; (literal)</td>
<td>GOTO Label</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>12</td>
<td>11</td>
<td>0</td>
</tr>
<tr>
<td>1111</td>
<td>n&lt;19:8&gt; (literal)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

n = 20-bit immediate value

<table>
<thead>
<tr>
<th>15</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPCODE</td>
<td>S</td>
<td>n&lt;7:0&gt; (literal)</td>
<td>CALL MYFUNC</td>
</tr>
<tr>
<td>15</td>
<td>12</td>
<td>11</td>
<td>0</td>
</tr>
<tr>
<td>1111</td>
<td>n&lt;19:8&gt; (literal)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

S = Fast bit

<table>
<thead>
<tr>
<th>15</th>
<th>11</th>
<th>10</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPCODE</td>
<td>n&lt;10:0&gt; (literal)</td>
<td>BRA MYFUNC</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>15</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPCODE</td>
<td>n&lt;7:0&gt; (literal)</td>
<td>BC MYFUNC</td>
<td></td>
</tr>
</tbody>
</table>
### TABLE 42-2: INSTRUCTION SET

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycles</th>
<th>16-Bit Instruction Word</th>
<th>Status Affected</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSb</td>
<td>LSb</td>
<td></td>
</tr>
</tbody>
</table>

#### BYTE-ORIENTED FILE REGISTER INSTRUCTIONS

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycles</th>
<th>16-Bit Instruction Word</th>
<th>Status Affected</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSb</td>
<td>LSb</td>
<td></td>
</tr>
</tbody>
</table>

#### BYTE-ORIENTED SKIP INSTRUCTIONS

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycles</th>
<th>16-Bit Instruction Word</th>
<th>Status Affected</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSb</td>
<td>LSb</td>
<td></td>
</tr>
</tbody>
</table>

#### BIT-ORIENTED FILE REGISTER INSTRUCTIONS

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycles</th>
<th>16-Bit Instruction Word</th>
<th>Status Affected</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSb</td>
<td>LSb</td>
<td></td>
</tr>
</tbody>
</table>

#### BIT-ORIENTED SKIP INSTRUCTIONS

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycles</th>
<th>16-Bit Instruction Word</th>
<th>Status Affected</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSb</td>
<td>LSb</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** If Program Counter (PC) is modified or a conditional test is true, the instruction requires an additional cycle. The extra cycle is executed as a NOP.

**Note 2:** Some instructions are multi word instructions. The second/third words of these instructions will be decoded as a NOP, unless the first word of the instruction retrieves the information embedded in these 16-bits. This ensures that all program memory locations have a valid instruction.

**Note 3:** fs and fd do not cover the full memory range. 2 MSBs of bank selection are forced to ‘b00 to limit the range of these instructions to lower 4k addressing space.
### TABLE 42-2: INSTRUCTION SET (CONTINUED)

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycles</th>
<th>16-Bit Instruction Word</th>
<th>Status Affected</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSb</td>
<td>LSb</td>
<td></td>
</tr>
<tr>
<td><strong>CONTROL INSTRUCTIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BC n</td>
<td>Branch if Carry</td>
<td>1 (2)</td>
<td>1110 0010 nnnn nnnn</td>
<td>None</td>
<td>1</td>
</tr>
<tr>
<td>BN n</td>
<td>Branch if Negative</td>
<td>1 (2)</td>
<td>1110 0110 nnnn nnnn</td>
<td>None</td>
<td>1</td>
</tr>
<tr>
<td>BNC n</td>
<td>Branch if Not Carry</td>
<td>1 (2)</td>
<td>1110 0011 nnnn nnnn</td>
<td>None</td>
<td>1</td>
</tr>
<tr>
<td>BNN n</td>
<td>Branch if Not Negative</td>
<td>1 (2)</td>
<td>1110 0111 nnnn nnnn</td>
<td>None</td>
<td>1</td>
</tr>
<tr>
<td>BNOV n</td>
<td>Branch if Not Overflow</td>
<td>1 (2)</td>
<td>1110 0101 nnnn nnnn</td>
<td>None</td>
<td>1</td>
</tr>
<tr>
<td>BNZ n</td>
<td>Branch if Not Zero</td>
<td>2</td>
<td>1110 0000 nnnn nnnn</td>
<td>None</td>
<td>1</td>
</tr>
<tr>
<td>BOV n</td>
<td>Branch if Overflow</td>
<td>1 (2)</td>
<td>1110 0100 nnnn nnnn</td>
<td>None</td>
<td>1</td>
</tr>
<tr>
<td>BRA n</td>
<td>Branch Unconditionally</td>
<td>1 (2)</td>
<td>1101 0nnn nnnn nnnn</td>
<td>None</td>
<td>1</td>
</tr>
<tr>
<td>BZ n</td>
<td>Branch if Zero</td>
<td>1 (2)</td>
<td>1110 0000 nnnn nnnn</td>
<td>None</td>
<td>1</td>
</tr>
<tr>
<td>CALL n, s</td>
<td>Call subroutine 1st word</td>
<td>2</td>
<td>1110 110s nnnn nnnn</td>
<td>None</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>2nd word</td>
<td></td>
<td>1111 nnnn nnnn nnnn</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GOTO n</td>
<td>Go to address 1st word</td>
<td>2</td>
<td>1110 1111 nnnn nnnn</td>
<td>None</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>2nd word</td>
<td></td>
<td>1111 nnnn nnnn nnnn</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CALLW —</td>
<td>W -&gt; PCL and Call subroutine</td>
<td>2</td>
<td>0000 0000 0001 0100</td>
<td>None</td>
<td>1</td>
</tr>
<tr>
<td>RCALL n</td>
<td>Relative Call</td>
<td>2</td>
<td>1101 1nnn nnnn nnnn</td>
<td>None</td>
<td>1</td>
</tr>
<tr>
<td>RETFIE s</td>
<td>Return from interrupt enable</td>
<td>2</td>
<td>0000 0000 0001 000s</td>
<td>None</td>
<td>1</td>
</tr>
<tr>
<td>RETLW k</td>
<td>Return with literal in WREG</td>
<td>2</td>
<td>0000 1100 kkkk kkkk</td>
<td>None</td>
<td>1</td>
</tr>
<tr>
<td>RETURN s</td>
<td>Return from Subroutine</td>
<td>2</td>
<td>0000 0000 0001 001s</td>
<td>None</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>INHERENT INSTRUCTIONS</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CLRWD —</td>
<td>Clear Watchdog Timer</td>
<td>1</td>
<td>0000 0000 0000 0100</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>DAW —</td>
<td>Decimal Adjust WREG</td>
<td>1</td>
<td>0000 0000 0000 0111</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>NOP —</td>
<td>No Operation</td>
<td>1</td>
<td>0000 0000 0000 0000</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>NOP —</td>
<td>No Operation</td>
<td>1</td>
<td>1111 xxxx xxxx xxxx</td>
<td>None</td>
<td>2</td>
</tr>
<tr>
<td>POP —</td>
<td>Pop top of return stack (TOS)</td>
<td>1</td>
<td>0000 0000 0000 0110</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>PUSH —</td>
<td>Push top of return stack (TOS)</td>
<td>1</td>
<td>0000 0000 0000 0101</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>RESET —</td>
<td>Software device Reset</td>
<td>1</td>
<td>0000 0000 1111 1111</td>
<td>All</td>
<td></td>
</tr>
<tr>
<td>SLEEP —</td>
<td>Go into Standby mode</td>
<td>1</td>
<td>0000 0000 0000 0011</td>
<td>None</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** If Program Counter (PC) is modified or a conditional test is true, the instruction requires an additional cycle. The extra cycle is executed as a **NOP**.

**Note 2:** Some instructions are multi word instructions. The second/third words of these instructions will be decoded as a **NOP**, unless the first word of the instruction retrieves the information embedded in these 16-bits. This ensures that all program memory locations have a valid instruction.

**Note 3:** $f_4$ and $f_9$ do not cover the full memory range. 2 MSBs of bank selection are forced to ‘b00 to limit the range of these instructions to lower 4k addressing space.
TABLE 42-2: INSTRUCTION SET (CONTINUED)

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycles</th>
<th>16-Bit Instruction Word</th>
<th>Status Affected</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSb</td>
<td>LSb</td>
<td></td>
</tr>
<tr>
<td>LITERAL INSTRUCTIONS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADDLW k</td>
<td>Add literal and WREG</td>
<td>1</td>
<td>0000 1111 kkkk kkkk</td>
<td>C, DC, Z, OV, N</td>
<td></td>
</tr>
<tr>
<td>ANDLW k</td>
<td>AND literal with WREG</td>
<td>1</td>
<td>0000 1011 kkkk kkkk</td>
<td>Z, N</td>
<td></td>
</tr>
<tr>
<td>IORLW k</td>
<td>Inclusive OR literal with WREG</td>
<td>1</td>
<td>0000 1001 kkkk kkkk</td>
<td>Z, N</td>
<td></td>
</tr>
<tr>
<td>LFSR fn, k</td>
<td>Load FSR(fn) with a 14-bit literal (k)</td>
<td>2</td>
<td>1110 1110 00ff kkkk</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>ADDFSR fn, k</td>
<td>Add FSR(fn) with (k)</td>
<td>1</td>
<td>1111 00kk kkkk kkkk</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>SUBFSR fn, k</td>
<td>Subtract (k) from FSR(fn)</td>
<td>1</td>
<td>1110 1001 ffkk kkkk</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>MOVLB k</td>
<td>Move literal to BSR&lt;5:0&gt;</td>
<td>1</td>
<td>0000 0001 00kk kkkk</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>MOVLLW k</td>
<td>Move literal to WREG</td>
<td>1</td>
<td>0000 1110 kkkk kkkk</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>MULLW k</td>
<td>Multiply literal with WREG</td>
<td>1</td>
<td>0000 1101 kkkk kkkk</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>RETLW k</td>
<td>Return with literal in WREG</td>
<td>2</td>
<td>0000 1100 kkkk kkkk</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>SUBLW k</td>
<td>Subtract WREG from literal</td>
<td>1</td>
<td>0000 1000 kkkk kkkk</td>
<td>C, DC, Z, OV, N</td>
<td></td>
</tr>
<tr>
<td>XORLW k</td>
<td>Exclusive OR literal with WREG</td>
<td>1</td>
<td>0000 1010 kkkk kkkk</td>
<td>Z, N</td>
<td></td>
</tr>
</tbody>
</table>

DATA MEMORY – PROGRAM MEMORY INSTRUCTIONS

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Description</th>
<th>Cycles</th>
<th>16-Bit Instruction Word</th>
<th>Status Affected</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSb</td>
<td>LSb</td>
<td></td>
</tr>
<tr>
<td>TBLRD*</td>
<td>Table Read</td>
<td>2 - 5</td>
<td>0000 0000 0000 1000</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>TBLRD'*+</td>
<td>Table Read with post-increment</td>
<td>2 - 5</td>
<td>0000 0000 0000 1001</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>TBLRD*-</td>
<td>Table Read with post-decrement</td>
<td>2 - 5</td>
<td>0000 0000 0000 1010</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>TBLRD'+</td>
<td>Table Read with pre-increment</td>
<td>2 - 5</td>
<td>0000 0000 0000 1011</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>TBLWT*</td>
<td>Table Write</td>
<td>2 - 5</td>
<td>0000 0000 0000 1100</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>TBLWT'+</td>
<td>Table Write with post-increment</td>
<td>2 - 5</td>
<td>0000 0000 0000 1101</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>TBLWT*-</td>
<td>Table Write with post-decrement</td>
<td>2 - 5</td>
<td>0000 0000 0000 1110</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>TBLWT*+</td>
<td>Table Write with pre-increment</td>
<td>2 - 5</td>
<td>0000 0000 0000 1111</td>
<td>None</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** If Program Counter (PC) is modified or a conditional test is true, the instruction requires an additional cycle. The extra cycle is executed as a **NOP**.

**Note 2:** Some instructions are multi word instructions. The second/third words of these instructions will be decoded as a **NOP**, unless the first word of the instruction retrieves the information embedded in these 16-bits. This ensures that all program memory locations have a valid instruction.

**Note 3:** fn and fd do not cover the full memory range. 2 MSBs of bank selection are forced to ‘b00 to limit the range of these instructions to lower 4k addressing space.
42.1.1 STANDARD INSTRUCTION SET

ADDFSR  Add Literal to FSR

Syntax: ADDFSR f, k
Operands: 0 ≤ k ≤ 63
          f ∈ {0, 1, 2}
Operation: FSR(f) + k → FSR(f)
Status Affected: None
Encoding: 1110 1000 ffkk kkkk
Description: The 6-bit literal ‘k’ is added to the contents of the FSR specified by ‘f’.
Words: 1
Cycles: 1
Q Cycle Activity:

Example: ADDFSR 2, 23h
Before Instruction
FSR2 = 03FFh
After Instruction
FSR2 = 0422h

ADDLW  ADD literal to W

Syntax: ADDLW k
Operands: 0 ≤ k ≤ 255
Operation: (W) + k → W
Status Affected: N, OV, C, DC, Z
Encoding: 0000 1111 kkkk kkkk
Description: The contents of W are added to the 8-bit literal ‘k’ and the result is placed in W.
Words: 1
Cycles: 1
Q Cycle Activity:

Example: ADDLW 15h
Before Instruction
W = 10h
After Instruction
W = 25h

Note: All PIC18 instructions may take an optional label argument preceding the instruction mnemonic for use in symbolic addressing. If a label is used, the instruction format then becomes: (label) instruction argument(s).
### ADDWFC

**ADD W and CARRY bit to f**

**Syntax:**
ADDWFC \( f, \{d, \{.a\}\} \)

**Operands:**
- \( 0 \leq f \leq 255 \)
- \( d \in [0,1] \)
- \( a \in [0,1] \)

**Operation:**
\( (W) + (f) + (C) \rightarrow \text{dest} \)

**Status Affected:**
N, OV, C, DC, Z

**Encoding:**
```
0010 00da ffff ffff
```

**Description:**
Add \( W \), the CARRY flag and data memory location \( f \). If \( d \) is '0', the result is placed in \( W \). If \( d \) is '1', the result is placed in data memory location \( f \).

If \( a \) is '0', the Access Bank is selected.
If \( a \) is '1', the BSR is used to select the GPR bank.

If \( a \) is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever \( f \leq 95 \) (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

**Words:** 1

**Cycles:** 1

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register ( f )</td>
<td>Process Data</td>
<td>Write to destination</td>
</tr>
</tbody>
</table>

**Example:**
ADDWFC REG, 0, 1

**Before Instruction**
- CARRY bit = 1
- REG = 02h
- W = 4Dh

**After Instruction**
- CARRY bit = 0
- REG = 02h
- W = 50h

---

### ANDLW

**AND literal with W**

**Syntax:**
ANDLW \( k \)

**Operands:**
- \( 0 \leq k \leq 255 \)

**Operation:**
\( (W) \ .AND. k \rightarrow W \)

**Status Affected:**
N, Z

**Encoding:**
```
0000 1011 kkkk kkkk
```

**Description:**
The contents of \( W \) are AND'ed with the 8-bit literal \( k \). The result is placed in \( W \).

**Words:** 1

**Cycles:** 1

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal ( k )</td>
<td>Process Data</td>
<td>Write to W</td>
</tr>
</tbody>
</table>

**Example:**
ANDLW 05Fh

**Before Instruction**
- \( W = \) A3h

**After Instruction**
- \( W = \) 03h
ANDWF  AND W with f

Syntax: ANDWF  f{,d{,(a)}}
Operands:  
0 ≤ f ≤ 255  
d ∈ {0,1}  
a ∈ {0,1}  
Operation: (W) .AND. (f) → dest  
Status Affected: N, Z  
Encoding: 0001 01da ffff ffff  
Description: The contents of W are AND’ed with register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default).
If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

Words: 1  
Cycles: 1  
Q Cycle Activity:

Example:  ANDWF REG, 0, 0  
Before Instruction  
W = 17h  
REG = C2h  
After Instruction  
W = 02h  
REG = C2h  

BC  Branch if Carry

Syntax: BC n  
Operands: -128 ≤ n ≤ 127  
Operation: if CARRY bit is '1'  
(PC) + 2 + 2n → PC  
Status Affected: None  
Encoding: 1110 0010 nnnn nnnn  
Description: If the CARRY bit is '1', then the program will branch.
The 2’s complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a 2-cycle instruction.

Words: 1  
Cycles: 1(2)  
Q Cycle Activity:

Example:  HERE BC 5  
Before Instruction  
PC = address (HERE)  
After Instruction  
If CARRY = 1;  
PC = address (HERE + 12)  
If CARRY = 0;  
PC = address (HERE + 2)
### BCF  Bit Clear f

**Syntax:**
```plaintext
BCF  f, b {,a}
```

**Operands:**
- `0 ≤ f ≤ 255`
- `0 ≤ b ≤ 7`
- `a ∈ [0,1]`

**Operation:**
- `0 → f< b>

**Status Affected:**
- None

**Encoding:**
```
1001  bbba  ffff  ffff
```

**Description:**
- Bit 'b' in register 'f' is cleared.
- If 'a' is '0', the Access Bank is selected.
- If 'a' is '1', the BSR is used to select the GPR bank.
- If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever `f ≤ 95 (5Fh)`. See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

**Words:**
- 1

**Cycles:**
- 1

**Q Cycle Activity:**
<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>Write register 'f'</td>
</tr>
</tbody>
</table>

**Example:**
```plaintext
BCF  FLAG_REG,  7, 0
```
- Before Instruction
  - FLAG_REG = C7h
- After Instruction
  - FLAG_REG = 47h

### BN  Branch if Negative

**Syntax:**
```plaintext
BN    n
```

**Operands:**
- `-128 ≤ n ≤ 127`

**Operation:**
- if NEGATIVE bit is ‘1’
  - `(PC) + 2 + 2n → PC`

**Status Affected:**
- None

**Encoding:**
```
1110  0110  nnnn  nnnn
```

**Description:**
- If the NEGATIVE bit is ‘1’, then the program will branch.
- The 2’s complement number ‘2n’ is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be `PC + 2 + 2n`. This instruction is then a 2-cycle instruction.

**Words:**
- 1

**Cycles:**
- 1(2)

**Q Cycle Activity:**

If Jump:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal 'n'</td>
<td>Process Data</td>
<td>Write to PC</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If No Jump:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal 'n'</td>
<td>Process Data</td>
<td>No operation</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**
```
HERE BN Jump
```
- Before Instruction
  - PC = address (HERE)
- After Instruction
  - If NEGATIVE = 1;
    - PC = address (Jump)
  - If NEGATIVE = 0;
    - PC = address (HERE + 2)
**BNC**  
*BNC* Branch if Not Carry

**Syntax:** BNC \ n

**Operands:** -128 ≤ \ n ≤ 127

**Operation:** if CARRY bit is '0'

(PC) + 2 + 2n → PC

**Status Affected:** None

**Encoding:**  1110 0011 nnnn nnnn

**Description:**  
If the CARRY bit is '0', then the program will branch.  
The 2's complement number '2n' is added to the PC.  
Since the PC will have incremented to fetch the next instruction,  
the new address will be PC + 2 + 2n.  
This instruction is then a 2-cycle instruction.

**Words:** 1

**Cycles:** 1(2)

**Q Cycle Activity:**

If Jump:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal</td>
<td>Process Data</td>
<td>Write to PC</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If No Jump:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal</td>
<td>Process Data</td>
<td>No operation</td>
</tr>
<tr>
<td>'n'</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**

**Before Instruction**

PC = address (HERE)

**After Instruction**

If CARRY = 0;

PC = address (Jump)

If CARRY = 1;

PC = address (HERE + 2)

---

**BNN**  
*BNN* Branch if Not Negative

**Syntax:** BNN \ n

**Operands:** -128 ≤ \ n ≤ 127

**Operation:** if NEGATIVE bit is '0'

(PC) + 2 + 2n → PC

**Status Affected:** None

**Encoding:**  1110 0111 nnnn nnnn

**Description:**  
If the NEGATIVE bit is '0', then the program will branch.  
The 2's complement number '2n' is added to the PC.  
Since the PC will have incremented to fetch the next instruction,  
the new address will be PC + 2 + 2n.  
This instruction is then a 2-cycle instruction.

**Words:** 1

**Cycles:** 1(2)

**Q Cycle Activity:**

If Jump:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal</td>
<td>Process Data</td>
<td>Write to PC</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If No Jump:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal</td>
<td>Process Data</td>
<td>No operation</td>
</tr>
<tr>
<td>'n'</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**

**Before Instruction**

PC = address (HERE)

**After Instruction**

If NEGATIVE = 0;

PC = address (Jump)

If NEGATIVE = 1;

PC = address (HERE + 2)
**BNOV** Branch if Not Overflow

**Syntax:**  BNOV  n

**Operands:**  -128 ≤ n ≤ 127

**Operation:**  if OVERFLOW bit is '0'

(PC) + 2 + 2n → PC

**Status Affected:**  None

**Encoding:**  1110 0101 nnnn nnnn

**Description:**  If the OVERFLOW bit is '0', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a 2-cycle instruction.

**Words:**  1

**Cycles:**  1(2)

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal 'n'</td>
<td>Process Data</td>
<td>Write to PC</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If Jump:

If No Jump:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal 'n'</td>
<td>Process Data</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**  HERE  BNOV  Jump

Before Instruction:

PC = address (HERE)

After Instruction:

If OVERFLOW = 0;

PC = address (Jump)

If OVERFLOW = 1;

PC = address (HERE + 2)

**BNZ** Branch if Not Zero

**Syntax:**  BNZ  n

**Operands:**  -128 ≤ n ≤ 127

**Operation:**  if ZERO bit is '0'

(PC) + 2 + 2n → PC

**Status Affected:**  None

**Encoding:**  1110 0001 nnnn nnnn

**Description:**  If the ZERO bit is '0', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a 2-cycle instruction.

**Words:**  1

**Cycles:**  1(2)

**Q Cycle Activity:**

If Jump:

If No Jump:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal 'n'</td>
<td>Process Data</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**  HERE  BNZ  Jump

Before Instruction:

PC = address (HERE)

After Instruction:

If ZERO = 0;

PC = address (Jump)

If ZERO = 1;

PC = address (HERE + 2)
BRA  Unconditional Branch
Syntax:  BRA n
Operands:  -1024 ≤ n ≤ 1023
Operation:  (PC) + 2 + 2n → PC
Status Affected:  None
Encoding:  1101 0nnn nnnn nnnn
Description:  Add the 2's complement number '2n' to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is a 2-cycle instruction.
Words:  1
Cycles:  2
Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal 'n'</td>
<td>Process Data</td>
<td>Write to PC</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

Example:
Before Instruction
PC = address (HERE)
After Instruction
PC = address (Jump)

BSF  Bit Set f
Syntax:  BSF f, b {,a}
Operands:  0 ≤ f ≤ 255
0 ≤ b ≤ 7
a ∈ [0,1]
Operation:  1 → f< b>
Status Affected:  None
Encoding:  1000 bbba ffff ffff
Description:  Bit 'b' in register 'f' is set.
If 'a' is '0', the Access Bank is selected.
If 'a' is '1', the BSR is used to select the GPR bank.
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.
Words:  1
Cycles:  1
Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>Write register 'f'</td>
</tr>
</tbody>
</table>

Example:
Before Instruction
BSF FLAG_REG, 7, 1
FLAG_REG = 0Ah
After Instruction
FLAG_REG = 8Ah
**BTFSC**

**Bit Test File, Skip if Clear**

**Syntax:**

```
BTFSC   f, b {,a}
```

**Operands:**

- `0 ≤ f ≤ 255`
- `0 ≤ b ≤ 7`
- `a ∈ [0,1]`

**Operation:**

skip if `(f<b>) = 0`

**Status Affected:**

None

**Encoding:**

```
1011 bbba ffff ffff
```

**Description:**

If bit 'b' in register 'f' is '0', then the next instruction is skipped. If bit 'b' is '0', then the next instruction fetched during the current instruction execution is discarded and a **NOP** is executed instead, making this a 2-cycle instruction. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever `f ≤ 95 (5Fh)`. See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

**Words:** 1

**Cycles:** 1(2)

**Note:** 3 cycles if skip and followed by a 2-word instruction.

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If skip:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If skip and followed by 2-word instruction:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**

```
HERE  BTFSC  FLAG, 1, 0
FALSE :  
TRUE :  
```

**Before Instruction**

- `PC = address (HERE)`

**After Instruction**

- If `FLAG<1>` = 0; `PC = address (TRUE)`
- If `FLAG<1>` = 1; `PC = address (FALSE)`

---

**BTFSS**

**Bit Test File, Skip if Set**

**Syntax:**

```
BTFSS   f, b {,a}
```

**Operands:**

- `0 ≤ f ≤ 255`
- `0 ≤ b < 7`
- `a ∈ [0,1]`

**Operation:**

skip if `(f<b>) = 1`

**Status Affected:**

None

**Encoding:**

```
1010 bbba ffff ffff
```

**Description:**

If bit 'b' in register 'f' is '1', then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution is discarded and a **NOP** is executed instead, making this a 2-cycle instruction. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever `f ≤ 95 (5Fh)`. See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

**Words:** 1

**Cycles:** 1(2)

**Note:** 3 cycles if skip and followed by a 2-word instruction.

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If skip:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If skip and followed by 2-word instruction:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**

```
HERE  BTFSS  FLAG, 1, 0
FALSE :  
TRUE :  
```

**Before Instruction**

- `PC = address (HERE)`

**After Instruction**

- If `FLAG<1>` = 0; `PC = address (FALSE)`
- If `FLAG<1>` = 1; `PC = address (TRUE)`
### BTG Bit Toggle f

**Syntax:** BTG f, b {,a}

**Operands:**
- \(0 \leq f \leq 255\)
- \(0 \leq b < 7\)
- \(a \in \{0, 1\}\)

**Operation:** \((f\langle b\rangle) \rightarrow f\langle b\rangle\)

**Status Affected:** None

**Encoding:**
```
0111 bbba ffff ffff
```

**Description:**
- Bit ‘b’ in data memory location ‘f’ is inverted.
- If ‘a’ is ‘0’, the Access Bank is selected.
- If ‘a’ is ‘1’, the BSR is used to select the GPR bank.
- If ‘a’ is ‘0’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever \(f \leq 95\) (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

| Words: | 1 |
| Cycles: | 1 |

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register ‘f’</td>
<td>Process Data</td>
<td>Write register ‘f’</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**

Before Instruction:
- \(\text{PORTC} = 0111 \ 0101\) [75h]

After Instruction:
- \(\text{PORTC} = 0110 \ 0101\) [65h]

---

### BOV Branch if Overflow

**Syntax:** BOV n

**Operands:** \(-128 \leq n \leq 127\)

**Operation:**
- If OVERFLOW bit is ‘1’, \((\text{PC}) + 2 + 2n \rightarrow \text{PC}\)

**Status Affected:** None

**Encoding:**
```
1110 0100 nnnn nnnn
```

**Description:**
- If the OVERFLOW bit is ‘1’, then the program will branch.
- The 2’s complement number ‘2n’ is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be \(\text{PC} + 2 + 2n\). This instruction is then a 2-cycle instruction.

| Words: | 1 |
| Cycles: | 1(2) |

**Q Cycle Activity:**

If Jump:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal ‘n’</td>
<td>Process Data</td>
<td>Write to PC</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If No Jump:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal ‘n’</td>
<td>Process Data</td>
<td>No operation</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**

Before Instruction:
- \(\text{PC} = \text{address (HERE)}\)

After Instruction:
- \(\text{PC} = \text{address (Jump)}\)
- \(\text{PC} = \text{address (HERE + 2)}\)
### BZ Branch if Zero

**Syntax:**

\[ BZ \ n \]

**Operands:**

\[-128 \leq n \leq 127\]

**Operation:**

If ZERO bit is ‘1’

\[(PC) + 2 + 2n \rightarrow PC\]

**Status Affected:**

None

**Encoding:**

<table>
<thead>
<tr>
<th>1110</th>
<th>0000</th>
<th>nnnn</th>
<th>nnnn</th>
</tr>
</thead>
</table>

**Description:**

If the ZERO bit is ‘1’, then the program will branch.

The 2’s complement number ‘2n’ is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a 2-cycle instruction.

**Words:** 1

**Cycles:** 1(2)

**Q Cycle Activity:**

If Jump:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal</td>
<td>Process Data</td>
<td>Write to PC</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If No Jump:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal</td>
<td>Process Data</td>
<td>No operation</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**

HERE BZ Jump

Before Instruction

PC = address (HERE)

After Instruction

If ZERO = 1;

PC = address (Jump)

If ZERO = 0;

PC = address (HERE + 2)

---

### CALL Subroutine Call

**Syntax:**

\[ CALL \ k \{s\} \]

**Operands:**

\[ 0 \leq k \leq 1048575 \]

\[ s \in [0,1] \]

**Operation:**

\[(PC) + 4 \rightarrow TOS,\]

\[ k \rightarrow PC<20:1>,\]

\[ \text{if } s = 1 \]

\[(W) \rightarrow WS,\]

\[(\text{Status}) \rightarrow \text{STATUSS},\]

\[(\text{BSR}) \rightarrow \text{BSRS}\]

**Status Affected:**

None

**Encoding:**

<table>
<thead>
<tr>
<th>1st word (k&lt;7:0&gt;)</th>
<th>2nd word (k&lt;19:8&gt;)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1110</td>
<td>1111</td>
</tr>
<tr>
<td>110s</td>
<td>k19kkk</td>
</tr>
<tr>
<td>k7kkk</td>
<td>kkkk0</td>
</tr>
<tr>
<td>kkkk8</td>
<td>kkkk9</td>
</tr>
</tbody>
</table>

**Description:**

Subroutine call of entire 2-Mbyte memory range. First, return address (PC + 4) is pushed onto the return stack. If ‘s’ = 1, the W, Status and BSR registers are also pushed into their respective shadow registers, WS, STATUSS and BSRS. If ‘s’ = 0, no update occurs (default). Then, the 20-bit value ‘k’ is loaded into PC<20:1>. CALL is a 2-cycle instruction.

**Words:** 2

**Cycles:** 2

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal</td>
<td>PUSH PC to stack</td>
<td>Read literal</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**

HERE CALL THERE, 1

Before Instruction

PC = address (HERE)

After Instruction

PC = address (THERE)

TOS = address (HERE + 4)

WS = W

BSRS = BSR

STATUSS = Status
CALLW Subroutine Call Using WREG

Syntax: CALLW
Operands: None
Operation: 
- (PC + 2) → TOS,
- (W) → PCL,
- (PCLATH) → PCH,
- (PCLATU) → PCU

Status Affected: None
Encoding: 0000 0000 0001 0100
Description: First, the return address (PC + 2) is pushed onto the return stack. Next, the contents of W are written to PCL; the existing value is discarded. Then, the contents of PCLATH and PCLATU are latched into PCH and PCU, respectively. The second cycle is executed as a NOP instruction while the new next instruction is fetched. Unlike CALL, there is no option to update W, Status or BSR.

Words: 1
Cycles: 2
Q Cycle Activity:

Example:
Before Instruction
PC = address (HERE)
PCLATH = 10h
PCLATU = 00h
W = 06h
After Instruction
PC = 001006h
TOS = address (HERE + 2)
PCLATH = 10h
PCLATU = 00h
W = 06h

CLRF Clear f

Syntax: CLRF f {a}
Operands: 0 ≤ f ≤ 255
- a ∈ [0, 1]
Operation: 000h → f
- 1 → Z

Status Affected: Z
Encoding: 0000 0000 0001 0100
Description: Clears the contents of the specified register. If ‘a’ is ‘0’, the Access Bank is selected. If ‘a’ is ‘1’, the BSR is used to select the GPR bank. If ‘a’ is ‘0’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

Words: 1
Cycles: 1
Q Cycle Activity:

Example: CLRF FLAG_REG, 1
Before Instruction
FLAG_REG = 5Ah
After Instruction
FLAG_REG = 00h
### CLRWDT

**Clear Watchdog Timer**

- **Syntax:** CLRWDT
- **Operands:** None
- **Operation:**
  - 000h → WDT,
  - 00h → WDT postscaler,
  - 1 → TO,
  - 1 → PD
- **Status Affected:**
  - TO, PD
- **Encoding:**
  - 0000 0000 0000 0100
- **Description:**
  - The CLRWDT instruction resets the Watchdog Timer. It also resets the postscaler of the WDT. Status bits, TO and PD, are set.
- **Words:** 1
- **Cycles:** 1

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Decode</th>
<th>Q2</th>
<th>Process Data</th>
<th>Q3</th>
<th>Q4</th>
<th>No operation</th>
</tr>
</thead>
</table>

**Example:** CLRWDT

- **Before Instruction**
  - WDT Counter = ?
- **After Instruction**
  - WDT Counter = 00h
  - WDT Postscaler = 0
  - TO = 1
  - PD = 1

### COMF

**Complement f**

- **Syntax:** COMF f, (d, (a))
- **Operands:**
  - 0 ≤ f ≤ 255
  - d ∈ [0, 1]
  - a ∈ [0, 1]
- **Operation:** (f) → dest
- **Status Affected:** N, Z
- **Encoding:**
  - 0001 lida ffff ffff
- **Description:**
  - The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default).
  - If 'a' is '0', the Access Bank is selected.
  - If 'a' is '1', the BSR is used to select the GPR bank.
  - If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.
- **Words:** 1
- **Cycles:** 1

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Decode</th>
<th>Q2</th>
<th>Read register 'f'</th>
<th>Q3</th>
<th>Q4</th>
<th>Process Data</th>
<th>Write to destination</th>
</tr>
</thead>
</table>

**Example:** COMF REG, 0, 0

- **Before Instruction**
  - REG = 13h
- **After Instruction**
  - REG = 13h
  - W = ECh
CPFSEQ

Compare f with W, skip if f = W

Syntax: CPFSEQ f{(a)"

Operands: 0 \leq f \leq 255
a \in [0,1]

Operation: (f) – (W),
skip if (f) = (W)
(unsigned comparison)

Status Affected: None

Encoding: 0110 001a ffff ffff

Description: Compares the contents of data memory
location 'f' to the contents of W by
performing an unsigned subtraction.
If f = W, then the fetched instruction is
discarded and a NOP is executed
instead, making this a 2-cycle
instruction.
If 'a' is '0', the Access Bank is selected.
If 'a' is '1', the BSR is used to select the
GPR bank.
If 'a' is '0' and the extended instruction
set is enabled, this instruction operates
in Indexed Literal Offset Addressing
mode whenever f \leq 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-
Oriented Instructions in Indexed Lit-
eral Offset Mode” for details.

Words: 1
Cycles: 1(2)

Note: 3 cycles if skip and followed
by a 2-word instruction.

Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If skip:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If skip and followed by 2-word instruction:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

Example:

HERE CPFSEQ REG, 0
NEQUAL :
EQUAL :

Before Instruction
PC Address = HERE
W = ?
REG = ?

After Instruction
If REG = W;
PC = Address (EQUAL)
If REG > W;
PC = Address (GREATER)
If REG \leq W;
PC = Address (NGREATER)
PIC18(L)F25/26K83

CPFSLT  Compare f with W, skip if f < W

Syntax: CPFSLT f {,a}
Operands: 0 ≤ f ≤ 255
          a ∈ [0,1]
Operation: (f) – (W),
skip if (f) < (W)
           (unsigned comparison)
Status Affected: None
Encoding: 0110 000a ffff ffff
Description: Compares the contents of data memory
location ‘f’ to the contents of W by
performing an unsigned subtraction.
If the contents of ‘f’ are less than the
contents of W, then the fetched
instruction is discarded and a NOP is
executed instead, making this a
2-cycle instruction.
If ‘a’ is ‘0’, the Access Bank is selected.
If ‘a’ is ‘1’, the BSR is used to select the
GPR bank.
Words: 1
Cycles: (1)(2)
Note: 3 cycles if skip and followed
by a 2-word instruction.
Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

If skip:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>operation</td>
<td>operation</td>
<td>operation</td>
<td>operation</td>
</tr>
</tbody>
</table>

If skip and followed by 2-word instruction:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>operation</td>
<td>operation</td>
<td>operation</td>
<td>operation</td>
</tr>
</tbody>
</table>

Example: HERE CPFSLT REG, 1
NLESS :
LESS :

Before Instruction
PC = Address (HERE)
W = ?
After Instruction
If REG < W:
PC = Address (LESS)
If REG ≥ W:
PC = Address (NLESS)

DAW  Decimal Adjust W Register

Syntax: DAW
Operands: None
Operation: If [W<3:0> > 9] or [DC = 1] then
           (W<3:0>) + 6 → W<3:0>;
         else
           W<3:0>;
If [W<7:4> + DC > 9] or [C = 1] then
           (W<7:4>) + 6 + DC → W<7:4>;
         else
           (W<7:4>) + DC → W<7:4>
Status Affected: C
Encoding: 0000 0000 0000 0111
Description: DAW adjusts the 8-bit value in W, resulting
from the earlier addition of two variables (each in packed BCD format) and
produces a correct packed BCD result.
Words: 1
Cycles: 1
Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Before Instruction

<table>
<thead>
<tr>
<th>Register W</th>
<th>Data</th>
<th>Process</th>
<th>Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>05h</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>C</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>DC</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Example 1:

<table>
<thead>
<tr>
<th>Data</th>
<th>Process</th>
<th>Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>05h</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>DC</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Example 2:

<table>
<thead>
<tr>
<th>Data</th>
<th>Process</th>
<th>Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>34h</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>DC</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
### DECF
**Decrement f**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>DECF f {,d {,a}}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>0 ≤ f ≤ 255</td>
</tr>
<tr>
<td></td>
<td>d ∈ [0,1]</td>
</tr>
<tr>
<td></td>
<td>a ∈ [0,1]</td>
</tr>
<tr>
<td>Operation:</td>
<td>(f) – 1 → dest</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>C, DC, N, OV, Z</td>
</tr>
<tr>
<td>Encoding:</td>
<td><img src="" alt="Encoding" /></td>
</tr>
<tr>
<td>Description:</td>
<td>Decrements register <code>f</code>. If <code>d</code> is '0', the result is stored in W. If <code>d</code> is '1', the result is stored back in register <code>f</code> (default). If <code>a</code> is '0', the Access Bank is selected. If <code>a</code> is '1', the BSR is used to select the GPR bank. If <code>a</code> is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.</td>
</tr>
<tr>
<td>Words:</td>
<td>1</td>
</tr>
<tr>
<td>Cycles:</td>
<td>1</td>
</tr>
</tbody>
</table>

#### Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Example:

**Before Instruction**

<table>
<thead>
<tr>
<th>CNT</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>01h</td>
<td>0</td>
</tr>
</tbody>
</table>

**After Instruction**

<table>
<thead>
<tr>
<th>CNT</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>1</td>
</tr>
</tbody>
</table>

### DECSZ
**Decrement f, skip if 0**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>DECFSZ f {,d {,a}}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>0 ≤ f ≤ 255</td>
</tr>
<tr>
<td></td>
<td>d ∈ [0,1]</td>
</tr>
<tr>
<td></td>
<td>a ∈ [0,1]</td>
</tr>
<tr>
<td>Operation:</td>
<td>(f) – 1 → dest,</td>
</tr>
<tr>
<td></td>
<td>skip if result = 0</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>None</td>
</tr>
<tr>
<td>Encoding:</td>
<td><img src="" alt="Encoding" /></td>
</tr>
<tr>
<td>Description:</td>
<td>The contents of register <code>f</code> are decremented. If <code>d</code> is '0', the result is placed in W. If <code>d</code> is '1', the result is placed back in register <code>f</code> (default). If the result is '0', the next instruction, which is already fetched, is discarded and a NOP is executed instead, making it a 2-cycle instruction. If <code>a</code> is '0', the Access Bank is selected. If <code>a</code> is '1', the BSR is used to select the GPR bank. If <code>a</code> is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.</td>
</tr>
<tr>
<td>Words:</td>
<td>1</td>
</tr>
<tr>
<td>Cycles:</td>
<td>1(2)</td>
</tr>
</tbody>
</table>

#### Note: 3 cycles if skip and followed by a 2-word instruction.

#### Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

If skip:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If skip and followed by 2-word instruction:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

#### Example:

**Before Instruction**

**HERE**

| DECFSZ CNT, 1, 1 |

**GOTO LOOP**

**CONTINUE**

| PC = Address (HERE) |

**After Instruction**

<table>
<thead>
<tr>
<th>CNT</th>
<th>PC</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNT - 1</td>
<td>Address (CONTINUE)</td>
</tr>
</tbody>
</table>

If CNT = 0:

| PC = Address (HERE + 2) |
DCFSNZ

Decrement f, skip if not 0

Syntax: DCFSNZ f {d {,a}}
Operands: 0 ≤ f ≤ 255
           d ∈ [0,1]
           a ∈ [0,1]
Operation: (f) – 1 → dest, skip if result ≠ 0
Status Affected: None
Encoding: 0100 11da ffff ffff
Description: The contents of register ‘f’ are decremented. If ‘d’ is ‘0’, the result is placed in W. If ‘d’ is ‘1’, the result is placed back in register ‘f’ (default). If the result is not ‘0’, the next instruction, which is already fetched, is discarded and a NOP is executed instead, making it a 2-cycle instruction.

          If ‘a’ is ‘0’, the Access Bank is selected.
          If ‘a’ is ‘1’, the BSR is used to select the GPR bank.
          If ‘a’ is ‘0’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

Words: 1
Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
| Decode | Read register ‘f’ | Process Data | Write to destination |
If skip:

| No operation | No operation | No operation | No operation |
If skip and followed by 2-word instruction:

| No operation | No operation | No operation | No operation |

Example:
HERE DCFSNZ TEMP, 1, 0
ZERO :
NZERO :

Before Instruction
TEMP = ?
After Instruction
TEMP = TEMP – 1,
If TEMP = 0;
PC = Address (ZERO)
If TEMP = 0;
PC = Address (NZERO)

GOTO

Unconditional Branch

Syntax: GOTO k
Operands: 0 ≤ k ≤ 1048575
Operation: k → PC<20:1>
Status Affected: None
Encoding: 0100 11da ffff ffff

Description: GOTO allows an unconditional branch anywhere within entire 2-Mbyte memory range. The 20-bit value ‘k’ is loaded into PC<20:1>. GOTO is always a 2-cycle instruction.

Words: 2
Cycles: 2

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
| Decode | Read literal ‘k<7:0>’, | No operation | Read literal ‘k<19:8>’, Write to PC |
| No operation | No operation | No operation | No operation |

Example: GOTO THERE
After Instruction
PC = Address (THERE)
INCF  

Syntax:   INCF f {,d {,a}}

Operands:  0 ≤ f ≤ 255
           d ∈ [0,1]
           a ∈ [0,1]

Operation:  (f) + 1 → dest

Status Affected:  C, DC, N, OV, Z

Encoding:   0010 10da ffff ffff

Description:  The contents of register 'f' are incremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

Words:  1
Cycles:  1

Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>Write to destination</td>
</tr>
</tbody>
</table>

Example:   INCF CNT, 1, 0

Before Instruction

CNT = FFh
Z = 0
C = ?
DC = ?

After Instruction

CNT = 00h
Z = 1
C = 1
DC = 1

INCFSZ  

Syntax:   INCFSZ f {,d {,a}}

Operands:  0 ≤ f ≤ 255
           d ∈ [0,1]
           a ∈ [0,1]

Operation:  (f) + 1 → dest, skip if result = 0

Status Affected:  None

Encoding:   0011 11da ffff ffff

Description:  The contents of register 'f' are incremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default). If the result is '0', the next instruction, which is already fetched, is discarded and a NOP is executed instead, making it a 2-cycle instruction.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

Words:  1
Cycles:  1(2)

Note:  3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>Write to destination</td>
</tr>
</tbody>
</table>

If skip:

Q1 | Q2 | Q3 | Q4 |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If skip and followed by 2-word instruction:

Q1 | Q2 | Q3 | Q4 |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

Example:   HERE INCFSZ CNT, 1, 0

NZERO :
ZERO :

Before Instruction

PC = Address (HERE)

After Instruction

CNT = CNT + 1
If CNT = 0;
PC = Address (ZERO)
If CNT > 0;
PC = Address (NZERO)
INFSNZ  Increment f, skip if not 0

Syntax:  INFSNZ  f{,d}{,a})
Operands:  0 ≤ f ≤ 255
           d ∈ [0,1]
           a ∈ [0,1]
Operation:  (f) + 1 → dest,
            skip if result ≠ 0
Status Affected:  None
Encoding:  0100 10da  ffff  ffff
Description:  The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in W. If ‘d’ is ‘1’, the result is placed back in register ‘f’ (default). If the result is not ‘0’, the next instruction, which is already fetched, is discarded and a NOP is executed instead, making it a 2-cycle instruction.
            If ‘a’ is ‘0’, the Access Bank is selected. If ‘a’ is ‘1’, the BSR is used to select the GPR bank.
            If ‘a’ is ‘0’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

Words:  1
Cycles:  1(2)

Q Cycle Activity:

Q Cycle Activity:

Example:  HERE  INFSNZ  REG, 1, 0
           ZERO
           NZERO

Before Instruction
PC = Address (HERE)
After Instruction
REG = REG + 1
If REG ≠ 0;
   PC = Address (NZERO)
If REG = 0;
   PC = Address (ZERO)

IORLW  Inclusive OR literal with W

Syntax:  IORLW  k
Operands:  0 ≤ k ≤ 255
Operation:  (W) .OR. k → W
Status Affected:  N, Z
Encoding:  0000 1001  kkkk  kkkk
Description:  The contents of W are ORed with the 8-bit literal ‘k’. The result is placed in W.

Words:  1
Cycles:  1

Q Cycle Activity:

Q Cycle Activity:

Example:  IORLW  35h
Before Instruction
W = 9Ah
After Instruction
W = BFh

Example:  HERE  INFSNZ  REG, 1, 0
           ZERO
           NZERO

Before Instruction
PC = Address (HERE)
After Instruction
REG = REG + 1
If REG ≠ 0;
   PC = Address (NZERO)
If REG = 0;
   PC = Address (ZERO)
IORWF     Inclusive OR W with f
Syntax:    IORWF   f, d {,a}
Operands:  0 ≤ f ≤ 255
          d ∈ [0,1]
          a ∈ [0,1]
Operation: (W) .OR. (f) → dest
Status Affected: N, Z
Encoding:  0001 00da ffff ffff
Description: Inclusive OR W with register 'f'. If 'd' is
             '0', the result is placed in W. If 'd' is '1',
             the result is placed back in register 'f'
             (default).
             If 'a' is '0', the Access Bank is selected.
             If 'a' is '1', the BSR is used to select the
             GPR bank.
             If 'a' is '0' and the extended instruction
             set is enabled, this instruction operates
             in Indexed Literal Offset Addressing
             mode whenever f ≤ 95 (5Fh). See Section
             42.2.3 “Byte-Oriented and Bit-
             Oriented Instructions in Indexed Lit-
             teral Offset Mode” for details.

Words: 1
Cycles: 1
Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>Write to destination</td>
</tr>
</tbody>
</table>

Example: IORWF RESULT, 0, 1

Before Instruction
RESULT = 13h
W = 91h

After Instruction
RESULT = 13h
W = 93h

LFSR     Load FSR
Syntax:   LFSR   f, k
Operands: 0 ≤ f ≤ 2
          0 ≤ k ≤ 16383
Operation: k → FSRf
Status Affected: None
Encoding:  1110 1111 0000 kkkk
            1110 0000 k;kkk kkkk
Description: The 14-bit literal 'k' is loaded into the
             File Select Register pointed to by 'f'.

Words: 2
Cycles: 2
Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal 'k' MSB</td>
<td>Process Data</td>
<td>Write literal 'k' MSB to FSRfH</td>
</tr>
<tr>
<td>Decode</td>
<td>Read literal 'k' LSB</td>
<td>Process Data</td>
<td>Write literal 'k' to FSRfL</td>
</tr>
</tbody>
</table>

Example: LFSR 2, 3ABh

After Instruction
FSR2H = 03h
FSR2L = ABh
**MOVF** Move f

Syntax:  
MOVF  f {,d {,a}}

Operands:  
0 ≤ f ≤ 255  
d ∈ [0,1]  
a ∈ [0,1]

Operation:  
f → dest

Status Affected:  
N, Z

Encoding:  
0101 00da ffff ffff

Description:  
The contents of register 'f' are moved to a destination dependent upon the status of ‘d’. If ‘d’ is ‘0’, the result is placed in W. If ‘d’ is ‘1’, the result is placed back in register ‘f’ (default). Location ‘f’ can be anywhere in the 256-byte bank. If ‘a’ is ‘0’, the Access Bank is selected. If ‘a’ is ‘1’, the BSR is used to select the GPR bank. If ‘a’ is ‘0’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

Words:  
1

Cycles:  
1

Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>Write W</td>
</tr>
</tbody>
</table>

Example:  
MOVF REG, 0, 0

Before Instruction
REG = 22h  
W = FFh

After Instruction
REG = 22h  
W = 22h

---

**MOVFF** Move f to f

Syntax:  
MOVFF   f s,fd

Operands:  
0 ≤ fs ≤ 4095  
0 ≤ fd ≤ 4095

Operation:  
(fs) → fd

Status Affected:  
None

Encoding:  
1st word (source)  
2nd word (destin.)

1100 1111  
ffff  ffff  ffff  ffff  ffff  ffff

Description:  
The contents of source register ‘fs’ are moved to destination register ‘fd’. Location of source ‘fs’ can be anywhere in the 4096-byte data space (000h to FFFh) and location of destination ‘fd’ can also be anywhere from 000h to FFFh. MOVFF has curtailed the source and destination range to the lower 4 Kbyte space of memory (Banks 1 through 15). For everything else, use MOVFFL.

Words:  
2

Cycles:  
2 (3)

Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f' (src)</td>
<td>Process Data</td>
<td>No operation</td>
</tr>
<tr>
<td>No operation</td>
<td>No dummy read</td>
<td>No operation</td>
<td>Write register 'f' (dest)</td>
</tr>
</tbody>
</table>

Example:  
MOVFF REG1, REG2

Before Instruction
REG1 = 33h  
REG2 = 11h

After Instruction
REG1 = 33h  
REG2 = 33h
MOVFFL  Move f to f (Long Range)

Syntax:  MOVFFL f_s, f_d
Operands:  0 ≤ f_s ≤ 16383
          0 ≤ f_d ≤ 16383
Operation:  (f_s) → f_d
Status Affected:  None
Encoding:
1st word  0000
2nd word  1111
3rd word  0000

Description:  The contents of source register 'f_s' are moved to destination register 'f_d'.
Location of source 'f_s' can be anywhere in the 16 Kbyte data space (0000h to 3FFFh). Either source or destination can be W (a useful special situation).
MOVFFL is particularly useful for transferring a data memory location to a peripheral register (such as the transmit buffer or an I/O port).
The MOVFFL instruction cannot use the PCL, TOSU, TOSH or TOSL as the destination register.

Words:  3
Cycles:  3
Q Cycle Activity:

Example:
MOVFFL 2000h, 200Ah
Before Instruction
Contents of 2000h = 33h
Contents of 200Ah = 11h
After Instruction
Contents of 2000h = 33h
Contents of 200Ah = 33h

MOVLB  Move literal to BSR

Syntax:  MOVLW k
Operands:  0 ≤ k ≤ 63
Operation:  k → BSR
Status Affected:  None
Encoding:
          0000 0001 00kk kkkk

Description:  The 6-bit literal 'k' is loaded into the Bank Select Register (BSR<5:0>). The value of BSR<7:6> always remains '0'.

Words:  1
Cycles:  1
Q Cycle Activity:

Example:
MOVLB 5
Before Instruction
BSR Register = 02h
After Instruction
BSR Register = 05h

Example:
MOVFFL 2000h, 200Ah
Before Instruction
Contents of 2000h = 33h
Contents of 200Ah = 11h
After Instruction
Contents of 2000h = 33h
Contents of 200Ah = 33h
MOVLW      Move literal to W

Syntax:      MOVLW  k
Operand:     0 ≤ k ≤ 255
Operation:   k → W
Status Affected: None
Encoding: 0000 1110 kkkk kkkk
Description: The 8-bit literal ‘k’ is loaded into W.
Words: 1
Cycles: 1
Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal ‘k’</td>
<td>Process Data</td>
<td>Write to W</td>
</tr>
</tbody>
</table>

Example: MOVLW 5Ah
After Instruction
W = 5Ah

MOVWF      Move W to f

Syntax: MOVWF  f {,a}
Operand: 0 ≤ f ≤ 255
Operation: (W) → f
Status Affected: None
Encoding: 0110 111a ffff ffff
Description: Move data from W to register ‘f’. Location ‘f’ can be anywhere in the 256-byte bank. If ‘a’ is ‘0’, the Access Bank is selected. If ‘a’ is ‘1’, the BSR is used to select the GPR bank. If ‘a’ is ‘0’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.
Words: 1
Cycles: 1
Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register ‘f’</td>
<td>Process Data</td>
<td>Write register ‘f’</td>
</tr>
</tbody>
</table>

Example: MOVWF REG, 0
Before Instruction
W = 4Fh
REG = FFh
After Instruction
W = 4Fh
REG = 4Fh
MULLW  Multiply literal with W

Syntax: MULLW k
Operands: 0 ≤ k ≤ 255
Operation: (W) x k → PRODH:PRODL
Status Affected: None
Encoding: 0000 1101 kkkk kkkk
Description: An unsigned multiplication is carried out between the contents of W and the 8-bit literal 'k'. The 16-bit result is placed in the PRODH:PRODL register pair. PRODH contains the high byte. W is unchanged. None of the Status flags are affected. Note that neither overflow nor carry is possible in this operation. A zero result is possible but not detected.

Words: 1
Cycles: 1
Q Cycle Activity:

Example: MULLW 0C4h

Before Instruction
W = E2h
PRODH = ?
PRODL = ?

After Instruction
W = E2h
PRODH = ADh
PRODL = 08h

MULWF  Multiply W with f

Syntax: MULWF f, (a)
Operands: 0 ≤ f ≤ 255
a ∈ [0,1]
Operation: (W) x (f) → PRODH:PRODL
Status Affected: None
Encoding: 0000 001a ffff ffff
Description: An unsigned multiplication is carried out between the contents of W and the register file location 'f'. The 16-bit result is stored in the PRODH:PRODL register pair. PRODH contains the high byte. Both W and 'f' are unchanged. None of the Status flags are affected. Note that neither overflow nor carry is possible in this operation. A zero result is possible but not detected.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

Words: 1
Cycles: 1
Q Cycle Activity:

Example: MULWF REG, 1

Before Instruction
W = C4h
REG = B5h
PRODH = ?
PRODL = ?

After Instruction
W = C4h
REG = B5h
PRODH = 8Ah
PRODL = 94h
NEGF Negate f

Syntax: NEGF f {,a}

Operands:
\[
0 \leq f \leq 255 \\
a \in [0,1]
\]

Operation: \((f + 1) \rightarrow f\)

Status Affected: N, OV, C, DC, Z

Encoding:
\[
0110\ 110a\ fffe\ fffe
\]

Description: Location ‘f’ is negated using two’s complement. The result is placed in the data memory location ‘f’.
If ‘a’ is ‘0’, the Access Bank is selected.
If ‘a’ is ‘1’, the BSR is used to select the GPR bank.
If ‘a’ is ‘0’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever \(f \leq 95\) (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

Words: 1
Cycles: 1

Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register ‘f’</td>
<td>Process Data</td>
<td>Write register ‘f’</td>
</tr>
</tbody>
</table>

Example:

Before Instruction
REG = 0011 1010 [3Ah]
After Instruction
REG = 1100 0110 [C6h]

NOP No Operation

Syntax: NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:
\[
0000 \ 0000 \ 0000 \ 0000 \\
1111 \ xxxx \ xxxx \ xxxx
\]

Description: No operation.

Words: 1
Cycles: 1

Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

Example:

None.
### POP

**Pop Top of Return Stack**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>POP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>None</td>
</tr>
<tr>
<td>Operation:</td>
<td>(TOS) → bit bucket</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>None</td>
</tr>
<tr>
<td>Encoding:</td>
<td>0000 0000 0000 0110</td>
</tr>
<tr>
<td>Description:</td>
<td>The TOS value is pulled off the return stack and is discarded. The TOS value then becomes the previous value that was pushed onto the return stack. This instruction is provided to enable the user to properly manage the return stack to incorporate a software stack.</td>
</tr>
</tbody>
</table>

| Words:        | 1 |
| Cycles:       | 1 |

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>No operation</td>
<td>POP TOS value</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**

Before Instruction

- TOS = 0031A2h
- Stack (1 level down) = 014332h

After Instruction

- TOS = 014332h
- PC = NEW

---

### PUSH

**Push Top of Return Stack**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>PUSH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>None</td>
</tr>
<tr>
<td>Operation:</td>
<td>(PC + 2) → TOS</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>None</td>
</tr>
<tr>
<td>Encoding:</td>
<td>0000 0000 0000 0101</td>
</tr>
<tr>
<td>Description:</td>
<td>The PC + 2 is pushed onto the top of the return stack. The previous TOS value is pushed down on the stack. This instruction allows implementing a software stack by modifying TOS and then pushing it onto the return stack.</td>
</tr>
</tbody>
</table>

| Words:        | 1 |
| Cycles:       | 1 |

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>PUSH PC + 2 onto return stack</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**

Before Instruction

- PC = 0124h
- TOS = 345Ah

After Instruction

- PC = 0126h
- TOS = 0126h
- Stack (1 level down) = 345Ah
### RCALL

**Syntax:**
```
RCALL n
```

**Operands:**
-1024 ≤ n ≤ 1023

**Operation:**
- \((PC) + 2 \rightarrow TOS, (PC) + 2 + 2n \rightarrow PC\)

**Status Affected:** None

**Encoding:**
```
1101 lnnn nnnn nnnn
```

**Description:**
Subroutine call with a jump up to 1K from the current location. First, return address \((PC + 2)\) is pushed onto the stack. Then, add the 2's complement number '2n' to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be \(PC + 2 + 2n\). This instruction is a 2-cycle instruction.

**Words:** 1

**Cycles:** 2

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal 'n'</td>
<td>Process Data</td>
<td>Write to PC</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**
```
HERE RCALL Jump
```

Before Instruction:
- PC = Address (HERE)

After Instruction:
- PC = Address (Jump)
- TOS = Address (HERE + 2)

---

### RESET

**Syntax:**
```
RESET
```

**Operands:** None

**Operation:** Reset all registers and flags that are affected by a MCLR Reset.

**Status Affected:** All

**Encoding:**
```
0000 0000 1111 1111
```

**Description:**
This instruction provides a way to execute a MCLR Reset by software.

**Words:** 1

**Cycles:** 1

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Start Reset</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**
```
RESET
```

After Instruction:
- Registers = Reset Value
- Flags* = Reset Value
### RETFIE (Return from Interrupt)

**Syntax:**
```
RETFIE \{s\}
```

**Operands:**
- `s ∈ [0,1]`

**Operation:**
- `(TOS) → PC`,
- if `s = 1`, context is restored into `WREG, STATUS, BSR, FSR0H, FSR0L, FSR1H, FSR1L, FSR2H, FSR2L, PRODH, PRODL, PCLATH` and `PCLATU` registers from the corresponding shadow registers.
- if `s = 0`, there is no change in status of any register.

**Status Affected:**
- `STAT<1:0>` in `INTCON1` register

**Encoding:**
```
0000 0000 0001 000s
```

**Description:**
- Return from interrupt. Stack is popped and Top-of-Stack (TOS) is loaded into the PC. Interrupts are enabled by setting either the high or low priority global interrupt enable bit. If `s = 1`, the contents of the shadow registers, `WREG, STATUS, BSR, FSR0H, FSR0L, FSR1H, FSR1L, FSR2H, FSR2L, PRODH, PRODL, PCLATH` and `PCLATU` are loaded into corresponding registers. There are two sets of shadow registers, main context and low context. The set retrieved on RETFIE instruction execution depends on what the state of operation of the CPU was when RETFIE was executed. If `s = 0`, no update of these registers occurs (default).

**Words:** 1

**Cycles:** 2

**Example:**
```
RETFIE 1
```

### RETLW (Return literal to W)

**Syntax:**
```
RETLW k
```

**Operands:**
- `0 ≤ k ≤ 255`

**Operation:**
- `k \rightarrow W, (TOS) \rightarrow PC, PCLATU, PCLATH` are unchanged

**Status Affected:**
- None

**Encoding:**
```
0000 1100 kkkk kkkk
```

**Description:**
- `W` is loaded with the 8-bit literal `k`. The Program Counter is loaded from the top of the stack (the return address). The high address latch (PCLATH) remains unchanged.

**Words:** 1

**Cycles:** 2

**Example:**
```
CALL TABLE ; W contains table offset value ; W now has ; table value :
TABLE
ADDWF PCL ; W = offset RETLW k0 ; Begin table RETLW k1 ;
;
RETLW kn ; End of table
Before Instruction
W = 07h
After Instruction
W = value of kn
```
**RETURN**  
Return from Subroutine

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>RETURN  {s}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>s ∈ [0,1]</td>
</tr>
<tr>
<td>Operation:</td>
<td>(TOS) → PC,</td>
</tr>
<tr>
<td></td>
<td>if s = 1</td>
</tr>
<tr>
<td></td>
<td>(WS) → W,</td>
</tr>
<tr>
<td></td>
<td>(STATUSS) → Status,</td>
</tr>
<tr>
<td></td>
<td>(BSRS) → BSR,</td>
</tr>
<tr>
<td></td>
<td>PCLATU, PCLATH are unchanged</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>None</td>
</tr>
<tr>
<td>Encoding:</td>
<td>0000 0000 0001 001s</td>
</tr>
<tr>
<td>Description:</td>
<td>Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the Program Counter. If 's' = 1, the contents of the shadow registers, WS, STATUSS and BSRS, are loaded into their corresponding registers, W, Status and BSR. If 's' = 0, no update of these registers occurs (default).</td>
</tr>
<tr>
<td>Words:</td>
<td>1</td>
</tr>
<tr>
<td>Cycles:</td>
<td>2</td>
</tr>
</tbody>
</table>

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>No operation</td>
<td>Process Data</td>
<td>POP PC from stack</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**

RETURN

After Instruction:

PC = TOS

---

**RLCF**  
Rotate Left f through Carry

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>RLCF  {d, (a)}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>0 ≤ f ≤ 255</td>
</tr>
<tr>
<td></td>
<td>d ∈ [0,1]</td>
</tr>
<tr>
<td></td>
<td>a ∈ [0,1]</td>
</tr>
<tr>
<td>Operation:</td>
<td>(f&lt;n&gt;) → dest&lt;n + 1&gt;,</td>
</tr>
<tr>
<td></td>
<td>(f&lt;7&gt;) → C,</td>
</tr>
<tr>
<td></td>
<td>(C) → dest&lt;0&gt;</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>C, N, Z</td>
</tr>
<tr>
<td>Encoding:</td>
<td>0011 01da ffff ffff</td>
</tr>
<tr>
<td>Description:</td>
<td>The contents of register 'f' are rotated one bit to the left through the CARRY flag. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.</td>
</tr>
<tr>
<td>Words:</td>
<td>1</td>
</tr>
<tr>
<td>Cycles:</td>
<td>1</td>
</tr>
</tbody>
</table>

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>Write to destination</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Example:**

RLCF      REG, 0, 0

Before Instruction

REG = 1110 0110
C = 0

After Instruction

REG = 1110 0110
W = 1100 1100
C = 1
**RLNCF**  Rotate Left f (No Carry)

**Syntax:**
RLNCF  f (d, (a))

**Operands:**
0 ≤ f ≤ 255  
d ∈ [0, 1]  
a ∈ [0, 1]

**Operation:**
(f<n>) → dest<n + 1>,  
(f<7>) → dest<0>

**Status Affected:**
N, Z

**Encoding:**
0100 01da  ffff  ffff

**Description:**
The contents of register 'f' are rotated one bit to the left. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f' (default).  
If 'a' is '0', the Access Bank is selected.  
If 'a' is '1', the BSR is used to select the GPR bank.  
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

**Words:** 1
**Cycles:** 1
**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read</td>
<td>Process</td>
<td>Write to destination</td>
</tr>
</tbody>
</table>

**Example:**  
Before Instruction  
REG = 1010 1011  
After Instruction  
REG = 0101 0111

---

**RRCF**  Rotate Right f through Carry

**Syntax:**
RRCF  f (d, (a))

**Operands:**
0 ≤ f ≤ 255  
d ∈ [0, 1]  
a ∈ [0, 1]

**Operation:**
(f<n>) → dest<n – 1>,  
(f<0>) → C,  
(C) → dest<7>

**Status Affected:**
C, N, Z

**Encoding:**
0011 00da  ffff  ffff

**Description:**
The contents of register 'f' are rotated one bit to the right through the CARRY flag. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default).  
If 'a' is '0', the Access Bank is selected.  
If 'a' is '1', the BSR is used to select the GPR bank.  
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

**Words:** 1
**Cycles:** 1
**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read</td>
<td>Process</td>
<td>Write to destination</td>
</tr>
</tbody>
</table>

**Example:**  
Before Instruction  
REG = 1110 0110  
C = 0  
After Instruction  
REG = 1110 0110  
W = 0111 0011  
C = 0
RRNCF  Rotate Right f (No Carry)

Syntax: \texttt{RRNCF\ f,\{d,\{a\}\}}

Operands: \[0 \leq f \leq 255\]
\[d \in [0,1]\]
\[a \in [0,1]\]

Operation:
\[(f\langle n \rangle) \rightarrow \text{dest}\langle n - 1 \rangle,\]
\[(f\langle 0 \rangle) \rightarrow \text{dest}\langle 7 \rangle\]

Status Affected: N, Z

Encoding: \[
\begin{array}{cccc}
0100 & 00da & ffff & ffff \\
\end{array}
\]

Description: The contents of register 'f' are rotated one bit to the right. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default). If 'a' is '0', the Access Bank will be selected (default), overriding the BSR value. If 'a' is '1', then the bank will be selected as per the BSR value. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever \(f \leq 95\) (5Fh). See Section 42.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.

Words: 1  
Cycles: 1

Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>Write to register 'f'</td>
</tr>
</tbody>
</table>

Example 1:
\texttt{RRNCF\ REG,\ 1,\ 0}

Before Instruction:
\[
\begin{align*}
\text{REG} & = 1101\ 0111 \\
\text{W} & = ?
\end{align*}
\]

After Instruction:
\[
\begin{align*}
\text{REG} & = 1110\ 1011 \\
\text{W} & = 1110\ 1011
\end{align*}
\]

Example 2:
\texttt{RRNCF\ REG,\ 0,\ 0}

Before Instruction:
\[
\begin{align*}
\text{REG} & = 1101\ 0111 \\
\text{W} & = ?
\end{align*}
\]

After Instruction:
\[
\begin{align*}
\text{REG} & = 1110\ 1011 \\
\text{W} & = 1110\ 1011
\end{align*}
\]

SETF  Set f

Syntax: \texttt{SETF\ f,\{a\}}

Operands: \[0 \leq f \leq 255\]
\[a \in [0,1]\]

Operation: \(FFh \rightarrow f\)

Status Affected: None

Encoding: \[
\begin{array}{cccc}
0110 & 100a & ffff & ffff \\
\end{array}
\]

Description: The contents of the specified register are set to FFh. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever \(f \leq 95\) (5Fh). See Section 42.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.

Words: 1
Cycles: 1

Q Cycle Activity:

Example:
\texttt{SETF\ REG,\ 1}

Before Instruction:
\[
\begin{align*}
\text{REG} & = 5Ah \\
\text{W} & = ?
\end{align*}
\]

After Instruction:
\[
\begin{align*}
\text{REG} & = \text{FFh}
\end{align*}
\]
**SLEEP**
Enter Sleep mode

**Syntax:**
SLEEP

**Operands:** None

**Operation:**
00h → WDT,
0 → WDT postscaler,
1 → TO,
0 → PD

**Status Affected:** TO, PD

**Encoding:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>No operation</td>
<td>Process Data</td>
<td>Go to Sleep</td>
</tr>
</tbody>
</table>

**Description:**
The Power-down Status bit (PD) is cleared. The Time-out Status bit (TO) is set. Watchdog Timer and its postscaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

**Words:** 1

**Cycles:** 1

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>Write to destination</td>
</tr>
</tbody>
</table>

**Example:**

Before Instruction

\[
\begin{align*}
\text{TO} & = ? \\
\text{PD} & = ? \\
\end{align*}
\]

After Instruction

\[
\begin{align*}
\text{TO} & = 1 \uparrow \\
\text{PD} & = 0 \\
\end{align*}
\]

† If WDT causes wake-up, this bit is cleared.

---

**SUBFSR**
Subtract Literal from FSR

**Syntax:**
SUBFSR f, k

**Operands:**

\[
0 \leq k \leq 63
\]

\[
f \in \{0, 1, 2\}
\]

**Operation:**

FSR(f) – k → FSRf

**Status Affected:** None

**Encoding:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>Write to destination</td>
</tr>
</tbody>
</table>

**Description:**
The 6-bit literal 'k' is subtracted from the contents of the FSR specified by 'f'.

**Words:** 1

**Cycles:** 1

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>Write to destination</td>
</tr>
</tbody>
</table>

**Example:**

Before Instruction

\[
\begin{align*}
\text{FSR2} & = 03FFh \\
\end{align*}
\]

After Instruction

\[
\begin{align*}
\text{FSR2} & = 03DCh \\
\end{align*}
\]
SUBFWB Subtract f from W with borrow

Syntax: SUBFWB f {,d {,a}}

Operands: 0 ≤ f ≤ 255
d ∈ [0,1]
a ∈ [0,1]

Operation: (W) – (f) – (C) → dest

Status Affected: N, OV, C, DC, Z

Encoding: 0101 01da ffff ffff

Description: Subtract register 'f' and CARRY flag (borrow) from W (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored in register 'f' (default).

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

Words: 1
Cycles: 1

Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>Write to destination</td>
</tr>
</tbody>
</table>

Example 1: SUBFWB REG, 1, 0

Before Instruction
REG = 3
W = 2
C = 1

After Instruction
REG = FF
W = 2
C = 0
Z = 0
N = 1 ; result is negative

Example 2: SUBFWB REG, 0, 0

Before Instruction
REG = 2
W = 5
C = 1

After Instruction
REG = 2
W = 3
C = 1
Z = 0
N = 0 ; result is positive

Example 3: SUBFWB REG, 1, 0

Before Instruction
REG = 1
W = 2
C = 0

After Instruction
REG = 0
W = 2
C = 1
Z = 1
N = 0 ; result is zero

SUBLW Subtract W from literal

Syntax: SUBLW k

Operands: 0 ≤ k ≤ 255

Operation: k – (W) → W

Status Affected: N, OV, C, DC, Z

Encoding: 0000 1000 kkkk kkkk

Description: W is subtracted from the 8-bit literal 'k'. The result is placed in W.

Words: 1
Cycles: 1

Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal 'k'</td>
<td>Process Data</td>
<td>Write to W</td>
</tr>
</tbody>
</table>

Example 1: SUBLW 02h

Before Instruction
W = 01h
C = ?

After Instruction
W = 00h
C = 1 ; result is zero
Z = 1
N = 0

Example 2: SUBLW 02h

Before Instruction
W = 02h
C = ?

After Instruction
W = 00h
C = 1 ; result is zero
Z = 1
N = 0

Example 3: SUBLW 02h

Before Instruction
W = 03h
C = ?

After Instruction
W = FFh ; (2's complement)
C = 0 ; result is negative
Z = 0
N = 1
SUBWF Subtract W from f

Syntax: \texttt{SUBWF \ f, \{d, \{a\}\}}

Operands: \(0 \leq f \leq 255\)
\(d \in [0,1]\)
\(a \in [0,1]\)

Operation: \((f) - (W) \rightarrow \text{dest}\)

Status Affected: N, OV, C, DC, Z

Encoding: 0101 11\text{da} ffff ffff

Description: Subtract W from register 'f' (2’s complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever \(f \leq 95\) (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

Words: 1

Cycles: 1

Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>Write to destination</td>
</tr>
</tbody>
</table>

Example 1:

Before Instruction
REG = 3
W = 2
C = ?

After Instruction
REG = 1
W = 2
C = 1; result is positive
Z = 0
N = 0

Example 2:

Before Instruction
REG = 2
W = 2
C = ?

After Instruction
REG = 2
W = 0
C = 1; result is zero
Z = 1
N = 0

Example 3:

Before Instruction
REG = 1
W = 2
C = ?

After Instruction
REG = FFh ;(2's complement)
W = 2
C = 0; result is negative
Z = 0
N = 1

SUBWFB Subtract W from f with Borrow

Syntax: \texttt{SUBWFB \ f, \{d, \{a\}\}}

Operands: \(0 \leq f \leq 255\)
\(d \in [0,1]\)
\(a \in [0,1]\)

Operation: \((f) - (W) - (C) \rightarrow \text{dest}\)

Status Affected: N, OV, C, DC, Z

Encoding: 0101 10\text{da} ffff ffff

Description: Subtract W and the CARRY flag (borrow) from register 'f' (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever \(f \leq 95\) (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

Words: 1

Cycles: 1

Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>Write to destination</td>
</tr>
</tbody>
</table>

Example 1:

Before Instruction
REG = 19h (0001 1001)
W = 0Dh (0000 1101)
C = 1

After Instruction
REG = 0Ch (0000 1100)
W = 0Dh (0000 1101)
C = 0
Z = 0; result is positive

Example 2:

Before Instruction
REG = 1Bh (0001 1011)
W = 1Ah (0001 1010)
C = 0

After Instruction
REG = 1Bh (0001 1011)
W = 00h
C = 1
Z = 1; result is zero
N = 0

Example 3:

Before Instruction
REG = 03h (0000 0011)
W = 0Eh (0000 1110)
C = 1

After Instruction
REG = F5h (1111 0101)
W = 0Eh (0000 1110)
C = 0
Z = 0
N = 1; result is negative
SWAPF  f

Syntax: \texttt{SWAPF } f \{,d \{,a\}\}

Operands: \begin{align*}
  0 &\leq f \leq 255 \\
  d &\in [0,1] \\
  a &\in [0,1]
\end{align*}

Operation: \begin{align*}
  (f\langle 3:0\rangle) &\rightarrow \text{dest}\langle 7:4\rangle, \\
  (f\langle 7:4\rangle) &\rightarrow \text{dest}\langle 3:0\rangle
\end{align*}

Status Affected: None

Encoding: \begin{tabular}{c|c|c|c|c}
  0011 & 10da & ffff & ffff \end{tabular}

Description: The upper and lower nibbles of register ‘f’ are exchanged. If ‘d’ is ‘0’, the result is placed in W. If ‘d’ is ‘1’, the result is placed in register ‘f’ (default). If ‘a’ is ‘0’, the Access Bank is selected. If ‘a’ is ‘1’, the BSR is used to select the GPR bank.

If ‘a’ is ‘0’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever \(f \leq 95\) (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.

Words: 1

Cycles: 1

Q Cycle Activity:

\begin{tabular}{|c|c|c|c|c|}
  \hline
  Q1 & Q2 & Q3 & Q4 \\
  \hline
  Decode & Read register ‘f’ & Process Data & Write to destination \\
  \hline
\end{tabular}

Example: \texttt{SWAPF REG, 1, 0}

Before Instruction
\begin{align*}
  \text{REG} &\quad = \quad 53h \\
\end{align*}

After Instruction
\begin{align*}
  \text{REG} &\quad = \quad 35h \\
\end{align*}
TBLRD  Table Read

Syntax:  TBLRD ( *, *+, *-, +*)

Operands:  None

Operation:
- if TBLRD *,
  (Prog Mem (TBLPTR)) → TABLAT;
  TBLPTR – No Change;
- if TBLRD *+,
  (Prog Mem (TBLPTR)) → TABLAT;
  (TBLPTR) + 1 → TBLPTR;
- if TBLRD *-,
  (Prog Mem (TBLPTR)) → TABLAT;
  (TBLPTR) – 1 → TBLPTR;
- if TBLRD +*,
  (TBLPTR) + 1 → TBLPTR;
  (Prog Mem (TBLPTR)) → TABLAT;

Status Affected:  None

Encoding:

<table>
<thead>
<tr>
<th>nn=0</th>
<th>0000</th>
<th>0000</th>
<th>0000</th>
<th>10nn</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>*</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 +</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2 –</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3 +</td>
</tr>
</tbody>
</table>

Description: This instruction is used to read the contents of Program Memory (P.M.). To address the program memory, a pointer called Table Pointer (TBLPTR) is used. The TBLPTR (a 21-bit pointer) points to each byte in the program memory. TBLPTR has a 2-Mbyte address range.

TBLPTR[0] = 0:  Least Significant Byte of Program Memory Word
TBLPTR[0] = 1:  Most Significant Byte of Program Memory Word

The TBLRD instruction can modify the value of TBLPTR as follows:
- no change
- post-increment
- post-decrement
- pre-increment

Words:  1
Cycles:  2

Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
<tr>
<td>No operation (Read Program Memory)</td>
<td>No operation</td>
<td>No operation (Write TABLAT)</td>
<td>No operation</td>
</tr>
</tbody>
</table>
TBLWT Table Write

Syntax: TBLWT (*; *+; *-; +*)
Operands: None
Operation:
if TBLWT*,
(TABLAT) → Holding Register;
TBLPTR – No Change;
if TBLWT*+,
(TABLAT) → Holding Register;
(TBLPTR) + 1 → TBLPTR;
if TBLWT*–,
(TABLAT) → Holding Register;
(TBLPTR) – 1 → TBLPTR;
if TBLWT+*,
(TBLPTR) + 1 → TBLPTR;
(TABLAT) → Holding Register;
Status Affected: None
Encoding:

0000 0000 0000 11nn
nn=0 *
n=1 *+
n=2 *–
n=3 +*

Description: This instruction uses the three LSBs of TBLPTR to determine which of the eight holding registers the TABLAT is written to. The holding registers are used to program the contents of Program Memory (P.M.). (Refer to Section 13.1 "Program Flash Memory" for additional details on programming Flash memory.) The TBLPTR (a 21-bit pointer) points to each byte in the program memory. TBLPTR has a 2-MByte address range. The LSB of the TBLPTR selects which byte of the program memory location to access.

TBLPTR[0] = 0: Least Significant Byte of Program Memory Word
TBLPTR[0] = 1: Most Significant Byte of Program Memory Word

The TBLWT instruction can modify the value of TBLPTR as follows:
• no change
• post-increment
• post-decrement
• pre-increment

Words: 1
Cycles: 2
Q Cycle Activity:

<table>
<thead>
<tr>
<th>Decode</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td></td>
</tr>
<tr>
<td>No operation</td>
<td>No operation (Read TABLAT)</td>
<td>No operation</td>
<td>No operation (Write to Holding Register)</td>
<td></td>
</tr>
</tbody>
</table>

Example 1: TBLWT *+;
Before Instruction
TABLAT = 55h
TBLPTR = 00A356h
HOLDING REGISTER (00A356h) = FFh
After Instructions (table write completion)
TABLAT = 55h
TBLPTR = 00A357h
HOLDING REGISTER (00A356h) = 55h

Example 2: TBLWT +*;
Before Instruction
TABLAT = 34h
TBLPTR = 01389Ah
HOLDING REGISTER (01389Ah) = FFh
HOLDING REGISTER (01389Bh) = FFh
After Instruction (table write completion)
TABLAT = 34h
TBLPTR = 01389Bh
HOLDING REGISTER (01389Ah) = FFh
HOLDING REGISTER (01389Bh) = 34h
TSTFSZ  Test f, skip if 0

Syntax: TSTFSZ f, [a]
Operands: \(0 \leq f \leq 255\)
\(a \in \{0, 1\}\)
Operation: skip if \(f = 0\)
Status Affected: None
Encoding:

```
0110 011a  ffff  ffff
```

Description:
If \(f = 0\), the next instruction fetched during the current instruction execution is discarded and a \texttt{NOP} is executed, making this a 2-cycle instruction.
If \(a = 0\), the Access Bank is selected.
If \(a = 1\), the BSR is used to select the GPR bank.
If \(a = 0\) and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever \(f \leq 95\) (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.
Words: 1
Cycles: 1(2)

Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If skip:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

If skip and followed by 2-word instruction:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
</tbody>
</table>

Example:

```
HERE    TSTFSZ  CNT, 1
NZERO   :
ZERO    :
```

Before Instruction

- \(PC = \text{Address (HERE)}\)

After Instruction

- If \(CNT = 00h\), \(PC = \text{Address (ZERO)}\)
- If \(CNT \neq 00h\), \(PC = \text{Address (NZERO)}\)

XORLW  Exclusive OR literal with W

Syntax: XORLW k
Operands: \(0 \leq k \leq 255\)
Operation: \((W) \text{ XOR } k \rightarrow W\)
Status Affected: N, Z
Encoding:

```
0000 1010  kkkk  kkkk
```

Description:
The contents of W are XORed with the 8-bit literal 'k'. The result is placed in W.
Words: 1
Cycles: 1

Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read literal 'k'</td>
<td>Process Data</td>
<td>Write to W</td>
</tr>
</tbody>
</table>

Example:

```
XORLW  0AFh
```

Before Instruction

- \(W = \text{B5h}\)

After Instruction

- \(W = \text{1Ah}\)
**XORWF**  Exclusive OR W with f

- **Syntax:** XORWF f {,d {,a}}
- **Operands:**
  - $0 \leq f \leq 255$
  - $d \in [0,1]$
  - $a \in [0,1]$
- **Operation:** $(W).\text{XOR.}(f) \rightarrow \text{dest}$
- **Status Affected:** N, Z
- **Encoding:**
  - 0001 10da ffff ffff
- **Description:** Exclusive OR the contents of W with register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in the register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See Section 42.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.
- **Words:** 1
- **Cycles:** 1

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read register 'f'</td>
<td>Process Data</td>
<td>Write to destination</td>
</tr>
</tbody>
</table>

**Example:** XORWF REG, 1, 0

- **Before Instruction**
  - REG = AFh
  - W = B5h
- **After Instruction**
  - REG = 1Ah
  - W = B5h
42.2 Extended Instruction Set

In addition to the standard 75 instructions of the PIC18 instruction set, PIC18(L)F25/26K83 devices also provide an optional extension to the core CPU functionality. The added features include eight additional instructions that augment indirect and indexed addressing operations and the implementation of Indexed Literal Offset Addressing mode for many of the standard PIC18 instructions.

The additional features of the extended instruction set are disabled by default. To enable them, users must set the XINST Configuration bit.

The instructions in the extended set can all be classified as literal operations, which either manipulate the File Select Registers, or use them for indexed addressing. Two of the instructions, ADDFSR and SUBFSR, each have an additional special instantiation for using FSR2. These versions (ADDULNK and SUBULNK) allow for automatic return after execution.

The extended instructions are specifically implemented to optimize re-entrant program code (that is, code that is recursive or that uses a software stack) written in high-level languages, particularly C. Among other things, they allow users working in high-level languages to perform certain operations on data structures more efficiently. These include:

- dynamic allocation and deallocation of software stack space when entering and leaving subroutines
- function pointer invocation
- software Stack Pointer manipulation
- manipulation of variables located in a software stack

A summary of the instructions in the extended instruction set is provided in Table 42-3. Detailed descriptions are provided in Section 42.2.2 “Extended Instruction Set”. The opcode field descriptions in Table 42-1 apply to both the standard and extended PIC18 instruction sets.

Note: The instruction set extension and the Indexed Literal Offset Addressing mode were designed for optimizing applications written in C; the user may likely never use these instructions directly in assembler. The syntax for these commands is provided as a reference for users who may be reviewing code that has been generated by a compiler.

42.2.1 EXTENDED INSTRUCTION SYNTAX

Most of the extended instructions use indexed arguments, using one of the File Select Registers and some offset to specify a source or destination register. When an argument for an instruction serves as part of indexed addressing, it is enclosed in square brackets ([ ]). This is done to indicate that the argument is used as an index or offset. MPASM™ Assembler will flag an error if it determines that an index or offset value is not bracketed.

When the extended instruction set is enabled, brackets are also used to indicate index arguments in byte-oriented and bit-oriented instructions. This is in addition to other changes in their syntax. For more details, see Section 42.2.3.1 “Extended Instruction Syntax with Standard PIC18 Commands”.

Note: In the past, square brackets have been used to denote optional arguments in the PIC18 and earlier instruction sets. In this text and going forward, optional arguments are denoted by braces (‘{ }’).
### Table 42-3: Extensions to the PIC18 Instruction Set

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycles</th>
<th>16-Bit Instruction Word</th>
<th>Status Affected</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSb</td>
<td>LSb</td>
</tr>
<tr>
<td>ADDULNK k</td>
<td>Add FSR2 with (k) &amp; return</td>
<td>2</td>
<td>1110 0000 11kk kkkk</td>
<td>None</td>
</tr>
<tr>
<td>MOVSF zs, fd</td>
<td>Move zs (source) to 1st word</td>
<td>2</td>
<td>1110 1011 0zzz zzzz</td>
<td>None</td>
</tr>
<tr>
<td>MOVSF z, fd</td>
<td>Opcode 1st word</td>
<td>2</td>
<td>1111 ffff ffff ffff</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td>Move zs (source) to 2nd word</td>
<td>2</td>
<td>0000 0000 0000 0010</td>
<td>None</td>
</tr>
<tr>
<td>MOVSS z, zd</td>
<td>Opcode 2nd word</td>
<td>2</td>
<td>1111 xxxz zzzz zzzf</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td>Move zs (source) to 3rd word</td>
<td>3</td>
<td>1110 ffff ffff ffff</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td>Move z (source) to 1st word</td>
<td>1</td>
<td>1110 1011 1zzz zzzz</td>
<td>None</td>
</tr>
<tr>
<td>PUSHL k</td>
<td>Push literal to POSTDEC2</td>
<td>1</td>
<td>1111 xxxx xxx zzzz zzzz</td>
<td>None</td>
</tr>
<tr>
<td>SUBULNK k</td>
<td>Subtract (k) from FSR2 &amp; return</td>
<td>2</td>
<td>1110 1001 11kk kkkk</td>
<td>None</td>
</tr>
</tbody>
</table>

**Note 1:** If Program Counter (PC) is modified or a conditional test is true, the instruction requires an additional cycle. The extra cycle is executed as a NOP.

**2:** Some instructions are multi word instructions. The second/third words of these instructions will be decoded as a NOP, unless the first word of the instruction retrieves the information embedded in these 16-bits. This ensures that all program memory locations have a valid instruction.

**3:** Only available when extended instruction set is enabled.

**4:** fs and fd do not cover the full memory range. Two MSBs of bank selection are forced to 'b00 to limit the range of these instructions to lower 4k addressing space.
## 42.2.2 EXTENDED INSTRUCTION SET

### ADDULNK

**Add Literal to FSR2 and Return**

<table>
<thead>
<tr>
<th>Syntax</th>
<th>ADDULNK k</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands</td>
<td>0 ≤ k ≤ 63</td>
</tr>
<tr>
<td>Operation</td>
<td>FSR2 + k → FSR2. (TOS) → PC</td>
</tr>
<tr>
<td>Status Affected</td>
<td>None</td>
</tr>
<tr>
<td>Encoding</td>
<td>1110 1000 11kk kkkk</td>
</tr>
<tr>
<td>Description</td>
<td>The 6-bit literal 'k' is added to the contents of FSR2. A RETURN is then executed by loading the PC with the TOS. The instruction takes two cycles to execute; a NOP is performed during the second cycle. This may be thought of as a special case of the ADDFSR instruction, where f = 3 (binary '11'); it operates only on FSR2.</td>
</tr>
<tr>
<td>Words</td>
<td>1</td>
</tr>
<tr>
<td>Cycles</td>
<td>2</td>
</tr>
</tbody>
</table>

### Q Cycle Activity:

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read</td>
<td>Process</td>
<td>Write</td>
</tr>
<tr>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Operation</td>
<td>Data</td>
<td>Operation</td>
<td>FSR</td>
</tr>
<tr>
<td>No</td>
<td>Operation</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>

### Example:

**ADDULNK 23h**

**Before Instruction**

- FSR2 = 03FFh
- PC = 0100h

**After Instruction**

- FSR2 = 0422h
- PC = (TOS)

### Note:

All PIC18 instructions may take an optional label argument preceding the instruction mnemonic for use in symbolic addressing. If a label is used, the instruction syntax then becomes: (label) instruction argument(s).
**MOVSF**

**Move Indexed to f**

Syntax:  
`MOVSF [zs], fd`

Operands:  
`
0 \leq zs \leq 127
0 \leq fd \leq 4095
`

Operation:  
`((FSR2) + zs) \rightarrow fd`

Status Affected:  
None

Encoding:  
```
<table>
<thead>
<tr>
<th>1st word (source)</th>
<th>2nd word (destin.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1110 1111 0zzz zzss</td>
<td>1111 ffff ffff fffffd</td>
</tr>
</tbody>
</table>
```

Description:  
The contents of the source register are moved to destination register `fd`. The actual address of the source register is determined by adding the 7-bit literal offset `zs` in the first word to the value of FSR2. The address of the destination register is specified by the 12-bit literal `fd` in the second word. Both addresses can be anywhere in the 4096-byte data space (000h to FFFh).

**Example:**  
`MOVSF [05h], REG2`

Before Instruction

| FSR2 Contents | 80h |
| REG2         | 11h |

After Instruction

| FSR2 Contents | 80h |
| REG2          | 33h |

**Words:** 2  
**Cycles:** 2

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Determine source addr</td>
<td>Determine source addr</td>
<td>Read source reg</td>
</tr>
<tr>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
<td>Write register <code>f</code> (dest)</td>
</tr>
</tbody>
</table>

**MOVSL**

**Move Indexed to f (Long Range)**

Syntax:  
`MOVSL [zs], fd`

Operands:  
`
0 \leq zs \leq 127
0 \leq fd \leq 16383
`

Operation:  
`((FSR2) + zs) \rightarrow fd`

Status Affected:  
None

Encoding:  
```
<table>
<thead>
<tr>
<th>1st word (opcode)</th>
<th>2nd word (source)</th>
<th>3rd word (full destin.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 0000 0110 0010</td>
<td>1111 xxxxx zzzz zzsff</td>
<td>1111 ffff ffff fffffd</td>
</tr>
</tbody>
</table>
```

Description:  
The contents of the source register are moved to destination register `fd`. The actual address of the source register is determined by adding the 7-bit literal offset `zs` in the first word to the value of FSR2 (14 bits). The address of the destination register is specified by the 14-bit literal `fd` in the second word. Both addresses can be anywhere in the 16 Kbyte data space (0000h to 3FFFh).

**Example:**  
`MOVSL [05h], REG2`

Before Instruction

| FSR2 = 80h |
| REG2 = 11h |

After Instruction

| FSR2 = 80h |
| REG2 = 33h |

**Words:** 3  
**Cycles:** 3

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>No operation</td>
<td>No operation</td>
<td>No operation</td>
</tr>
<tr>
<td>Read register <code>z</code> (src.)</td>
<td>Process data</td>
<td>No operation</td>
<td></td>
</tr>
</tbody>
</table>

| Decode | No operation | No operation | Write register `f` (dest.) |
| Read register `z` (src.) | Process data | No operation |

| Decode | No operation | No dummy read | Write register `f` (dest.) |
| No operation | No dummy read | No operation |
| No operation | No dummy read | No operation |

**Example:**  
`MOVSL [05h], REG2`

Before Instruction

| FSR2 = 80h |
| REG2 = 11h |

After Instruction

| FSR2 = 80h |
| REG2 = 33h |

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### MOVSS

**Move Indexed to Indexed**

**Syntax:**

\[
\text{MOVSS } [z_s], [z_d]
\]

**Operands:**

\[
0 \leq z_s \leq 127 \\
0 \leq z_d \leq 127
\]

**Operation:**

\[
((\text{FSR2}) + z_s) \rightarrow ((\text{FSR2}) + z_d)
\]

**Status Affected:**

None

**Encoding:**

<table>
<thead>
<tr>
<th>1st word (source)</th>
<th>2nd word (dest.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1110</td>
<td>1111</td>
</tr>
<tr>
<td>1011</td>
<td>1011</td>
</tr>
<tr>
<td>lzzz</td>
<td>lzzz</td>
</tr>
<tr>
<td>zzzz_s</td>
<td>zzzz_d</td>
</tr>
</tbody>
</table>

**Description:**

The contents of the source register are moved to the destination register. The addresses of the source and destination registers are determined by adding the 7-bit literal offsets 'zs' or 'zd', respectively, to the value of FSR2. Both registers can be located anywhere in the 4096-byte data memory space (000h to FFFh).

The MOVSS instruction cannot use the PCL, TOSU, TOSH or TOSL as the destination register.

If the resultant source address points to an indirect addressing register, the value returned will be 00h. If the resultant destination address points to an indirect addressing register, the instruction will execute as a NOP.

**Words:** 2  
**Cycles:** 2

**Example:**

**Before Instruction**

- FSR2H:FSR2L = 01ECh
- Memory (01ECh) = 00h

**After Instruction**

- FSR2H:FSR2L = 01EBh
- Memory (01ECh) = 08h

### PUSHL

**Store Literal at FSR2, Decrement FSR2**

**Syntax:**

\[
\text{PUSHL } k
\]

**Operands:**

\[
0 \leq k \leq 255
\]

**Operation:**

\[
k \rightarrow (\text{FSR2}), \\
\text{FSR2} – 1 \rightarrow \text{FSR2}
\]

**Status Affected:**

None

**Encoding:**

<table>
<thead>
<tr>
<th>source</th>
<th>dest.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>1010</td>
</tr>
<tr>
<td>kkkk</td>
<td>kkkk</td>
</tr>
</tbody>
</table>

**Description:**

The 8-bit literal 'k' is written to the data memory address specified by FSR2. FSR2 is decremented by 1 after the operation. This instruction allows users to push values onto a software stack.

**Words:** 1  
**Cycles:** 1

**Example:**

**Before Instruction**

- FSR2H:FSR2L = 01ECh
- Memory (01ECh) = 00h

**After Instruction**

- FSR2H:FSR2L = 01EBh
- Memory (01ECh) = 08h
### SUBULNK

**Subtract Literal from FSR2 and Return**

**Syntax:**

```
SUBULNK k
```

**Operands:**

```
0 ≤ k ≤ 63
```

**Operation:**

```
FSR2 – k → FSR2
(TOS) → PC
```

**Status Affected:** None

**Encoding:**

```
1110 1001 11kk kkkk
```

**Description:**

The 6-bit literal 'k' is subtracted from the contents of the FSR2. A RETURN is then executed by loading the PC with the TOS. The instruction takes two cycles to execute; a NOP is performed during the second cycle. This may be thought of as a special case of the SUBFSR instruction, where f = 3 (binary '11'); it operates only on FSR2.

**Words:** 1

**Cycles:** 2

**Q Cycle Activity:**

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decode</td>
<td>Read</td>
<td>Process</td>
<td>Write to</td>
</tr>
<tr>
<td>No Operation</td>
<td>No Operation</td>
<td>No Operation</td>
<td>No Operation</td>
</tr>
</tbody>
</table>

**Example:**

```
SUBULNK 23h
```

**Before Instruction**

```
FSR2 = 03FFh
PC = 0100h
```

**After Instruction**

```
FSR2 = 03DCh
PC = (TOS)
```
42.2.3 BYTE-ORIENTED AND BIT-ORIENTED INSTRUCTIONS IN INDEXED LITERAL OFFSET MODE

Note: Enabling the PIC18 instruction set extension may cause legacy applications to behave erratically or fail entirely.

In addition to eight new commands in the extended set, enabling the extended instruction set also enables Indexed Literal Offset Addressing mode (Section 4.8.1 “Indexed Addressing with Literal Offset”). This has a significant impact on the way that many commands of the standard PIC18 instruction set are interpreted.

When the extended set is disabled, addresses embedded in opcodes are treated as literal memory locations: either as a location in the Access Bank (‘a’ = 0), or in a GPR bank designated by the BSR (‘a’ = 1). When the extended instruction set is enabled and ‘a’ = 0, however, a file register argument of 5Fh or less is interpreted as an offset from the pointer value in FSR2 and not as a literal address. For practical purposes, this means that all instructions that use the Access RAM bit as an argument – that is, all byte-oriented and bit-oriented instructions, or almost half of the core PIC18 instructions – may behave differently when the extended instruction set is enabled.

When the content of FSR2 is 00h, the boundaries of the Access RAM are essentially remapped to their original values. This may be useful in creating backward compatible code. If this technique is used, it may be necessary to save the value of FSR2 and restore it when moving back and forth between C and assembly routines in order to preserve the Stack Pointer. Users must also keep in mind the syntax requirements of the extended instruction set (see Section 42.2.3.1 “Extended Instruction Syntax with Standard PIC18 Commands”).

Although the Indexed Literal Offset Addressing mode can be very useful for dynamic stack and pointer manipulation, it can also be very annoying if a simple arithmetic operation is carried out on the wrong register. Users who are accustomed to the PIC18 programming must keep in mind that, when the extended instruction set is enabled, register addresses of 5Fh or less are used for Indexed Literal Offset Addressing.

Representative examples of typical byte-oriented and bit-oriented instructions in the Indexed Literal Offset Addressing mode are provided on the following page to show how execution is affected. The operand conditions shown in the examples are applicable to all instructions of these types.

42.2.3.1 Extended Instruction Syntax with Standard PIC18 Commands

When the extended instruction set is enabled, the file register argument, ‘f’, in the standard byte-oriented and bit-oriented commands is replaced with the literal offset value, ‘k’. As already noted, this occurs only when ‘f’ is less than or equal to 5Fh. When an offset value is used, it must be indicated by square brackets (’[ ]’). As with the extended instructions, the use of brackets indicates to the compiler that the value is to be interpreted as an index or an offset. Omitting the brackets, or using a value greater than 5Fh within brackets, will generate an error in the MPASM assembler.

If the index argument is properly bracketed for Indexed Literal Offset Addressing, the Access RAM argument is never specified; it will automatically be assumed to be ‘0’. This is in contrast to standard operation (extended instruction set disabled) when ‘a’ is set on the basis of the target address. Declaring the Access RAM bit in this mode will also generate an error in the MPASM assembler.

The destination argument, ‘d’, functions as before.

In the latest versions of the MPASM™ assembler, language support for the extended instruction set must be explicitly invoked. This is done with either the command line option, /y, or the PE directive in the source listing.

42.2.4 CONSIDERATIONS WHEN ENABLING THE EXTENDED INSTRUCTION SET

It is important to note that the extensions to the instruction set may not be beneficial to all users. In particular, users who are not writing code that uses a software stack may not benefit from using the extensions to the instruction set.

Additionally, the Indexed Literal Offset Addressing mode may create issues with legacy applications written to the PIC18 assembler. This is because instructions in the legacy code may attempt to address registers in the Access Bank below 5Fh. Since these addresses are interpreted as literal offsets to FSR2 when the instruction set extension is enabled, the application may read or write to the wrong data addresses.

When porting an application to the PIC18(L)F25/26K83, it is very important to consider the type of code. A large, re-entrant application that is written in ‘C’ and would benefit from efficient compilation will do well when using the instruction set extensions. Legacy applications that heavily use the Access Bank will most likely not benefit from using the extended instruction set.
ADDWF  ADD W to Indexed (Indexed Literal Offset mode)

Syntax: ADDWF [k] {,d}
Operands: \(0 \leq k \leq 95\)
\(d \in [0,1]\)
Operation: \((W) + ((FSR2) + k) \rightarrow \text{dest}\)
Status Affected: N, OV, C, DC, Z
Encoding: 
```
0010 01d0 kkkk kkkk
```
Description: The contents of W are added to the contents of the register indicated by FSR2, offset by the value \(k\). If \(d\) is 0, the result is stored in W. If \(d\) is 1, the result is stored back in register \(f\) (default).

Words: 1
Cycles: 1
Q Cycle Activity:
```
Q1  Q2  Q3  Q4
Decode  Read 'k'  Process Data  Write to destination
```
Example: ADDWF [OFST], 0
Before Instruction
\(W = 17h\)
\(OFST = 2Ch\)
\(FSR2 = 0A00h\)
Contents of 0A2Ch = 00h
After Instruction
\(W = 37h\)
Contents of 0A2Ch = 20h

BSF  Bit Set Indexed (Indexed Literal Offset mode)

Syntax: BSF [k], b
Operands: \(0 \leq f \leq 95\)
\(0 \leq b \leq 7\)
Operation: \(1 \rightarrow ((FSR2) + k)<b>\)
Status Affected: None
Encoding: 
```
1000 bbb0 kkkk kkkk
```
Description: Bit \(b\) of the register indicated by FSR2, offset by the value \(k\), is set.

Words: 1
Cycles: 1
Q Cycle Activity:
```
Q1  Q2  Q3  Q4
Decode  Read 'f'  Process Data  Write to destination
```
Example: BSF [FLAG_OFST], 7
Before Instruction
\(\text{FLAG\_OFST} = 0Ah\)
\(FSR2 = 0A00h\)
Contents of 0A0Ah = 00h
After Instruction
Contents of 0A0Ah = D5h

SETF  Set Indexed (Indexed Literal Offset mode)

Syntax: SETF [k]
Operands: \(0 \leq k \leq 95\)
Operation: \(FFh \rightarrow ((FSR2) + k)\)
Status Affected: None
Encoding: 
```
0110 1000 kkkk kkkk
```
Description: The contents of the register indicated by FSR2, offset by \(k\), are set to FFh.

Words: 1
Cycles: 1
Q Cycle Activity:
```
Q1  Q2  Q3  Q4
Decode  Read 'k'  Process Data  Write to register
```
Example: SETF [OFST]
Before Instruction
\(\text{OFST} = 2Ch\)
\(FSR2 = 0A00h\)
Contents of 0A2Ch = 00h
After Instruction
Contents of 0A2Ch = FFh
42.2.5 SPECIAL CONSIDERATIONS WITH MICROCHIP MPLAB® IDE TOOLS

The latest versions of Microchip’s software tools have been designed to fully support the extended instruction set of the PIC18(L)F25/26K83 family of devices. This includes the MPLAB C18 C compiler, MPASM assembly language and MPLAB Integrated Development Environment (IDE).

When selecting a target device for software development, MPLAB IDE will automatically set default Configuration bits for that device. The default setting for the XINST Configuration bit is ‘0’, disabling the extended instruction set and Indexed Literal Offset Addressing mode. For proper execution of applications developed to take advantage of the extended instruction set, XINST must be set during programming.

To develop software for the extended instruction set, the user must enable support for the instructions and the Indexed Addressing mode in their language tool(s). Depending on the environment being used, this may be done in several ways:

• A menu option, or dialog box within the environment, that allows the user to configure the language tool and its settings for the project
• A command line option
• A directive in the source code

These options vary between different compilers, assemblers and development environments. Users are encouraged to review the documentation accompanying their development systems for the appropriate information.
### 43.0 REGISTER SUMMARY

#### TABLE 43-1: REGISTER FILE SUMMARY FOR PIC18(L)F25/26K83 DEVICES

<table>
<thead>
<tr>
<th>Addr</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3FFFh</td>
<td>TOSU</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Top-of-Stack Upper byte</td>
</tr>
<tr>
<td>3FFEh</td>
<td>TOSH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Top-of-Stack High byte</td>
</tr>
<tr>
<td>3FDFh</td>
<td>TSL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Top-of-Stack Low byte</td>
</tr>
<tr>
<td>3FFCh</td>
<td>STKPTR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Stack Pointer</td>
</tr>
<tr>
<td>3FFBh</td>
<td>PCLATU</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Holding Register for PC Upper byte</td>
</tr>
<tr>
<td>3FFAh</td>
<td>PCLATH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Holding Register for PC High byte</td>
</tr>
<tr>
<td>3FF9h</td>
<td>PC</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>PC Low byte</td>
</tr>
<tr>
<td>3FFEh</td>
<td>TBLPTRU</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Program Memory Table Pointer Upper byte</td>
</tr>
<tr>
<td>3FF7h</td>
<td>TBLPTRH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Program Memory Table Pointer High byte</td>
</tr>
<tr>
<td>3FF6h</td>
<td>TBLPTRL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Program Memory Table Pointer Low byte</td>
</tr>
<tr>
<td>3FF5h</td>
<td>TABLAT</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Table Latch</td>
</tr>
<tr>
<td>3FF4h</td>
<td>PRODH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Product Register High byte</td>
</tr>
<tr>
<td>3FF3h</td>
<td>PRODL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Product Register Low byte</td>
</tr>
<tr>
<td>3FF2h</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Unimplemented</td>
</tr>
<tr>
<td>3FF1h</td>
<td>PCON1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Indirect Data Memory Address Pointer 0 High</td>
</tr>
<tr>
<td>3FF0h</td>
<td>PCON0</td>
<td>STKOVF</td>
<td>STKUNF</td>
<td>WDTWV</td>
<td>RWDT</td>
<td>RMCLR</td>
<td>RI</td>
<td>POR</td>
<td>BOR</td>
<td>Indirect Data Memory Address Pointer 0 Low</td>
</tr>
<tr>
<td>3FEFh</td>
<td>INDF0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Uses contents of FSR0 to address data memory – value of FSR0 not changed</td>
</tr>
<tr>
<td>3FECh</td>
<td>POSTINC0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Uses contents of FSR0 to address data memory – value of FSR0 post-incremented</td>
</tr>
<tr>
<td>3FEDh</td>
<td>POSTDEC0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Uses contents of FSR0 to address data memory – value of FSR0 post-decremented</td>
</tr>
<tr>
<td>3FEbh</td>
<td>PREINC0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented</td>
</tr>
<tr>
<td>3FEah</td>
<td>PLUSW0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented – value of FSR0 offset by W</td>
</tr>
<tr>
<td>3FE9h</td>
<td>FSR0L</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Indirect Data Memory Address Pointer 0 High</td>
</tr>
<tr>
<td>3FE8h</td>
<td>WREG</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Working Register</td>
</tr>
<tr>
<td>3FE7h</td>
<td>INDF1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Uses contents of FSR1 to address data memory – value of FSR1 not changed</td>
</tr>
<tr>
<td>3FE6h</td>
<td>POSTINC1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Uses contents of FSR1 to address data memory – value of FSR1 post-incremented</td>
</tr>
<tr>
<td>3FE5h</td>
<td>POSTDEC1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Uses contents of FSR1 to address data memory – value of FSR1 post-decremented</td>
</tr>
<tr>
<td>3FE4h</td>
<td>PREINC1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Uses contents of FSR1 to address data memory – value of FSR1 pre-incremented</td>
</tr>
<tr>
<td>3FE3h</td>
<td>PLUSW1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Uses contents of FSR1 to address data memory – value of FSR1 pre-incremented – value of FSR1 offset by W</td>
</tr>
<tr>
<td>3FE2h</td>
<td>FSR1H</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Indirect Data Memory Address Pointer 1 High</td>
</tr>
<tr>
<td>3FE1h</td>
<td>FSR1L</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Indirect Data Memory Address Pointer 1 Low</td>
</tr>
<tr>
<td>3FE0h</td>
<td>BSR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Bank Select Register</td>
</tr>
<tr>
<td>3FDFh</td>
<td>INDF2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Uses contents of FSR2 to address data memory – value of FSR2 not changed</td>
</tr>
<tr>
<td>3FDEh</td>
<td>POSTINC2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Uses contents of FSR2 to address data memory – value of FSR2 post-incremented</td>
</tr>
<tr>
<td>3FDDh</td>
<td>POSTDEC2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Uses contents of FSR2 to address data memory – value of FSR2 post-decremented</td>
</tr>
<tr>
<td>3FDCh</td>
<td>PREINC2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Uses contents of FSR2 to address data memory – value of FSR2 pre-incremented</td>
</tr>
<tr>
<td>3FDBh</td>
<td>PLUSW2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Uses contents of FSR2 to address data memory - value of FSR2 pre-incremented – value of FSR2 offset by W</td>
</tr>
<tr>
<td>3FDAh</td>
<td>FSR2H</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Indirect Data Memory Address Pointer 2 High</td>
</tr>
<tr>
<td>3FD9h</td>
<td>FSR2L</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Indirect Data Memory Address Pointer 2 Low</td>
</tr>
<tr>
<td>3FD8h</td>
<td>STATUS</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Indirect Data Memory Address Pointer 2 Low</td>
</tr>
<tr>
<td>3FD7h</td>
<td>IVTBASEU</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>BASE20</td>
</tr>
<tr>
<td>3FD6h</td>
<td>IVTBASEH</td>
<td>BASE15</td>
<td>BASE14</td>
<td>BASE13</td>
<td>BASE12</td>
<td>BASE11</td>
<td>BASE10</td>
<td>BASE9</td>
<td>BASE8</td>
<td>BASE7</td>
</tr>
<tr>
<td>3FD5h</td>
<td>IVTBASEL</td>
<td>BASE7</td>
<td>BASE6</td>
<td>BASE5</td>
<td>BASE4</td>
<td>BASE3</td>
<td>BASE2</td>
<td>BASE1</td>
<td>BASE0</td>
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</tr>
<tr>
<td>3FD4h</td>
<td>IVTLOCK</td>
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<td>—</td>
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<td>—</td>
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<tr>
<td>3FD3h</td>
<td>INTCN1</td>
<td>STAT</td>
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</tr>
<tr>
<td>3FD2h</td>
<td>INTCN0</td>
<td>GIE</td>
<td>GIEL</td>
<td>IPEN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>3FD1h-3FD0h</td>
<td>—</td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Legend:**
- x = unknown
- u = unchanged
- — = unimplemented
- q = value depends on condition

**Note 1:** Not present in LF devices.
### TABLE 43-1: REGISTER FILE SUMMARY FOR PIC18(L)F25/26K83 DEVICES (CONTINUED)

<table>
<thead>
<tr>
<th>Addr</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
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<th>Bit 1</th>
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**Legend:**  
- x = unknown, u = unchanged, — = unimplemented, q = value depends on condition  

**Note 1:** Not present in LF devices.
### TABLE 43-1: REGISTER FILE SUMMARY FOR PIC18(L)F25/26K83 DEVICES (CONTINUED)

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Legend:  
- x = unknown, u = unchanged, — = unimplemented, q = value depends on condition  
Note 1: Not present in LF devices.
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**Legend:**  
- *x* = unknown, *u* = unchanged, — = unimplemented, *q* = value depends on condition  
**Note 1:** Not present in LF devices.
### TABLE 43-1: REGISTER FILE SUMMARY FOR PIC18(L)F25/26K83 DEVICES (CONTINUED)

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**Legend:**
- **x** = unknown
- **u** = unchanged
- **—** = unimplemented
- **q** = value depends on condition

**Note:**
1. Not present in LF devices.
### TABLE 43-1: REGISTER FILE SUMMARY FOR PIC18(L)F25/26K83 DEVICES (CONTINUED)

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**Legend:**  
- unknown, u = unchanged, — = unimplemented, q = value depends on condition  
**Note 1:** Not present in LF devices.
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**Legend:**
- **x** = unknown, **u** = unchanged, **—** = unimplemented, **q** = value depends on condition

**Note 1:** Not present in LF devices.
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**Legend:**  
- x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

**Note 1:** Not present in LF devices.
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**Legend:**  
- x = unknown, u = unchanged, — = unimplemented, q = value depends on condition  
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**Legend:**
- x = unknown
- u = unchanged
- — = unimplemented
- q = value depends on condition

**Note 1:** Not present in LF devices.
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**Legend:**  
- x = unknown, u = unchanged, — = unimplemented, q = value depends on condition  

**Note:**  
1. Not present in LF devices.
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**Legend:**  
- x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

**Note 1:** Not present in LF devices.
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Legend:  x = unknown, u = unchanged, — = unimplemented, q = value depends on condition
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**Legend:**
- x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

**Note 1:** Not present in LF devices.
TABLE 43-1: REGISTER FILE SUMMARY FOR PIC18(L)F25/26K83 DEVICES (CONTINUED)

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Legend:  x = unknown, u = unchanged, — = unimplemented, q = value depends on condition
Note 1: Not present in LF devices.
### TABLE 43-1: REGISTER FILE SUMMARY FOR PIC18(L)F25/26K83 DEVICES (CONTINUED)

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**Legend:**  
- x = unknown, u = unchanged, — = unimplemented, q = value depends on condition  

**Note 1:** Not present in LF devices.
### TABLE 43-1: REGISTER FILE SUMMARY FOR PIC18(L)F25/26K83 DEVICES (CONTINUED)

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**Legend:**
- x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

**Note 1:** Not present in LF devices.
### TABLE 43-1: REGISTER FILE SUMMARY FOR PIC18(L)F25/26K83 DEVICES (CONTINUED)

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**Legend:**
- x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

**Note 1:** Not present in LF devices.
### TABLE 43-1: REGISTER FILE SUMMARY FOR PIC18(L)F25/26K83 DEVICES (CONTINUED)

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**Legend:**  
- x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

**Note 1:** Not present in LF devices.
### TABLE 43-1: REGISTER FILE SUMMARY FOR PIC18(L)F25/26K83 DEVICES (CONTINUED)

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**Legend:**  
- x = unknown, u = unchanged, — = unimplemented, q = value depends on condition  
**Note 1:** Not present in LF devices.
### TABLE 43-1: REGISTER FILE SUMMARY FOR PIC18(L)F25/26K83 DEVICES (CONTINUED)

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<td>SEG2PHTS</td>
<td>SAM</td>
<td>SEG1PH2</td>
<td>SEG1PH1</td>
<td>SEG1PH0</td>
<td>PRSEG2</td>
<td>PRSEG1</td>
<td>PRSEG0</td>
<td>641</td>
</tr>
<tr>
<td>3703h</td>
<td>BRGCON1</td>
<td>SJW1</td>
<td>SJW0</td>
<td>BRP5</td>
<td>BRP4</td>
<td>BRP3</td>
<td>BRP2</td>
<td>BRP1</td>
<td>BRP0</td>
<td>640</td>
</tr>
<tr>
<td>3702h</td>
<td>TXERRCNT</td>
<td>TEC7</td>
<td>TEC6</td>
<td>TEC5</td>
<td>TEC4</td>
<td>TEC3</td>
<td>TEC2</td>
<td>TEC1</td>
<td>TEC0</td>
<td>612</td>
</tr>
<tr>
<td>3701h</td>
<td>RXERRCNT</td>
<td>REC7</td>
<td>REC6</td>
<td>REC5</td>
<td>REC4</td>
<td>REC3</td>
<td>REC2</td>
<td>REC1</td>
<td>REC0</td>
<td>621</td>
</tr>
<tr>
<td>3700h</td>
<td>CIIOC1</td>
<td>TX1SRC</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>643</td>
</tr>
</tbody>
</table>

**Legend:**
- x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

**Note 1:** Not present in LF devices.
44.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/
    MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for
    Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards,
  Evaluation Kits and Starter Kits
- Third-party development tools

44.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and
  provides hints as you type
- Automatic code formatting based on user-defined
  rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar
  buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker
44.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip’s 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

44.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

44.4 MPLINK Object Linker/
MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object link/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

44.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility
44.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

44.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip’s next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer’s PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

44.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip’s most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer’s PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

44.9 PICkit 3 In-Circuit Debugger/Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The PICkit 3 is connected to the design engineer’s PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

44.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.
44.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

44.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®
45.0 ELECTRICAL SPECIFICATIONS

45.1 Absolute Maximum Ratings(†)

Ambient temperature under bias...................................................................................................... -40°C to +125°C
Storage temperature ........................................................................................................................ -65°C to +150°C

Voltage on pins with respect to VSS

on VDD pin
PIC18F25/26K83 ...................................................................................................... -0.3V to +6.5V
PIC18LF25/26K83 .................................................................................................... -0.3V to +4.0V
on MCLR pin .......................................................................................................................... -0.3V to +9.0V
on all other pins ............................................................................................................ -0.3V to (VDD + 0.3V)

Maximum current

on Vss pin(1)
-40°C ≤ TA ≤ +85°C .............................................................................................................. 350 mA
85°C < TA ≤ +125°C ........................................................................................................... 120 mA

on VDD pin for 28-Pin devices(1)
-40°C ≤ TA ≤ +85°C .............................................................................................................. 250 mA
85°C < TA ≤ +125°C ............................................................................................................... 85 mA

on any standard I/O pin ...................................................................................................................... ±50 mA

Clamp current, IK (VPIN < 0 or VPIN > VDD) .............................................................................. ±20 mA

Total power dissipation(2)................................................................................................................................ 800 mW

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Table 45-6 to calculate device specifications.

2: Power dissipation is calculated as follows:

\[ P_{DIS} = VDD \times (IDD - \sum IOH) + \sum (VDD - VOH) \times IOH + \sum (VOI \times IOL) \]

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation ratings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.
45.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:
Operating Voltage: \( V_{DD\text{MIN}} \leq V_{DD} \leq V_{DD\text{MAX}} \)
Operating Temperature: \( TA_{\text{MIN}} \leq TA \leq TA_{\text{MAX}} \)

**VDD — Operating Supply Voltage\(^{(1)}\)**

<table>
<thead>
<tr>
<th>PIC18LF25/26K83</th>
<th>VDDMIN (Fosc ( \leq 16) MHz)</th>
<th>+1.8V</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VDDMIN (Fosc ( \leq 32) MHz)</td>
<td>+2.5V</td>
</tr>
<tr>
<td></td>
<td>VDDMIN (Fosc ( \leq 64) MHz)</td>
<td>+2.7V</td>
</tr>
<tr>
<td></td>
<td>VDDMAX</td>
<td>+3.6V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PIC18F25/26K83</th>
<th>VDDMIN (Fosc ( \leq 16) MHz)</th>
<th>+2.3V</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VDDMIN (Fosc ( \leq 32) MHz)</td>
<td>+2.5V</td>
</tr>
<tr>
<td></td>
<td>VDDMIN (Fosc ( \leq 64) MHz)</td>
<td>+3.0V</td>
</tr>
<tr>
<td></td>
<td>VDDMAX</td>
<td>+5.5V</td>
</tr>
</tbody>
</table>

**TA — Operating Ambient Temperature Range**

<table>
<thead>
<tr>
<th>Industrial Temperature</th>
<th>TA_MIN</th>
<th>-40°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TA_MAX</td>
<td>+85°C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Extended Temperature</th>
<th>TA_MIN</th>
<th>-40°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TA_MAX</td>
<td>+125°C</td>
</tr>
</tbody>
</table>

**Note 1:** See Parameter Supply Voltage, DS Characteristics: Supply Voltage.
FIGURE 45-1: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C, PIC18F25/26K83 ONLY

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 45-7 for each Oscillator mode’s supported frequencies.

FIGURE 45-2: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C, PIC18LF25/26K83 ONLY

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 45-7 for each Oscillator mode’s supported frequencies.
## 45.3 DC Characteristics

### TABLE 45-1: SUPPLY VOLTAGE

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ.†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D002</td>
<td>VDD</td>
<td>Supply Voltage</td>
<td>1.8</td>
<td>3.6</td>
<td>5.5</td>
<td>V</td>
<td>FOSC ≤ 16 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.8</td>
<td>3.6</td>
<td>5.5</td>
<td>V</td>
<td>FOSC &gt; 16 MHz</td>
</tr>
<tr>
<td>D002</td>
<td></td>
<td></td>
<td>2.3</td>
<td>5.5</td>
<td>5.5</td>
<td>V</td>
<td>FOSC ≤ 16 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.3</td>
<td>5.5</td>
<td>5.5</td>
<td>V</td>
<td>FOSC &gt; 16 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.7</td>
<td>5.5</td>
<td>5.5</td>
<td>V</td>
<td>FOSC ≤ 32 MHz</td>
</tr>
</tbody>
</table>

**RAM Data Retention**

| D003       | VDR  | 1.5                      | —    | —     | —    | —     | Device in Sleep mode         |
| D003       |      | 1.7                      | —    | —     | —    | —     | Device in Sleep mode         |

**Power-on Reset Release Voltage**

| D004       | VPOR | —                        | 1.6  | —     | —    | —     | BOR or LPBOR disabled        |
| D004       |      | —                        | 1.8  | —     | —    | —     | BOR or LPBOR disabled        |

**Power-on Reset Rearm Voltage**

| D005       | VPORR| —                        | 0.8  | —     | —    | —     | BOR or LPBOR disabled        |
| D005       |      | —                        | 1.5  | —     | —    | —     | BOR or LPBOR disabled        |

**VDD Rise Rate to ensure internal Power-on Reset signal**

| D006       | SVDD | 0.05                     | —    | —     | —    | V/ms  | BOR or LPBOR disabled        |
| D006       |      | 0.05                     | —    | —     | —    | V/ms  | BOR or LPBOR disabled        |

† Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1**: This is the limit to which Vdd can be lowered in Sleep mode without losing RAM data.

**Note 2**: See Figure 45-3, POR and POR REARM with Slow Rising Vdd.

**Note 3**: See Table 45-11 for BOR and LPBOR trip point information.
FIGURE 45-3: POR AND POR REARM WITH SLOW RISING VDD

Note 1: When NPOR is low, the device is held in Reset.
2: TPOR 1 μs typical.
3: TVLOW 2.7 μs typical.
### TABLE 45-2: SUPPLY CURRENT (I\(\text{DD}\))\(^{(1,2,4)}\)

<table>
<thead>
<tr>
<th>Device Characteristics</th>
<th>Min.</th>
<th>Typ. (\dagger)</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>D100 I(\text{DD}_{\text{XT4}}) (\text{XT} = 4\ \text{MHz})</td>
<td>—</td>
<td>590</td>
<td>1200</td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>D100 I(\text{DD}_{\text{XT4}}) (\text{XT} = 4\ \text{MHz})</td>
<td>—</td>
<td>770</td>
<td>1300</td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>D100A I(\text{DD}_{\text{XT4}}) (\text{XT} = 4\ \text{MHz})</td>
<td>—</td>
<td>390</td>
<td>850</td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>D100A I(\text{DD}_{\text{XT4}}) (\text{XT} = 4\ \text{MHz})</td>
<td>—</td>
<td>620</td>
<td>950</td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>D101 I(\text{DD}_{\text{HF016}}) (\text{HFINTOSC} = 16\ \text{MHz})</td>
<td>—</td>
<td>2.3</td>
<td>5.0</td>
<td>(\text{mA})</td>
</tr>
<tr>
<td>D101 I(\text{DD}_{\text{HF016}}) (\text{HFINTOSC} = 16\ \text{MHz})</td>
<td>—</td>
<td>2.4</td>
<td>5.1</td>
<td>(\text{mA})</td>
</tr>
<tr>
<td>D101A I(\text{DD}_{\text{HF016}}) (\text{HFINTOSC} = 16\ \text{MHz})</td>
<td>—</td>
<td>1.5</td>
<td>3.2</td>
<td>(\text{mA})</td>
</tr>
<tr>
<td>D102 I(\text{DD}_{\text{HF0PLL}}) (\text{HFINTOSC} = 64\ \text{MHz})</td>
<td>—</td>
<td>8.4</td>
<td>16.5</td>
<td>(\text{mA})</td>
</tr>
<tr>
<td>D102A I(\text{DD}_{\text{HF0PLL}}) (\text{HFINTOSC} = 64\ \text{MHz})</td>
<td>—</td>
<td>8.4</td>
<td>19</td>
<td>(\text{mA})</td>
</tr>
<tr>
<td>D103 I(\text{DD}_{\text{HSPLL64}}) (\text{HS+PLL} = 64\ \text{MHz})</td>
<td>—</td>
<td>8.4</td>
<td>19</td>
<td>(\text{mA})</td>
</tr>
<tr>
<td>D103A I(\text{DD}_{\text{HSPLL64}}) (\text{HS+PLL} = 64\ \text{MHz})</td>
<td>—</td>
<td>8.4</td>
<td>20</td>
<td>(\text{mA})</td>
</tr>
<tr>
<td>D104 I(\text{DD}_{\text{IDLE}}) (\text{IDLE} \text{ mode, HFINTOSC} = 16\ \text{MHz})</td>
<td>—</td>
<td>1.9</td>
<td>4.5</td>
<td>(\text{mA})</td>
</tr>
<tr>
<td>D105 I(\text{DD}_{\text{DOZE}}) (\text{DOZE} \text{ mode, HFINTOSC} = 16\ \text{MHz}, \text{Doze Ratio} = 16)</td>
<td>—</td>
<td>1.9</td>
<td>—</td>
<td>(\text{mA})</td>
</tr>
</tbody>
</table>

\(\dagger\) Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note**

1. The test conditions for all I\(\text{DD}\) measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins are outputs driven low; MCLR = V\(\text{DD}\); WDT disabled.
2. The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
3. I\(\text{DD}_{\text{DOZE}}\) = \[
\frac{\text{I\(\text{DD}_{\text{IDLE}}\)}(\text{IDLE} \text{ mode, HFINTOSC} = 16\ \text{MHz}) \times \text{N}}{\text{DOZE Ratio}}\]
where N = Doze Ratio (Register 10-2).
4. PMD bits are all in the default state, no modules are disabled.
## TABLE 45-3: POWER-DOWN CURRENT (I\textsubscript{PD}(1,2))

### PIC18LF25/26K83

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Symbol</th>
<th>Device Characteristics</th>
<th>Min.</th>
<th>Typ.†</th>
<th>Max. +85°C</th>
<th>Max. +125°C</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D200</td>
<td>IPD</td>
<td>IPD Base</td>
<td>—</td>
<td>0.07</td>
<td>2</td>
<td>6</td>
<td>μA</td>
<td>3.0V</td>
</tr>
<tr>
<td>D200A</td>
<td>IPD</td>
<td>IPD Base</td>
<td>—</td>
<td>0.4</td>
<td>2.5</td>
<td>8</td>
<td>μA</td>
<td>3.0V</td>
</tr>
<tr>
<td>D201</td>
<td>IPD_WDT</td>
<td>Low-Frequency Internal Oscillator/ WDT</td>
<td>—</td>
<td>0.9</td>
<td>2.9</td>
<td>9</td>
<td>μA</td>
<td>3.0V</td>
</tr>
<tr>
<td>D201</td>
<td>IPD_WDT</td>
<td>Low-Frequency Internal Oscillator/ WDT</td>
<td>—</td>
<td>1.1</td>
<td>3.3</td>
<td>9</td>
<td>μA</td>
<td>3.0V</td>
</tr>
<tr>
<td>D202</td>
<td>IPD_SOSC</td>
<td>Secondary Oscillator (SOSC)</td>
<td>—</td>
<td>0.6</td>
<td>2.2</td>
<td>13</td>
<td>μA</td>
<td>3.0V LP mode</td>
</tr>
<tr>
<td>D202</td>
<td>IPD_SOSC</td>
<td>Secondary Oscillator (SOSC)</td>
<td>—</td>
<td>0.8</td>
<td>3.2</td>
<td>15</td>
<td>μA</td>
<td>3.0V LP mode</td>
</tr>
<tr>
<td>D203</td>
<td>IPD_FVR</td>
<td>FVR</td>
<td>—</td>
<td>3.1</td>
<td>7.0</td>
<td>7.5</td>
<td>μA</td>
<td>3.0V FVRCON = 0x81 or 0x84</td>
</tr>
<tr>
<td>D203</td>
<td>IPD_FVR</td>
<td>FVR</td>
<td>—</td>
<td>3.6</td>
<td>7.0</td>
<td>7.0</td>
<td>μA</td>
<td>3.0V FVRCON = 0x81 or 0x84</td>
</tr>
<tr>
<td>D204</td>
<td>IPD_BOR</td>
<td>Brown-out Reset (BOR)</td>
<td>—</td>
<td>9.4</td>
<td>16.0</td>
<td>19</td>
<td>μA</td>
<td>3.0V</td>
</tr>
<tr>
<td>D204</td>
<td>IPD_BOR</td>
<td>Brown-out Reset (BOR)</td>
<td>—</td>
<td>9.4</td>
<td>17.0</td>
<td>19</td>
<td>μA</td>
<td>3.0V</td>
</tr>
<tr>
<td>D205</td>
<td>IPD_LPBOR</td>
<td>Low-Power Brown-out Reset (LPBOR)</td>
<td>—</td>
<td>0.2</td>
<td>3.0</td>
<td>6</td>
<td>μA</td>
<td>3.0V</td>
</tr>
<tr>
<td>D205</td>
<td>IPD_LPBOR</td>
<td>Low-Power Brown-out Reset (LPBOR)</td>
<td>—</td>
<td>0.5</td>
<td>5.0</td>
<td>5</td>
<td>μA</td>
<td>3.0V</td>
</tr>
<tr>
<td>D206</td>
<td>IPD_HLVD</td>
<td>High/Low Voltage Detect (HLVD)</td>
<td>—</td>
<td>9.5</td>
<td>16.0</td>
<td>19</td>
<td>μA</td>
<td>3.0V</td>
</tr>
<tr>
<td>D206</td>
<td>IPD_HLVD</td>
<td>High/Low Voltage Detect (HLVD)</td>
<td>—</td>
<td>9.7</td>
<td>17.0</td>
<td>20</td>
<td>μA</td>
<td>3.0V</td>
</tr>
<tr>
<td>D207</td>
<td>IPD_ADCA</td>
<td>ADC - Active</td>
<td>—</td>
<td>400</td>
<td>—</td>
<td>—</td>
<td>μA</td>
<td>3.0V ADC is converting (4)</td>
</tr>
<tr>
<td>D207</td>
<td>IPD_ADCA</td>
<td>ADC - Active</td>
<td>—</td>
<td>400</td>
<td>—</td>
<td>—</td>
<td>μA</td>
<td>3.0V ADC is converting (4)</td>
</tr>
<tr>
<td>D208</td>
<td>IPD_CMP</td>
<td>Comparator</td>
<td>—</td>
<td>33.0</td>
<td>50.0</td>
<td>55</td>
<td>μA</td>
<td>3.0V</td>
</tr>
<tr>
<td>D208</td>
<td>IPD_CMP</td>
<td>Comparator</td>
<td>—</td>
<td>30.0</td>
<td>50.0</td>
<td>60</td>
<td>μA</td>
<td>3.0V</td>
</tr>
</tbody>
</table>

† Data in “Typ.” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The peripheral current is the sum of the base I\textsubscript{DD} and the additional current consumed when this peripheral is enabled. The peripheral current can be determined by subtracting the base I\textsubscript{DD} or I\textsubscript{PD} current from this limit. Max. values should be used when calculating total current consumption.

**Note 2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode with all I/O pins in high-impedance state and tied to VSS.

**Note 3:** All peripheral currents listed are on a per-peripheral basis if more than one instance of a peripheral is available.

**Note 4:** ADC clock source is FRC.
### Table 45-4: I/O Ports

**Standard Operating Conditions** (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VIL</strong></td>
<td></td>
<td><strong>Input Low Voltage</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D300</td>
<td></td>
<td>I/O PORT: with TTL buffer</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>VDD ≤ 5.5V</td>
</tr>
<tr>
<td>D301</td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>0.15</td>
<td>V Ddo</td>
<td>1.8V ≤ VDD ≤ 4.5V</td>
</tr>
<tr>
<td>D302</td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>0.2</td>
<td>V Ddo</td>
<td>2.0V ≤ VDD ≤ 5.5V</td>
</tr>
<tr>
<td>D303</td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>0.3</td>
<td>V Ddo</td>
<td></td>
</tr>
<tr>
<td>D304</td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V Ddo</td>
<td>2.7V ≤ VDD ≤ 5.5V</td>
</tr>
<tr>
<td>D305</td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V Ddo</td>
<td>1.8V ≤ VDD ≤ 5.5V</td>
</tr>
<tr>
<td>D306</td>
<td></td>
<td>MCLR</td>
<td>—</td>
<td>—</td>
<td>0.2</td>
<td>V Ddo</td>
<td></td>
</tr>
<tr>
<td><strong>VIH</strong></td>
<td></td>
<td><strong>Input High Voltage</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D320</td>
<td></td>
<td>I/O PORT: with TTL buffer</td>
<td>2.0</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>VDD ≤ 5.5V</td>
</tr>
<tr>
<td>D321</td>
<td></td>
<td></td>
<td>0.25</td>
<td>—</td>
<td>—</td>
<td>V Ddo</td>
<td>1.8V ≤ VDD ≤ 4.5V</td>
</tr>
<tr>
<td>D322</td>
<td></td>
<td></td>
<td>0.6</td>
<td>—</td>
<td>—</td>
<td>V Ddo</td>
<td>2.0V ≤ VDD ≤ 5.5V</td>
</tr>
<tr>
<td>D323</td>
<td></td>
<td></td>
<td>0.7</td>
<td>—</td>
<td>—</td>
<td>V Ddo</td>
<td></td>
</tr>
<tr>
<td>D324</td>
<td></td>
<td></td>
<td>2.1</td>
<td>—</td>
<td>—</td>
<td>V Ddo</td>
<td>2.7V ≤ VDD ≤ 5.5V</td>
</tr>
<tr>
<td>D325</td>
<td></td>
<td></td>
<td>1.35</td>
<td>—</td>
<td>—</td>
<td>V Ddo</td>
<td>1.8V ≤ VDD ≤ 5.5V</td>
</tr>
<tr>
<td>D326</td>
<td></td>
<td>MCLR</td>
<td>—</td>
<td>—</td>
<td>0.7</td>
<td>V Ddo</td>
<td></td>
</tr>
<tr>
<td><strong>IIL</strong></td>
<td></td>
<td><strong>Input Leakage Current</strong>(1)</td>
<td>±5</td>
<td>±125</td>
<td>±125</td>
<td>nA</td>
<td>VSS ≤ VPIN ≤ VDD, Pin at high-impedance, 85°C</td>
</tr>
<tr>
<td>D340</td>
<td></td>
<td>I/O Ports</td>
<td>—</td>
<td>—</td>
<td>±5</td>
<td>±1000</td>
<td>nA</td>
</tr>
<tr>
<td>D341</td>
<td></td>
<td>MCLR(2)</td>
<td>—</td>
<td>—</td>
<td>±50</td>
<td>±200</td>
<td>nA</td>
</tr>
<tr>
<td><strong>IPUR</strong></td>
<td></td>
<td><strong>Weak Pull-up Current</strong></td>
<td>—</td>
<td>—</td>
<td>25</td>
<td>120</td>
<td>200</td>
</tr>
<tr>
<td>D350</td>
<td></td>
<td>I/O ports</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>±5</td>
<td>±1000</td>
</tr>
<tr>
<td>D360</td>
<td></td>
<td>All I/O pins</td>
<td>—</td>
<td>—</td>
<td>5</td>
<td>50</td>
<td>pF</td>
</tr>
</tbody>
</table>

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Negative current is defined as current sourced by the pin.

**Note 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
## TABLE 45-5: MEMORY PROGRAMMING SPECIFICATIONS

### Standard Operating Conditions (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM20</td>
<td>E_D</td>
<td>DataEE Byte Endurance</td>
<td>100k</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>E/W -40°C ≤ TA ≤ +85°C</td>
</tr>
<tr>
<td>MEM21</td>
<td>T_D_RET</td>
<td>Characteristic Retention</td>
<td>—</td>
<td>40</td>
<td>—</td>
<td>Year</td>
<td>Provided no other specifications are violated</td>
</tr>
<tr>
<td>MEM22</td>
<td>N_DREF</td>
<td>Total Erase/Write Cycles before Refresh</td>
<td>1M</td>
<td>10M</td>
<td>—</td>
<td>—</td>
<td>E/W -40°C ≤ TA ≤ +60°C -40°C ≤ TA ≤ +85°C</td>
</tr>
<tr>
<td>MEM23</td>
<td>V_D_RW</td>
<td>VDD for Read or Erase/Write operation</td>
<td>VDDMIN</td>
<td>—</td>
<td>VDDMAX</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>MEM24</td>
<td>T_D_BEW</td>
<td>Byte Erase and Write Cycle Time</td>
<td>—</td>
<td>4.0</td>
<td>5.0</td>
<td>ms</td>
<td>—</td>
</tr>
</tbody>
</table>

### Program Flash Memory Specifications

| MEM30     | E_P  | Memory Cell Endurance | 10k  | —    | —    | —     | E/W -40°C ≤ TA ≤ +85°C (Note 1) |
| MEM32     | T_P_RET | Characteristic Retention | —   | 40   | —    | Year  | Provided no other specifications are violated |
| MEM33     | V_P_RD | VDD for Read operation | VDDMIN | —   | VDDMAX | V     | —          |
| MEM34     | V_P_REW | VDD for Row Erase or Write operation | VDDMIN | —   | VDDMAX | V     | —          |
| MEM35     | T_P_REW | Self-Timed Row Erase or Self-Timed Write | —   | 2.0  | 2.5  | ms    | —          |

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Memory Cell Endurance for the Program memory is defined as: One Row Erase operation and one Self-Timed Write.
<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Typ.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>TH01</td>
<td>θJA</td>
<td>Thermal Resistance Junction to Ambient</td>
<td>60</td>
<td>°C/W</td>
<td>28-pin SPDIP package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>80</td>
<td>°C/W</td>
<td>28-pin SOIC package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>90</td>
<td>°C/W</td>
<td>28-pin SSOP package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>27.5</td>
<td>°C/W</td>
<td>28-pin UQFN 4x4 mm package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>27.5</td>
<td>°C/W</td>
<td>28-pin QFN 6x6mm package</td>
</tr>
<tr>
<td>TH02</td>
<td>θJC</td>
<td>Thermal Resistance Junction to Case</td>
<td>31.4</td>
<td>°C/W</td>
<td>28-pin SPDIP package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>24</td>
<td>°C/W</td>
<td>28-pin SOIC package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>24</td>
<td>°C/W</td>
<td>28-pin SSOP package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>24</td>
<td>°C/W</td>
<td>28-pin UQFN 4x4 mm package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>24</td>
<td>°C/W</td>
<td>28-pin QFN 6x6mm package</td>
</tr>
<tr>
<td>TH03</td>
<td>TJMAX</td>
<td>Maximum Junction Temperature</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>TH04</td>
<td>PD</td>
<td>Power Dissipation</td>
<td>—</td>
<td>W</td>
<td>PD = PINTERNAL + PI/O(3)</td>
</tr>
<tr>
<td>TH05</td>
<td>PINTERNAL</td>
<td>Internal Power Dissipation</td>
<td>—</td>
<td>W</td>
<td>PINTERNAL = IDD x VDD(1)</td>
</tr>
<tr>
<td>TH06</td>
<td>PI/O</td>
<td>I/O Power Dissipation</td>
<td>—</td>
<td>W</td>
<td>PI/O = (\sum(IOL \times VOL) + \sum(IOH \times (VDD - VOH)))</td>
</tr>
<tr>
<td>TH07</td>
<td>PDER</td>
<td>Derated Power</td>
<td>—</td>
<td>W</td>
<td>PDER = PDMAX (TJ - TA)/(θJA)(2)</td>
</tr>
</tbody>
</table>

**Note 1:** IDD is current to run the chip alone without driving any load on the output pins.

**Note 2:** TA = Ambient Temperature, TJ = Junction Temperature

**Note 3:** See absolute maximum ratings for total power dissipation.
45.4 AC Characteristics

FIGURE 45-4: LOAD CONDITIONS

Legend: CL=50 pF for all pins
FIGURE 45-5: CLOCK TIMING

Note 1: See Table 45-7.

TABLE 45-7: EXTERNAL CLOCK/OSCILLATOR TIMING REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECL Oscillator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OS1</td>
<td>F_{ECL}</td>
<td>Clock Frequency</td>
<td>—</td>
<td>—</td>
<td>500</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>OS2</td>
<td>T_{ECL,DC}</td>
<td>Clock Duty Cycle</td>
<td>40</td>
<td>—</td>
<td>60</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>ECM Oscillator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OS3</td>
<td>F_{ECM}</td>
<td>Clock Frequency</td>
<td>—</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>OS4</td>
<td>T_{ECM,DC}</td>
<td>Clock Duty Cycle</td>
<td>40</td>
<td>—</td>
<td>60</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>ECH Oscillator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OS5</td>
<td>F_{ECH}</td>
<td>Clock Frequency</td>
<td>—</td>
<td>—</td>
<td>32</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>OS6</td>
<td>T_{ECH,DC}</td>
<td>Clock Duty Cycle</td>
<td>40</td>
<td>—</td>
<td>60</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>LP Oscillator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OS7</td>
<td>F_{LP}</td>
<td>Clock Frequency</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>kHz</td>
<td>Note 4</td>
</tr>
<tr>
<td>XT Oscillator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OS8</td>
<td>F_{XT}</td>
<td>Clock Frequency</td>
<td>—</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
<td>Note 4</td>
</tr>
<tr>
<td>HS Oscillator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OS9</td>
<td>F_{HS}</td>
<td>Clock Frequency</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>MHz</td>
<td>Note 4</td>
</tr>
<tr>
<td>Secondary Oscillator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OS10</td>
<td>F_{SEC}</td>
<td>Clock Frequency</td>
<td>32.4</td>
<td>32.768</td>
<td>33.1</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>System Oscillator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OS20</td>
<td>F_{OSC}</td>
<td>System Clock Frequency</td>
<td>—</td>
<td>—</td>
<td>64</td>
<td>MHz</td>
<td>(Note 2, Note 3)</td>
</tr>
</tbody>
</table>

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock applied to OSC1 pin. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

2: The system clock frequency (Fosc) is selected by the “main clock switch controls” as described in Section 10.0 “Power-Saving Operation Modes”.

3: The system clock frequency (Fosc) must meet the voltage requirements defined in the Section 45.2 “Standard Operating Conditions”.

4: LP, XT and HS oscillator modes require an appropriate crystal or resonator to be connected to the device. For clocking the device with the external square wave, one of the EC mode selections must be used.
### TABLE 45-7: EXTERNAL CLOCK/OSCILLATOR TIMING REQUIREMENTS (CONTINUED)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS21</td>
<td>$F_{CY}$</td>
<td>Instruction Frequency</td>
<td>—</td>
<td>$F_{osc}/4$</td>
<td>—</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>OS22</td>
<td>$T_{CY}$</td>
<td>Instruction Period</td>
<td>62.5</td>
<td>1/$F_{CY}$</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period ($T_{CY}$) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock applied to OSC1 pin. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

2: The system clock frequency ($F_{osc}$) is selected by the “main clock switch controls” as described in Section 10.0 “Power-Saving Operation Modes”.

3: The system clock frequency ($F_{osc}$) must meet the voltage requirements defined in the Section 45.2 “Standard Operating Conditions”.

4: LP, XT and HS oscillator modes require an appropriate crystal or resonator to be connected to the device. For clocking the device with the external square wave, one of the EC mode selections must be used.
TABLE 45-8: INTERNAL OSCILLATOR PARAMETERS(1)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS50</td>
<td>FHFOSC</td>
<td>Precision Calibrated HFINTOSC Frequency</td>
<td>—</td>
<td>4</td>
<td>—</td>
<td>MHz</td>
<td>(Note 2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>8</td>
<td></td>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>12</td>
<td></td>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>16</td>
<td></td>
<td>16</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>48</td>
<td></td>
<td>48</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>64</td>
<td></td>
<td>64</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OS51</td>
<td>FHFOSCP</td>
<td>Low-Power Optimized HFINTOSC Frequency</td>
<td>0.93</td>
<td>1</td>
<td>0.93</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.86</td>
<td>2</td>
<td>1.86</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>OS53*</td>
<td>FLFOSC</td>
<td>Internal LFINTOSC Frequency</td>
<td>—</td>
<td>31</td>
<td>—</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>OS54*</td>
<td>THFOSCST</td>
<td>HFINTOSC Wake-up from Sleep Start-up Time</td>
<td>—</td>
<td>11</td>
<td>—</td>
<td>μs</td>
<td>VREGPM = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20</td>
<td>50</td>
<td>20</td>
<td>μs</td>
<td>VREGPM = 1</td>
</tr>
<tr>
<td>OS56</td>
<td>TLFOSCST</td>
<td>LFINTOSC Wake-up from Sleep Start-up Time</td>
<td>—</td>
<td>0.2</td>
<td>—</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

**Note 2:** See Figure 45-6: Precision Calibrated HFINTOSC Frequency Accuracy Over Device VDD and Temperature.

FIGURE 45-6: PRECISION CALIBRATED HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE
### TABLE 45-9: PLL SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) VDD \( \geq 2.5V \)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL01</td>
<td>FPLLIN</td>
<td>PLL Input Frequency Range</td>
<td>4</td>
<td>—</td>
<td>16</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>PLL02</td>
<td>FPLLOUT</td>
<td>PLL Output Frequency Range</td>
<td>16</td>
<td>—</td>
<td>64</td>
<td>MHz</td>
<td>Note 1</td>
</tr>
<tr>
<td>PLL03</td>
<td>TPLLST</td>
<td>PLL Lock Time from Start-up</td>
<td>—</td>
<td>200</td>
<td>—</td>
<td>( \mu )s</td>
<td></td>
</tr>
<tr>
<td>PLL04</td>
<td>FPLLJIT</td>
<td>PLL Output Frequency Stability (Jitter)</td>
<td>-0.25</td>
<td>—</td>
<td>0.25</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The output frequency of the PLL must meet the FOSC requirements listed in Parameter D002.
FIGURE 45-7: CLKOUT AND I/O TIMING

TABLE 45-10: I/O AND CLKOUT TIMING SPECIFICATIONS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>IO1*</td>
<td>T_CLKOUTH</td>
<td>CLKOUT rising edge delay (rising edge Fosc (Q1 cycle) to falling edge CLKOUT)</td>
<td>—</td>
<td>—</td>
<td>70</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>IO2*</td>
<td>T_CLKOUTL</td>
<td>CLKOUT falling edge delay (rising edge Fosc (Q3 cycle) to rising edge CLKOUT)</td>
<td>—</td>
<td>—</td>
<td>72</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>IO3*</td>
<td>T_IO_VALID</td>
<td>Port output valid time (rising edge Fosc (Q1 cycle) to port valid)</td>
<td>—</td>
<td>50</td>
<td>70</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>IO4*</td>
<td>T_IO_SETUP</td>
<td>Port input setup time (Setup time before rising edge Fosc – Q2 cycle)</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>IO5*</td>
<td>T_IO_HOLD</td>
<td>Port input hold time (Hold time after rising edge Fosc – Q2 cycle)</td>
<td>50</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>IO6*</td>
<td>T_IO_RSLREN</td>
<td>Port I/O rise time, slew rate enabled</td>
<td>25</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>VDD = 3.0V</td>
</tr>
<tr>
<td>IO7*</td>
<td>T_IO_RSLRD</td>
<td>Port I/O rise time, slew rate disabled</td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>VDD = 3.0V</td>
</tr>
<tr>
<td>IO8*</td>
<td>T_IO_FSLREN</td>
<td>Port I/O fall time, slew rate enabled</td>
<td>25</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>VDD = 3.0V</td>
</tr>
<tr>
<td>IO9*</td>
<td>T_IO_FSLRD</td>
<td>Port I/O fall time, slew rate disabled</td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>VDD = 3.0V</td>
</tr>
<tr>
<td>IO10*</td>
<td>T_INT</td>
<td>INT pin high or low time to trigger an interrupt</td>
<td>25</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>IO11*</td>
<td>T_IOC</td>
<td>Interrupt-on-Change minimum high or low time to trigger interrupt</td>
<td>25</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

*These parameters are characterized but not tested.
FIGURE 45-8:  
RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

VDD
MCLR
Internal POR
PWRT Time-out
OSC Start-up Time
Internal Reset⁽¹⁾
Watchdog Timer Reset⁽¹⁾
I/O pins

Note 1: Asserted low.

FIGURE 45-9:  
BROWN-OUT RESET TIMING AND CHARACTERISTICS

VDD
VBOR
(DEVICE IN BROWN-OUT RESET)
VBOR AND VHYST
(DEVICE NOT IN BROWN-OUT RESET)
RST09
Reset (due to B0R)

Note 4: Delay depends on PWRT<1:0> Configuration bits.
## TABLE 45-11: RESET, WDT, OSCILLATOR START-UP TIMER, POWER-UP TIMER, BROWN-OUT RESET AND LOW-POWER BROWN-OUT RESET SPECIFICATIONS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>RST01*</td>
<td>TmCLR</td>
<td>MCLR Pulse Width Low to ensure Reset</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>RST02*</td>
<td>TiOZ</td>
<td>I/O high-impedance from Reset detection</td>
<td>—</td>
<td>—</td>
<td>2</td>
<td>µs</td>
<td>Ticks 1:12 Prescaler</td>
</tr>
<tr>
<td>RST03</td>
<td>TWDt</td>
<td>Watchdog Timer Time-out Period</td>
<td>—</td>
<td>16</td>
<td>—</td>
<td>ms</td>
<td>PWRTS = 00</td>
</tr>
<tr>
<td>RST04*</td>
<td>TPWRT</td>
<td>Power-up Timer Period</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>ms</td>
<td>PWRTS = 01</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>16</td>
<td>—</td>
<td>ms</td>
<td>PWRTS = 10</td>
</tr>
<tr>
<td>RST05</td>
<td>TOST</td>
<td>Oscillator Start-up Timer Period(1,2)</td>
<td>—</td>
<td>1024</td>
<td>—</td>
<td>T Osc</td>
<td></td>
</tr>
<tr>
<td>RST06</td>
<td>VbOR</td>
<td>Brown-out Reset Voltage(4)</td>
<td>2.7</td>
<td>2.85</td>
<td>3.0</td>
<td>V</td>
<td>BORV = 00</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.55</td>
<td>2.7</td>
<td>2.85</td>
<td>V</td>
<td>BORV = 01</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.3</td>
<td>2.45</td>
<td>2.6</td>
<td>V</td>
<td>BORV = 10</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.3</td>
<td>2.45</td>
<td>2.6</td>
<td>V</td>
<td>BORV = 11 (PIC18Fxxx)</td>
</tr>
<tr>
<td>RST07</td>
<td>VBORHS</td>
<td>Brown-out Reset Hysteresis</td>
<td>—</td>
<td>40</td>
<td>—</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>RST08</td>
<td>Tbordc</td>
<td>Brown-out Reset Response Time</td>
<td>—</td>
<td>3</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>RST09</td>
<td>Vlpbor</td>
<td>Low-Power Brown-out Reset Voltage</td>
<td>1.8</td>
<td>1.9</td>
<td>2.2</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** By design, the Oscillator Start-up Timer (OST) counts the first 1024 cycles, independent of frequency.

**Note 2:** To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

## TABLE 45-12: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>HLVD01</td>
<td>VDET</td>
<td>Voltage Detection</td>
<td>1.90</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>HLVDSEL&lt;3:0&gt;=0000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>2.10</td>
<td>—</td>
<td>V</td>
<td>HLVDSEL&lt;3:0&gt;=0001</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>2.25</td>
<td>—</td>
<td>V</td>
<td>HLVDSEL&lt;3:0&gt;=0010</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>2.50</td>
<td>—</td>
<td>V</td>
<td>HLVDSEL&lt;3:0&gt;=0011</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>2.60</td>
<td>—</td>
<td>V</td>
<td>HLVDSEL&lt;3:0&gt;=0100</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>2.75</td>
<td>—</td>
<td>V</td>
<td>HLVDSEL&lt;3:0&gt;=0101</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>2.90</td>
<td>—</td>
<td>V</td>
<td>HLVDSEL&lt;3:0&gt;=0110</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>3.15</td>
<td>—</td>
<td>V</td>
<td>HLVDSEL&lt;3:0&gt;=0111</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>3.35</td>
<td>—</td>
<td>V</td>
<td>HLVDSEL&lt;3:0&gt;=1000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>3.60</td>
<td>—</td>
<td>V</td>
<td>HLVDSEL&lt;3:0&gt;=1001</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>3.75</td>
<td>—</td>
<td>V</td>
<td>HLVDSEL&lt;3:0&gt;=1010</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>4.00</td>
<td>—</td>
<td>V</td>
<td>HLVDSEL&lt;3:0&gt;=1011</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>4.20</td>
<td>—</td>
<td>V</td>
<td>HLVDSEL&lt;3:0&gt;=1100</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>4.35</td>
<td>—</td>
<td>V</td>
<td>HLVDSEL&lt;3:0&gt;=1101</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>4.65</td>
<td>—</td>
<td>V</td>
<td>HLVDSEL&lt;3:0&gt;=1110</td>
</tr>
</tbody>
</table>
### TABLE 45-13: ANALOG-TO-DIGITAL CONVERTER (ADC) ACCURACY SPECIFICATIONS\(^{(1,2)}\)

**Operating Conditions** (unless otherwise stated)  
\( V_{DD} = 3.0\, \text{V}, \, T_A = 25^\circ\, \text{C}, \, T_{AD} = 1\, \mu\text{s} \)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD01</td>
<td>NR</td>
<td>Resolution</td>
<td>—</td>
<td>—</td>
<td>12</td>
<td>bit</td>
<td></td>
</tr>
<tr>
<td>AD02</td>
<td>EIL</td>
<td>Integral Error</td>
<td>—</td>
<td>±0.1</td>
<td>±2.0</td>
<td>LSb</td>
<td>( V_{ADCREF+} = 3.0, \text{V}, , V_{ADCREF-} = 0, \text{V} )</td>
</tr>
<tr>
<td>AD03</td>
<td>EDL</td>
<td>Differential Error</td>
<td>—</td>
<td>±0.1</td>
<td>±1.0</td>
<td>LSb</td>
<td>( V_{ADCREF+} = 3.0, \text{V}, , V_{ADCREF-} = 0, \text{V} )</td>
</tr>
<tr>
<td>AD04</td>
<td>EOFF</td>
<td>Offset Error</td>
<td>—</td>
<td>0.5</td>
<td>6.0</td>
<td>LSb</td>
<td>( V_{ADCREF+} = 3.0, \text{V}, , V_{ADCREF-} = 0, \text{V} )</td>
</tr>
<tr>
<td>AD05</td>
<td>EG</td>
<td>Gain Error</td>
<td>—</td>
<td>±0.2</td>
<td>±6.0</td>
<td>LSb</td>
<td>( V_{ADCREF+} = 3.0, \text{V}, , V_{ADCREF-} = 0, \text{V} )</td>
</tr>
<tr>
<td>AD06</td>
<td>VADREF</td>
<td>ADC Reference Voltage (( V_{ADCREF+} - V_{ADCREF-} ))</td>
<td>1.8</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>AD07</td>
<td>VAIN</td>
<td>Full-Scale Range</td>
<td>( V_{ADCREF-} )</td>
<td>—</td>
<td>( V_{ADCREF+} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AD08</td>
<td>ZAIN</td>
<td>Recommended Impedance of Analog Voltage Source</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>AD09</td>
<td>RVREF</td>
<td>ADC Voltage Reference Ladder Impedance</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td>kΩ</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.  
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Total Absolute Error is the sum of the offset, gain and integral non-linearity (INL) errors.  
2: The ADC conversion result never decreases with an increase in the input and has no missing codes.  
3: This is the impedance seen by the VREF pads when the external reference pads are selected.
### Table 45-14: Analog-to-Digital Converter (ADC) Conversion Timing Specifications

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD20</td>
<td>TAD</td>
<td>ADC Clock Period</td>
<td>1</td>
<td>—</td>
<td>9</td>
<td>μs</td>
<td>Using FOSC as the ADC clock source ADOCS = 0</td>
</tr>
<tr>
<td>AD21</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>μs</td>
<td>Using FRC as the ADC clock source ADOCS = 1</td>
</tr>
<tr>
<td>AD22</td>
<td>TCNV</td>
<td>Conversion Time(1)</td>
<td>—</td>
<td>13+3 TAD</td>
<td>—</td>
<td>TAD</td>
<td>Set of GO/DONE bit to Clear of GO/DONE bit</td>
</tr>
<tr>
<td>AD23</td>
<td>TACQ</td>
<td>Acquisition Time</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>μs</td>
<td>—</td>
</tr>
<tr>
<td>AD24</td>
<td>ThCD</td>
<td>Sample and Hold Capacitor Disconnect Time</td>
<td>3</td>
<td>—</td>
<td>—</td>
<td>TAD</td>
<td>FOSC-based clock source FRC-based clock source</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Does not apply for the ADCRC oscillator.

### Figure 45-10: ADC Conversion Timing (ADC Clock FOSC-Based)
FIGURE 45-11: ADC CONVERSION TIMING (ADC CLOCK FROM ADCRC)

Note 1: If the ADC clock source is selected as ADCRC, a time of TCY is added before the ADC clock starts. This allows the SLEEP instruction to be executed.
### TABLE 45-15: COMPARATOR SPECIFICATIONS

<table>
<thead>
<tr>
<th>Operating Conditions (unless otherwise stated)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD} = 3.0V$, $T_A = 25^\circ C$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CM01</td>
<td>VIOFF</td>
<td>Input Offset Voltage</td>
<td>—</td>
<td>—</td>
<td>±40</td>
<td>mV</td>
<td>$V_{IOFF} = V_{DD}/2$</td>
</tr>
<tr>
<td>CM02</td>
<td>VICM</td>
<td>Input Common Mode Range</td>
<td>GND</td>
<td>—</td>
<td>$V_{DD}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CM03</td>
<td>CMRR</td>
<td>Common Mode Input Rejection Ratio</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>CM04</td>
<td>VHYST</td>
<td>Comparator Hysteresis</td>
<td>10</td>
<td>25</td>
<td>40</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>CM05</td>
<td>TRESP&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>Response Time, Rising Edge</td>
<td>—</td>
<td>300</td>
<td>600</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Response Time, Falling Edge</td>
<td>—</td>
<td>220</td>
<td>500</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

<sup>1</sup> These parameters are characterized but not tested.

1. Response time measured with one comparator input at $V_{DD}/2$, while the other input transitions from $V_{SS}$ to $V_{DD}$.
2. A mode change includes changing any of the control register values, including module enable.

### TABLE 45-16: 5-BIT DAC SPECIFICATIONS

<table>
<thead>
<tr>
<th>Standard Operating Conditions (unless otherwise stated)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD} = 3.0V$, $T_A = 25^\circ C$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>DSB01</td>
<td>VLSB</td>
<td>Step Size</td>
<td>—</td>
<td>$V_{DACREF} + (V_{DACREF} - V_{DACREF}) / 32$</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>DSB01</td>
<td>VACC</td>
<td>Absolute Accuracy</td>
<td>—</td>
<td>—</td>
<td>±0.5</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>DSB03*</td>
<td>RUNIT</td>
<td>Unit Resistor Value</td>
<td>—</td>
<td>5000</td>
<td>—</td>
<td>$\Omega$</td>
<td></td>
</tr>
<tr>
<td>DSB04*</td>
<td>TST</td>
<td>Settling Time&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>$\mu$s</td>
<td></td>
</tr>
</tbody>
</table>

<sup>1</sup> These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Settling time measured while DACR<4:0> transitions from '00000' to '01111'.

### TABLE 45-17: FIXED VOLTAGE REFERENCE (FVR) SPECIFICATIONS

<table>
<thead>
<tr>
<th>Standard Operating Conditions (unless otherwise stated)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>FVR01</td>
<td>VFVR1</td>
<td>1x Gain (1.024V)</td>
<td>-4</td>
<td>—</td>
<td>+4</td>
<td>%</td>
<td>$V_{DD} \geq 2.5V, -40^\circ C \text{ to } 85^\circ C$</td>
</tr>
<tr>
<td>FVR02</td>
<td>VFVR2</td>
<td>2x Gain (2.048V)</td>
<td>-4</td>
<td>—</td>
<td>+4</td>
<td>%</td>
<td>$V_{DD} \geq 2.5V, -40^\circ C \text{ to } 85^\circ C$</td>
</tr>
<tr>
<td>FVR03</td>
<td>VFVR4</td>
<td>4x Gain (4.096V)</td>
<td>-5</td>
<td>—</td>
<td>+5</td>
<td>%</td>
<td>$V_{DD} \geq 4.75V, -40^\circ C \text{ to } 85^\circ C$</td>
</tr>
<tr>
<td>FVR04</td>
<td>TPVRST</td>
<td>FVR Start-up Time</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>us</td>
<td></td>
</tr>
</tbody>
</table>

### TABLE 45-18: ZERO CROSS DETECT (ZCD) SPECIFICATIONS

<table>
<thead>
<tr>
<th>Standard Operating Conditions (unless otherwise stated)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD} = 3.0V$, $T_A = 25^\circ C$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristics</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZC01</td>
<td>VPINZC</td>
<td>Voltage on Zero Cross Pin</td>
<td>—</td>
<td>0.75</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>ZC02</td>
<td>IZCD_MAX</td>
<td>Maximum source or sink current</td>
<td>—</td>
<td>—</td>
<td>600</td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>ZC03</td>
<td>TRESPH</td>
<td>Response Time, Rising Edge</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>$\mu$s</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TRESPL</td>
<td>Response Time, Falling Edge</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>$\mu$s</td>
<td></td>
</tr>
</tbody>
</table>

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
**TABLE 45-19: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS**

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>40*</td>
<td>T0H</td>
<td>T0CKI High Pulse Width</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>No Prescaler</td>
<td>0.5 TCY + 20</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>41*</td>
<td>T0L</td>
<td>T0CKI Low Pulse Width</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>No Prescaler</td>
<td>0.5 TCY + 20</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>42*</td>
<td>T0P</td>
<td>T0CKI Period</td>
<td>Greater of:</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td>N = prescale value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 or TCY + 40</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>N</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>45*</td>
<td>T1H</td>
<td>T1CKI High Time</td>
<td>Synchronous, No Prescaler</td>
<td>0.5 TCY + 20</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Synchronous, with Prescaler</td>
<td>15</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Asynchronous</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>46*</td>
<td>T1L</td>
<td>T1CKI Low Time</td>
<td>Synchronous, No Prescaler</td>
<td>0.5 TCY + 20</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Synchronous, with Prescaler</td>
<td>15</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Asynchronous</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>47*</td>
<td>T1P</td>
<td>T1CKI Input Period</td>
<td>Synchronous</td>
<td>Greater of:</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>30 or TCY + 40</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>N</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>49*</td>
<td>TCXE2</td>
<td>Delay from External Clock Edge to Timer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Increment</td>
<td>2 Tosc</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
### FIGURE 45-13: CAPTURE/COMPARE/PWM TIMINGS (CCP)

![Diagram of Capture/Compare/PWM Timings](image)

**Note:** Refer to Figure 45-4 for load conditions.

### TABLE 45-20: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC01*</td>
<td>TccL</td>
<td>CCPx Input Low Time</td>
<td>No Prescaler</td>
<td>0.5Tcy + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>CC02*</td>
<td>TccH</td>
<td>CCPx Input High Time</td>
<td>No Prescaler</td>
<td>0.5Tcy + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>CC03*</td>
<td>TccP</td>
<td>CCPx Input Period</td>
<td>3Tcy + 40N</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>N = prescale value</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
FIGURE 45-14: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

FIGURE 45-15: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)

Note: Refer to Figure 45-4 for load conditions.
FIGURE 45-16: SPI SLAVE MODE TIMING (CKE = 0)

Note: Refer to Figure 45-4 for load conditions.

FIGURE 45-17: SPI SLAVE MODE TIMING (CKE = 1)

Note: Refer to Figure 45-4 for load conditions.
### TABLE 45-21: SPI MODE REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>SP70*</td>
<td>TssL2sch, TssL2scL</td>
<td>SS↓ to SCK↑ or SCK↑ input</td>
<td>2.25*Tcy</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP71*</td>
<td>TscH</td>
<td>SCK input high time (Slave mode)</td>
<td>Tcy + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP72*</td>
<td>TscL</td>
<td>SCK input low time (Slave mode)</td>
<td>Tcy + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP73*</td>
<td>To/V2sch, To/V2scL</td>
<td>Setup time of SDI data input to SCK edge</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP74*</td>
<td>TsclH2diL, TsclL2diL</td>
<td>Hold time of SDI data input to SCK edge</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP75*</td>
<td>TooR</td>
<td>SDO data output rise time</td>
<td>—</td>
<td>10</td>
<td>25</td>
<td>ns</td>
<td>3.0V ≤ Vdd ≤ 5.5V</td>
</tr>
<tr>
<td>SP76*</td>
<td>TooF</td>
<td>SDO data output fall time</td>
<td>—</td>
<td>10</td>
<td>25</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP77*</td>
<td>Tssh2ooZ</td>
<td>SS↑ to SDO output high-impedance</td>
<td>—</td>
<td>10</td>
<td>50</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP78*</td>
<td>TscR</td>
<td>SCK output rise time (Master mode)</td>
<td>—</td>
<td>10</td>
<td>25</td>
<td>ns</td>
<td>3.0V ≤ Vdd ≤ 5.5V</td>
</tr>
<tr>
<td>SP79*</td>
<td>TscF</td>
<td>SCK output fall time (Master mode)</td>
<td>—</td>
<td>10</td>
<td>25</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP80*</td>
<td>TsclH2ooV, TsclL2ooV</td>
<td>SDO data output valid after SCK edge</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>ns</td>
<td>3.0V ≤ Vdd ≤ 5.5V</td>
</tr>
<tr>
<td>SP81*</td>
<td>TooV2scH, TooV2scL</td>
<td>SDO data output setup to SCK edge</td>
<td>—</td>
<td>1 Tcy</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP82*</td>
<td>Tssl2ooV</td>
<td>SDO data output valid after SS↑ edge</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP83*</td>
<td>TsclH2ssH, TsclL2ssH</td>
<td>SS↑ after SCK edge</td>
<td>—</td>
<td>—</td>
<td>1.5 Tcy + 40</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
TABLE 45-22: \( \text{I}^2\text{C} \) BUS START/STOP BITS REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>SP90*</td>
<td>TSU:STA</td>
<td>Start condition</td>
<td>100 kHz mode</td>
<td>4700</td>
<td>—</td>
<td>ns</td>
<td>Only relevant for Repeated Start condition</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Setup time</td>
<td>400 kHz mode</td>
<td>600</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SP91*</td>
<td>THD:STA</td>
<td>Start condition</td>
<td>100 kHz mode</td>
<td>4000</td>
<td>—</td>
<td>ns</td>
<td>After this period, the first clock pulse is generated</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hold time</td>
<td>400 kHz mode</td>
<td>600</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SP92*</td>
<td>TSU:STO</td>
<td>Stop condition</td>
<td>100 kHz mode</td>
<td>4700</td>
<td>—</td>
<td>ns</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Setup time</td>
<td>400 kHz mode</td>
<td>600</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SP93</td>
<td>THD:STO</td>
<td>Stop condition</td>
<td>100 kHz mode</td>
<td>4000</td>
<td>—</td>
<td>ns</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hold time</td>
<td>400 kHz mode</td>
<td>600</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.

Note: Refer to Figure 45-4 for load conditions.
<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>SP100*</td>
<td>T_HIGH</td>
<td>Clock high time</td>
<td>100 kHz mode</td>
<td>4.0</td>
<td>—</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>0.6</td>
<td>—</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SSP module</td>
<td>1.5T CY</td>
<td>—</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SP101*</td>
<td>T_LOW</td>
<td>Clock low time</td>
<td>100 kHz mode</td>
<td>4.7</td>
<td>—</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>1.3</td>
<td>—</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SSP module</td>
<td>1.5T CY</td>
<td>—</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SP102*</td>
<td>TR</td>
<td>SDA and SCL rise time</td>
<td>100 kHz mode</td>
<td>—</td>
<td>1000</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>20 + 0.1C_B</td>
<td>380</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SP103*</td>
<td>TF</td>
<td>SDA and SCL fall time</td>
<td>100 kHz mode</td>
<td>—</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>20 + 0.1C_B</td>
<td>250</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SP106*</td>
<td>THD:DAT</td>
<td>Data input hold time</td>
<td>100 kHz mode</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>0</td>
<td>0.9</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>SP107*</td>
<td>TSU:DAT</td>
<td>Data input setup time</td>
<td>100 kHz mode</td>
<td>250</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>100</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP109*</td>
<td>TAA</td>
<td>Output valid from clock</td>
<td>100 kHz mode</td>
<td>—</td>
<td>3500</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP110*</td>
<td>T_BUF</td>
<td>Bus free time</td>
<td>100 kHz mode</td>
<td>4.7</td>
<td>—</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>1.3</td>
<td>—</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>SP111</td>
<td>C_B</td>
<td>Bus capacitive loading</td>
<td>—</td>
<td>400</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I²C bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement \( \text{TSU:DAT} \geq 250 \text{ ns} \) must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line \( \text{TR max.} + \text{TSU:DAT} = 1000 + 250 = 1250 \text{ ns} \) (according to the Standard mode I²C bus specification), before the SCL line is released.
46.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Graphs and tables are not available at this time.
47.0 PACKAGING INFORMATION

Package Marking Information

Legend: XX...X Customer-specific information or Microchip part number
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code
Pb-free JEDEC® designator for Matte Tin (Sn)
\* This package is Pb-free. The Pb-free JEDEC designator (\*3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
### Package Marking Information (Continued)

#### 28-Lead QFN (6x6 mm)

**Example**

```
PIN 1

XXXXXXXX
XXXXXXXX
YYWWNNNN
```

#### 28-Lead UQFN (6x6x0.5 mm)

**Example**

```
PIN 1

• XXXXX
XXXXXX
XXXXXX
YWWNNN
```

---

**Legend:**
- **XX...X:** Customer-specific information or Microchip part number
- **Y:** Year code (last digit of calendar year)
- **YY:** Year code (last 2 digits of calendar year)
- **WWW:** Week code (week of January 1 is week ‘01’)
- **NNN:** Alphanumeric traceability code
- **e3:** Pb-free JEDEC® designator for Matte Tin (Sn)

Note: This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

---

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
47.1 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

![Package Diagram]

<table>
<thead>
<tr>
<th>Units</th>
<th></th>
<th>INCHES</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
<td>NOM</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
<td>28</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
<td>.100 BSC</td>
</tr>
<tr>
<td>Top to Seating Plane</td>
<td>A</td>
<td>–</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
<td>.120</td>
</tr>
<tr>
<td>Base to Seating Plane</td>
<td>A1</td>
<td>.015</td>
</tr>
<tr>
<td>Shoulder to Shoulder Width</td>
<td>E</td>
<td>.290</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
<td>.240</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
<td>1.345</td>
</tr>
<tr>
<td>Tip to Seating Plane</td>
<td>L</td>
<td>.110</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
<td>.008</td>
</tr>
<tr>
<td>Upper Lead Width</td>
<td>b1</td>
<td>.040</td>
</tr>
<tr>
<td>Lower Lead Width</td>
<td>b</td>
<td>.014</td>
</tr>
<tr>
<td>Overall Row Spacing §</td>
<td>eB</td>
<td>–</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B
28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing C04-052C Sheet 1 of 2
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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<tbody>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Chamfer (Optional)</td>
<td>h</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Lead Angle</td>
<td>Θ</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
<tr>
<td>Mold Draft Angle Top</td>
<td>α</td>
</tr>
<tr>
<td>Mold Draft Angle Bottom</td>
<td>β</td>
</tr>
</tbody>
</table>

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.
28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
</tr>
<tr>
<td>Contact Pad Width (X28)</td>
<td>X</td>
</tr>
<tr>
<td>Contact Pad Length (X28)</td>
<td>Y</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>Gx</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A
28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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<thead>
<tr>
<th>Units</th>
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<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
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<td>c</td>
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<tr>
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<td>φ</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
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Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B
28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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**RECOMMENDED LAND PATTERN**

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<tbody>
<tr>
<td>Dimension Limits</td>
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</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
</tr>
<tr>
<td>Contact Pad Width (X28)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X28)</td>
<td>Y1</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A
28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN] With 0.55 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing C04-105C Sheet 1 of 2
28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN] 
With 0.55 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at 
http://www.microchip.com/packaging

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<td>Dimension</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Terminal Thickness</td>
<td>A3</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E2</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D2</td>
</tr>
<tr>
<td>Terminal Width</td>
<td>b</td>
</tr>
<tr>
<td>Terminal Length</td>
<td>L</td>
</tr>
<tr>
<td>Terminal-to-Exposed Pad</td>
<td>K</td>
</tr>
</tbody>
</table>

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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**RECOMMENDED LAND PATTERN**

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<table>
<thead>
<tr>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td>Dimension</td>
<td>Limits</td>
</tr>
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<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Optional Center Pad Width</td>
<td>W2</td>
</tr>
<tr>
<td>Optional Center Pad Length</td>
<td>T2</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C1</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C2</td>
</tr>
<tr>
<td>Contact Pad Width (X28)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X28)</td>
<td>Y1</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
28-Lead Plastic Quad Flat, No Lead Package (MX) - 6x6x0.5mm Body [UQFN]
Ultra-Thin with 0.40 x 0.60 mm Terminal Width/Length and Corner Anchors

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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<thead>
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<th>Units</th>
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<td>Pitch</td>
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<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Terminal Thickness</td>
<td>(A3)</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
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<td>Exposed Pad Width</td>
<td>E2</td>
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</tr>
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<td>Terminal Width</td>
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<tr>
<td>Corner Pad</td>
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<tr>
<td>Corner Pad, Metal Free Zone</td>
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<td>Terminal Length</td>
<td>L</td>
</tr>
<tr>
<td>Terminal-to-Exposed Pad</td>
<td>K</td>
</tr>
</tbody>
</table>

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.
4. Outermost portions of corner structures may vary slightly.

Microchip Technology Drawing C04-0209 Rev C Sheet 2 of 2
RECOMMENDED LAND PATTERN

<table>
<thead>
<tr>
<th>Units</th>
<th>MILIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Optional Center Pad Width</td>
<td>W1</td>
</tr>
<tr>
<td>Optional Center Pad Length</td>
<td>T2</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C1</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C2</td>
</tr>
<tr>
<td>Contact Pad Width (X28)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X28)</td>
<td>Y1</td>
</tr>
<tr>
<td>Corner Pad Width (X4)</td>
<td>X2</td>
</tr>
<tr>
<td>Corner Pad Length (X4)</td>
<td>Y2</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REVISION HISTORY

Revision A (8/2017)
Initial release of the document.
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<table>
<thead>
<tr>
<th>Device:</th>
<th>PIC18F25K83, PIC18LF25K83</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tape and Reel Option:</td>
<td>Blank = standard packaging (tube or tray)</td>
</tr>
<tr>
<td>Temperature Range:</td>
<td>E = -40°C to +125°C (Extended)</td>
</tr>
<tr>
<td>Package:</td>
<td>ML = 28-lead QFN 6x6mm</td>
</tr>
<tr>
<td>Pattern:</td>
<td>QTP, SQTP, Code or Special Requirements</td>
</tr>
</tbody>
</table>

Examples:

- PIC18F25K83-E/P 301 = Extended temp., SPDIP package, QTP pattern #301.
- PIC18F26K83-E/SO = Extended temp., SOIC package.
- PIC18F25K83T-I/ML = Tape and reel, Industrial temp., QFN package.

Note 1: Tape and Reel option is available for ML, MV, SO and SS packages with industrial Temperature Range only.

Note 2: Tape and Reel identifier only appears in catalog part number description. This identifier is used for ordering purposes and is not printed on the device package.
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