High-Performance RISC CPU:
- Only 49 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - DC – 125 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs)
  - FSRs can read program and data memory

Memory Features:
- Up to 8 KW Flash Program Memory:
  - Self-programmable under software control
  - Programmable code protection
  - Programmable write protection
- 256 Bytes of Data EEPROM
- Up to 1024 Bytes of RAM

High-Performance PWM Controller:
- Three Programmable Switch Mode Controller (PSMC) modules:
  - Digital and/or analog feedback control of PWM frequency and pulse begin/end times
  - 16-bit Period, Duty Cycle and Phase
  - 16 ns clock resolution
  - Supports Single PWM, Complementary, Push-Pull and 3-phase modes of operation
  - Dead-band control with 8-bit counter
  - Auto-shutdown and restart
  - Leading and falling edge blanking
  - Burst mode

Extreme Low-Power Management
PIC16LF1784/6/7 with XLP:
- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Timer1 Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 μA @ 32 kHz, 1.8V, typical
  - 32 μA/MHz @ 1.8V, typical

Analog Peripheral Features:
- Analog-to-Digital Converter (ADC):
  - Fully differential 12-bit converter
  - Up to 75 ksps conversion rate
  - 11 single-ended channels
  - 5 differential channels
  - Positive and negative reference selection
- 8-bit Digital-to-Analog Converter (DAC):
  - Output available externally
  - Positive and negative reference selection
  - Internal connections to comparators, op amps, Fixed Voltage Reference (FVR) and ADC
- Four High-Speed Comparators:
  - 50 ns response time @ VDD = 5V
  - Rail-to-rail inputs
  - Software selectable hysteresis
  - Internal connection to op amps, FVR and DAC
- Up to three Operational Amplifiers:
  - Rail-to-rail inputs/outputs
  - High/Low selectable Gain Bandwidth Product
  - Internal connection to DAC and FVR
- Fixed Voltage Reference (FVR):
  - 1.024V, 2.048V and 4.096V output levels
  - Internal connection to ADC, comparators and DAC

I/O Features:
- Up to 36 I/O Pins and 1 Input-only Pin:
- High Current Sink/Source for LED Drivers
- Individually Programmable Interrupt-on-Change Pins
- Individually Programmable Weak Pull-Ups
- Individual Input Level Selection
- Individually Programmable Slew Rate Control
- Individually Programmable Open Drain Outputs
Digital Peripheral Features:

- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Dedicated low-power 32 kHz oscillator driver
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Two Capture/Compare/PWM modules (CCP):
  - 16-bit capture, maximum resolution 12.5 ns
  - 16-bit compare, max resolution 31.25 ns
  - 10-bit PWM, max frequency 32 kHz
- Master Synchronous Serial Port (SSP) with SPI and I²C™ with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, RS-485 and LIN compatible
  - Auto-baud detect
  - Auto-wake-up on start

Oscillator Features:

- Operate up to 32 MHz from Precision Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency range from 32 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- 32.768 kHz Timer1 Oscillator:
  - Available as system clock
  - Low-power RTC
- External Oscillator Block with:
  - 4 crystal/resonator modes up to 32 MHz using 4x PLL
  - 3 external clock modes up to 32 MHz
- 4x Phase-Locked Loop (PLL)
- Fail-Safe Clock Monitor:
  - Detect and recover from external oscillator failure
- Two-Speed Start-up:
  - Minimize latency between code execution and external oscillator start-up

General Microcontroller Features:

- Power-Saving Sleep mode
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with Selectable Trip Point
- Extended Watchdog Timer (WDT)
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Debug (ICD)
- Enhanced Low-Voltage Programming (LVP)
- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF1784/6/7)
  - 2.3V to 5.5V (PIC16F1784/6/7)
### PIC16(L)F178X Family Types

<table>
<thead>
<tr>
<th>Device</th>
<th>Data Sheet Index</th>
<th>Program Memory Flash (words)</th>
<th>Data EEPROM (bytes)</th>
<th>Data SRAM (bytes)</th>
<th>I/O’s (3)</th>
<th>12-bit ADC (ch)</th>
<th>Operational Amplifiers</th>
<th>DAC (8/5-bit)</th>
<th>Timers (8/16-bit)</th>
<th>Programmable Switch Mode Controllers (PSMC)</th>
<th>CCP</th>
<th>EUSART</th>
<th>MSSP (I2C™/SPI)</th>
<th>Debug(1)</th>
<th>XLP</th>
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<tbody>
<tr>
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<td>2048</td>
<td>256</td>
<td>256</td>
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<td>2/1</td>
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<td>1/0</td>
<td>2/1</td>
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<td>1</td>
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<td>2/1</td>
<td>3</td>
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<td>4</td>
<td>2</td>
<td>1/3</td>
<td>4</td>
<td>3</td>
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<td>1</td>
<td>1</td>
<td>Y</td>
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<tr>
<td>PIC16(L)F1789</td>
<td>(3)</td>
<td>16384</td>
<td>256</td>
<td>2048</td>
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<td>4</td>
<td>3</td>
<td>1/3</td>
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<td>3</td>
<td>1</td>
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<td>1</td>
<td>Y</td>
</tr>
</tbody>
</table>

**Note 1:** I - Debugging, Integrated on Chip; H - Debugging, available using Debug Header.  
2: One pin is input-only.

**Data Sheet Index:** (Unshaded devices are described in this document.)

1: DS40001579 PIC16(L)F1782/3 Data Sheet, 28-Pin Flash, 8-bit Advanced Analog MCUs.  
2: DS40001637 PIC16(L)F1784/6/7 Data Sheet, 28/40/44-Pin Flash, 8-bit Advanced Analog MCUs.  
3: DS40001675 PIC16(L)F1788/9 Data Sheet, 28/40/44-Pin Flash, 8-bit Advanced Analog MCUs.

**Note:** For other small form-factor package availability and marking information, please visit [http://www.microchip.com/packaging](http://www.microchip.com/packaging) or contact your local sales office.
**Pin Diagram – 28-Pin SPDIP, SOIC, SSOP**

Note: See Table 1 for the location of all peripheral functions.

**Pin Diagram – 28-Pin QFN**

Note: See Table 1 for the location of all peripheral functions.
Note: See Table 2 for the location of all peripheral functions.
Pin Diagram – 40-Pin UQFN (5x5)

Note: See Table 2 for the location of all peripheral functions.
Note: See Table 2 for the location of all peripheral functions.
Note: See Table 2 for the location of all peripheral functions.
### PIN ALLOCATION TABLE

**TABLE 1: 28-PIN ALLOCATION TABLE (PIC16(L)F1786)**

<table>
<thead>
<tr>
<th>IO</th>
<th>28-Pin SPDIP, SOIC, SSOP</th>
<th>28-Pin QFN, ADC</th>
<th>Reference</th>
<th>Comparator</th>
<th>Operation Amplifiers</th>
<th>8-bit DAC</th>
<th>Timers</th>
<th>PSIM</th>
<th>CCP</th>
<th>BUSAR</th>
<th>MESSP</th>
<th>Interrupt</th>
<th>Pull-up</th>
<th>Basic</th>
</tr>
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<tbody>
<tr>
<td>RA0</td>
<td>2</td>
<td>27</td>
<td>AN0</td>
<td>—</td>
<td>C1IN0-C2IN0-C3IN0-C4IN0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
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<td>IOC</td>
<td>Y</td>
</tr>
<tr>
<td>RA1</td>
<td>3</td>
<td>28</td>
<td>AN1</td>
<td>—</td>
<td>C1IN1-C2IN1-C3IN1-C4IN1</td>
<td>OPA1OUT</td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IOC</td>
<td>Y</td>
</tr>
<tr>
<td>RA2</td>
<td>4</td>
<td>1</td>
<td>AN2</td>
<td>—</td>
<td>VREF-DAC1VREF+</td>
<td>DAC1OUT1</td>
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<td>—</td>
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<td>IOC</td>
<td>Y</td>
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<tr>
<td>RA3</td>
<td>5</td>
<td>2</td>
<td>AN3</td>
<td>—</td>
<td>VREF+DAC1VREF+</td>
<td>C1IN1+</td>
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<td>—</td>
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<td>IOC</td>
<td>Y</td>
</tr>
<tr>
<td>RA4</td>
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<td>—</td>
<td>—</td>
<td>C1OUT</td>
<td>OPA1In+</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
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<td>RA5</td>
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<td>C2OUT</td>
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<td>IOC</td>
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<td>RA6</td>
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<td>—</td>
<td>C2OUT[1]</td>
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<tr>
<td>RA7</td>
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<td>—</td>
<td>—</td>
<td>PSMC1CLK</td>
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<td>—</td>
<td>IOC</td>
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</tr>
<tr>
<td>RB0</td>
<td>21</td>
<td>18</td>
<td>AN12</td>
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<td>C2IN1+</td>
<td>PSMC1IN</td>
<td>CCP1[1]</td>
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<td>—</td>
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<td>—</td>
<td>—</td>
<td>INT</td>
<td>IOC</td>
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<tr>
<td>RB1</td>
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<td>19</td>
<td>AN10</td>
<td>—</td>
<td>C1IN3-C2IN3-C3IN3-C4IN3</td>
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<td>—</td>
<td>—</td>
<td>—</td>
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<td>RB2</td>
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<td>AN8</td>
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<td>OPA2In-</td>
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<td>IOC</td>
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<tr>
<td>RB3</td>
<td>24</td>
<td>21</td>
<td>AN9</td>
<td>—</td>
<td>C1IN2-C2IN2-C3IN2-C4IN2</td>
<td>OPA2In+</td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IOC</td>
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<tr>
<td>RB4</td>
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<td>22</td>
<td>AN11</td>
<td>—</td>
<td>C3IN1+</td>
<td>OPA2In+</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
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<td>C4IN2-C3OUT</td>
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<td>IOC</td>
<td>Y</td>
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</table>

**Note 1:** Alternate pin function selected with the APFCON1 (Register 13-1) and APFCON2 (Register 13-2) registers.
### TABLE 1: 28-PIN ALLOCATION TABLE (PIC16(L)F1786) (Continued)

<table>
<thead>
<tr>
<th>I/O</th>
<th>28-Pin SPDIP</th>
<th>28-Pin QFN, SSOP</th>
<th>28-Pin QFN, ADC</th>
<th>Comparator</th>
<th>Operation Amplifiers</th>
<th>8-bit DAC</th>
<th>Timers</th>
<th>PS/RC</th>
<th>CCP</th>
<th>EUSART</th>
<th>MSSP</th>
<th>Interrupt</th>
<th>Pull-up</th>
<th>Basic</th>
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<tbody>
<tr>
<td>RB7</td>
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<td>—</td>
<td>RX(1)</td>
<td>SCK(1)</td>
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<td>T1CKI</td>
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<td>SDA</td>
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<td>CCP2</td>
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<td>IOC</td>
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<td>C4OUT</td>
<td>PSMC2B</td>
<td>CCP2</td>
<td>TX</td>
<td>—</td>
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<td>IOC</td>
<td>Y</td>
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<td>—</td>
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<td>—</td>
<td>—</td>
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<td>Y</td>
<td>Vpp</td>
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<td>17</td>
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<td>—</td>
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<td>—</td>
<td>VDD</td>
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<td>8, 19</td>
<td>5, 16</td>
<td>—</td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>Vss</td>
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</tr>
</tbody>
</table>

**Note 1:** Alternate pin function selected with the APFCON1 (Register 13-1) and APFCON2 (Register 13-2) registers.
<table>
<thead>
<tr>
<th>I/O</th>
<th>40-Pin PDIP</th>
<th>40-Pin UGPN</th>
<th>44-Pin TQFP</th>
<th>44-Pin GPN</th>
<th>ADC</th>
<th>Reference</th>
<th>Comparator</th>
<th>Op Amps</th>
<th>8-bit DAC</th>
<th>Timers</th>
<th>PSMC</th>
<th>EUSART</th>
<th>MSSP</th>
<th>Interrupt</th>
<th>Pull-up</th>
<th>Basic</th>
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**Note 1:** Alternate pin function selected with the APFCON1 (Register 13-1) and APFCON2 (Register 13-2) registers.
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**Note 1:** Alternate pin function selected with the APFCON1 (Register 13-1) and APFCON2 (Register 13-2) registers.
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1.0 DEVICE OVERVIEW

The PIC16(L)F1784/6/7 are described within this data sheet. The block diagram of these devices are shown in Figure 1-1. The available peripherals are shown in Table 1-1, and the pin out descriptions are shown in Table 1-2.

### TABLE 1-1: DEVICE PERIPHERAL SUMMARY

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<td>(5-bit DAC) D2</td>
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<td>(5-bit DAC) D3</td>
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<td>(5-bit DAC) D4</td>
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<td>Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)</td>
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<td>Op Amp 2</td>
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<td>Op Amp 3</td>
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<td>Programmable Switch Mode Controller (PSMC)</td>
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<td>Timers</td>
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</tr>
<tr>
<td>Timer0</td>
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<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Timer1</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
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<tr>
<td>Timer2</td>
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<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
</tbody>
</table>
FIGURE 1-1: PIC16(L)F1784/6/7 BLOCK DIAGRAM

Note 1: PIC16(L)F1784/7 only.
2: See applicable chapters for more information on peripherals.
**TABLE 1-2: PIC16(L)F1784/6/7 PINOUT DESCRIPTION**

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
<th>Input Type</th>
<th>Output Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RA0/AN0/C1IN0-/C2IN0-/C3IN0-/C4IN0-</td>
<td>RA0</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td></td>
<td>AN0</td>
<td>AN</td>
<td>—</td>
<td>ADC Channel 0 input.</td>
</tr>
<tr>
<td></td>
<td>C1IN0-</td>
<td>AN</td>
<td>—</td>
<td>Comparator C1 negative input.</td>
</tr>
<tr>
<td></td>
<td>C2IN0-</td>
<td>AN</td>
<td>—</td>
<td>Comparator C2 negative input.</td>
</tr>
<tr>
<td></td>
<td>C3IN0-</td>
<td>AN</td>
<td>—</td>
<td>Comparator C3 negative input.</td>
</tr>
<tr>
<td></td>
<td>C4IN0-</td>
<td>AN</td>
<td>—</td>
<td>Comparator C4 negative input.</td>
</tr>
<tr>
<td>RA1/AN1/C1IN1-/C2IN1-/C3IN1-/C4IN1-/OPA1OUT</td>
<td>RA1</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td></td>
<td>AN1</td>
<td>AN</td>
<td>—</td>
<td>ADC Channel 1 input.</td>
</tr>
<tr>
<td></td>
<td>C1IN1-</td>
<td>AN</td>
<td>—</td>
<td>Comparator C1 negative input.</td>
</tr>
<tr>
<td></td>
<td>C2IN1-</td>
<td>AN</td>
<td>—</td>
<td>Comparator C2 negative input.</td>
</tr>
<tr>
<td></td>
<td>C3IN1-</td>
<td>AN</td>
<td>—</td>
<td>Comparator C3 negative input.</td>
</tr>
<tr>
<td></td>
<td>C4IN1-</td>
<td>AN</td>
<td>—</td>
<td>Comparator C4 negative input.</td>
</tr>
<tr>
<td></td>
<td>OPA1OUT</td>
<td>—</td>
<td>AN</td>
<td>Operational Amplifier 1 output.</td>
</tr>
<tr>
<td>RA2/AN2/C1IN0+/C2IN0+/C3IN0+/C4IN0+/DAC1OUT1/VREF-/DAC1VREF-/OPA1IN-</td>
<td>RA2</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td></td>
<td>AN2</td>
<td>AN</td>
<td>—</td>
<td>ADC Channel 2 input.</td>
</tr>
<tr>
<td></td>
<td>C1IN0+</td>
<td>AN</td>
<td>—</td>
<td>Comparator C1 positive input.</td>
</tr>
<tr>
<td></td>
<td>C2IN0+</td>
<td>AN</td>
<td>—</td>
<td>Comparator C2 positive input.</td>
</tr>
<tr>
<td></td>
<td>C3IN0+</td>
<td>AN</td>
<td>—</td>
<td>Comparator C3 positive input.</td>
</tr>
<tr>
<td></td>
<td>C4IN0+</td>
<td>AN</td>
<td>—</td>
<td>Comparator C4 positive input.</td>
</tr>
<tr>
<td></td>
<td>DAC1OUT1</td>
<td>—</td>
<td>AN</td>
<td>Digital-to-Analog Converter output.</td>
</tr>
<tr>
<td></td>
<td>VREF-</td>
<td>AN</td>
<td>—</td>
<td>ADC Negative Voltage Reference input.</td>
</tr>
<tr>
<td></td>
<td>DAC1VREF-</td>
<td>AN</td>
<td>—</td>
<td>Digital-to-Analog Converter negative reference.</td>
</tr>
<tr>
<td>RA3/AN3/VREF+/C1IN1+/DAC1VREF+</td>
<td>RA3</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td></td>
<td>AN3</td>
<td>AN</td>
<td>—</td>
<td>ADC Channel 3 input.</td>
</tr>
<tr>
<td></td>
<td>VREF+</td>
<td>AN</td>
<td>—</td>
<td>ADC Voltage Reference input.</td>
</tr>
<tr>
<td></td>
<td>C1IN1+</td>
<td>AN</td>
<td>—</td>
<td>Comparator C1 positive input.</td>
</tr>
<tr>
<td></td>
<td>DAC1VREF+</td>
<td>AN</td>
<td>—</td>
<td>Digital-to-Analog Converter positive reference.</td>
</tr>
<tr>
<td>RA4/C1OUT/OPA1IN+/T0CKI</td>
<td>RA4</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td></td>
<td>C1OUT</td>
<td>—</td>
<td>CMOS</td>
<td>Comparator C1 output.</td>
</tr>
<tr>
<td></td>
<td>OPA1IN+</td>
<td>AN</td>
<td>—</td>
<td>Operational Amplifier 1 non-inverting input.</td>
</tr>
<tr>
<td></td>
<td>T0CKI</td>
<td>ST</td>
<td>—</td>
<td>Timer0 clock input.</td>
</tr>
<tr>
<td>RA5/AN4/C2OUT(1)/OPA1IN-/SS</td>
<td>RA5</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td></td>
<td>AN4</td>
<td>AN</td>
<td>—</td>
<td>ADC Channel 4 input.</td>
</tr>
<tr>
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<td>C2OUT</td>
<td>—</td>
<td>CMOS</td>
<td>Comparator C2 output.</td>
</tr>
<tr>
<td></td>
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<td>AN</td>
<td>—</td>
<td>Operational Amplifier 1 inverting input.</td>
</tr>
<tr>
<td></td>
<td>SS</td>
<td>ST</td>
<td>—</td>
<td>Slave Select input.</td>
</tr>
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</table>

**Legend:**
- AN = Analog input or output
- CMOS = CMOS compatible input or output
- OD = Open Drain
- TTL = TTL compatible input
- ST = Schmitt Trigger input with CMOS levels
- HV = High Voltage
- XTAL = Crystal
- I<sup>2</sup>C™ = Schmitt Trigger input with I<sup>2</sup>C levels

**Note:**
1. Pin functions can be assigned to one of two locations via software. See Register 13-1.
2. All pins have interrupt-on-change functionality.
3. PIC16(L)F1784/6 only.
4. PIC16(L)F1786 only.
### TABLE 1-2: PIC16(L)F1784/6/7 PINOUT DESCRIPTION (CONTINUED)

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
<th>Input Type</th>
<th>Output Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RA6/C2OUT(1)/OSC2/CLKOUT/VCAP</td>
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<td>CMOS</td>
<td>Comparator C2 output.</td>
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<tr>
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<td>OSC2</td>
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<td>XTAL</td>
<td>Crystal/Resonator (LP, XT, HS modes).</td>
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<tr>
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<td>CLKOUT</td>
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<td>CMOS</td>
<td>Fosc/4 output.</td>
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<tr>
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<td>VCAP</td>
<td>Power</td>
<td>Power</td>
<td>Filter capacitor for Voltage Regulator.</td>
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<td>RA7/PSMC1CLK/PSMC2CLK/PSMC3CLK/OSC1/CLKin</td>
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<td>General purpose I/O.</td>
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<td>PSMC2CLK</td>
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<td>—</td>
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<tr>
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<td>OSC1</td>
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<td>XTAL</td>
<td>Crystal/Resonator (LP, XT, HS modes).</td>
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<tr>
<td></td>
<td>CLKin</td>
<td>st</td>
<td>—</td>
<td>External clock input (EC mode).</td>
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<td>RB0/AN12/C2IN1+/PSMC1IN/PSMC2IN/PSMC3IN/CCP1(1)/INT</td>
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<td>CMOS</td>
<td>General purpose I/O.</td>
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<td>ST</td>
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<td>PSMC1 Event Trigger input.</td>
</tr>
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<td>PSMC2IN</td>
<td>ST</td>
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<td>ST</td>
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<td>CMOS</td>
<td>Capture/Compare/PWM1.</td>
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<tr>
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<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
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</tr>
<tr>
<td></td>
<td>C2IN3-</td>
<td>AN</td>
<td>—</td>
<td>Comparator C2 negative input.</td>
</tr>
<tr>
<td></td>
<td>C3IN3-</td>
<td>AN</td>
<td>—</td>
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</tr>
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<td>C4IN3-</td>
<td>AN</td>
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<tr>
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<td>AN</td>
<td>Operational Amplifier 2 output.</td>
</tr>
<tr>
<td>RB2/AN8/OPA2IN-/CLKR</td>
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<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
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<td>AN8</td>
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<td>—</td>
<td>ADC Channel 8 input.</td>
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<tr>
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<td>OPA2IN-</td>
<td>AN</td>
<td>—</td>
<td>Operational Amplifier 2 inverting input.</td>
</tr>
<tr>
<td></td>
<td>CLKR</td>
<td>—</td>
<td>CMOS</td>
<td>Clock output.</td>
</tr>
<tr>
<td>RB3/AN9/C1IN2-/C2IN2-/C3IN2-/OPA2IN+/CCP2(1)</td>
<td>RB3</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
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<td>AN9</td>
<td>AN</td>
<td>—</td>
<td>ADC Channel 9 input.</td>
</tr>
<tr>
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<td>C1IN2-</td>
<td>AN</td>
<td>—</td>
<td>Comparator C1 negative input.</td>
</tr>
<tr>
<td></td>
<td>C2IN2-</td>
<td>AN</td>
<td>—</td>
<td>Comparator C2 negative input.</td>
</tr>
<tr>
<td></td>
<td>C3IN2-</td>
<td>AN</td>
<td>—</td>
<td>Comparator C3 negative input.</td>
</tr>
<tr>
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<td>OPA2IN+</td>
<td>AN</td>
<td>—</td>
<td>Operational Amplifier 2 non-inverting input.</td>
</tr>
<tr>
<td></td>
<td>CCP2</td>
<td>ST</td>
<td>CMOS</td>
<td>Capture/Compare/PWM2.</td>
</tr>
<tr>
<td>RB4/AN11/C3IN1+</td>
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<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
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<td>AN11</td>
<td>AN</td>
<td>—</td>
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</tr>
<tr>
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<td>C3IN1+</td>
<td>AN</td>
<td>—</td>
<td>Comparator C3 positive input.</td>
</tr>
</tbody>
</table>

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C™ = Schmitt Trigger input with I²C levels HV = High Voltage XTAL = Crystal

Note 1: Pin functions can be assigned to one of two locations via software. See Register 13-1.
2: All pins have interrupt-on-change functionality.
3: PIC16(L)F1784/7 only.
4: PIC16(L)F1786 only.
<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
<th>Input Type</th>
<th>Output Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RB5/AN13/C4IN2-/T1G/CCP3(1) SDO(1)</td>
<td>RB5</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td>AN13</td>
<td>AN</td>
<td>—</td>
<td>—</td>
<td>ADC Channel 13 input.</td>
</tr>
<tr>
<td>C4IN2-</td>
<td>AN</td>
<td>—</td>
<td>—</td>
<td>Comparator C4 negative input.</td>
</tr>
<tr>
<td>T1G</td>
<td>ST</td>
<td>—</td>
<td>—</td>
<td>Timer1 gate input.</td>
</tr>
<tr>
<td>CCP3</td>
<td>ST</td>
<td>CMOS</td>
<td>Capture/Compare/PWM3.</td>
<td></td>
</tr>
<tr>
<td>SDO</td>
<td>—</td>
<td>CMOS</td>
<td>SPI data output.</td>
<td></td>
</tr>
<tr>
<td>RB6/C4IN1+/TX(1)/CK(1)/SD(1)/SDA(1)/ICSPCLK</td>
<td>RB6</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td>C4IN1+</td>
<td>AN</td>
<td>—</td>
<td>—</td>
<td>Comparator C4 positive input.</td>
</tr>
<tr>
<td>TX</td>
<td>—</td>
<td>CMOS</td>
<td>EUSART asynchronous transmit.</td>
<td></td>
</tr>
<tr>
<td>CK</td>
<td>ST</td>
<td>CMOS</td>
<td>EUSART synchronous clock.</td>
<td></td>
</tr>
<tr>
<td>SDI</td>
<td>ST</td>
<td>—</td>
<td>—</td>
<td>SPI data input.</td>
</tr>
<tr>
<td>SDA</td>
<td>I²C</td>
<td>OD</td>
<td>I²C™ data input/output.</td>
<td></td>
</tr>
<tr>
<td>ICSPCLK</td>
<td>ST</td>
<td>—</td>
<td>—</td>
<td>Serial Programming Clock.</td>
</tr>
<tr>
<td>RB7/DAC1OUT2/RX(1)/DT(1)/SCK(1)/SCL(1)/ICSPDAT</td>
<td>RB7</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td>DAC1OUT2</td>
<td>—</td>
<td>AN</td>
<td>Voltage Reference output.</td>
<td></td>
</tr>
<tr>
<td>RX</td>
<td>ST</td>
<td>—</td>
<td>—</td>
<td>EUSART asynchronous input.</td>
</tr>
<tr>
<td>DT</td>
<td>ST</td>
<td>CMOS</td>
<td>EUSART synchronous data.</td>
<td></td>
</tr>
<tr>
<td>SCK</td>
<td>ST</td>
<td>CMOS</td>
<td>SPI clock.</td>
<td></td>
</tr>
<tr>
<td>SCL</td>
<td>I²C</td>
<td>OD</td>
<td>I²C™ clock.</td>
<td></td>
</tr>
<tr>
<td>ICSPDAT</td>
<td>ST</td>
<td>CMOS</td>
<td>ICSP™ Data I/O.</td>
<td></td>
</tr>
<tr>
<td>RC0/T1OSO/T1CKI/PSMC1A</td>
<td>RC0</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td>T1OSO</td>
<td>XTAL</td>
<td>XTAL</td>
<td>Timer1 Oscillator Connection.</td>
<td></td>
</tr>
<tr>
<td>T1CKI</td>
<td>ST</td>
<td>—</td>
<td>—</td>
<td>Timer1 clock input.</td>
</tr>
<tr>
<td>PSMC1A</td>
<td>—</td>
<td>CMOS</td>
<td>PSMC1 output A.</td>
<td></td>
</tr>
<tr>
<td>RC1/T1OSI/PSMC1B/CCP2</td>
<td>RC1</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td>T1OSI</td>
<td>XTAL</td>
<td>XTAL</td>
<td>Timer1 Oscillator Connection.</td>
<td></td>
</tr>
<tr>
<td>PSMC1B</td>
<td>—</td>
<td>CMOS</td>
<td>PSMC1 output B.</td>
<td></td>
</tr>
<tr>
<td>CCP2</td>
<td>ST</td>
<td>CMOS</td>
<td>Capture/Compare/PWM2.</td>
<td></td>
</tr>
<tr>
<td>RC2/PSMC1C/CCP1</td>
<td>RC2</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td>PSMC1C</td>
<td>—</td>
<td>CMOS</td>
<td>PSMC1 output C.</td>
<td></td>
</tr>
<tr>
<td>CCP1</td>
<td>ST</td>
<td>CMOS</td>
<td>Capture/Compare/PWM1.</td>
<td></td>
</tr>
<tr>
<td>RC3/PSMC1D/SCK(1)/SCL(1)</td>
<td>RC3</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td>PSMC1D</td>
<td>—</td>
<td>CMOS</td>
<td>PSMC1 output D.</td>
<td></td>
</tr>
<tr>
<td>SCK</td>
<td>ST</td>
<td>CMOS</td>
<td>SPI clock.</td>
<td></td>
</tr>
<tr>
<td>SCL</td>
<td>I²C</td>
<td>OD</td>
<td>I²C™ clock.</td>
<td></td>
</tr>
<tr>
<td>RC4/PSMC1E/SDI(1)/SDA(1)</td>
<td>RC4</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td>PSMC1E</td>
<td>—</td>
<td>CMOS</td>
<td>PSMC1 output E.</td>
<td></td>
</tr>
<tr>
<td>SDI</td>
<td>ST</td>
<td>—</td>
<td>—</td>
<td>SPI data input.</td>
</tr>
<tr>
<td>SDA</td>
<td>I²C</td>
<td>OD</td>
<td>I²C™ data input/output.</td>
<td></td>
</tr>
</tbody>
</table>

Legend:  
AN = Analog input or output  
CMOS = CMOS compatible input or output  
OD = Open Drain  
TTL = TTL compatible input  
ST = Schmitt Trigger input with CMOS levels  
I²C™ = Schmitt Trigger input with I²C levels  
HV = High Voltage  
XTAL = Crystal

Note  
1: Pin functions can be assigned to one of two locations via software. See Register 13-1.  
2: All pins have interrupt-on-change functionality.  
3: PIC16(L)F1784/7 only.  
4: PIC16(L)F1786 only.
### TABLE 1-2: PIC16(L)F1784/6/7 PINOUT DESCRIPTION (CONTINUED)

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
<th>Input Type</th>
<th>Output Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RC5/PSMC1F/SDO(1)</td>
<td>RC5</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td></td>
<td>PSMC1F</td>
<td>—</td>
<td>CMOS</td>
<td>PSMC1 output F.</td>
</tr>
<tr>
<td></td>
<td>SDO</td>
<td>—</td>
<td>CMOS</td>
<td>SPI data output.</td>
</tr>
<tr>
<td>RC6/PSMC2A/TX(1)/CK(1)</td>
<td>RC6</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td></td>
<td>PSMC2A</td>
<td>—</td>
<td>CMOS</td>
<td>PSMC2 output A.</td>
</tr>
<tr>
<td></td>
<td>TX</td>
<td>—</td>
<td>CMOS</td>
<td>EUSART asynchronous transmit.</td>
</tr>
<tr>
<td></td>
<td>CK</td>
<td>ST</td>
<td>CMOS</td>
<td>EUSART synchronous clock.</td>
</tr>
<tr>
<td>RC7/PSMC2B/RX(1)/DT(1)/</td>
<td>RC7</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td>C4OUT(4)</td>
<td>PSMC2B</td>
<td>—</td>
<td>CMOS</td>
<td>PSMC2 output B.</td>
</tr>
<tr>
<td></td>
<td>RX</td>
<td>ST</td>
<td>—</td>
<td>EUSART asynchronous input.</td>
</tr>
<tr>
<td></td>
<td>DT</td>
<td>ST</td>
<td>CMOS</td>
<td>EUSART synchronous data.</td>
</tr>
<tr>
<td></td>
<td>C4OUT</td>
<td>—</td>
<td>CMOS</td>
<td>Comparator C4 output.</td>
</tr>
<tr>
<td>RD0(3)/OPA3IN+</td>
<td>RD0</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td></td>
<td>OPA3IN+</td>
<td>—</td>
<td>AN</td>
<td>Operational Amplifier 3 non-inverting input.</td>
</tr>
<tr>
<td>RD1(3)/AN21/C1IN4-/C2IN4-</td>
<td>RD1</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td>C3IN4-/C4IN4-/OPA3OUT</td>
<td>AN21</td>
<td>—</td>
<td>AN</td>
<td>ADC Channel 21 input.</td>
</tr>
<tr>
<td></td>
<td>C1IN4-</td>
<td>—</td>
<td>AN</td>
<td>Comparator C4 negative input.</td>
</tr>
<tr>
<td></td>
<td>C2IN4-</td>
<td>—</td>
<td>AN</td>
<td>Comparator C4 negative input.</td>
</tr>
<tr>
<td></td>
<td>C3IN4-</td>
<td>—</td>
<td>AN</td>
<td>Comparator C4 negative input.</td>
</tr>
<tr>
<td></td>
<td>C4IN4-</td>
<td>—</td>
<td>AN</td>
<td>Comparator C4 negative input.</td>
</tr>
<tr>
<td></td>
<td>OPA3OUT</td>
<td>—</td>
<td>AN</td>
<td>Operational Amplifier 3 output.</td>
</tr>
<tr>
<td>RD2(3)/OPA3IN-</td>
<td>RD2</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td></td>
<td>OPA3IN-</td>
<td>—</td>
<td>AN</td>
<td>Operational Amplifier 3 inverting input.</td>
</tr>
<tr>
<td>RD3(3)</td>
<td>RD3</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td>RD4(3)/PSMC3F</td>
<td>RD4</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td></td>
<td>PSMC3F</td>
<td>—</td>
<td>CMOS</td>
<td>PSMC3 output F.</td>
</tr>
<tr>
<td>RD5(3)/PSMC3E</td>
<td>RD5</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td></td>
<td>PSMC3E</td>
<td>—</td>
<td>CMOS</td>
<td>PSMC3 output E.</td>
</tr>
<tr>
<td>RD6(3)/C3OUT/PSMC3D</td>
<td>RD6</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td></td>
<td>C3OUT</td>
<td>—</td>
<td>CMOS</td>
<td>Comparator C3 output.</td>
</tr>
<tr>
<td></td>
<td>PSMC3D</td>
<td>—</td>
<td>CMOS</td>
<td>PSMC3 output D.</td>
</tr>
<tr>
<td>RD7(3)/C4OUT/PSMC3C</td>
<td>RD7</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td></td>
<td>C4OUT</td>
<td>—</td>
<td>CMOS</td>
<td>Comparator C4 output.</td>
</tr>
<tr>
<td></td>
<td>PSMC3C</td>
<td>—</td>
<td>CMOS</td>
<td>PSMC3 output C.</td>
</tr>
<tr>
<td>RE0(3)/AN5/CCP3(1)</td>
<td>RE0</td>
<td>TTL/ST</td>
<td>—</td>
<td>General purpose input.</td>
</tr>
<tr>
<td></td>
<td>AN5</td>
<td>—</td>
<td>AN</td>
<td>ADC Channel 5 input.</td>
</tr>
<tr>
<td></td>
<td>CCP3</td>
<td>ST</td>
<td>CMOS</td>
<td>Capture/Compare/PWM3.</td>
</tr>
<tr>
<td>RE1(3)/AN6/PSMC3B</td>
<td>RE1</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td></td>
<td>AN6</td>
<td>—</td>
<td>AN</td>
<td>ADC Channel 6 input.</td>
</tr>
<tr>
<td></td>
<td>PSMC3B</td>
<td>—</td>
<td>CMOS</td>
<td>PSMC3 output B.</td>
</tr>
</tbody>
</table>

**Legend:**
- **AN** = Analog input or output
- **CMOS** = CMOS compatible input or output
- **OD** = Open Drain
- **TTL** = TTL compatible input
- **ST** = Schmitt Trigger input with CMOS levels
- **HV** = High Voltage
- **XTAL** = Crystal levels
- **I²C™** = Schmitt Trigger input with I²C levels

**Note**
1. Pin functions can be assigned to one of two locations via software. See **Register 13-1**.
2. All pins have interrupt-on-change functionality.
3. PIC16(L)F1784/7 only.
4. PIC16(L)F1786 only.
### TABLE 1-2: PIC16(L)F1784/6/7 PINOUT DESCRIPTION (CONTINUED)

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
<th>Input Type</th>
<th>Output Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RE2(3)/AN7/PSMC3A</td>
<td>RE2</td>
<td>TTL/ST</td>
<td>CMOS</td>
<td>General purpose I/O.</td>
</tr>
<tr>
<td>AN7</td>
<td>AN</td>
<td>—</td>
<td>—</td>
<td>ADC Channel 7 input.</td>
</tr>
<tr>
<td>PSMC3A</td>
<td>—</td>
<td>CMOS</td>
<td>PSMC3 output A.</td>
<td></td>
</tr>
<tr>
<td>RE3/MCLR/VPP</td>
<td>RE3</td>
<td>TTL/ST</td>
<td>—</td>
<td>General purpose input.</td>
</tr>
<tr>
<td>MCLR</td>
<td>ST</td>
<td>—</td>
<td>Master Clear with internal pull-up.</td>
<td></td>
</tr>
<tr>
<td>VPP</td>
<td>HV</td>
<td>—</td>
<td>Programming voltage.</td>
<td></td>
</tr>
<tr>
<td>VDD</td>
<td>VDD</td>
<td>Power</td>
<td>—</td>
<td>Positive supply.</td>
</tr>
<tr>
<td>VSS</td>
<td>VSS</td>
<td>Power</td>
<td>—</td>
<td>Ground reference.</td>
</tr>
</tbody>
</table>

**Legend:**
- AN = Analog input or output
- CMOS = CMOS compatible input or output
- OD = Open Drain
- TTL = TTL compatible input
- ST = Schmitt Trigger input with CMOS levels
- HV = High Voltage
- XTAL = Crystal
- I²C™ = Schmitt Trigger input with I²C levels
- XTAL = Crystal

**Note 1:** Pin functions can be assigned to one of two locations via software. See Register 13-1.

**Note 2:** All pins have interrupt-on-change functionality.

**Note 3:** PIC16(L)F1784/7 only.

**Note 4:** PIC16(L)F1786 only.
2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.
- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 2-1: CORE BLOCK DIAGRAM
2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See 8.5 “Automatic Context Saving”, for more information.

2.2 16-level Stack with Overflow and Underflow

These devices have an external stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled will cause a software Reset. See Section 3.5 “Stack” for more details.

2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See Section 3.6 “Indirect Addressing” for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See Section 29.0 “Instruction Set Summary” for more details.
3.0 MEMORY ORGANIZATION

These devices contain the following types of memory:

- Program Memory
  - Configuration Words
  - Device ID
  - User ID
  - Flash Program Memory
- Data Memory
  - Core Registers
  - Special Function Registers
  - General Purpose RAM
  - Common RAM
- Data EEPROM memory\(^{(1)}\)

The following features are associated with access and control of program memory and data memory:

- PCL and PCLATH
- Stack
- Indirect Addressing

3.1 Program Memory Organization

The enhanced mid-range core has a 15-bit program counter capable of addressing a 32K x 14 program memory space. Table 3-1 shows the memory sizes implemented for the PIC16(L)F1784/6/7 family. Accessing a location above these boundaries will cause a wrap-around within the implemented memory space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figures 3-1 and 3-2).

Note 1: The Data EEPROM Memory and the method to access Flash memory through the EECON registers is described in Section 12.0 “Data EEPROM and Flash Program Memory Control”.

<table>
<thead>
<tr>
<th>Device</th>
<th>Program Memory Space (Words)</th>
<th>Last Program Memory Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC16(L)F1784</td>
<td>4,096</td>
<td>0FFFH</td>
</tr>
<tr>
<td>PIC16(L)F1786/7</td>
<td>8,192</td>
<td>1FFFH</td>
</tr>
</tbody>
</table>
FIGURE 3-1: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1786/7

PC<14:0> 0000h 0004h 0005h
Stack Level 0
Stack Level 1
Stack Level 15
Reset Vector
Interrupt Vector
Page 0
Page 1
Page 2
Page 3
Rollover to Page 0
Rollover to Page 3

On-chip Program Memory

CALL, CALLW
RETURN, RETLW
Interrupt, RETFIE

FIGURE 3-2: PROGRAM MEMORY MAP AND STACK FOR PIC16(L)F1784

PC<14:0> 0000h 0004h 0005h
Stack Level 0
Stack Level 1
Stack Level 15
Reset Vector
Interrupt Vector
Page 0
Page 1
Rollover to Page 0
Rollover to Page 1

On-chip Program Memory

CALL, CALLW
RETURN, RETLW
Interrupt, RETFIE

Page 3
17FFh 1800h 1FFFFh 2000h
Page 2
0FFFFh 1000h 0FFFh 0800h
Page 1
07FFh 0800h
Page 0
3.1.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.1.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

```
EXAMPLE 3-1: RETLW INSTRUCTION

<table>
<thead>
<tr>
<th>constants</th>
</tr>
</thead>
<tbody>
<tr>
<td>BRW</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>RETLW DATA0</td>
</tr>
<tr>
<td>RETLW DATA1</td>
</tr>
<tr>
<td>RETLW DATA2</td>
</tr>
<tr>
<td>RETLW DATA3</td>
</tr>
</tbody>
</table>

my_function              |
| ;... LOTS OF CODE...    |
| MOVWI DATA_INDEX        |
| call constants          |
| ;... THE CONSTANT IS IN W |
```

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.1.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower 8 bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

```
EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

<table>
<thead>
<tr>
<th>constants</th>
</tr>
</thead>
<tbody>
<tr>
<td>RETLW DATA0</td>
</tr>
<tr>
<td>RETLW DATA1</td>
</tr>
<tr>
<td>RETLW DATA2</td>
</tr>
<tr>
<td>RETLW DATA3</td>
</tr>
<tr>
<td>my_function</td>
</tr>
<tr>
<td>;... LOTS OF CODE...</td>
</tr>
<tr>
<td>MOVWF FSR1L</td>
</tr>
<tr>
<td>MOVWF FSR1H</td>
</tr>
<tr>
<td>MOVWI 0[FSR1]</td>
</tr>
<tr>
<td>;THE PROGRAM MEMORY IS IN W</td>
</tr>
</tbody>
</table>
```

The high directive will set bit<7> if a label points to a location in program memory.
3.2 Data Memory Organization

The data memory is partitioned in 32 memory banks with 128 bytes in a bank. Each bank consists of (Figure 3-3):
- 12 core registers
- 20 Special Function Registers (SFR)
- Up to 80 bytes of General Purpose RAM (GPR)
- 16 bytes of common RAM

The active bank is selected by writing the bank number into the Bank Select Register (BSR). Unimplemented memory will read as ‘0’. All data memory can be accessed either directly (via instructions that use the file registers) or indirectly via the two File Select Registers (FSR). See Section 3.6 “Indirect Addressing” for more information.

Data memory uses a 12-bit address. The upper 5 bits of the address define the Bank address and the lower 7 bits select the registers/RAM in that bank.

3.2.1 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers occupy the first 12 addresses of every data memory bank (addresses x00h/x08h through x0Bh/x8Bh). These registers are listed below in Table 3-2. For detailed information, see Table 3-11.

<table>
<thead>
<tr>
<th>Addresses</th>
<th>BANKx</th>
</tr>
</thead>
<tbody>
<tr>
<td>x00h or x08h</td>
<td>INDF0</td>
</tr>
<tr>
<td>x01h or x09h</td>
<td>INDF1</td>
</tr>
<tr>
<td>x02h or x0Ah</td>
<td>PCL</td>
</tr>
<tr>
<td>x03h or x0Bh</td>
<td>STATUS</td>
</tr>
<tr>
<td>x04h or x0Ch</td>
<td>FSR0L</td>
</tr>
<tr>
<td>x05h or x0Dh</td>
<td>FSR0H</td>
</tr>
<tr>
<td>x06h or x0Eh</td>
<td>FSR1L</td>
</tr>
<tr>
<td>x07h or x0Fh</td>
<td>FSR1H</td>
</tr>
<tr>
<td>x08h or x10h</td>
<td>BSR</td>
</tr>
<tr>
<td>x09h or x11h</td>
<td>WREG</td>
</tr>
<tr>
<td>x0Ah or x12h</td>
<td>PCLATH</td>
</tr>
<tr>
<td>x0Bh or x13h</td>
<td>INTCON</td>
</tr>
</tbody>
</table>
3.2.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as ‘000u u uu’ (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to Section 29.0 “Instruction Set Summary”).

Note: The C and DC bits operate as Borrow and Digit Borrow out bits, respectively, in subtraction.

3.3 Register Definitions: Status

REGISTER 3-1: STATUS: STATUS REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R-1/q</th>
<th>R-1/q</th>
<th>R/W-0/u</th>
<th>R/W-0/u</th>
<th>R/W-0/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TO</td>
<td>PD</td>
<td>Z</td>
<td>DC(1)</td>
<td>C(1)</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit   W = Writable bit   U = Unimplemented bit, read as ’0’
u = Bit is unchanged    x = Bit is unknown   -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set     ‘0’ = Bit is cleared   q = Value depends on condition

bit 7-5 Unimplemented: Read as ‘0’
bit 4 TO: Time-Out bit
1 = After power-up, CLRWDT instruction or SLEEP instruction
0 = A WDT time-out occurred
bit 3 PD: Power-Down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction
bit 2 Z: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero
bit 1 DC: Digit Carry/Digit Borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result
bit 0 C: Carry/Borrow bit(1)(ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For Borrow, the polarity is reversed. A subtraction is executed by adding the two’s complement of the second operand.
3.3.1 SPECIAL FUNCTION REGISTER
The Special Function Registers (SFR) are registers used by the application to control the desired operation of peripheral functions in the device. The SFR occupies the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of each peripheral are described in the corresponding peripheral chapters of this data sheet.

3.3.2 GENERAL PURPOSE RAM
There are up to 80 bytes of General Purpose Registers (GPR) in each data memory bank. The GPR occupies the space immediately after the SFR of selected data memory banks. The number of banks selected depends on the total amount of GPR space available in the device.

3.3.2.1 Linear Access to GPR
The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See Section 3.6.2 “Linear Data Memory” for more information.

3.3.3 COMMON RAM
There are 16 bytes of common RAM accessible from all banks.
### 3.3.4 DEVICE MEMORY MAPS

The memory maps for Bank 0 through Bank 31 are shown in the tables in this section.

#### TABLE 3-3: PIC16(L)F1784 MEMORY MAP (BANKS 0-7)

<table>
<thead>
<tr>
<th>BANK 0</th>
<th>BANK 1</th>
<th>BANK 2</th>
<th>BANK 3</th>
<th>BANK 4</th>
<th>BANK 5</th>
<th>BANK 6</th>
<th>BANK 7</th>
</tr>
</thead>
<tbody>
<tr>
<td>000h</td>
<td>080h</td>
<td>100h</td>
<td>180h</td>
<td>200h</td>
<td>280h</td>
<td>300h</td>
<td>380h</td>
</tr>
<tr>
<td>008h</td>
<td>088h</td>
<td>108h</td>
<td>188h</td>
<td>208h</td>
<td>288h</td>
<td>308h</td>
<td>388h</td>
</tr>
<tr>
<td>00Ch</td>
<td>08Ch</td>
<td>10Ch</td>
<td>18Ch</td>
<td>20Ch</td>
<td>28Ch</td>
<td>30Ch</td>
<td>38Ch</td>
</tr>
<tr>
<td>00Dh</td>
<td>08Dh</td>
<td>10Dh</td>
<td>18Dh</td>
<td>20Dh</td>
<td>28Dh</td>
<td>30Dh</td>
<td>38Dh</td>
</tr>
<tr>
<td>00Eh</td>
<td>08Eh</td>
<td>10Eh</td>
<td>18Eh</td>
<td>20Eh</td>
<td>28Eh</td>
<td>30Eh</td>
<td>38Eh</td>
</tr>
<tr>
<td>00Fh</td>
<td>08Fh</td>
<td>10Fh</td>
<td>18Fh</td>
<td>20Fh</td>
<td>28Fh</td>
<td>30Fh</td>
<td>38Fh</td>
</tr>
<tr>
<td>010h</td>
<td>090h</td>
<td>110h</td>
<td>190h</td>
<td>210h</td>
<td>290h</td>
<td>310h</td>
<td>390h</td>
</tr>
<tr>
<td>011h</td>
<td>091h</td>
<td>111h</td>
<td>191h</td>
<td>211h</td>
<td>291h</td>
<td>311h</td>
<td>391h</td>
</tr>
<tr>
<td>012h</td>
<td>092h</td>
<td>112h</td>
<td>192h</td>
<td>212h</td>
<td>292h</td>
<td>312h</td>
<td>392h</td>
</tr>
<tr>
<td>013h</td>
<td>093h</td>
<td>113h</td>
<td>193h</td>
<td>213h</td>
<td>293h</td>
<td>313h</td>
<td>393h</td>
</tr>
<tr>
<td>014h</td>
<td>094h</td>
<td>114h</td>
<td>194h</td>
<td>214h</td>
<td>294h</td>
<td>314h</td>
<td>394h</td>
</tr>
<tr>
<td>015h</td>
<td>095h</td>
<td>115h</td>
<td>195h</td>
<td>215h</td>
<td>295h</td>
<td>315h</td>
<td>395h</td>
</tr>
<tr>
<td>016h</td>
<td>096h</td>
<td>116h</td>
<td>196h</td>
<td>216h</td>
<td>296h</td>
<td>316h</td>
<td>396h</td>
</tr>
<tr>
<td>017h</td>
<td>097h</td>
<td>117h</td>
<td>197h</td>
<td>217h</td>
<td>297h</td>
<td>317h</td>
<td>397h</td>
</tr>
<tr>
<td>018h</td>
<td>098h</td>
<td>118h</td>
<td>198h</td>
<td>218h</td>
<td>298h</td>
<td>318h</td>
<td>398h</td>
</tr>
<tr>
<td>019h</td>
<td>099h</td>
<td>119h</td>
<td>199h</td>
<td>219h</td>
<td>299h</td>
<td>319h</td>
<td>399h</td>
</tr>
<tr>
<td>01Ah</td>
<td>09Ah</td>
<td>11Ah</td>
<td>19Ah</td>
<td>21Ah</td>
<td>29Ah</td>
<td>31Ah</td>
<td>39Ah</td>
</tr>
<tr>
<td>01Bh</td>
<td>09Bh</td>
<td>11Bh</td>
<td>19Bh</td>
<td>21Bh</td>
<td>29Bh</td>
<td>31Bh</td>
<td>39Bh</td>
</tr>
<tr>
<td>01Ch</td>
<td>09Ch</td>
<td>11Ch</td>
<td>19Ch</td>
<td>21Ch</td>
<td>29Ch</td>
<td>31Ch</td>
<td>39Ch</td>
</tr>
<tr>
<td>01Dh</td>
<td>09Dh</td>
<td>11Dh</td>
<td>19Dh</td>
<td>21Dh</td>
<td>29Dh</td>
<td>31Dh</td>
<td>39Dh</td>
</tr>
<tr>
<td>01Eh</td>
<td>09Eh</td>
<td>11Eh</td>
<td>19Eh</td>
<td>21Eh</td>
<td>29Eh</td>
<td>31Eh</td>
<td>39Eh</td>
</tr>
<tr>
<td>01Fh</td>
<td>09Fh</td>
<td>11Fh</td>
<td>19Fh</td>
<td>21Fh</td>
<td>29Fh</td>
<td>31Fh</td>
<td>39Fh</td>
</tr>
<tr>
<td>020h</td>
<td>0A0h</td>
<td>1A0h</td>
<td>1A0h</td>
<td>2A0h</td>
<td>2A0h</td>
<td>2A0h</td>
<td>2A0h</td>
</tr>
</tbody>
</table>

Legend: ≠ Unimplemented data memory locations, read as ‘0’.

Note 1: PIC16F1784 only.
<table>
<thead>
<tr>
<th>BANK 0</th>
<th>BANK 1</th>
<th>BANK 2</th>
<th>BANK 3</th>
<th>BANK 4</th>
<th>BANK 5</th>
<th>BANK 6</th>
<th>BANK 7</th>
</tr>
</thead>
<tbody>
<tr>
<td>000h</td>
<td></td>
<td></td>
<td>080h</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>00Bh</td>
<td>08Bh</td>
<td>08Bh</td>
<td>08Bh</td>
<td>08Bh</td>
<td>08Bh</td>
<td>08Bh</td>
<td>08Bh</td>
</tr>
<tr>
<td>00Ch</td>
<td>PORTA</td>
<td>TRISA</td>
<td>LATA</td>
<td>ANSELA</td>
<td>WPUA</td>
<td>ODCONA</td>
<td>SLRCONA</td>
</tr>
<tr>
<td>00Dh</td>
<td>PORTB</td>
<td>TRISB</td>
<td>LATB</td>
<td>ANSELB</td>
<td>WPUB</td>
<td>ODCONS</td>
<td>SLRCONB</td>
</tr>
<tr>
<td>00Eh</td>
<td>PORTC</td>
<td>TRISC</td>
<td>LATC</td>
<td>ANSELB</td>
<td>WPUA</td>
<td>ODCONB</td>
<td>SLRCONC</td>
</tr>
<tr>
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<td>PORTD</td>
<td>TRISD</td>
<td>LATD</td>
<td>ANSELB</td>
<td>WPUA</td>
<td>ODCONC</td>
<td>SLRCONC</td>
</tr>
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<td>TRISE</td>
<td>LATE</td>
<td>EEDRL</td>
<td>WPEU</td>
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<tr>
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<td>PIR1</td>
<td>PIE1</td>
<td>CM1CON0</td>
<td>EEDRL</td>
<td>SSP1BUF</td>
<td>31rh</td>
<td>31rh</td>
</tr>
<tr>
<td>012h</td>
<td>PIR2</td>
<td>PIE2</td>
<td>CM1CON1</td>
<td>EEDRH</td>
<td>SSP1ADD</td>
<td>32rh</td>
<td>32rh</td>
</tr>
<tr>
<td>013h</td>
<td>093h</td>
<td>093h</td>
<td>CM2CON0</td>
<td>EEDATL</td>
<td>SSP1SK</td>
<td>33rh</td>
<td>33rh</td>
</tr>
<tr>
<td>014h</td>
<td>PIR4</td>
<td>PIE4</td>
<td>CM2CON1</td>
<td>EEDATH</td>
<td>SSP1STAT</td>
<td>34rh</td>
<td>34rh</td>
</tr>
<tr>
<td>015h</td>
<td>TMR0</td>
<td>OPTION_REG</td>
<td>CMOUT</td>
<td>EECON1</td>
<td>SSPICON1</td>
<td>35rh</td>
<td>35rh</td>
</tr>
<tr>
<td>016h</td>
<td>TMR1</td>
<td>PCON</td>
<td>CMOUT</td>
<td>EECON2</td>
<td>SSPICON2</td>
<td>36rh</td>
<td>36rh</td>
</tr>
<tr>
<td>017h</td>
<td>TMR1H</td>
<td>WDTCN</td>
<td>CMOUT</td>
<td>EECON3</td>
<td>SSPICON3</td>
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<td>37rh</td>
</tr>
<tr>
<td>018h</td>
<td>T1CON</td>
<td>OSCRTUNE</td>
<td>CMOUT</td>
<td>EECON4</td>
<td>SSPICON4</td>
<td>38rh</td>
<td>38rh</td>
</tr>
<tr>
<td>019h</td>
<td>T1GCON</td>
<td>OSCR</td>
<td>CMOUT</td>
<td>EECON5</td>
<td>SSPICON5</td>
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<td>39rh</td>
</tr>
<tr>
<td>01Ah</td>
<td>T2CON</td>
<td>ADRESL</td>
<td>CMOUT</td>
<td>EECON6</td>
<td>SSPICON6</td>
<td>3A9h</td>
<td>3A9h</td>
</tr>
<tr>
<td>01Bh</td>
<td>T2CON</td>
<td>ADCNO</td>
<td>CMOUT</td>
<td>EECON7</td>
<td>SSPICON7</td>
<td>3Afh</td>
<td>3Afh</td>
</tr>
<tr>
<td>01Fh</td>
<td>0Fh</td>
<td>ADCCON2</td>
<td>CMOUT</td>
<td>EECON8</td>
<td>SSPICON8</td>
<td>3Bfh</td>
<td>3Bfh</td>
</tr>
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<td>020h</td>
<td>A0h</td>
<td></td>
<td>CMOUT</td>
<td>EECON9</td>
<td>SSPICON9</td>
<td>3Chf</td>
<td>3Chf</td>
</tr>
<tr>
<td>06Fh</td>
<td>0Fh</td>
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<td>CMOUT</td>
<td>EECON10</td>
<td>SSPICON10</td>
<td>3Dfh</td>
<td>3Dfh</td>
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<tr>
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<td></td>
<td>CMOUT</td>
<td>EECON11</td>
<td>SSPICON11</td>
<td>3Efh</td>
<td>3Efh</td>
</tr>
</tbody>
</table>

Legend: 
- Unimplemented data memory locations, read as ‘0’. 

Note 1: PIC16F1786 only.
### TABLE 3-5: PIC16(L)F1787 MEMORY MAP (BANKS 0-7)

<table>
<thead>
<tr>
<th>BANK 0</th>
<th>BANK 1</th>
<th>BANK 2</th>
<th>BANK 3</th>
<th>BANK 4</th>
<th>BANK 5</th>
<th>BANK 6</th>
<th>BANK 7</th>
</tr>
</thead>
<tbody>
<tr>
<td>000h</td>
<td>008h</td>
<td>010h</td>
<td>008h</td>
<td>010h</td>
<td>018h</td>
<td>020h</td>
<td>028h</td>
</tr>
<tr>
<td>002h</td>
<td>008h</td>
<td>010h</td>
<td>008h</td>
<td>010h</td>
<td>018h</td>
<td>020h</td>
<td>028h</td>
</tr>
<tr>
<td>004h</td>
<td>008h</td>
<td>010h</td>
<td>008h</td>
<td>010h</td>
<td>018h</td>
<td>020h</td>
<td>028h</td>
</tr>
<tr>
<td>006h</td>
<td>008h</td>
<td>010h</td>
<td>008h</td>
<td>010h</td>
<td>018h</td>
<td>020h</td>
<td>028h</td>
</tr>
</tbody>
</table>

**Legend:**
- = Unimplemented data memory locations, read as ‘0’.

**Note 1:** PIC16F1787 only.
## TABLE 3-6: PIC16(L)F1784 MEMORY MAP (BANKS 8-31)

<table>
<thead>
<tr>
<th>BANK 8</th>
<th>BANK 9</th>
<th>BANK 10</th>
<th>BANK 11</th>
<th>BANK 12</th>
<th>BANK 13</th>
<th>BANK 14</th>
<th>BANK 15</th>
</tr>
</thead>
<tbody>
<tr>
<td>800h</td>
<td>880h</td>
<td>900h</td>
<td>980h</td>
<td>A00h</td>
<td>A80h</td>
<td>700h</td>
<td>780h</td>
</tr>
<tr>
<td>870h</td>
<td>866Fh</td>
<td>970h</td>
<td>9F0h</td>
<td>70h – 7Fh</td>
<td>70h – 7Fh</td>
<td>70h – 7Fh</td>
<td>70h – 7Fh</td>
</tr>
<tr>
<td>80Bh</td>
<td>88Bh</td>
<td>90Bh</td>
<td>98Bh</td>
<td>A0Bh</td>
<td>A8Bh</td>
<td>70Bh</td>
<td>78Bh</td>
</tr>
</tbody>
</table>

Legend:
- **Unimplemented** data memory locations, read as '0'
- **OPA1CON**
- **OPA2CON**
- **CLRRCON**
- **Core Registers** (Table 3-2)
- **Common RAM** (Accesses 70h – 7Fh)
<table>
<thead>
<tr>
<th>BANK 8</th>
<th>BANK 9</th>
<th>BANK 10</th>
<th>BANK 11</th>
<th>BANK 12</th>
<th>BANK 13</th>
<th>BANK 14</th>
<th>BANK 15</th>
</tr>
</thead>
<tbody>
<tr>
<td>400h</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
</tr>
<tr>
<td>40Bh</td>
<td>480h</td>
<td>500h</td>
<td>580h</td>
<td>600h</td>
<td>680h</td>
<td>700h</td>
<td>70h</td>
</tr>
<tr>
<td>40Ch</td>
<td>48Ch</td>
<td>50Ch</td>
<td>58Ch</td>
<td>60Ch</td>
<td>68Ch</td>
<td>70Ch</td>
<td>70h</td>
</tr>
<tr>
<td>41Fh</td>
<td>Unimplemented Read as ‘0’</td>
<td>420h</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
</tr>
<tr>
<td>480h</td>
<td>Unimplemented Read as ‘0’</td>
<td>480h</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
</tr>
<tr>
<td>48Bh</td>
<td>Unimplemented Read as ‘0’</td>
<td>48Bh</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
</tr>
<tr>
<td>48Ch</td>
<td>Unimplemented Read as ‘0’</td>
<td>48Ch</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
<td>Core Registers (Table 3-2)</td>
</tr>
<tr>
<td>49Fh</td>
<td>General Purpose Register 80 Bytes</td>
<td>50Fh</td>
<td>General Purpose Register 80 Bytes</td>
<td>General Purpose Register 80 Bytes</td>
<td>General Purpose Register 80 Bytes</td>
<td>General Purpose Register 80 Bytes</td>
<td>General Purpose Register 80 Bytes</td>
</tr>
<tr>
<td>4AFh</td>
<td>General Purpose Register 80 Bytes</td>
<td>5AFh</td>
<td>General Purpose Register 80 Bytes</td>
<td>General Purpose Register 80 Bytes</td>
<td>General Purpose Register 80 Bytes</td>
<td>General Purpose Register 80 Bytes</td>
<td>General Purpose Register 80 Bytes</td>
</tr>
<tr>
<td>4EFh</td>
<td>56Fh</td>
<td>57Fh</td>
<td>57Fh</td>
<td>57Fh</td>
<td>57Fh</td>
<td>57Fh</td>
<td>57Fh</td>
</tr>
<tr>
<td>4FFh</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
<td>4FFh</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
</tr>
<tr>
<td>470h</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
<td>470h</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
</tr>
<tr>
<td>47Fh</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
<td>47Fh</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
</tr>
</tbody>
</table>

**TABLE 3-8**

- **Purpose:** See Table 3-8
- **Register:** 64F
- **Register:** 650
- **Register:** 80 Bytes
- **Purpose:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented

**TABLE 3-9**

- **Purpose:** See Table 3-9
- **Register:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented

**TABLE 3-10**

- **Purpose:** See Table 3-10
- **Register:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented
- **Register:** Unimplemented

---

Unimplemented data memory locations, read as ‘0’
### TABLE 3-8: PIC16(L)F1786/7 MEMORY MAP (BANK 10 DETAILS)

<table>
<thead>
<tr>
<th>Address</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>500h</td>
<td>Core Registers (Table 3-2)</td>
</tr>
<tr>
<td>50Bh</td>
<td>Unimplemented Read as '0'</td>
</tr>
<tr>
<td>50Ch</td>
<td>OPA1CON</td>
</tr>
<tr>
<td>510h</td>
<td>—</td>
</tr>
<tr>
<td>511h</td>
<td>OPA2CON</td>
</tr>
<tr>
<td>512h</td>
<td>Unimplemented Read as '0'</td>
</tr>
<tr>
<td>513h</td>
<td>CLKRCON</td>
</tr>
<tr>
<td>514h</td>
<td>Unimplemented Read as '0'</td>
</tr>
<tr>
<td>519h</td>
<td>General Purpose Register</td>
</tr>
<tr>
<td>51Ah</td>
<td>80 Bytes</td>
</tr>
<tr>
<td>51Fh</td>
<td>Common RAM (Accesses 70h – 7Fh)</td>
</tr>
<tr>
<td>520h</td>
<td></td>
</tr>
<tr>
<td>56Fh</td>
<td></td>
</tr>
<tr>
<td>570h</td>
<td></td>
</tr>
<tr>
<td>57Fh</td>
<td></td>
</tr>
</tbody>
</table>

Legend: ■ = Unimplemented data memory locations, read as '0'.

### TABLE 3-9: PIC16(L)F1784/6/7 MEMORY MAP (BANK 31 DETAILS)

<table>
<thead>
<tr>
<th>Address</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F8Ch</td>
<td>Unimplemented Read as '0'</td>
</tr>
<tr>
<td>FE3h</td>
<td>STATUS_SHAD</td>
</tr>
<tr>
<td>FE4h</td>
<td>WREG_SHAD</td>
</tr>
<tr>
<td>FE5h</td>
<td>BSR_SHAD</td>
</tr>
<tr>
<td>FE6h</td>
<td>PCLATH_SHAD</td>
</tr>
<tr>
<td>FE7h</td>
<td>FSR0L_SHAD</td>
</tr>
<tr>
<td>FE8h</td>
<td>FSR0H_SHAD</td>
</tr>
<tr>
<td>FE9h</td>
<td>FSR1L_SHAD</td>
</tr>
<tr>
<td>FEAh</td>
<td>FSR1H_SHAD</td>
</tr>
<tr>
<td>FEBh</td>
<td>TOSL</td>
</tr>
<tr>
<td>FEDh</td>
<td>STKPTR</td>
</tr>
<tr>
<td>FEEh</td>
<td>TOSL</td>
</tr>
<tr>
<td>FEFh</td>
<td>TOSL</td>
</tr>
</tbody>
</table>

Legend: ■ = Unimplemented data memory locations, read as '0'.

---

This page contains detailed memory maps for the PIC16(L)F1784/6/7 microcontrollers, specifying the addresses and contents of various memory banks. The maps include details on core registers, unimplemented data memory locations, and general purpose registers. The legend at the bottom of the page explains the meaning of the symbols used in the tables.
**TABLE 3-10: PIC16(L)F1784/6/7 MEMORY MAP (BANK 16 DETAILS)**

<table>
<thead>
<tr>
<th>BANK 16</th>
<th>BANK 16</th>
<th>BANK 16</th>
</tr>
</thead>
<tbody>
<tr>
<td>811h</td>
<td>PSMC1CON</td>
<td>831h</td>
</tr>
<tr>
<td>812h</td>
<td>PSMC1MDL</td>
<td>832h</td>
</tr>
<tr>
<td>813h</td>
<td>PSMC1SYNC</td>
<td>833h</td>
</tr>
<tr>
<td>814h</td>
<td>PSMC1CLK</td>
<td>834h</td>
</tr>
<tr>
<td>815h</td>
<td>PSMC1OEN</td>
<td>835h</td>
</tr>
<tr>
<td>816h</td>
<td>PSMC1POL</td>
<td>836h</td>
</tr>
<tr>
<td>817h</td>
<td>PSMC1BLNK</td>
<td>837h</td>
</tr>
<tr>
<td>818h</td>
<td>PSMC1REBS</td>
<td>838h</td>
</tr>
<tr>
<td>819h</td>
<td>PSMC1FEBS</td>
<td>839h</td>
</tr>
<tr>
<td>81Ah</td>
<td>PSMC1PHS</td>
<td>83Ah</td>
</tr>
<tr>
<td>81Bh</td>
<td>PSMC1SYNC</td>
<td>83Bh</td>
</tr>
<tr>
<td>81Ch</td>
<td>PSMC1SYNC</td>
<td>83Ch</td>
</tr>
<tr>
<td>81Dh</td>
<td>PSMC1ASDC</td>
<td>83Dh</td>
</tr>
<tr>
<td>81Eh</td>
<td>PSMC1ASDD</td>
<td>83Eh</td>
</tr>
<tr>
<td>81Fh</td>
<td>PSMC1ASDS</td>
<td>83Fh</td>
</tr>
<tr>
<td>820h</td>
<td>PSMC1INT</td>
<td>840h</td>
</tr>
<tr>
<td>821h</td>
<td>PSMC1PHL</td>
<td>841h</td>
</tr>
<tr>
<td>822h</td>
<td>PSMC1PHH</td>
<td>842h</td>
</tr>
<tr>
<td>823h</td>
<td>PSMC1DCL</td>
<td>843h</td>
</tr>
<tr>
<td>824h</td>
<td>PSMC1DCH</td>
<td>844h</td>
</tr>
<tr>
<td>825h</td>
<td>PSMC1PRL</td>
<td>845h</td>
</tr>
<tr>
<td>826h</td>
<td>PSMC1PRH</td>
<td>846h</td>
</tr>
<tr>
<td>827h</td>
<td>PSMC1TMRL</td>
<td>847h</td>
</tr>
<tr>
<td>828h</td>
<td>PSMC1TMRH</td>
<td>848h</td>
</tr>
<tr>
<td>829h</td>
<td>PSMC1DBR</td>
<td>849h</td>
</tr>
<tr>
<td>82Ah</td>
<td>PSMC1DBF</td>
<td>84Ah</td>
</tr>
<tr>
<td>82Bh</td>
<td>PSMC1BLKR</td>
<td>84Bh</td>
</tr>
<tr>
<td>82Ch</td>
<td>PSMC1BLKF</td>
<td>84Ch</td>
</tr>
<tr>
<td>82Dh</td>
<td>PSMC1FFA</td>
<td>84Dh</td>
</tr>
<tr>
<td>82Eh</td>
<td>PSMC1STR0</td>
<td>84Eh</td>
</tr>
<tr>
<td>82Fh</td>
<td>PSMC1STR1</td>
<td>84Fh</td>
</tr>
<tr>
<td>830h</td>
<td>—</td>
<td>850h</td>
</tr>
</tbody>
</table>

Legend: ➥ = Unimplemented data memory locations, read as '0'.

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### 3.3.5 CORE FUNCTION REGISTERS

**SUMMARY**

The Core Function registers listed in Table 3-11 can be addressed from any Bank.

<table>
<thead>
<tr>
<th>Addr</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>x00h</td>
<td>INDF0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxx xxxx</td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>x01h</td>
<td>INDF1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxx xxxx</td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>x02h</td>
<td>PCL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>x03h</td>
<td>STATUS</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>T5</td>
<td>T5</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
<td>——1 1000</td>
<td>——q quuu</td>
</tr>
<tr>
<td>x04h</td>
<td>FSR0L</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>x05h</td>
<td>FSR0H</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>x06h</td>
<td>FSR1L</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>x07h</td>
<td>FSR1H</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>x08h</td>
<td>BSR</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>BSR4</td>
<td>BSR3</td>
<td>BSR2</td>
<td>BSR1</td>
<td>BSR0</td>
<td>——0 0000</td>
<td>——0 0000</td>
</tr>
<tr>
<td>x09h</td>
<td>WREG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>xA0h</td>
<td>PCLATH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Write Buffer for the upper 7 bits of the Program Counter</td>
<td>0000 0000</td>
<td>0000 0000</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>xB0h</td>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INT</td>
<td>IOIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
</tbody>
</table>

**Legend:**
- \( x \) = unknown,
- \( u \) = unchanged,
- \( q \) = value depends on condition,
- \( - \) = unimplemented, read as '0',
- \( r \) = reserved.

Shaded locations are unimplemented, read as ‘0’.
### TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY

<table>
<thead>
<tr>
<th>Addr</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>00Ch</td>
<td>PORTA</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>00Dh</td>
<td>PORTB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>00Eh</td>
<td>PORTC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>00Fh</td>
<td>PORTD(3)</td>
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<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>010h</td>
<td>PORTE</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>011h</td>
<td>PIR1</td>
<td>TMR1GIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1IF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>0000 0000 0000 0000</td>
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</tr>
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<td>PIR2</td>
<td>OSIF</td>
<td>C2IF</td>
<td>C1IF</td>
<td>EEIF</td>
<td>BCL1IF</td>
<td>C4IF</td>
<td>C3IF</td>
<td>CCP2IF</td>
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<td>13h</td>
<td>PIR3</td>
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<td>014h</td>
<td>PIR4</td>
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</tr>
<tr>
<td>015h</td>
<td>TMR0</td>
<td>Timer0 Module Register</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxxx xxxxx uuuu uuuu</td>
<td></td>
</tr>
<tr>
<td>016h</td>
<td>TMR1L</td>
<td>Holding Register for the Least Significant Byte of the 16-bit TMR1 Register</td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td>xxxxx xxxxx uuuu uuuu</td>
<td></td>
</tr>
<tr>
<td>017h</td>
<td>TMR1H</td>
<td>Holding Register for the Most Significant Byte of the 16-bit TMR1 Register</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxxx xxxxx uuuu uuuu</td>
<td></td>
</tr>
<tr>
<td>018h</td>
<td>T1CON</td>
<td>TMR1CS1</td>
<td>TMR1CS0</td>
<td>T1CKPS1</td>
<td>T1CKPS0</td>
<td>T1OSCEN</td>
<td>T1SYNC</td>
<td>—</td>
<td>TMR1ON</td>
<td>0000 00-0 0000 uuuu uuuu</td>
<td></td>
</tr>
<tr>
<td>019h</td>
<td>T1GCON</td>
<td>TMR1GE</td>
<td>T1GPOL</td>
<td>T1GMT</td>
<td>T1GSPM</td>
<td>T1GGO/ DNE</td>
<td>T1GVAL</td>
<td>T1GSS&lt;1:0&gt;</td>
<td></td>
<td>0000 0x00 uuuu uuuu</td>
<td></td>
</tr>
<tr>
<td>016h</td>
<td>TMR2</td>
<td>Holding Register for the Least Significant Byte of the 16-bit TMR2 Register</td>
<td>xxxxx xxxxx uuuu uuuu</td>
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<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>017h</td>
<td>PR2</td>
<td>Holding Register for the Most Significant Byte of the 16-bit TMR2 Register</td>
<td>xxxxx xxxxx uuuu uuuu</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>018h</td>
<td>T2CON</td>
<td>—</td>
<td>T2OUTPS&lt;3:0&gt;</td>
<td>TMR2ON</td>
<td>T2CKPS&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>^1000 0000</td>
<td>^0000 0000</td>
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<td>—</td>
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</table>

**Legend:**
- x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', * = reserved.

**Note 1:** These registers can be addressed from any bank.

**Note 2:** Unimplemented, read as '1'.

**Note 3:** PIC16(L)F1784/7 only.

**Note 4:** PIC16F1784/6/7 only.
### TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

<table>
<thead>
<tr>
<th>Bank 2</th>
<th>Addr</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets</th>
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<tbody>
<tr>
<td>10Ch</td>
<td>LATA</td>
<td>PORTA Data Latch</td>
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<td>PORTB Data Latch</td>
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<td></td>
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<td>LATC</td>
<td>PORTC Data Latch</td>
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<td>LATD</td>
<td>PORTD Data Latch</td>
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<tr>
<td>111h</td>
<td>CM1CON0</td>
<td>C1ON</td>
<td>C1OUT</td>
<td>C1OE</td>
<td>C1POL</td>
<td>C1ZLF</td>
<td>C1SP</td>
<td>C1SYS</td>
<td>C1SYNC</td>
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<tr>
<td>112h</td>
<td>CM1CON1</td>
<td>C1INTP</td>
<td>C1INTN</td>
<td>C1PCH&lt;2:0&gt;</td>
<td>C1NCH&lt;2:0&gt;</td>
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<td>CM2CON0</td>
<td>C2ON</td>
<td>C2OUT</td>
<td>C2OE</td>
<td>C2POL</td>
<td>C2ZLF</td>
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<td>C2SYS</td>
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<td>C2INTN</td>
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<td>C2NCH&lt;2:0&gt;</td>
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<td>MC4OUT&lt;3&gt;</td>
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<td>117h</td>
<td>FVRCON</td>
<td>FVREN</td>
<td>FVRDY</td>
<td>TSEN</td>
<td>TSRNG</td>
<td>CDAVF&lt;1:0&gt;</td>
<td>ADFVR&lt;1:0&gt;</td>
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<td>118h</td>
<td>DAC1CON0</td>
<td>DAC1EN</td>
<td>—</td>
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<td>—</td>
<td>—</td>
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<td>—</td>
<td>—</td>
<td>DAC1POSS&lt;1:0&gt;</td>
<td>—</td>
</tr>
</tbody>
</table>

### Bank 3

| 18Ch | ANSELA | ANSA7 | ANSA5 | ANSA4 | ANSA3 | ANSA2 | ANSA1 | ANSA0 |      |      |                  |                          |
| 18Dh | ANSELB | — | ANSB6 | ANSB5 | ANSB4 | ANSB3 | ANSB2 | ANSB1 | ANSB0 |      |                  |                          |
| 18 Eh | Unimplemented | — | — | — | — | — | — | — |      |      |                  |                          |
| 18Fh | ANSELD<3> | — | — | — | — | — | — | — |      | — |                  |                          |
| 190h | ANSELE<3> | — | — | — | — | — | ANSE2 | ANSE1 | ANSE0 |      |                  |                          |
| 191h | EEADRL | EEPROM / Program Memory Address Register Low Byte |      |      |      |      |      |      |      |      |      |                  | 0000 0000 0000 0000     |
| 192h | EEADRH | —<2> | EEPROM / Program Memory Address Register High Byte |      |      |      |      |      |      |      |      |      |                  | 1000 0000 1000 0000     |
| 193h | EEADTL | EEPROM / Program Memory Read Data Register Low Byte |      |      |      |      |      |      |      |      |      |                  | 0000 0000 0000 0000     |
| 194h | EEADTH | — | EEPROM / Program Memory Read Data Register High Byte |      |      |      |      |      |      |      |      |      |                  | 0000 0000 0000 0000     |
| 195h | EECON1 | EEPOGD | CFGS | LWLO | FREE | WRERR | WREN | WR | RD |      |                  | 0000 x000 0000 q000     |
| 196h | EECON2 | EEPROM / Program Memory Control Register 2 |      |      |      |      |      |      |      |      |      |                  | 0000 0000 0000 0000     |
| 197h | VREGCON<4> | — | — | — | — | — | — | — |      | VREGPM | Reserved |                  | 00 00 00 00 00 00 00 00 |
| 198h | — | Unimplemented | — | — | — | — | — | — | — |      |                  |                          |
| 199h | RCREG | EUSART Receive Data Register |      |      |      |      |      |      |      |      |      |                  | 0000 0000 0000 0000     |
| 19 Ah | TXREG | EUSART Transmit Data Register |      |      |      |      |      |      |      |      |      |                  | 0000 0000 0000 0000     |
| 19 Bh | SPBRG | BRG<7:0> |      |      |      |      |      |      |      |      |      |                  | 0000 0000 0000 0000     |
| 19Ch | SPBRGH | BRG<15:8> |      |      |      |      |      |      |      |      |      |                  | 0000 0000 0000 0000     |
| 19 Dh | RCSTA | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D |      |                  | 0000 0000 0000 0000     |
| 19 Eh | TXSTA | CSR | TX9 | TXEN | SYNC | SENDS | BRGH | TRMT | TX9D |      |                  | 0000 0010 0000 0010     |
| 19Fh | BAUDCON | ABDIOF | RCIDL | — | SCKP | BRG16 | — | WUE | ABDEN |      |                  | 01 0 0 0 0 0 0 0 0     |

**Legend:**
- `x` = unknown, `u` = unchanged, `q` = value depends on condition, `-` = unimplemented, read as ‘0’, `r` = reserved.
- Shaded locations are unimplemented, read as ‘0’.

**Note:**
1. These registers can be addressed from any bank.
2. Unimplemented, read as ‘1’.
3. PIC16(L)F1784/7 only.
4. PIC16F1784/6/7 only.
### TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

<table>
<thead>
<tr>
<th>Addr</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bank 4</td>
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<td>20Ch</td>
<td>WPUA</td>
<td>WPUA7</td>
<td>WPUA6</td>
<td>WPUA5</td>
<td>WPUA4</td>
<td>WPUA3</td>
<td>WPUA2</td>
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<td>WPUA0</td>
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<td>WPUB</td>
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<td>WPUE2(R)</td>
<td>WPUE1(R)</td>
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<td>SSP1ADD</td>
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<td>213h</td>
<td>SSP1MSK</td>
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<td>214h</td>
<td>SSP1STAT</td>
<td>SMP</td>
<td>CKE</td>
<td>D/A</td>
<td>P</td>
<td>S</td>
<td>R/W</td>
<td>UA</td>
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<td>SSPOV</td>
<td>SSPE1</td>
<td>CKP</td>
<td>SSPM&lt;3:0&gt;</td>
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<td>ACKSTAT</td>
<td>ACKDT</td>
<td>ACKEN</td>
<td>RCEN</td>
<td>PEN</td>
<td>RSEN</td>
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<td>DHEN</td>
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<td>28Ch</td>
<td>ODCONA</td>
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<tr>
<td>28Eh</td>
<td>ODCONC</td>
<td>Open Drain Control for PORTC</td>
<td>0000 0000 0000 0000</td>
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<td>28Fh</td>
<td>ODCOND(R)</td>
<td>Open Drain Control for PORTD</td>
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<td>ODE0</td>
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<td>Capture/Compare/PWM Register 2 (LSB)</td>
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<td>Capture/Compare/PWM Register 2 (MSB)</td>
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<td>DC2B&lt;1:0&gt;</td>
<td>CCP2M&lt;3:0&gt;</td>
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<tr>
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<td>SLRCONA</td>
<td>Slew Rate Control for PORTA</td>
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<td></td>
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<tr>
<td>30Dh</td>
<td>SLRCONB</td>
<td>Slew Rate Control for PORTB</td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>30Eh</td>
<td>SLRCONC</td>
<td>Slew Rate Control for PORTC</td>
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<td></td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>30Fh</td>
<td>SLRCOND(R)</td>
<td>Slew Rate Control for PORTD</td>
<td>0000 0000 0000 0000</td>
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<td></td>
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<tr>
<td>310h</td>
<td>SLRCONE(R)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SLRE2</td>
<td>SLRE1</td>
<td>SLRE0</td>
<td>1111 1111 1111 1111</td>
</tr>
<tr>
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**Legend:**
- x = unknown
- u = unchanged
- q = value depends on condition
- - = unimplemented, read as '0'
- r = reserved

**Note:**
1. These registers can be addressed from any bank.
2. Unimplemented, read as '1'.
3. PIC16(L)F1784/7 only.
4. PIC16F1784/6/7 only.
<table>
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<th>Addr</th>
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<th>Bit 3</th>
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</table>

**Legend:**
- `x` = unknown,
- `u` = unchanged,
- `q` = value depends on condition,
- `-` = unimplemented, read as '0',
- `r` = reserved.
- Shaded locations are unimplemented, read as '0'.

**Note**
1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1784/7 only.
4: PIC16F1784/6/7 only.
### TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

<table>
<thead>
<tr>
<th>Addr</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
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<th>Value on all other Resets</th>
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<td>x0Ch or x8Ch to x6Fh or xEFh</td>
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</tbody>
</table>

**Legend:**
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**Shaded locations are unimplemented, read as '0'**.

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<tr>
<th>Addr</th>
<th>Name</th>
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<th>Bit 6</th>
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<th>Bit 4</th>
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**Legend:**  
- x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.

Shaded locations are unimplemented, read as '0'.

**Note:**
1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1784/7 only.
4: PIC16F1784/67 only.
TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

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<thead>
<tr>
<th>Addr</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
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<th>Value on all other Resets</th>
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Legend:  
- = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.

Note  
1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1784/7 only.
4: PIC16F1784/6/7 only.

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TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

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**Legend:**
- *x* = unknown, *u* = unchanged, *v* = value depends on condition, *–* = unimplemented, read as ‘0’, *r* = reserved.
- Shaded locations are unimplemented, read as ‘0’.

**Note:**
1. These registers can be addressed from any bank.
2. Unimplemented, read as ‘1’.
3. PIC16(L)F1784/7 only.
4. PIC16F1784/6/7 only.
### TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

<table>
<thead>
<tr>
<th>Addr</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets</th>
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**Legend:**
- \(x\) = unknown, \(u\) = unchanged, \(q\) = value depends on condition, - = unimplemented, read as '0', \(r\) = reserved.
- Shaded locations are unimplemented, read as '0'.

**Note**
1. These registers can be addressed from any bank.
2. Unimplemented, read as '1'.
3. PIC16(L)F1784/7 only.
4. PIC16F1784/6/7 only.
3.4 PCL and PCLATH

The Program Counter (PC) is 15 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<14:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 3-4 shows the five situations for the loading of the PC.

**FIGURE 3-4: LOADING OF PC IN DIFFERENT SITUATIONS**

<table>
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<tr>
<th>PC</th>
<th>PCH</th>
<th>PCL</th>
<th>0</th>
<th>Instruction with PCL as Destination</th>
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<tbody>
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<td>PCLATH</td>
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<table>
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<th>PCL</th>
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<th>GOTO, CALL</th>
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<th>PCL</th>
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<th>CALLW</th>
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<tr>
<td>W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PC</th>
<th>PCH</th>
<th>PCL</th>
<th>0</th>
<th>BRW</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC + W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PC</th>
<th>PCH</th>
<th>PCL</th>
<th>0</th>
<th>BRA</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC + OPCODE &lt;8:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3.4.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<14:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper 7 bits to the PCLATH register. When the lower 8 bits are written to the PCL register, all 15 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

3.4.2 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to Application Note AN556, "Implementing a Table Read" (DS00556).

3.4.3 COMPUTED FUNCTION CALLS

A computed function CALL allows programs to maintain tables of functions and provide another way to execute state machines or look-up tables. When performing a table read using a computed function CALL, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block).

If using the CALL instruction, the PCH<2:0> and PCL registers are loaded with the operand of the CALL instruction. PCH<6:3> is loaded with PCLATH<6:3>.

The CALLW instruction enables computed calls by combining PCLATH and W to form the destination address. A computed CALLW is accomplished by loading the W register with the desired address and executing CALLW. The PCL register is loaded with the value of W and PCH is loaded with PCLATH.

3.4.4 BRANCING

The branching instructions add an offset to the PC. This allows relocatable code and code that crosses page boundaries. There are two forms of branching, BRW and BRA. The PC will have incremented to fetch the next instruction in both cases. When using either branching instruction, a PCL memory boundary may be crossed.

If using BRW, load the W register with the desired unsigned address and execute BRW. The entire PC will be loaded with the address PC + 1 + W.

If using BRA, the entire PC will be loaded with PC + 1 +, the signed value of the operand of the BRA instruction.
3.5 Stack

All devices have a 16-level x 15-bit wide hardware stack (refer to Figures 3-1 and 3-2). The stack space is not part of either program or data space. The PC is PUSHed onto the stack when CALL or CALLW instructions are executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer if the STVREN bit is programmed to '0' (Configuration Words). This means that after the stack has been PUSHed sixteen times, the seventeenth PUSH overwrites the value that was stored from the first PUSH. The eighteenth PUSH overwrites the second PUSH (and so on). The STKOVF and STKUNF flag bits will be set on an Overflow/Underflow, regardless of whether the Reset is enabled.

Note: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, CALLW, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

3.5.1 ACCESSING THE STACK

The stack is available through the TOSH, TOSL and STKPTR registers. STKPTR is the current value of the Stack Pointer. TOSH:TOSL register pair points to the TOP of the stack. Both registers are read/writeable. TOS is split into TOSH and TOSL due to the 15-bit size of the PC. To access the stack, adjust the value of STKPTR, which will position TOSH:TOSL, then read/write to TOSH:TOSL. STKPTR is 5 bits to allow detection of overflow and underflow.

Note: Care should be taken when modifying the STKPTR while interrupts are enabled.

During normal program operation, CALL, CALLW and interrupts will increment STKPTR while RETLW, RETURN, and RETFIE will decrement STKPTR. At any time, STKPTR can be inspected to see how much stack is left. The STKPTR always points at the currently used place on the stack. Therefore, a CALL or CALLW will increment the STKPTR and then write the PC, and a return will unload the PC and then decrement the STKPTR.

Reference Figure 3-5 through Figure 3-8 for examples of accessing the stack.

FIGURE 3-5: ACCESSING THE STACK EXAMPLE 1

<table>
<thead>
<tr>
<th>TOSH:TOSL</th>
<th>0x0F</th>
<th>Stack Reset Disabled (STVREN = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0E</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x0D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x0C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x0B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x0A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x09</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x08</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x07</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x06</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x05</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x04</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x03</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x02</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x01</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x00</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| Initial Stack Configuration: |
| After Reset, the stack is empty. The empty stack is initialized so the Stack Pointer is pointing at 0x1F. If the Stack Overflow/Underflow Reset is enabled, the TOSH/TOSL registers will return '0'. If the Stack Overflow/Underflow Reset is disabled, the TOSH/TOSL registers will return the contents of stack address 0x0F. |

<table>
<thead>
<tr>
<th>TOSH:TOSL</th>
<th>0x1F</th>
<th>0x0000</th>
<th>Stack Reset Enabled (STVREN = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>StkPTR = 0x1F</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
This figure shows the stack configuration after the first CALL or a single interrupt. If a RETURN instruction is executed, the return address will be placed in the Program Counter and the Stack Pointer decremented to the empty state (0x1F).

After seven CALLs or six CALLs and an interrupt, the stack looks like the figure on the left. A series of RETURN instructions will repeatedly place the return addresses into the Program Counter and pop the stack.
3.5.2 OVERFLOW/UNDERFLOW RESET

If the STVREN bit in Configuration Words is programmed to '1', the device will be reset if the stack is PUSHed beyond the sixteenth level or POPed beyond the first level, setting the appropriate bits (STKOVF or STKUNF, respectively) in the PCON register.

3.6 Indirect Addressing

The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the File Select Registers (FSR). If the FSRn address specifies one of the two INDFn registers, the read will return '0' and the write will not occur (though Status bits may be affected). The FSRn register value is created by the pair FSRnH and FSRnL.

The FSR registers form a 16-bit address that allows an addressing space with 65536 locations. These locations are divided into three memory regions:

- Traditional Data Memory
- Linear Data Memory
- Program Flash Memory
FIGURE 3-9: INDIRECT ADDRESSING

FSR Address Range

Traditional Data Memory
- 0x0000
- 0x0FFF

Reserved
- 0x1000
- 0x1FFF
- 0x2000
- 0x29F
- 0x29B0
- 0x29AF
- 0x7FFF
- 0x8000
- 0xFFFF

Linear Data Memory
- 0x1FFF

Program Flash Memory
- 0x0000
- 0x7FFF

Note: Not all memory regions are completely implemented. Consult device memory tables for memory limits.
3.6.1 TRADITIONAL DATA MEMORY

The traditional data memory is a region from FSR address 0x000 to FSR address 0xFFF. The addresses correspond to the absolute addresses of all SFR, GPR and common registers.

FIGURE 3-10: TRADITIONAL DATA MEMORY MAP

<table>
<thead>
<tr>
<th>Direct Addressing</th>
<th>Indirect Addressing</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 BSR 0 6 From Opcode 0</td>
<td>7 FSRxH 0 7 FSRxL 0</td>
</tr>
<tr>
<td>Bank Select</td>
<td>Location Select</td>
</tr>
<tr>
<td>Bank Select</td>
<td>Location Select</td>
</tr>
</tbody>
</table>

![Diagram of Traditional Data Memory Map]

Bank 0 Bank 1 Bank 2 Bank 31
3.6.2 LINEAR DATA MEMORY

The linear data memory is the region from FSR address 0x2000 to FSR address 0x29AF. This region is a virtual region that points back to the 80-byte blocks of GPR memory in all the banks.

Unimplemented memory reads as 0x00. Use of the linear data memory region allows buffers to be larger than 80 bytes because incrementing the FSR beyond one bank will go directly to the GPR memory of the next bank.

The 16 bytes of common memory are not included in the linear data memory region.

FIGURE 3-11: LINEAR DATA MEMORY MAP

3.6.3 PROGRAM FLASH MEMORY

To make constant data access easier, the entire program Flash memory is mapped to the upper half of the FSR address space. When the MSB of FSRnH is set, the lower 15 bits are the address in program memory which will be accessed through INDF. Only the lower 8 bits of each memory location is accessible via INDF. Writing to the program Flash memory cannot be accomplished via the FSR/INDF interface. All instructions that access program Flash memory via the FSR/INDF interface will require one additional instruction cycle to complete.

FIGURE 3-12: PROGRAM FLASH MEMORY MAP
4.0 DEVICE CONFIGURATION

Device configuration consists of Configuration Words, Code Protection and Device ID.

4.1 Configuration Words

There are several Configuration Word bits that allow different oscillator and memory protection options. These are implemented as Configuration Word 1 at 8007h and Configuration Word 2 at 8008h.

Note: The DEBUG bit in Configuration Words is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a ‘1’.
## 4.2 Register Definitions: Configuration Words

**REGISTER 4-1: CONFIG1: CONFIGURATION WORD 1**

<table>
<thead>
<tr>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>FCMEN</td>
<td>IESO</td>
<td>CLKOUTEN</td>
<td>BOREN&lt;1:0&gt;</td>
<td>CPD</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **P** = Programmable bit
- **U** = Unimplemented bit, read as ‘1’
- ‘0’ = Bit is cleared
- ‘1’ = Bit is set
- ‘-n’ = Value when blank or after Bulk Erase

- **bit 13** FCMEN: Fail-Safe Clock Monitor Enable bit
  - **1** = Fail-Safe Clock Monitor and internal/external switchover are both enabled.
  - **0** = Fail-Safe Clock Monitor is disabled

- **bit 12** IESO: Internal External Switchover bit
  - **1** = Internal/External Switchover mode is enabled
  - **0** = Internal/External Switchover mode is disabled

- **bit 11** CLKOUTEN: Clock Out Enable bit
  - **1** = CLKOUT function is disabled. Oscillator function on the CLKOUT pin.
  - **0** = CLKOUT function is enabled on the CLKOUT pin

- **bit 10-9** BOREN<1:0>: Brown-out Reset Enable bits
  - **11** = BOR enabled
  - **10** = BOR enabled during operation and disabled in Sleep
  - **01** = BOR controlled by SBOREN bit of the BORCON register
  - **00** = BOR disabled

- **bit 8** CPD: Data Code Protection bit
  - **1** = Data memory code protection is disabled
  - **0** = Data memory code protection is enabled

- **bit 7** CP: Code Protection bit
  - **1** = Program memory code protection is disabled
  - **0** = Program memory code protection is enabled

- **bit 6** MCLRE: MCLR/VPP Pin Function Select bit
  - If LVP bit = 1:
    - This bit is ignored.
  - If LVP bit = 0:
    - **1** = MCLR/VPP pin function is MCLR; Weak pull-up enabled.
    - **0** = MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of WPUE3 bit.

- **bit 5** PWRTE: Power-up Timer Enable bit
  - **1** = PWRT disabled
  - **0** = PWRT enabled

- **bit 4-3** WDTE<1:0>: Watchdog Timer Enable bit
  - **11** = WDT enabled
  - **10** = WDT enabled while running and disabled in Sleep
  - **01** = WDT controlled by the SWDTEN bit in the WDTCON register
  - **00** = WDT disabled
REGISTER 4-1: CONFIG1: CONFIGURATION WORD 1 (CONTINUED)

bit 2-0 \( \text{FOSC}<2:0> \): Oscillator Selection bits

- 111 = ECH: External Clock, High-Power mode (4-20 MHz): device clock supplied to CLKin pin
- 110 = ECM: External Clock, Medium-Power mode (0.5-4 MHz): device clock supplied to CLKin pin
- 101 = ECL: External Clock, Low-Power mode (0-0.5 MHz): device clock supplied to CLKin pin
- 100 = INTOSC oscillator: I/O function on CLKin pin
- 011 = EXTRC oscillator: External RC circuit connected to CLKin pin
- 010 = HS oscillator: High-speed crystal/resonator connected between OSC1 and OSC2 pins
- 001 = XT oscillator: Crystal/resonator connected between OSC1 and OSC2 pins
- 000 = LP oscillator: Low-power crystal connected between OSC1 and OSC2 pins

**Note 1:** The entire data EEPROM will be erased when the code protection is turned off during an erase. Once the Data Code Protection bit is enabled, \( \text{CPD} = 0 \), the Bulk Erase Program Memory Command (through ICSP) can disable the Data Code Protection \( \text{CPD} = 1 \). When a Bulk Erase Program Memory Command is executed, the entire Program Flash Memory, Data EEPROM and configuration memory will be erased.
REGISTER 4-2: CONFIG2: CONFIGURATION WORD 2

<table>
<thead>
<tr>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVP</td>
<td>DEBUG</td>
<td>LPBOR</td>
<td>BORV</td>
<td>STVREN</td>
<td>PLL EN</td>
</tr>
</tbody>
</table>

bit 13: **LVP**: Low-Voltage Programming Enable bit\(^1\)
- \(1\) = Low-voltage programming enabled
- \(0\) = High-voltage on MCLR must be used for programming

bit 12: **DEBUG**: In-Circuit Debugger Mode bit\(^3\)
- \(1\) = In-Circuit Debugger disabled, ICSPCLK and ICSPDAT are general purpose I/O pins
- \(0\) = In-Circuit Debugger enabled, ICSPCLK and ICSPDAT are dedicated to the debugger

bit 11: **LPBOR**: Low-Power BOR Enable bit
- \(1\) = Low-Power Brown-out Reset is disabled
- \(0\) = Low-Power Brown-out Reset is enabled

bit 10: **BORV**: Brown-out Reset Voltage Selection bit\(^4\)
- \(1\) = Brown-out Reset voltage (\(V_{BOR}\)), low trip point selected.
- \(0\) = Brown-out Reset voltage (\(V_{BOR}\)), high trip point selected.

bit 9: **STVREN**: Stack Overflow/Underflow Reset Enable bit
- \(1\) = Stack Overflow or Underflow will cause a Reset
- \(0\) = Stack Overflow or Underflow will not cause a Reset

bit 8: **PLLEN**: PLL Enable bit
- \(1\) = 4xPLL enabled
- \(0\) = 4xPLL disabled

bit 7-6: Unimplemented: Read as ‘1’

bit 5: **VCAPEN**: Voltage Regulator Capacitor Enable bit\(^2\)
- \(1\) = \(V_{CAP}\) functionality is disabled on RA6
- \(0\) = \(V_{CAP}\) functionality is enabled on RA6

bit 4-2: Unimplemented: Read as ‘1’

bit 1-0: **WRT<1:0>**: Flash Memory Self-Write Protection bits
- 4 k\(\times\)Flash memory (PIC16(L)F1784 only):
  - \(11\) = Write protection off
  - \(10\) = 000h to 1FFh write-protected, 200h to FFFh may be modified by EECON control
  - \(01\) = 000h to 7FFh write-protected, 800h to FFFh may be modified by EECON control
  - \(00\) = 000h to FFFh write-protected, no addresses may be modified by EECON control
- 8 k\(\times\)Flash memory (PIC16(L)F1786/7 only):
  - \(11\) = Write protection off
  - \(10\) = 0000h to 1FFFh write-protected, 0200h to 1FFFh may be modified by EECON control
  - \(01\) = 0000h to 0FFFh write-protected, 1000h to 1FFFh may be modified by EECON control
  - \(00\) = 0000h to 1FFFh write-protected, no addresses may be modified by EECON control

**Note**
1. The LVP bit cannot be programmed to ‘0’ when Programming mode is entered via LVP.
2. Not implemented on “LF” devices.
3. The DEBUG bit in Configuration Words is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a ‘1’.
4. See \(V_{BOR}\) parameter for specific trip point voltages.
4.3 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data EEPROM protection are controlled independently. Internal access to the program memory and data EEPROM are unaffected by any code protection setting.

4.3.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the CP bit in Configuration Words. When CP = 0, external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Writing the program memory is dependent upon the write protection setting. See Section 4.4 “Write Protection” for more information.

4.3.2 DATA EEPROM PROTECTION

The entire data EEPROM is protected from external reads and writes by the CPD bit. When CPD = 0, external reads and writes of data EEPROM are inhibited. The CPU can continue to read and write data EEPROM regardless of the protection bit settings.

4.4 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as bootloader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in Configuration Words define the size of the program memory block that is protected.

4.5 User ID

Four memory locations (8000h-8003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See Section 12.5 “User ID, Device ID and Configuration Word Access” for more information on accessing these memory locations. For more information on checksum calculation, see the “PIC16(L)F178X Memory Programming Specification” (DS41457).
4.6 Device ID and Revision ID

The memory location 8006h is where the Device ID and Revision ID are stored. The upper nine bits hold the Device ID. The lower five bits hold the Revision ID. See Section 12.5 “User ID, Device ID and Configuration Word Access” for more information on accessing these memory locations.

Development tools, such as device programmers and debuggers, may be used to read the Device ID and Revision ID.

4.7 Register Definitions: Device and Revision

REGISTER 4-3: DEVID: DEVICE ID REGISTER

<table>
<thead>
<tr>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEV&lt;8:3&gt;</td>
<td>bit 13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEV&lt;2:0&gt;</td>
<td>REV&lt;4:0&gt;</td>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit

'1' = Bit is set

'0' = Bit is cleared

bit 13-5 DEV<8:0>: Device ID bits

<table>
<thead>
<tr>
<th>Device</th>
<th>DEVICEID&lt;13:0&gt; Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC16F1784</td>
<td>10 1010 010 x xxxx</td>
</tr>
<tr>
<td>PIC16LF1784</td>
<td>10 1010 111 x xxxx</td>
</tr>
<tr>
<td>PIC16F1786</td>
<td>10 1010 011 x xxxx</td>
</tr>
<tr>
<td>PIC16LF1786</td>
<td>10 1011 000 x xxxx</td>
</tr>
<tr>
<td>PIC16F1787</td>
<td>10 1010 100 x xxxx</td>
</tr>
<tr>
<td>PIC16LF1787</td>
<td>10 1011 001 x xxxx</td>
</tr>
</tbody>
</table>

bit 4-0 REV<4:0>: Revision ID bits

These bits are used to identify the revision (see Table under DEV<8:0> above).
5.0 RESETS

There are multiple ways to reset this device:

- Power-On Reset (POR)
- Brown-Out Reset (BOR)
- Low-Power Brown-Out Reset (LPBOR)
- MCLR Reset
- WDT Reset
- RESET instruction
- Stack Overflow
- Stack Underflow
- Programming mode exit

To allow VDD to stabilize, an optional Power-up Timer can be enabled to extend the Reset time after a BOR or POR event.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 5-1.

**FIGURE 5-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**

Note 1: See Table 5-1 for BOR active conditions.
5.1 Power-On Reset (POR)

The POR circuit holds the device in Reset until VDD has reached an acceptable level for minimum operation. Slow rising VDD, fast operating speeds or analog performance may require greater than minimum VDD. The PWRT, BOR or MCLR features can be used to extend the start-up period until all device operation conditions have been met.

5.1.1 POWER-UP TIMER (PWRT)

The Power-up Timer provides a nominal 64 ms time-out on POR or Brown-out Reset. The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the VDD to rise to an acceptable level. The Power-up Timer is enabled by clearing the PWRTEN bit in Configuration Words.

The Power-up Timer starts after the release of the POR and BOR.

For additional information, refer to Application Note AN607, “Power-up Trouble Shooting” (DS00607).

5.2 Brown-Out Reset (BOR)

The BOR circuit holds the device in Reset when VDD reaches a selectable minimum level. Between the POR and BOR, complete voltage range coverage for execution protection can be implemented.

The Brown-out Reset module has four operating modes controlled by the BOREN<1:0> bits in Configuration Words. The four operating modes are:

- BOR is always on
- BOR is off when in Sleep
- BOR is controlled by software
- BOR is always off

Refer to Table 5-1 for more information.

The Brown-out Reset voltage level is selectable by configuring the BORV bit in Configuration Words. A VDD noise rejection filter prevents the BOR from triggering on small events. If VDD falls below VBOR for a duration greater than parameter TBORDC, the device will reset. See Figure 5-2 for more information.

### TABLE 5-1: BOR OPERATING MODES

<table>
<thead>
<tr>
<th>BOREN&lt;1:0&gt;</th>
<th>SBOREN</th>
<th>Device Mode</th>
<th>BOR Mode</th>
<th>Instruction Execution upon: Release of POR or Wake-up from Sleep</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>X</td>
<td>X</td>
<td>Active</td>
<td>Waits for BOR ready⁽¹⁾ (BORRDY = 1)</td>
</tr>
<tr>
<td>10</td>
<td>X</td>
<td>Awake</td>
<td>Active</td>
<td>Waits for BOR ready (BORRDY = 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sleep</td>
<td>Disabled</td>
<td></td>
</tr>
<tr>
<td>01</td>
<td>1</td>
<td>X</td>
<td>Active</td>
<td>waits for BOR ready⁽¹⁾ (BORRDY = 1)</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>X</td>
<td>Disabled</td>
<td>Begins immediately (BORRDY = x)</td>
</tr>
<tr>
<td>00</td>
<td>X</td>
<td>X</td>
<td>Disabled</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: In these specific cases, “Release of POR” and “Wake-up from Sleep”, there is no delay in start-up. The BOR ready flag, (BORRDY = 1), will be set before the CPU is ready to execute instructions because the BOR circuit is forced on by the BOREN<1:0> bits.

5.2.1 BOR IS ALWAYS ON

When the BOREN bits of Configuration Words are programmed to ‘11’, the BOR is always on. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is active during Sleep. The BOR does not delay wake-up from Sleep.

5.2.2 BOR IS OFF IN SLEEP

When the BOREN bits of Configuration Words are programmed to ‘10’, the BOR is off, except in Sleep. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is not active during Sleep. The device wake-up will be delayed until the BOR is ready.

5.2.3 BOR CONTROLLED BY SOFTWARE

When the BOREN bits of Configuration Words are programmed to ‘01’, the BOR is controlled by the SBOREN bit of the BORCON register. The device start-up is not delayed by the BOR ready condition or the VDD level.

BOR protection begins as soon as the BOR circuit is ready. The status of the BOR circuit is reflected in the BORRDY bit of the BORCON register.

BOR protection is unchanged by Sleep.
5.3 Register Definitions: BOR Control

REGISTER 5-1: BORCON: BROWN-OUT RESET CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-1/u</th>
<th>R/W-0/u</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R-q/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBOREN</td>
<td>BORFS</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>BORRDY</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- '1' = Bit is set
- '0' = Bit is cleared
- n/n = Value at POR and BOR/Value at all other Resets
- q = Value depends on condition

**bit 7** 
**SBOREN**: Software Brown-out Reset Enable bit
- If BOREN <1:0> in Configuration Words ≠ 01:
  - SBOREN is read/write, but has no effect on the BOR.
- If BOREN <1:0> in Configuration Words = 01:
  - 1 = BOR Enabled
  - 0 = BOR Disabled

**bit 6** 
**BORFS**: Brown-out Reset Fast Start bit(1)
- If BOREN<1:0> = 11 (Always on) or BOREN<1:0> = 00 (Always off)
  - BORFS is Read/Write, but has no effect.
- If BOREN <1:0> = 10 (Disabled in Sleep) or BOREN<1:0> = 01 (Under software control):
  - 1 = Band gap is forced on always (covers sleep/wake-up/operating cases)
  - 0 = Band gap operates normally, and may turn off

**bit 5-1** 
Unimplemented: Read as '0'

**bit 0** 
**BORRDY**: Brown-out Reset Circuit Ready Status bit
- 1 = The Brown-out Reset circuit is active
- 0 = The Brown-out Reset circuit is inactive

**Note 1**: BOREN<1:0> bits are located in Configuration Words.

---

**FIGURE 5-2: BROWN-OUT SITUATIONS**

- **SBOREN**: Software Brown-out Reset Enable bit
  - If BOREN<1:0> in Configuration Words ≠ 01:
    - SBOREN is read/write, but has no effect on the BOR.
  - If BOREN <1:0> in Configuration Words = 01:
    - 1 = BOR Enabled
    - 0 = BOR Disabled

- **BORFS**: Brown-out Reset Fast Start bit(1)
  - If BOREN<1:0> = 11 (Always on) or BOREN<1:0> = 00 (Always off)
    - BORFS is Read/Write, but has no effect.
  - If BOREN <1:0> = 10 (Disabled in Sleep) or BOREN<1:0> = 01 (Under software control):
    - 1 = Band gap is forced on always (covers sleep/wake-up/operating cases)
    - 0 = Band gap operates normally, and may turn off

- **BORRDY**: Brown-out Reset Circuit Ready Status bit
  - 1 = The Brown-out Reset circuit is active
  - 0 = The Brown-out Reset circuit is inactive

**Note 1**: TPWRT delay only if PWRTE bit is programmed to '0'.
5.4 Low-Power Brown-Out Reset (LPBOR)

The Low-Power Brown-Out Reset (LPBOR) is an essential part of the Reset subsystem. Refer to Figure 5-1 to see how the BOR interacts with other modules.

The LPBOR is used to monitor the external VDD pin. When too low of a voltage is detected, the device is held in Reset. When this occurs, a register bit (BOR) is changed to indicate that a BOR Reset has occurred. The same bit is set for both the BOR and the LPBOR. Refer to Register 5-2.

5.4.1 ENABLING LPBOR

The LPBOR is controlled by the LPBOR bit of Configuration Words. When the device is erased, the LPBOR module defaults to disabled.

5.4.1.1 LPBOR Module Output

The output of the LPBOR module is a signal indicating whether or not a Reset is to be asserted. This signal is OR'd together with the Reset signal of the BOR module to provide the generic BOR signal, which goes to the PCON register and to the power control block.

5.5 MCLR

The MCLR is an optional external input that can reset the device. The MCLR function is controlled by the MCLRE bit of Configuration Words and the LVP bit of Configuration Words (Table 5-2).

<table>
<thead>
<tr>
<th>MCLRE</th>
<th>LVP</th>
<th>MCLR</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Disabled</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Enabled</td>
</tr>
<tr>
<td>x</td>
<td>1</td>
<td>Enabled</td>
</tr>
</tbody>
</table>

5.5.1 MCLR ENABLED

When MCLR is enabled and the pin is held low, the device is held in Reset. The MCLR pin is connected to VDD through an internal weak pull-up.

The device has a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

Note: A Reset does not drive the MCLR pin low.

5.5.2 MCLR DISABLED

When MCLR is disabled, the pin functions as a general purpose input and the internal weak pull-up is under software control. See Section 13.11 “PORTE Registers” for more information.

5.6 Watchdog Timer (WDT) Reset

The Watchdog Timer generates a Reset if the firmware does not issue a CLRWD instruction within the time-out period. The TO and PD bits in the STATUS register are changed to indicate the WDT Reset. See Section 11.0 “Watchdog Timer (WDT)” for more information.

5.7 RESET Instruction

A RESET instruction will cause a device Reset. The RI bit in the PCON register will be set to ‘0’. See Table 5-4 for default conditions after a RESET instruction has occurred.

5.8 Stack Overflow/Underflow Reset

The device can reset when the Stack Overflows or Underflows. The STKOVF or STKUNF bits of the PCON register indicate the Reset condition. These Resets are enabled by setting the STVREN bit in Configuration Words. See Section 5.8 “Stack Overflow/Underflow Reset” for more information.

5.9 Programming Mode Exit

Upon exit of Programming mode, the device will behave as if a POR had just occurred.

5.10 Power-Up Timer

The Power-up Timer optionally delays device execution after a BOR or POR event. This timer is typically used to allow VDD to stabilize before allowing the device to start running.

The Power-up Timer is controlled by the PWRTE bit of Configuration Words.

5.11 Start-up Sequence

Upon the release of a POR or BOR, the following must occur before the device will begin executing:

1. Power-up Timer runs to completion (if enabled).
2. Oscillator start-up timer runs to completion (if required for oscillator source).
3. MCLR must be released (if enabled).

The total time-out will vary based on oscillator configuration and Power-up Timer configuration. See Section 6.0 “Oscillator Module (with Fail-Safe Clock Monitor)” for more information.

The Power-up Timer and oscillator start-up timer run independently of MCLR Reset. If MCLR is kept low long enough, the Power-up Timer and oscillator start-up timer will expire. Upon bringing MCLR high, the device will begin execution immediately (see Figure 5-3). This is useful for testing purposes or to synchronize more than one device operating in parallel.
FIGURE 5-3:  RESET START-UP SEQUENCE

VDD  
Internal POR  

Power-up Timer  

MCLR  
Internal RESET  

Oscillator Modes  

External Crystal  
Oscillator Start-up Timer  

Oscillator  
Fosc  

Internal Oscillator  

Oscillator  
Fosc  

External Clock (EC)  

CLKIN  
Fosc
5.12 Determining the Cause of a Reset

Upon any Reset, multiple bits in the STATUS and PCON register are updated to indicate the cause of the Reset. Table 5-3 and Table 5-4 show the Reset conditions of these registers.

#### TABLE 5-3: RESET STATUS BITS AND THEIR SIGNIFICANCE

<table>
<thead>
<tr>
<th>STKOVF</th>
<th>STKUNF</th>
<th>RWDT</th>
<th>RMCLR</th>
<th>RI</th>
<th>POR</th>
<th>BOR</th>
<th>T0</th>
<th>PD</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>x</td>
<td>1</td>
<td>1</td>
<td>Power-on Reset</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>x</td>
<td>0</td>
<td>x</td>
<td>Illegal, TO is set on POR</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>x</td>
<td>x</td>
<td>0</td>
<td>Illegal, PD is set on POR</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>u</td>
<td>1</td>
<td>1</td>
<td>u</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Brown-out Reset</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>0</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>0</td>
<td>WDT Reset</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>0</td>
<td>WDT Wake-up from Sleep</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>1</td>
<td>0</td>
<td>Interrupt Wake-up from Sleep</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>u</td>
<td>0</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>MCLR Reset during normal operation</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>u</td>
<td>0</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>1</td>
<td>0</td>
<td>MCLR Reset during Sleep</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>0</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>RESET Instruction Executed</td>
</tr>
<tr>
<td>l</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>Stack Overflow Reset (STVREN = 1)</td>
</tr>
<tr>
<td>u</td>
<td>1</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>Stack Underflow Reset (STVREN = 1)</td>
</tr>
</tbody>
</table>

#### TABLE 5-4: RESET CONDITION FOR SPECIAL REGISTERS

<table>
<thead>
<tr>
<th>Condition</th>
<th>Program Counter</th>
<th>STATUS Register</th>
<th>PCON Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-on Reset</td>
<td>0000h</td>
<td>---1 1000</td>
<td>00-- 110x</td>
</tr>
<tr>
<td>MCLR Reset during normal operation</td>
<td>0000h</td>
<td>---- u uuuu</td>
<td>uu-- 0uuu</td>
</tr>
<tr>
<td>MCLR Reset during Sleep</td>
<td>0000h</td>
<td>----1 0uuu</td>
<td>uu-- 0uuu</td>
</tr>
<tr>
<td>WDT Reset</td>
<td>0000h</td>
<td>----0 uuuu</td>
<td>uu-- uuuu</td>
</tr>
<tr>
<td>WDT Wake-up from Sleep</td>
<td>PC + 1</td>
<td>----0 0uuu</td>
<td>uu-- uuuu</td>
</tr>
<tr>
<td>Brown-out Reset</td>
<td>0000h</td>
<td>----1 1uuu</td>
<td>00-- 11u0</td>
</tr>
<tr>
<td>Interrupt Wake-up from Sleep</td>
<td>PC + 1(1)</td>
<td>----1 0uuu</td>
<td>uu-- uuuu</td>
</tr>
<tr>
<td>RESET Instruction Executed</td>
<td>0000h</td>
<td>---- u uuuu</td>
<td>uu-- u0uuu</td>
</tr>
<tr>
<td>Stack Overflow Reset (STVREN = 1)</td>
<td>0000h</td>
<td>---- u uuuu</td>
<td>1u-- uuuu</td>
</tr>
<tr>
<td>Stack Underflow Reset (STVREN = 1)</td>
<td>0000h</td>
<td>---- u uuuu</td>
<td>u1-- uuuu</td>
</tr>
</tbody>
</table>

Legend:  
- = unchanged,  x = unknown,  - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and Global Enable bit (GIE) is set, the return address is pushed on the stack and PC is loaded with the interrupt vector (0004h) after execution of PC + 1.
5.13 Power Control (PCON) Register
The Power Control (PCON) register contains flag bits to differentiate between a:
- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Reset Instruction Reset (RI)
- MCLR Reset (RMCLR)
- Watchdog Timer Reset (RWDT)
- Stack Underflow Reset (STKUNF)
- Stack Overflow Reset (STKOVF)

The PCON register bits are shown in Register 5-2.

5.14 Register Definitions: Power Control

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value/Condition</th>
</tr>
</thead>
</table>
| 7   | STKOVF: Stack Overflow Flag bit | 1 = A Stack Overflow occurred  
0 = A Stack Overflow has not occurred or cleared by firmware |
| 6   | STKUNF: Stack Underflow Flag bit | 1 = A Stack Underflow occurred  
0 = A Stack Underflow has not occurred or cleared by firmware |
| 5   | Unimplemented: Read as '0'    |                                               |
| 4   | RWDT: Watchdog Timer Reset Flag bit | 1 = A Watchdog Timer Reset has not occurred or set to '1' by firmware  
0 = A Watchdog Timer Reset has occurred (cleared by hardware) |
| 3   | RMCLR: MCLR Reset Flag bit | 1 = A MCLR Reset has not occurred or set to '1' by firmware  
0 = A MCLR Reset has occurred (cleared by hardware) |
| 2   | RI: RESET Instruction Flag bit | 1 = A RESET instruction has not been executed or set to '1' by firmware  
0 = A RESET instruction has been executed (cleared by hardware) |
| 1   | POR: Power-on Reset Status bit | 1 = No Power-on Reset occurred  
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs) |
| 0   | BOR: Brown-out Reset Status bit | 1 = No Brown-out Reset occurred  
0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs) |

Legend:
- HC = Bit is cleared by hardware
- HS = Bit is set by hardware
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- q = Value depends on condition
- m/n = Value at POR and BOR/Value at all other Resets
### TABLE 5-5: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>BORCON</td>
<td>SBOREN</td>
<td>BORFS</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>BORRDY 61</td>
</tr>
<tr>
<td>PCON</td>
<td>STKOVF</td>
<td>STKUNF</td>
<td>—</td>
<td>RWDT</td>
<td>RMCLR</td>
<td>RI</td>
<td>POR</td>
<td>BOR</td>
<td>65</td>
</tr>
<tr>
<td>STATUS</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TÖ</td>
<td>PD</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
<td>27</td>
</tr>
<tr>
<td>WDTCN</td>
<td>—</td>
<td>—</td>
<td>TD</td>
<td>WDTPS&lt;4:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SWDTEN 110</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented location, read as ‘0’. Shaded cells are not used by Resets.
6.0 OSCILLATOR MODULE (WITH FAIL-SAFE CLOCK MONITOR)

6.1 Overview

The oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 6-1 illustrates a block diagram of the oscillator module.

Clock sources can be supplied from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be supplied from one of two internal oscillators and PLL circuits, with a choice of speeds selectable via software. Additional clock features include:

- Selectable system clock source between external or internal sources via software.
- Two-Speed Start-up mode, which minimizes latency between external oscillator start-up and code execution.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, EC or RC modes) and switch automatically to the internal oscillator.
- Oscillator Start-up Timer (OST) ensures stability of crystal oscillator sources

The oscillator module can be configured in one of eight clock modes.

1. ECL – External Clock Low-Power mode (0 MHz to 0.5 MHz)
2. ECM – External Clock Medium-Power mode (0.5 MHz to 4 MHz)
3. ECH – External Clock High-Power mode (4 MHz to 32 MHz)
4. LP – 32 kHz Low-Power Crystal mode.
5. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode (up to 4 MHz)
6. HS – High Gain Crystal or Ceramic Resonator mode (4 MHz to 20 MHz)
8. INTOSC – Internal oscillator (31 kHz to 32 MHz).

Clock Source modes are selected by the FOSC<2:0> bits in the Configuration Words. The FOSC bits determine the type of oscillator that will be used when the device is first powered.

The EC clock mode relies on an external logic level signal as the device clock source. The LP, XT, and HS clock modes require an external crystal or resonator to be connected to the device. Each mode is optimized for a different frequency range. The RC clock mode requires an external resistor and capacitor to set the oscillator frequency.

The INTOSC internal oscillator block produces low, medium, and high-frequency clock sources, designated LFINTOSC, MFINTOSC and HFINTOSC. (see Internal Oscillator Block, Figure 6-1). A wide selection of device clock frequencies may be derived from these three clock sources.
FIGURE 6-1: SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM

Note 1: This selection should not be made when the PSMC is using the 64 MHz clock option.
6.2 Clock Source Types

Clock sources can be classified as external or internal. External clock sources rely on external circuitry for the clock source to function. Examples are: oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.

Internal clock sources are contained within the oscillator module. The internal oscillator block has two internal oscillators and a dedicated Phase-Lock Loop (HFPLL) that are used to generate three internal system clock sources: the 16 MHz High-Frequency Internal Oscillator (HFINTOSC), 500 kHz (MFINTOSC) and the 31 kHz Low-Frequency Internal Oscillator (LFINTOSC).

The system clock can be selected between external or internal clock sources via the System Clock Select (SCS) bits in the OSCCON register. See Section 6.3 “Clock Switching” for additional information.

6.2.1 EXTERNAL CLOCK SOURCES

An external clock source can be used as the device system clock by performing one of the following actions:

• Program the FOSC<2:0> bits in the Configuration Words to select an external clock source that will be used as the default system clock upon a device Reset.
• Write the SCS<1:0> bits in the OSCCON register to switch the system clock source to:
  - Timer1 oscillator during run-time, or
  - An external clock source determined by the value of the FOSC bits.

See Section 6.3 “Clock Switching” for more information.

6.2.1.1 EC Mode

The External Clock (EC) mode allows an externally generated logic level signal to be the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. Figure 6-2 shows the pin connections for EC mode.

EC mode has three power modes to select from through Configuration Words:

• High power, 4-32 MHz (FOSC = 111)
• Medium power, 0.5-4 MHz (FOSC = 110)
• Low power, 0-0.5 MHz (FOSC = 101)

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 6-2: EXTERNAL CLOCK (EC) MODE OPERATION

6.2.1.2 LP, XT, HS Modes

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 6-3). The three modes select a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 6-3 and Figure 6-4 show typical circuits for quartz crystal and ceramic resonators, respectively.
6.2.1.3 Oscillator Start-up Timer (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended, unless either FSCM or Two-Speed Start-Up are enabled. In this case, code will continue to execute at the selected INTOSC frequency while the OST is counting. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see Section 6.4 “Two-Speed Clock Start-up Mode”).

Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

3: For oscillator design assistance, reference the following Microchip Applications Notes:
- AN826, "Crystal Oscillator Basics and Crystal Selection for rPIC® and PIC® Devices" (DS00826)
- AN849, “Basic PIC® Oscillator Design” (DS00849)
- AN943, “Practical PIC® Oscillator Analysis and Design” (DS00943)
- AN949, “Making Your Oscillator Work” (DS00949)

Note 1: A series resistor (Rs) may be required for quartz crystals with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

3: An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.
6.2.1.4 4x PLL

The oscillator module contains a 4x PLL that can be used with both external and internal clock sources to provide a system clock source. The input frequency for the 4x PLL must fall within specifications. See the PLL Clock Timing Specifications in Section 30.0 “Electrical Specifications”.

The 4x PLL may be enabled for use by one of two methods:
1. Program the PLLEN bit in Configuration Words to a ‘1’.
2. Write the SPLLEN bit in the OSCCON register to a ‘1’. If the PLLEN bit in Configuration Words is programmed to a ‘1’, then the value of SPLLEN is ignored.

6.2.1.5 TIMER1 Oscillator

The Timer1 oscillator is a separate crystal oscillator that is associated with the Timer1 peripheral. It is optimized for timekeeping operations with a 32.768 kHz crystal connected between the T1OSO and T1OSI device pins.

The Timer1 oscillator can be used as an alternate system clock source and can be selected during run-time using clock switching. Refer to Section 6.3 “Clock Switching” for more information.

FIGURE 6-5: QUARTZ CRYSTAL OPERATION (TIMER1 OSCILLATOR)

Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

3: For oscillator design assistance, reference the following Microchip Applications Notes:
   • AN826, “Crystal Oscillator Basics and Crystal Selection for rPIC® and PIC® Devices” (DS00826)
   • AN849, “Basic PIC® Oscillator Design” (DS00849)
   • AN943, “Practical PIC® Oscillator Analysis and Design” (DS00943)
   • AN949, “Making Your Oscillator Work” (DS00949)
   • TB097, “Interfacing a Micro Crystal MS1V-T1K 32.768 kHz Tuning Fork Crystal to a PIC16F690/SS” (DS91097)
   • AN1288, “Design Practices for Low-Power External Oscillators” (DS01288)
6.2.1.6 External RC Mode

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required.

The RC circuit connects to OSC1. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. The function of the OSC2/CLKOUT pin is determined by the CLKOUTEN bit in Configuration Words.

Figure 6-6 shows the external RC mode connections.

**FIGURE 6-6: EXTERNAL RC MODES**

![Diagram showing external RC mode connections](image)

The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. Other factors affecting the oscillator frequency are:
- threshold voltage variation
- component tolerances
- packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

6.2.2 INTERNAL CLOCK SOURCES

The device may be configured to use the internal oscillator block as the system clock by performing one of the following actions:

- Program the FOSC<2:0> bits in Configuration Words to select the INTOSC clock source, which will be used as the default system clock upon a device Reset.
- Write the SCS<1:0> bits in the OSCCON register to switch the system clock source to the internal oscillator during run-time. See Section 6.3 “Clock Switching” for more information.

In INTOSC mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT is available for general purpose I/O or CLKOUT.

The function of the OSC2/CLKOUT pin is determined by the CLKOUTEN bit in Configuration Words.

The internal oscillator block has two independent oscillators and a dedicated Phase-Lock Loop, HFPLL that can produce one of three internal system clock sources.

1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory calibrated and operates at 16 MHz. The HFINTOSC source is generated from the 500 kHz MFINTOSC source and the dedicated Phase-Lock Loop, HFPLL. The frequency of the HFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 6-3).

2. The **MFINTOSC** (Medium-Frequency Internal Oscillator) is factory calibrated and operates at 500 kHz. The frequency of the MFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 6-3).

3. The **LFINTOSC** (Low-Frequency Internal Oscillator) is uncalibrated and operates at 31 kHz.
6.2.2.1 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 16 MHz internal clock source. The frequency of the HFINTOSC can be altered via software using the OSCTUNE register (Register 6-3).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 6-1). One of multiple frequencies derived from the HFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See Section 6.2.2.7 “Internal Oscillator Clock Switch Timing” for more information.

The HFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to ‘1x’.

A fast startup oscillator allows internal circuits to power up and stabilize before switching to HFINTOSC.

The High Frequency Internal Oscillator Ready bit (HFIOFR) of the OSCSTAT register indicates when the HFINTOSC is running.

The High Frequency Internal Oscillator Status Locked bit (HFIOFL) of the OSCSTAT register indicates when the HFINTOSC is running within 2% of its final value.

The High Frequency Internal Oscillator Stable bit (HFIOFS) of the OSCSTAT register indicates when the HFINTOSC is running within 0.5% of its final value.

6.2.2.2 MFINTOSC

The Medium-Frequency Internal Oscillator (MFINTOSC) is a factory calibrated 500 kHz internal clock source. The frequency of the MFINTOSC can be altered via software using the OSCTUNE register (Register 6-3).

The output of the MFINTOSC connects to a postscaler and multiplexer (see Figure 6-1). One of nine frequencies derived from the MFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See Section 6.2.2.7 “Internal Oscillator Clock Switch Timing” for more information. The MFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals.

The MFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired LF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to ‘1x’.

6.2.2.3 Internal Oscillator Frequency Adjustment

The 500 kHz internal oscillator is factory calibrated. This internal oscillator can be adjusted in software by writing to the OSCTUNE register (Register 6-3). Since the HFINTOSC and MFINTOSC clock sources are derived from the 500 kHz internal oscillator a change in the OSCTUNE register value will apply to both.

The default value of the OSCTUNE register is ‘0’. The value is a 6-bit two’s complement number. A value of 1Fh will provide an adjustment to the maximum frequency. A value of 20h will provide an adjustment to the minimum frequency.

When the OSCTUNE register is modified, the oscillator frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are not affected by the change in frequency.

6.2.2.4 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is an uncalibrated 31 kHz internal clock source. The output of the LFINTOSC connects to a multiplexer (see Figure 6-1). Select 31 kHz, via software, using the IRCF<3:0> bits of the OSCCON register. See Section 6.2.2.7 “Internal Oscillator Clock Switch Timing” for more information. The LFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF<3:0> bits of the OSCCON register = 000) as the system clock source (SCS bits of the OSCCON register = 1x), or when any of the following are enabled:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired LF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to ‘1x’.

Peripherals that use the LFINTOSC are:

- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)

The Low-Frequency Internal Oscillator Ready bit (LFIOFR) of the OSCSTAT register indicates when the LFINTOSC is running.
6.2.2.5 Internal Oscillator Frequency Selection

The system clock speed can be selected via software using the Internal Oscillator Frequency Select bits IRCF<3:0> of the OSCCON register.

The output of the 16 MHz HFINTOSC, 500 kHz MFINTOSC, and 31 kHz LFINTOSC connects to a postscaler and multiplexer (see Figure 6-1). The Internal Oscillator Frequency Select bits IRCF<3:0> of the OSCCON register select the frequency output of the internal oscillators. One of the following frequencies can be selected via software:

- 32 MHz (requires 4x PLL)
- 16 MHz
- 8 MHz
- 4 MHz
- 2 MHz
- 1 MHz
- 500 kHz (default after Reset)
- 250 kHz
- 125 kHz
- 62.5 kHz
- 31.25 kHz
- 31 kHz (LFINTOSC)

The IRCF<3:0> bits of the OSCCON register allow duplicate selections for some frequencies. These duplicate choices can offer system design trade-offs. Lower power consumption can be obtained when changing oscillator sources for a given frequency. Faster transition times can be obtained between frequency changes that use the same oscillator source.

6.2.2.6 32 MHz Internal Oscillator Frequency Selection

The Internal Oscillator Block can be used with the 4x PLL associated with the External Oscillator Block to produce a 32 MHz internal system clock source. The following settings are required to use the 32 MHz internal clock source:

- The FOSC bits in Configuration Words must be set to use the INTOSC source as the device system clock (FOSC<2:0> = 100).
- The SCS bits in the OSCCON register must be cleared to use the clock determined by FOSC<2:0> in Configuration Words (SCS<1:0> = 00).
- The IRCF bits in the OSCCON register must be set to the 8 MHz or 16 MHz HFINTOSC set to use (IRCF<3:0> = 111x).
- The SPLLEN bit in the OSCCON register must be set to enable the 4x PLL, or the PLLEN bit of the Configuration Words must be programmed to a '1'.

Note: When using the PLLEN bit of the Configuration Words, the 4x PLL cannot be disabled by software and the SPLLEN option will not be available.

The 4x PLL is not available for use with the internal oscillator when the SCS bits of the OSCCON register are set to '1x'. The SCS bits must be set to '00' to use the 4x PLL with the internal oscillator.
6.2.2.7 Internal Oscillator Clock Switch Timing

When switching between the HFINTOSC, MFINTOSC and the LFINTOSC, the new oscillator may already be shut down to save power (see Figure 6-7). If this is the case, there is a delay after the IRCF<3:0> bits of the OSCCON register are modified before the frequency selection takes place. The OSCSTAT register will reflect the current active status of the HFINTOSC, MFINTOSC and LFINTOSC oscillators. The sequence of a frequency selection is as follows:

1. IRCF<3:0> bits of the OSCCON register are modified.
2. If the new clock is shut down, a clock start-up delay is started.
3. Clock switch circuitry waits for a falling edge of the current clock.
4. The current clock is held low and the clock switch circuitry waits for a rising edge in the new clock.
5. The new clock is now active.
6. The OSCSTAT register is updated as required.
7. Clock switch is complete.

See Figure 6-7 for more details.

If the internal oscillator speed is switched between two clocks of the same source, there is no start-up delay before the new frequency is selected. Clock switching time delays are shown in Table 6-1.

Start-up delay specifications are located in the oscillator tables of Section 30.0 “Electrical Specifications”.

FIGURE 6-7: INTERNAL OSCILLATOR SWITCH TIMING

HFINTOSC/→ LFINTOSC (FSCM and WDT disabled)

<table>
<thead>
<tr>
<th>HFINTOSC/</th>
<th>MFINTOSC</th>
<th>LFINTOSC</th>
<th>IRCF &lt;3:0&gt;</th>
<th>System Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>≠ 0</td>
<td>= 0</td>
</tr>
</tbody>
</table>

Start-up Time 2-cycle Sync Running

HFINTOSC/→ LFINTOSC (Either FSCM or WDT enabled)

<table>
<thead>
<tr>
<th>HFINTOSC/</th>
<th>MFINTOSC</th>
<th>LFINTOSC</th>
<th>IRCF &lt;3:0&gt;</th>
<th>System Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>≠ 0</td>
<td>= 0</td>
</tr>
</tbody>
</table>

Start-up Time 2-cycle Sync Running

LFINTOSC → HFINTOSC/MFINTOSC

<table>
<thead>
<tr>
<th>LFINTOSC</th>
<th>HFINTOSC/</th>
<th>IRCF &lt;3:0&gt;</th>
<th>System Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MFINTOSC</td>
<td>= 0</td>
<td></td>
</tr>
</tbody>
</table>

Start-up Time 2-cycle Sync Running

LFINTOSC turns off unless WDT or FSCM is enabled
6.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bits of the OSCCON register. The following clock sources can be selected using the SCS bits:

- Default system oscillator determined by FOSC bits in Configuration Words
- Timer1 32 kHz crystal oscillator
- Internal Oscillator Block (INTOSC)

6.3.1 SYSTEM CLOCK SELECT (SCS) BITS

The System Clock Select (SCS) bits of the OSCCON register selects the system clock source that is used for the CPU and peripherals.

- When the SCS bits of the OSCCON register = 00, the system clock source is determined by the value of the FOSC<2:0> bits in the Configuration Words.
- When the SCS bits of the OSCCON register = 01, the system clock source is the Timer1 oscillator.
- When the SCS bits of the OSCCON register = 1x, the system clock source is chosen by the internal oscillator frequency selected by the IRCF<3:0> bits of the OSCCON register. After a Reset, the SCS bits of the OSCCON register are always cleared.

Note: Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bits of the OSCCON register. The user can monitor the OSTS bit of the OSCSTAT register to determine the current system clock source.

When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 6-1.

6.3.2 OSCILLATOR START-UP TIMER STATUS (OSTS) BIT

The Oscillator Start-up Timer Status (OSTS) bit of the OSCSTAT register indicates whether the system clock is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Words, or from the internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes. The OST does not reflect the status of the Timer1 oscillator.

6.3.3 TIMER1 OSCILLATOR

The Timer1 oscillator is a separate crystal oscillator associated with the Timer1 peripheral. It is optimized for timekeeping operations with a 32.768 kHz crystal connected between the T1OSO and T1OSI device pins.

The Timer1 oscillator is enabled using the T1OSCEN control bit in the T1CON register. See Section 22.0 “Timer1 Module with Gate Control” for more information about the Timer1 peripheral.

6.3.4 TIMER1 OSCILLATOR READY (T1OSCR) BIT

The user must ensure that the Timer1 oscillator is ready to be used before it is selected as a system clock source. The Timer1 Oscillator Ready (T1OSCR) bit of the OSCSTAT register indicates whether the Timer1 oscillator is ready to be used. After the T1OSCR bit is set, the SCS bits can be configured to select the Timer1 oscillator.

Note: Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bits of the OSCCON register. The user can monitor the OSTS bit of the OSCSTAT register to determine the current system clock source.
6.4 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device. This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC internal oscillator block as the clock source and go back to Sleep without waiting for the external oscillator to become stable.

Two-Speed Start-up provides benefits when the oscillator module is configured for LP, XT or HS modes. The Oscillator Start-up Timer (OST) is enabled for these modes and must count 1024 oscillations before the oscillator can be used as the system clock source.

If the oscillator module is configured for any mode other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

If the OST count reaches 1024 before the device enters Sleep mode, the OSTS bit of the OSCSTAT register is set and program execution switches to the external oscillator. However, the system may never operate from the external oscillator if the time spent awake is very short.

**Note:** Executing a SLEEP instruction will abort the oscillator start-up time and will cause the OSTS bit of the OSCSTAT register to remain clear.

### TABLE 6-1: OSCILLATOR SWITCHING DELAYS

<table>
<thead>
<tr>
<th>Switch From</th>
<th>Switch To</th>
<th>Frequency</th>
<th>Oscillator Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sleep/POR</td>
<td>LFINTOSC(1)</td>
<td>31 kHz</td>
<td>Oscillator Warm-up Delay (T_WARM)</td>
</tr>
<tr>
<td></td>
<td>MFINTOSC(1)</td>
<td>31.25 kHz-500 kHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>HFINTOSC(1)</td>
<td>31.25 kHz-16 MHz</td>
<td></td>
</tr>
<tr>
<td>Sleep/POR</td>
<td>EC, RC(1)</td>
<td>DC – 32 MHz</td>
<td>2 cycles</td>
</tr>
<tr>
<td>LFINTOSC</td>
<td>EC, RC(1)</td>
<td>DC – 32 MHz</td>
<td>1 cycle of each</td>
</tr>
<tr>
<td>Sleep/POR</td>
<td>Timer1 Oscillator LP, XT, HS(1)</td>
<td>32 kHz-20 MHz</td>
<td>1024 Clock Cycles (OST)</td>
</tr>
<tr>
<td>Any clock source</td>
<td>MFINTOSC(1)</td>
<td>31.25 kHz-500 kHz</td>
<td>2 µs (approx.)</td>
</tr>
<tr>
<td>Any clock source</td>
<td>HFINTOSC(1)</td>
<td>31.25 kHz-16 MHz</td>
<td></td>
</tr>
<tr>
<td>Any clock source</td>
<td>LFINTOSC(1)</td>
<td>31 kHz</td>
<td>1 cycle of each</td>
</tr>
<tr>
<td>Any clock source</td>
<td>Timer1 Oscillator</td>
<td>32 kHz</td>
<td>1024 Clock Cycles (OST)</td>
</tr>
<tr>
<td>PLL inactive</td>
<td>PLL active</td>
<td>16-32 MHz</td>
<td>2 ms (approx.)</td>
</tr>
</tbody>
</table>

**Note 1:** PLL inactive.
6.4.2 TWO-SPEED START-UP SEQUENCE
1. Wake-up from Power-on Reset or Sleep.
2. Instructions begin execution by the internal oscillator at the frequency set in the IRCF<3:0> bits of the OSCCON register.
3. OST enabled to count 1024 clock cycles.
4. OST timed out, wait for falling edge of the internal oscillator.
5. OSTS is set.
6. System clock held low until the next falling edge of new clock (LP, XT or HS mode).
7. System clock is switched to external clock source.

6.4.3 CHECKING TWO-SPEED CLOCK STATUS
Checking the state of the OSTS bit of the OSCSTAT register will confirm if the microcontroller is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Words, or the internal oscillator.

FIGURE 6-8: TWO-SPEED START-UP
6.5 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM can detect oscillator failure any time after the Oscillator Start-up Timer (OST) has expired. The FSCM is enabled by setting the FCMEN bit in the Configuration Words. The FSCM is applicable to all external Oscillator modes (LP, XT, HS, EC, Timer1 Oscillator and RC).

FIGURE 6-9: FSCM BLOCK DIAGRAM

6.5.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 6-9. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the external clock goes low.

6.5.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the device clock to an internal clock source and sets the bit flag OSFIF of the PIR2 register. Setting this flag will generate an interrupt if the OSFIE bit of the PIE2 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation.

The internal clock source chosen by the FSCM is determined by the IRCF<3:0> bits of the OSCCON register. This allows the internal oscillator to be configured before a failure occurs.

6.5.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, executing a SLEEP instruction or changing the SCS bits of the OSCCON register. When the SCS bits are changed, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON. When the OST times out, the Fail-Safe condition is cleared after successfully switching to the external clock source. The OSFIF bit should be cleared prior to switching to the external clock source. If the Fail-Safe condition still exists, the OSFIF flag will again become set by hardware.

6.5.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC or RC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed. When the FSCM is enabled, the Two-Speed Start-up is also enabled. Therefore, the device will always be executing code while the OST is operating.

Note: Due to the wide range of oscillator start-up times, the Fail-Safe circuit is not active during oscillator start-up (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the Status bits in the OSCSTAT register to verify the oscillator start-up and that the system clock switchover has successfully completed.
FIGURE 6-10: FSCM TIMING DIAGRAM

Note: The system clock is normally at a much higher frequency than the sample clock. The relative frequencies in this example have been chosen for clarity.
### 6.6 Register Definitions: Oscillator Control

**REGISTER 6-1: OSCON: OSCILLATOR CONTROL REGISTER**

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6-3</th>
<th>Bit 2</th>
<th>Bit 1-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPLLEN</td>
<td>IRCF&lt;3:0&gt;</td>
<td>Unimplemented</td>
<td>SCS&lt;1:0&gt;</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- ‘-n/n’ = Value at POR and BOR/Value at all other Resets

**bit 7**  
SPLLEN: Software PLL Enable bit

If PLLLEN in Configuration Words = 1:
SPLLEN bit is ignored. 4x PLL is always enabled (subject to oscillator requirements)

If PLLLEN in Configuration Words = 0:
1 = 4x PLL is enabled
0 = 4x PLL is disabled

**bit 6-3**  
IRCF<3:0>: Internal Oscillator Frequency Select bits

<table>
<thead>
<tr>
<th>Value</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>16 MHz HF or 32 MHz HF(2)</td>
</tr>
<tr>
<td>1110</td>
<td>8 MHz or 32 MHz HF(2)</td>
</tr>
<tr>
<td>1101</td>
<td>4 MHz HF</td>
</tr>
<tr>
<td>1100</td>
<td>2 MHz HF</td>
</tr>
<tr>
<td>1011</td>
<td>1 MHz HF</td>
</tr>
<tr>
<td>1010</td>
<td>500 kHz HF(1)</td>
</tr>
<tr>
<td>1001</td>
<td>250 kHz HF(1)</td>
</tr>
<tr>
<td>1000</td>
<td>125 kHz HF(1)</td>
</tr>
<tr>
<td>0111</td>
<td>500 kHz MF (default upon Reset)</td>
</tr>
<tr>
<td>0110</td>
<td>250 kHz MF</td>
</tr>
<tr>
<td>0101</td>
<td>125 kHz MF</td>
</tr>
<tr>
<td>0100</td>
<td>62.5 kHz MF</td>
</tr>
<tr>
<td>0011</td>
<td>31.25 kHz HF(1)</td>
</tr>
<tr>
<td>0010</td>
<td>31.25 kHz MF</td>
</tr>
<tr>
<td>000x</td>
<td>31 kHz LF</td>
</tr>
</tbody>
</table>

**bit 2**  
Unimplemented: Read as ‘0’

**bit 1-0**  
SCS<1:0>: System Clock Select bits

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1x</td>
<td>Internal oscillator block</td>
</tr>
<tr>
<td>01</td>
<td>Timer1 oscillator</td>
</tr>
<tr>
<td>00</td>
<td>Clock determined by FOSC&lt;2:0&gt; in Configuration Words.</td>
</tr>
</tbody>
</table>

**Note 1:** Duplicate frequency derived from HFINTOSC.

**Note 2:** 32 MHz when SPLLEN bit is set. Refer to Section 6.2.2.6 “32 MHz Internal Oscillator Frequency Selection”.
## REGISTER 6-2: OSCSTAT: OSCILLATOR STATUS REGISTER

<table>
<thead>
<tr>
<th>R-1/q</th>
<th>R-0/q</th>
<th>R-q/q</th>
<th>R-0/q</th>
<th>R-0/q</th>
<th>R-q/q</th>
<th>R-0/0</th>
<th>R-0/q</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1OSCR</td>
<td>PLLR</td>
<td>OSTS</td>
<td>HFIOFR</td>
<td>HFIOFL</td>
<td>MFIOFR</td>
<td>LFIOFR</td>
<td>HFIOFS</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **q** = Conditional

### bit 7: T1OSCR: Timer1 Oscillator Ready bit

- If T1OSCEN = 1:
  - 1 = Timer1 oscillator is ready
  - 0 = Timer1 oscillator is not ready
- If T1OSCEN = 0:
  - 1 = Timer1 clock source is always ready

### bit 6: PLLR 4x PLL Ready bit

- 1 = 4x PLL is ready
- 0 = 4x PLL is not ready

### bit 5: OSTS: Oscillator Start-up Timer Status bit

- 1 = Running from the clock defined by the FOSC<2:0> bits of the Configuration Words
- 0 = Running from an internal oscillator (FOSC<2:0> = 100)

### bit 4: HFIOFR: High-Frequency Internal Oscillator Ready bit

- 1 = HFINTOSC is ready
- 0 = HFINTOSC is not ready

### bit 3: HFIOFL: High-Frequency Internal Oscillator Locked bit

- 1 = HFINTOSC is at least 2% accurate
- 0 = HFINTOSC is not 2% accurate

### bit 2: MFIOFR: Medium-Frequency Internal Oscillator Ready bit

- 1 = MFINTOSC is ready
- 0 = MFINTOSC is not ready

### bit 1: LFIOFR: Low-Frequency Internal Oscillator Ready bit

- 1 = LFINTOSC is ready
- 0 = LFINTOSC is not ready

### bit 0: HFIOFS: High-Frequency Internal Oscillator Stable bit

- 1 = HFINTOSC is at least 0.5% accurate
- 0 = HFINTOSC is not 0.5% accurate
TABLE 6-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSCCON</td>
<td>SPLLEN</td>
<td>IRCF&lt;3:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>SCS&lt;1:0&gt;</td>
<td>82</td>
</tr>
<tr>
<td>OSCSTAT</td>
<td>T1OSCR</td>
<td>PLLR</td>
<td>OSTS</td>
<td>HFIOFR</td>
<td>HFIOFL</td>
<td>MFIOR</td>
<td>LFIOFR</td>
<td>HFIOFS</td>
<td>83</td>
</tr>
<tr>
<td>OSCTUNE</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TUN&lt;5:0&gt;</td>
<td>84</td>
</tr>
<tr>
<td>PIE2</td>
<td>OSFIE</td>
<td>C2IE</td>
<td>C1IE</td>
<td>EEIE</td>
<td>BCL1IE</td>
<td>C4IE</td>
<td>C3IE</td>
<td>CCP2IE</td>
<td>95</td>
</tr>
<tr>
<td>PIR2</td>
<td>OSFIF</td>
<td>C2IF</td>
<td>C1IF</td>
<td>EEIF</td>
<td>BCL1IF</td>
<td>C4IF</td>
<td>C3IF</td>
<td>CCP2IF</td>
<td>99</td>
</tr>
<tr>
<td>T1CON</td>
<td>TM1CS&lt;1:0&gt;</td>
<td>T1CKPS&lt;1:0&gt;</td>
<td>T1OSCEN</td>
<td>T1SYNC</td>
<td>—</td>
<td>TMR1ON</td>
<td>207</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

TABLE 6-3: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES

<table>
<thead>
<tr>
<th>Name</th>
<th>Bits</th>
<th>Bit -7</th>
<th>Bit -6</th>
<th>Bit 13/5</th>
<th>Bit 12/4</th>
<th>Bit 11/3</th>
<th>Bit 10/2</th>
<th>Bit 9/1</th>
<th>Bit 8/0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG1</td>
<td>13:8</td>
<td>—</td>
<td>—</td>
<td>FCMEN</td>
<td>IESO</td>
<td>CLKOUTEN</td>
<td>BOREN&lt;1:0&gt;</td>
<td>CPD</td>
<td>—</td>
<td>54</td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td>CP</td>
<td>MCLRE</td>
<td>PWRT</td>
<td>WDTE&lt;1:0&gt;</td>
<td>FOSC&lt;2:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

Legend: = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

Note 1: PIC16F1784/6/7 only.
7.0 REFERENCE CLOCK MODULE

The reference clock module provides the ability to send a divided clock to the clock output pin of the device (CLKR). This module is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application. The reference clock module includes the following features:

- System clock is the source
- Available in all oscillator configurations
- Programmable clock divider
- Output enable to a port pin
- Selectable duty cycle
- Slew rate control

The reference clock module is controlled by the CLKRCON register (Register 7-1) and is enabled when setting the CLKREN bit. To output the divided clock signal to the CLKR port pin, the CLKROE bit must be set. The CLKRDIV<2:0> bits enable the selection of eight different clock divider options. The CLKRDC<1:0> bits can be used to modify the duty cycle of the output clock(1). The CLKRSLR bit controls slew rate limiting.

7.1 Slew Rate

The slew rate limitation on the output port pin can be disabled. The slew rate limitation is removed by clearing the CLKRSLR bit in the CLKRCON register.

7.2 Effects of a Reset

Upon any device Reset, the reference clock module is disabled. The user’s firmware is responsible for initializing the module before enabling the output. The registers are reset to their default values.

7.3 Conflicts with the CLKR Pin

There are two cases when the reference clock output signal cannot be output to the CLKR pin, if:

- LP, XT or HS Oscillator mode is selected.
- CLKOUT function is enabled.

7.3.1 OSCILLATOR MODES

If LP, XT or HS oscillator modes are selected, the OSC2/CLKR pin must be used as an oscillator input pin and the CLKR output cannot be enabled. See Section 6.2 “Clock Source Types” for more information on different oscillator modes.

7.3.2 CLKOUT FUNCTION

The CLKOUT function has a higher priority than the reference clock module. Therefore, if the CLKOUT function is enabled by the CLKOUTEN bit in Configuration Words, Fosc/4 will always be output on the port pin. Reference Section 4.0 “Device Configuration” for more information.

7.4 Operation During Sleep

As the reference clock module relies on the system clock as its source, and the system clock is disabled in Sleep, the module does not function in Sleep, even if an external clock source or the Timer1 clock source is configured as the system clock. The module outputs will remain in their current state until the device exits Sleep.

Note 1: If the base clock rate is selected without a divider, the output clock will always have a duty cycle equal to that of the source clock, unless a 0% duty cycle is selected. If the clock divider is set to base clock/2, then 25% and 75% duty cycle accuracy will be dependent upon the source clock.
7.5 Register Definition: Reference Clock Control

REGISTER 7-1: CLKRCON: REFERENCE CLOCK CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKREN</td>
<td>CLKROE</td>
<td>CLKRSLR</td>
<td>CLKRDC&lt;1:0&gt;</td>
<td>CLKRDIV&lt;2:0&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'  
u = Bit is unchanged  
x = Bit is unknown  
'1' = Bit is set  
'0' = Bit is cleared

bit 7  
CLKREN: Reference Clock Module Enable bit  
1 = Reference clock module is enabled  
0 = Reference clock module is disabled

bit 6  
CLKROE: Reference Clock Output Enable bit  
1 = Reference clock output is enabled on CLKR pin  
0 = Reference clock output disabled on CLKR pin

bit 5  
CLKRSLR: Reference Clock Slew Rate Control Limiting Enable bit  
1 = Slew rate limiting is enabled  
0 = Slew rate limiting is disabled

bit 4-3  
CLKRDC<1:0>: Reference Clock Duty Cycle bits  
11 = Clock outputs duty cycle of 75%  
10 = Clock outputs duty cycle of 50%  
01 = Clock outputs duty cycle of 25%  
00 = Clock outputs duty cycle of 0%

bit 2-0  
CLKRDIV<2:0>: Reference Clock Divider bits  
111 = Base clock value divided by 128  
110 = Base clock value divided by 64  
101 = Base clock value divided by 32  
100 = Base clock value divided by 16  
011 = Base clock value divided by 8  
010 = Base clock value divided by 4  
001 = Base clock value divided by 2\(^{(1)}\)  
000 = Base clock value\(^{(2)}\)

Note 1: In this mode, the 25% and 75% duty cycle accuracy will be dependent on the source clock duty cycle.

2: In this mode, the duty cycle will always be equal to the source clock duty cycle, unless a duty cycle of 0% is selected.

3: To route CLKR to pin, CLKOUTEN of Configuration Words = 1 is required. CLKOUTEN of Configuration Words = 0 will result in Fosc/4. See Section 7.3 “Conflicts with the CLKR Pin” for details.
### TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH REFERENCE CLOCK SOURCES

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKRCON</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>86</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented locations read as ‘0’. Shaded cells are not used by reference clock sources.

### TABLE 7-2: SUMMARY OF CONFIGURATION WORD WITH REFERENCE CLOCK SOURCES

<table>
<thead>
<tr>
<th>Name</th>
<th>Bits</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 13/5</th>
<th>Bit 12/4</th>
<th>Bit 11/3</th>
<th>Bit 10/2</th>
<th>Bit 9/1</th>
<th>Bit 8/0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG1</td>
<td>13:8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>54</td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td>CP</td>
<td>MCLRE</td>
<td>PWRTE</td>
<td>WDTE1&lt;:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: — = unimplemented locations read as ‘0’. Shaded cells are not used by reference clock sources.
8.0 INTERRUPTS

The interrupt feature allows certain events to preempt normal program flow. Firmware is used to determine the source of the interrupt and act accordingly. Some interrupts can be configured to wake the MCU from Sleep mode.

This chapter contains the following information for Interrupts:

- Operation
- Interrupt Latency
- Interrupts During Sleep
- INT Pin
- Automatic Context Saving

Many peripherals produce interrupts. Refer to the corresponding chapters for details.

A block diagram of the interrupt logic is shown in Figure 8-1.

**FIGURE 8-1: INTERRUPT LOGIC**

![Diagram of interrupt logic](image)
8.1 Operation

Interrupts are disabled upon any device Reset. They are enabled by setting the following bits:

- GIE bit of the INTCON register
- Interrupt Enable bit(s) for the specific interrupt event(s)
- PEIE bit of the INTCON register (if the Interrupt Enable bit of the interrupt event is contained in the PIE1 or PIE2 registers)

The INTCON, PIR1 and PIR2 registers record individual interrupts via interrupt flag bits. Interrupt flag bits will be set, regardless of the status of the GIE, PEIE and individual interrupt enable bits.

The following events happen when an interrupt event occurs while the GIE bit is set:

- Current prefetched instruction is flushed
- GIE bit is cleared
- Current Program Counter (PC) is pushed onto the stack
- Critical registers are automatically saved to the shadow registers (See “Section 8.5 Automatic Context Saving”.)
- PC is loaded with the interrupt vector 0004h

The firmware within the Interrupt Service Routine (ISR) should determine the source of the interrupt by polling the interrupt flag bits. The interrupt flag bits must be cleared before exiting the ISR to avoid repeated interrupts. Because the GIE bit is cleared, any interrupt that occurs while executing the ISR will be recorded through its interrupt flag, but will not cause the processor to redirect to the interrupt vector.

The RETFIE instruction exits the ISR by popping the previous address from the stack, restoring the saved context from the shadow registers and setting the GIE bit.

For additional information on a specific interrupt's operation, refer to its peripheral chapter.

Note 1: Individual interrupt flag bits are set, regardless of the state of any other enable bits.

2: All interrupts will be ignored while the GIE bit is cleared. Any interrupt occurring while the GIE bit is clear will be serviced when the GIE bit is set again.

8.2 Interrupt Latency

Interrupt latency is defined as the time from when the interrupt event occurs to the time code execution at the interrupt vector begins. The latency for synchronous interrupts is three or four instruction cycles. For asynchronous interrupts, the latency is three to five instruction cycles, depending on when the interrupt occurs. See Figure 8-2 and Figure 8.3 for more details.
FIGURE 8-2: INTERRUPT LATENCY

OSC1

Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4

CLKR

Interrupt

GIE

PC

PC-1 PC PC+1 0004h 0005h

Execute

1 Cycle Instruction at PC

Inst(PC) NOP NOP Inst(0004h)

Interrupt

GIE

PC

PC-1 PC PC+1/FSR ADDR New PC/PC+1 0004h 0005h

Execute

2 Cycle Instruction at PC

Inst(PC) NOP NOP Inst(0004h)

Interrupt

GIE

PC

PC-1 PC FSR ADDR PC+1 PC+2 0004h 0005h

Execute

3 Cycle Instruction at PC

INST(PC) NOP NOP NOP Inst(0004h) Inst(0005h)

Interrupt

GIE

PC

PC-1 PC FSR ADDR PC+1 PC+2 0004h 0005h

Execute

3 Cycle Instruction at PC

INST(PC) NOP NOP NOP NOP Inst(0004h)
Figure 8-3: INT Pin Interrupt Timing

OSC1

CLKOUT

INT pin

INTF

GIE

INSTRUCTION FLOW

PC

Instruction Fetched

Instruction Executed

Note 1: INTF flag is sampled here (every Q1).

2: Asynchronous interrupt latency = 3-5 Tcy. Synchronous latency = 3-4 Tcy, where Tcy = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: CLKOUT not available in all oscillator modes.

4: For minimum width of INT pulse, refer to AC specifications in Section 30.0 "Electrical Specifications".

5: INTF is enabled to be set any time during the Q4-Q1 cycles.
8.3 Interrupts During Sleep

Some interrupts can be used to wake from Sleep. To wake from Sleep, the peripheral must be able to operate without the system clock. The interrupt source must have the appropriate Interrupt Enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the SLEEP instruction. The instruction directly after the SLEEP instruction will always be executed before branching to the ISR. Refer to Section 9.0 “Power-Down Mode (Sleep)” for more details.

8.4 INT Pin

The INT pin can be used to generate an asynchronous edge-triggered interrupt. This interrupt is enabled by setting the INTE bit of the INTCON register. The INTEDG bit of the OPTION_REG register determines on which edge the interrupt will occur. When the INTEDG bit is set, the rising edge will cause the interrupt. When the INTEDG bit is clear, the falling edge will cause the interrupt. The INTF bit of the INTCON register will be set when a valid edge appears on the INT pin. If the GIE and INTE bits are also set, the processor will redirect program execution to the interrupt vector.

8.5 Automatic Context Saving

Upon entering an interrupt, the return PC address is saved on the stack. Additionally, the following registers are automatically saved in the shadow registers:

- W register
- STATUS register (except for TO and PD)
- BSR register
- FSR registers
- PCLATH register

Upon exiting the Interrupt Service Routine, these registers are automatically restored. Any modifications to these registers during the ISR will be lost. If modifications to any of these registers are desired, the corresponding shadow register should be modified and the value will be restored when exiting the ISR. The shadow registers are available in Bank 31 and are readable and writable. Depending on the user’s application, other registers may also need to be saved.
8.6 Register Definitions: Interrupt Control

REGISTER 8-1: INTCON: INTERRUPT CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R-0/0</th>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF(1)</td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GIE: Global Interrupt Enable bit</td>
<td>1 = Enables all active interrupts</td>
<td>0 = Disables all interrupts</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 6</td>
<td>PEIE: Peripheral Interrupt Enable bit</td>
<td>1 = Enables all active peripheral interrupts</td>
<td>0 = Disables all peripheral interrupts</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 5</td>
<td>TMR0IE: Timer0 Overflow Interrupt Enable bit</td>
<td>1 = Enables the Timer0 interrupt</td>
<td>0 = Disables the Timer0 interrupt</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 4</td>
<td>INTE: INT External Interrupt Enable bit</td>
<td>1 = Enables the INT external interrupt</td>
<td>0 = Disables the INT external interrupt</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 3</td>
<td>IOCIE: Interrupt-on-Change Enable bit</td>
<td>1 = Enables the interrupt-on-change</td>
<td>0 = Disables the interrupt-on-change</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 2</td>
<td>TMR0IF: Timer0 Overflow Interrupt Flag bit</td>
<td>1 = TMR0 register has overflowed</td>
<td>0 = TMR0 register did not overflow</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 1</td>
<td>INTF: INT External Interrupt Flag bit</td>
<td>1 = The INT external interrupt occurred</td>
<td>0 = The INT external interrupt did not occur</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 0</td>
<td>IOCIF: Interrupt-on-Change Interrupt Flag bit(1)</td>
<td>1 = When at least one of the interrupt-on-change pins changed state</td>
<td>0 = None of the interrupt-on-change pins have changed state</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

Note 1: The IOCIF Flag bit is read-only and cleared when all the Interrupt-on-change flags in the IOCBF register have been cleared by software.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.
## REGISTER 8-2: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>TMR1GIE</td>
<td>Timer1 Gate Interrupt Enable bit</td>
</tr>
<tr>
<td>6</td>
<td>ADIE</td>
<td>Analog-to-Digital Converter (ADC) Interrupt Enable bit</td>
</tr>
<tr>
<td>5</td>
<td>RCIE</td>
<td>EUSART Receive Interrupt Enable bit</td>
</tr>
<tr>
<td>4</td>
<td>TXIE</td>
<td>EUSART Transmit Interrupt Enable bit</td>
</tr>
<tr>
<td>3</td>
<td>SSP1IE</td>
<td>Synchronous Serial Port (MSSP) Interrupt Enable bit</td>
</tr>
<tr>
<td>2</td>
<td>CCP1IE</td>
<td>CCP1 Interrupt Enable bit</td>
</tr>
<tr>
<td>1</td>
<td>TMR2IE</td>
<td>TMR2 to PR2 Match Interrupt Enable bit</td>
</tr>
<tr>
<td>0</td>
<td>TMR1IE</td>
<td>Timer1 Overflow Interrupt Enable bit</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets

- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

### Bit Descriptions:
- **bit 7** TMR1GIE: Timer1 Gate Interrupt Enable bit
  - 1 = Enables the Timer1 gate acquisition interrupt
  - 0 = Disables the Timer1 gate acquisition interrupt
- **bit 6** ADIE: Analog-to-Digital Converter (ADC) Interrupt Enable bit
  - 1 = Enables the ADC interrupt
  - 0 = Disables the ADC interrupt
- **bit 5** RCIE: EUSART Receive Interrupt Enable bit
  - 1 = Enables the EUSART receive interrupt
  - 0 = Disables the EUSART receive interrupt
- **bit 4** TXIE: EUSART Transmit Interrupt Enable bit
  - 1 = Enables the EUSART transmit interrupt
  - 0 = Disables the EUSART transmit interrupt
- **bit 3** SSP1IE: Synchronous Serial Port (MSSP) Interrupt Enable bit
  - 1 = Enables the MSSP interrupt
  - 0 = Disables the MSSP interrupt
- **bit 2** CCP1IE: CCP1 Interrupt Enable bit
  - 1 = Enables the CCP1 interrupt
  - 0 = Disables the CCP1 interrupt
- **bit 1** TMR2IE: TMR2 to PR2 Match Interrupt Enable bit
  - 1 = Enables the Timer2 to PR2 match interrupt
  - 0 = Disables the Timer2 to PR2 match interrupt
- **bit 0** TMR1IE: Timer1 Overflow Interrupt Enable bit
  - 1 = Enables the Timer1 overflow interrupt
  - 0 = Disables the Timer1 overflow interrupt

### Note:
Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.
### REGISTER 8-3: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>OSFIE</td>
<td>Oscillator Fail Interrupt Enable bit</td>
</tr>
<tr>
<td>6</td>
<td>C2IE</td>
<td>Comparator C2 Interrupt Enable bit</td>
</tr>
<tr>
<td>5</td>
<td>C1IE</td>
<td>Comparator C1 Interrupt Enable bit</td>
</tr>
<tr>
<td>4</td>
<td>EEIE</td>
<td>EEPROM Write Completion Interrupt Enable bit</td>
</tr>
<tr>
<td>3</td>
<td>BCL1IE</td>
<td>MSSP Bus Collision Interrupt Enable bit</td>
</tr>
<tr>
<td>2</td>
<td>C4IE</td>
<td>Comparator C4 Interrupt Enable bit</td>
</tr>
<tr>
<td>1</td>
<td>C3IE</td>
<td>Comparator C3 Interrupt Enable bit</td>
</tr>
<tr>
<td>0</td>
<td>CCP2IE</td>
<td>CCP2 Interrupt Enable bit</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **‘0’** = Bit is cleared

**Note:** Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.
**REGISTER 8-4: PIE3: PERIPHERAL INTERRUPT ENABLE REGISTER 3**

<table>
<thead>
<tr>
<th></th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7-5</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CCP3IE</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

- **bit 7-5** Unimplemented: Read as ‘0’
- **bit 4** CCP3IE: CCP3 Interrupt Enable bit
  - 1 = Enables the CCP3 interrupt
  - 0 = Disables the CCP3 interrupt
- **bit 3-0** Unimplemented: Read as ‘0’
## REGISTER 8-5: PIE4: PERIPHERAL INTERRUPT ENABLE REGISTER 4

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PSMC3TIE</td>
<td>PSMC2TIE</td>
<td>PSMC1TIE</td>
<td></td>
<td>PSMC3SIE</td>
<td>PSMC2SIE</td>
<td>PSMC1SIE</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

<table>
<thead>
<tr>
<th>bit 7</th>
<th>Unimplemented: Read as ‘0’</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 6</td>
<td><strong>PSMC3TIE</strong>: PSMC3 Time Base Interrupt Enable bit</td>
</tr>
<tr>
<td></td>
<td>1 = Enables PSMC3 time base generated interrupts</td>
</tr>
<tr>
<td></td>
<td>0 = Disables PSMC3 time base generated interrupts</td>
</tr>
<tr>
<td>bit 5</td>
<td><strong>PSMC2TIE</strong>: PSMC2 Time Base Interrupt Enable bit</td>
</tr>
<tr>
<td></td>
<td>1 = Enables PSMC2 time base generated interrupts</td>
</tr>
<tr>
<td></td>
<td>0 = Disables PSMC2 time base generated interrupts</td>
</tr>
<tr>
<td>bit 4</td>
<td><strong>PSMC1TIE</strong>: PSMC1 Time Base Interrupt Enable bit</td>
</tr>
<tr>
<td></td>
<td>1 = Enables PSMC1 time base generated interrupts</td>
</tr>
<tr>
<td></td>
<td>0 = Disables PSMC1 time base generated interrupts</td>
</tr>
<tr>
<td>bit 3</td>
<td>Unimplemented: Read as ‘0’</td>
</tr>
<tr>
<td>bit 2</td>
<td><strong>PSMC3SIE</strong>: PSMC3 Auto-Shutdown Interrupt Enable bit</td>
</tr>
<tr>
<td></td>
<td>1 = Enables PSMC3 auto-shutdown interrupts</td>
</tr>
<tr>
<td></td>
<td>0 = Disables PSMC3 auto-shutdown interrupts</td>
</tr>
<tr>
<td>bit 1</td>
<td><strong>PSMC2SIE</strong>: PSMC2 Auto-Shutdown Interrupt Enable bit</td>
</tr>
<tr>
<td></td>
<td>1 = Enables PSMC2 auto-shutdown interrupts</td>
</tr>
<tr>
<td></td>
<td>0 = Disables PSMC2 auto-shutdown interrupts</td>
</tr>
<tr>
<td>bit 0</td>
<td><strong>PSMC1SIE</strong>: PSMC1 Auto-Shutdown Interrupt Enable bit</td>
</tr>
<tr>
<td></td>
<td>1 = Enables PSMC1 auto-shutdown interrupts</td>
</tr>
<tr>
<td></td>
<td>0 = Disables PSMC1 auto-shutdown interrupts</td>
</tr>
</tbody>
</table>

### Note:
- Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.
REGISTER 8-6: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R-0/0</th>
<th>R-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMR1GIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1IF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

- **bit 7** TMR1GIF: Timer1 Gate Interrupt Flag bit
  - 1 = Interrupt is pending
  - 0 = Interrupt is not pending

- **bit 6** ADIF: ADC Converter Interrupt Flag bit
  - 1 = Interrupt is pending
  - 0 = Interrupt is not pending

- **bit 5** RCIF: EUSART Receive Interrupt Flag bit
  - 1 = Interrupt is pending
  - 0 = Interrupt is not pending

- **bit 4** TXIF: EUSART Transmit Interrupt Flag bit
  - 1 = Interrupt is pending
  - 0 = Interrupt is not pending

- **bit 3** SSP1IF: Synchronous Serial Port (MSSP) Interrupt Flag bit
  - 1 = Interrupt is pending
  - 0 = Interrupt is not pending

- **bit 2** CCP1IF: CCP1 Interrupt Flag bit
  - 1 = Interrupt is pending
  - 0 = Interrupt is not pending

- **bit 1** TMR2IF: Timer2 to PR2 Interrupt Flag bit
  - 1 = Interrupt is pending
  - 0 = Interrupt is not pending

- **bit 0** TMR1IF: Timer1 Overflow Interrupt Flag bit
  - 1 = Interrupt is pending
  - 0 = Interrupt is not pending

**Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.
REGISTER 8-7:  PIR2: PERIPHERAL INTERRUPT REQUEST REGISTER 2

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSFIF</td>
<td>C2IF</td>
<td>C1IF</td>
<td>EEIF</td>
<td>BCL1IF</td>
<td>C4IF</td>
<td>C3IF</td>
<td>CCP2IF</td>
</tr>
</tbody>
</table>

bit 7         OSFIF: Oscillator Fail Interrupt Flag bit
                1 = Interrupt is pending
                0 = Interrupt is not pending

bit 6         C2IF: Comparator C2 Interrupt Flag bit
                1 = Interrupt is pending
                0 = Interrupt is not pending

bit 5         C1IF: Comparator C1 Interrupt Flag bit
                1 = Interrupt is pending
                0 = Interrupt is not pending

bit 4         EEIF: EEPROM Write Completion Interrupt Flag bit
                1 = Interrupt is pending
                0 = Interrupt is not pending

bit 3         BCL1IF: MSSP Bus Collision Interrupt Flag bit
                1 = Interrupt is pending
                0 = Interrupt is not pending

bit 2         C4IF: Comparator C4 Interrupt Flag bit
                1 = Interrupt is pending
                0 = Interrupt is not pending

bit 1         C3IF: Comparator C3 Interrupt Flag bit
                1 = Interrupt is pending
                0 = Interrupt is not pending

bit 0         CCP2IF: CCP2 Interrupt Flag bit
                1 = Interrupt is pending
                0 = Interrupt is not pending

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are cleared prior to enabling an interrupt.
REGISTER 8-8: PIR3: PERIPHERAL INTERRUPT REQUEST REGISTER 3

<table>
<thead>
<tr>
<th>bit 7-5</th>
<th>bit 4</th>
<th>bit 3-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>U-0</td>
<td>R/W-0/0</td>
<td>U-0</td>
</tr>
<tr>
<td>CCP3IF</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>CCP3IF</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

**bit 7-5 Unimplemented**: Read as ‘0’

**bit 4 CCP3IF**: CCP3 Interrupt Flag bit
- **1** = Interrupt is pending
- **0** = Interrupt is not pending

**bit 3-0 Unimplemented**: Read as ‘0’
REGISTER 8-9:  PIR4: PERIPHERAL INTERRUPT REQUEST REGISTER 4

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>U-0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>—</td>
<td>PSMC3TIF</td>
<td>PSMC2TIF</td>
<td>PSMC1TIF</td>
<td>—</td>
<td>PSMC3SIF</td>
<td>PSMC2SIF</td>
<td>PSMC1SIF</td>
</tr>
</tbody>
</table>

**Legend:**

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**Legend:**

- PSMC3TIF: PSMC3 Time Base Interrupt Flag bit
- PSMC2TIF: PSMC2 Time Base Interrupt Flag bit
- PSMC1TIF: PSMC1 Time Base Interrupt Flag bit
- PSMC3SIF: PSMC3 Auto-shutdown Flag bit
- PSMC2SIF: PSMC2 Auto-shutdown Flag bit
- PSMC1SIF: PSMC1 Auto-shutdown Flag bit

**Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.
### TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCN</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>93</td>
</tr>
<tr>
<td>OPTION_REG</td>
<td>WPUEN</td>
<td>INTEDG</td>
<td>TMR0CS</td>
<td>TMR0SE</td>
<td>PSA</td>
<td>PS&lt;2:0&gt;</td>
<td></td>
<td></td>
<td>198</td>
</tr>
<tr>
<td>PIE1</td>
<td>TMR1GIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSP1IE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>94</td>
</tr>
<tr>
<td>PIE2</td>
<td>OSFIE</td>
<td>C2IE</td>
<td>C1IE</td>
<td>EEIE</td>
<td>BCL1IE</td>
<td>C4IE</td>
<td>C3IE</td>
<td>CCP2IE</td>
<td>95</td>
</tr>
<tr>
<td>PIE3</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CCP3IE</td>
<td>96</td>
</tr>
<tr>
<td>PIE4</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>97</td>
</tr>
<tr>
<td>PIR1</td>
<td>TMR1GIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1IF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>98</td>
</tr>
<tr>
<td>PIR2</td>
<td>OSFIF</td>
<td>C2IF</td>
<td>C1IF</td>
<td>EEIF</td>
<td>BCL1IF</td>
<td>C4IF</td>
<td>C3IF</td>
<td>CCP2IF</td>
<td>99</td>
</tr>
<tr>
<td>PIR3</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CCP3IF</td>
<td>100</td>
</tr>
<tr>
<td>PIR4</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>101</td>
</tr>
</tbody>
</table>

**Legend:**
- = unimplemented location, read as "0". Shaded cells are not used by interrupts.
9.0 POWER-DOWN MODE (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction.

Upon entering Sleep mode, the following conditions exist:

1. WDT will be cleared but keeps running, if enabled for operation during Sleep.
2. PD bit of the STATUS register is cleared.
3. TO bit of the STATUS register is set.
4. CPU clock is disabled.
5. 31 kHz LFINTOSC is unaffected and peripherals that operate from it may continue operation in Sleep.
6. Timer1 and peripherals that operate from Timer1 continue operation in Sleep when the Timer1 clock source selected is:
   • LFINTOSC
   • T1CKI
   • Timer1 oscillator
7. ADC is unaffected, if the dedicated FRC oscillator is selected.
8. I/O ports maintain the status they had before SLEEP was executed (driving high, low or high-impedance).
9. Resets other than WDT are not affected by Sleep mode.

Refer to individual chapters for more details on peripheral operation during Sleep.

To minimize current consumption, the following conditions should be considered:

- I/O pins should not be floating
- External circuitry sinking current from I/O pins
- Internal circuitry sourcing current from I/O pins
- Current draw from pins with internal weak pull-ups
- Modules using 31 kHz LFINTOSC
- Modules using Timer1 oscillator

I/O pins that are high-impedance inputs should be pulled to VDD or VSS externally to avoid switching currents caused by floating inputs.

Examples of internal circuitry that might be sourcing current include modules such as the DAC and FVR modules. See Section 19.0 “Digital-to-Analog Converter (DAC) Module” and Section 15.0 “Fixed Voltage Reference (FVR)” for more information on these modules.

9.1 Wake-up from Sleep

The device can wake-up from Sleep through one of the following events:

1. External Reset input on MCLR pin, if enabled
2. BOR Reset, if enabled
3. POR Reset
4. Watchdog Timer, if enabled
5. Any external interrupt
6. Interrupts by peripherals capable of running during Sleep (see individual peripheral for more information)

The first three events will cause a device Reset. The last three events are considered a continuation of program execution. To determine whether a deviceReset or wake-up event occurred, refer to Section 5.12 “Determining the Cause of a Reset”.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be enabled. Wake-up will occur regardless of the state of the GIE bit. If the GIE bit is disabled, the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is enabled, the device executes the instruction after the SLEEP instruction, the device will then call the Interrupt Service Routine. In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

The WDT is cleared when the device wakes up from Sleep, regardless of the source of wake-up.
9.1.1 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction:
  - SLEEP instruction will execute as a NOP.
  - WDT and WDT prescaler will not be cleared.
  - TO bit of the STATUS register will not be set.
  - PD bit of the STATUS register will not be cleared.

- If the interrupt occurs **during or after** the execution of a SLEEP instruction:
  - SLEEP instruction will be completely executed.
  - Device will immediately wake-up from Sleep.
  - WDT and WDT prescaler will be cleared.
  - TO bit of the STATUS register will be set.
  - PD bit of the STATUS register will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the PD bit. If the PD bit is set, the SLEEP instruction was executed as a NOP.

**FIGURE 9-1: WAKE-UP FROM SLEEP THROUGH INTERRUPT**

<table>
<thead>
<tr>
<th>Inst(PC) = Sleep*</th>
<th>Inst(PC - 1)</th>
<th>Inst(PC + 1)</th>
<th>Inst(PC + 2)</th>
<th>Inst(0004h)</th>
<th>Inst(0005h)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC</td>
<td>PC + 1</td>
<td>PC + 2</td>
<td>PC + 2</td>
<td>0004h</td>
<td>0005h</td>
</tr>
</tbody>
</table>

**Note**

1: External clock. High, Medium, Low mode assumed.
2: CLKOUT is shown here for timing reference.
3: Tosc; See Section 30.0 “Electrical Specifications”.
4: GIE = 1 assumed. In this case after wake-up, the processor calls the ISR at 0004h. If GIE = 0, execution will continue in-line.
9.2 Low-Power Sleep Mode

"F" devices contain an internal Low Dropout (LDO) voltage regulator, which allows the device I/O pins to operate at voltages up to 5.5V while the internal device logic operates at a lower voltage. The LDO and its associated reference circuitry must remain active when the device is in Sleep mode. "F" devices allow the user to optimize the operating current in Sleep, depending on the application requirements.

A Low-Power Sleep mode can be selected by setting the VREGPM bit of the VREGCON register. With this bit set, the LDO and reference circuitry are placed in a low-power state when the device is in Sleep.

9.2.1 SLEEP CURRENT VS. WAKE-UP TIME

In the default operating mode, the LDO and reference circuitry remain in the normal configuration while in Sleep. The device is able to exit Sleep mode quickly since all circuits remain active. In Low-Power Sleep mode, when waking up from Sleep, an extra delay time is required for these circuits to return to the normal configuration and stabilize.

The Low-Power Sleep mode is beneficial for applications that stay in Sleep mode for long periods of time. The normal mode is beneficial for applications that need to wake from Sleep quickly and frequently.

9.2.2 PERIPHERAL USAGE IN SLEEP

Some peripherals that can operate in Sleep mode will not operate properly with the Low-Power Sleep mode selected. The LDO will remain in the normal power mode when those peripherals are enabled. The Low-Power Sleep mode is intended for use with these peripherals:

- Brown-Out Reset (BOR)
- Watchdog Timer (WDT)
- External interrupt pin/Interrupt-on-change pins
- Timer1 (with external clock source)

Note: "LF" devices do not have a configurable Low-Power Sleep mode. "LF" devices are an unregulated device and are always in the lowest power state when in Sleep, with no wake-up time penalty. These devices have a lower maximum Vdd and I/O voltage than "F" devices. See Section 30.0 “Electrical Specifications” for more information.
9.3 Register Definitions: Voltage Regulator Control

REGISTER 9-1: VREGCON: VOLTAGE REGULATOR CONTROL REGISTER(1)

| Bit 7-2 | Unimplemented: Read as ‘0’ |
| Bit 1  | VREGPM: Voltage Regulator Power Mode Selection bit |
|        | 1 = Low-Power Sleep mode enabled in Sleep(2) |
|        | Draws lowest current in Sleep, slower wake-up |
|        | 0 = Normal-Power mode enabled in Sleep(2) |
|        | Draws higher current in Sleep, faster wake-up |
| Bit 0  | Reserved: Read as ‘1’. Maintain this bit set. |

Note 1: “F” devices only.
2: See Section 30.0 “Electrical Specifications”.

TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMROIE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>RAIF</td>
<td>93</td>
</tr>
<tr>
<td>IOCBF</td>
<td>IOCBI</td>
<td>IOCBI</td>
<td>IOCBI</td>
<td>IOCBI</td>
<td>IOCBI</td>
<td>IOCBI</td>
<td>IOCBI</td>
<td>IOCBI</td>
<td>159</td>
</tr>
<tr>
<td>IOCBN</td>
<td>IOCBN</td>
<td>IOCBN</td>
<td>IOCBN</td>
<td>IOCBN</td>
<td>IOCBN</td>
<td>IOCBN</td>
<td>IOCBN</td>
<td>IOCBN</td>
<td>158</td>
</tr>
<tr>
<td>IOCBP</td>
<td>IOCBP</td>
<td>IOCBP</td>
<td>IOCBP</td>
<td>IOCBP</td>
<td>IOCBP</td>
<td>IOCBP</td>
<td>IOCBP</td>
<td>IOCBP</td>
<td>158</td>
</tr>
<tr>
<td>PIE1</td>
<td>TMR1GIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSP1IE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>94</td>
</tr>
<tr>
<td>PIE2</td>
<td>OSFIE</td>
<td>C2IE</td>
<td>C1IE</td>
<td>EEIE</td>
<td>BCL1IE</td>
<td>C4IE</td>
<td>C3IE</td>
<td>CCP2IE</td>
<td>95</td>
</tr>
<tr>
<td>PIE3</td>
<td></td>
<td>C2IE</td>
<td>C1IE</td>
<td>EEIE</td>
<td>BCL1IE</td>
<td>C4IE</td>
<td>C3IE</td>
<td>CCP2IE</td>
<td>95</td>
</tr>
<tr>
<td>PIE4</td>
<td></td>
<td>PSMC3TIE</td>
<td>PSMC2TIE</td>
<td>PSMC1TIE</td>
<td>PSMC3TIE</td>
<td>PSMC2TIE</td>
<td>PSMC1TIE</td>
<td>97</td>
<td></td>
</tr>
<tr>
<td>PIR1</td>
<td>TMR1GIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1IF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>94</td>
</tr>
<tr>
<td>PIR2</td>
<td>OSFIF</td>
<td>C2IF</td>
<td>C1IF</td>
<td>EEIF</td>
<td>BCL1IF</td>
<td>C4IF</td>
<td>C3IF</td>
<td>CCP2IF</td>
<td>99</td>
</tr>
<tr>
<td>PIR3</td>
<td></td>
<td></td>
<td>C1IF</td>
<td>EEIF</td>
<td>BCL1IF</td>
<td>C4IF</td>
<td>C3IF</td>
<td>CCP2IF</td>
<td>99</td>
</tr>
<tr>
<td>PIR4</td>
<td></td>
<td>PSMC3TIF</td>
<td>PSMC2TIF</td>
<td>PSMC1TIF</td>
<td>PSMC3TIF</td>
<td>PSMC2TIF</td>
<td>PSMC1TIF</td>
<td>101</td>
<td></td>
</tr>
<tr>
<td>STATUS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TO</td>
<td>PD</td>
<td>Z</td>
<td>DC</td>
<td>27</td>
</tr>
<tr>
<td>VREGCON</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VREGPM</td>
<td></td>
<td>106</td>
</tr>
<tr>
<td>WDTCON</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>WDTPS&lt;4:0&gt;</td>
<td></td>
<td>SWDTEN</td>
<td>110</td>
<td></td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used in Power-Down mode.
10.0 LOW DROPOUT (LDO) VOLTAGE REGULATOR

The "F" devices have an internal Low Dropout Regulator (LDO) which provide operation above 3.6V. The LDO regulates a voltage for the internal device logic while permitting the VDD and I/O pins to operate at a higher voltage. There is no user enable/disable control available for the LDO, it is always active. The "LF" devices operate at a maximum VDD of 3.6V and does not incorporate an LDO.

A device I/O pin may be configured as the LDO voltage output, identified as the VCAP pin. Although not required, an external low-ESR capacitor may be connected to the VCAP pin for additional regulator stability.

The VCAPEN bit of Configuration Words determines if which pin is assigned as the VCAP pin. Refer to Table 10-1.

### TABLE 10-1: VCAPEN SELECT BIT

<table>
<thead>
<tr>
<th>VCAPEN</th>
<th>Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>No VCAP</td>
</tr>
<tr>
<td>0</td>
<td>RA6</td>
</tr>
</tbody>
</table>

### TABLE 10-2: SUMMARY OF CONFIGURATION WORD WITH LDO

<table>
<thead>
<tr>
<th>Name</th>
<th>Bits</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 13/5</th>
<th>Bit 12/4</th>
<th>Bit 11/3</th>
<th>Bit 10/2</th>
<th>Bit 9/1</th>
<th>Bit 8/0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG2</td>
<td>13:8</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>LVP</td>
<td>DEBUG</td>
<td>LPBOR</td>
<td>BORV</td>
<td>STVREN</td>
<td>PLLEN</td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td>—</td>
<td>—</td>
<td>VCAPEN(1)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WRT&lt;1:0&gt;</td>
<td>56</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented locations read as ‘0’. Shaded cells are not used by LDO.

Note 1: “F” devices only.

On power-up, the external capacitor will load the LDO voltage regulator. To prevent erroneous operation, the device is held in Reset while a constant current source charges the external capacitor. After the cap is fully charged, the device is released from Reset. For more information on the constant current rate, refer to the LDO Regulator Characteristics Table in Section 30.0 “Electrical Specifications”.

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11.0 WATCHDOG TIMER (WDT)

The Watchdog Timer is a system timer that generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events.

The WDT has the following features:

- Independent clock source
- Multiple operating modes
  - WDT is always on
  - WDT is off when in Sleep
  - WDT is controlled by software
  - WDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (nominal)
- Multiple Reset conditions
- Operation during Sleep

FIGURE 11-1: WATCHDOG TIMER BLOCK DIAGRAM
11.1 Independent Clock Source

The WDT derives its time base from the 31 kHz LFINTOSC internal oscillator. Time intervals in this chapter are based on a nominal interval of 1 ms. See Section 30.0 “Electrical Specifications” for the LFINTOSC tolerances.

11.2 WDT Operating Modes

The Watchdog Timer module has four operating modes controlled by the WDTE<1:0> bits in Configuration Words. See Table 11-1.

11.2.1 WDT IS ALWAYS ON

When the WDTE bits of Configuration Words are set to ‘11’, the WDT is always on.
WDT protection is active during Sleep.

11.2.2 WDT IS OFF IN SLEEP

When the WDTE bits of Configuration Words are set to ‘10’, the WDT is on, except in Sleep.
WDT protection is not active during Sleep.

11.2.3 WDT CONTROLLED BY SOFTWARE

When the WDTE bits of Configuration Words are set to ‘01’, the WDT is controlled by the SWDTEN bit of the WDTCON register.
WDT protection is unchanged by Sleep. See Table 11-1 for more details.

<table>
<thead>
<tr>
<th>WDTE&lt;1:0&gt;</th>
<th>SWDTEN</th>
<th>Device Mode</th>
<th>WDT Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>X</td>
<td>X</td>
<td>Active</td>
</tr>
<tr>
<td>10</td>
<td>X</td>
<td>Awake</td>
<td>Active</td>
</tr>
<tr>
<td>01</td>
<td>1</td>
<td>Sleep</td>
<td>Disabled</td>
</tr>
<tr>
<td>00</td>
<td>X</td>
<td>X</td>
<td>Disabled</td>
</tr>
</tbody>
</table>

TABLE 11-2: WDT CLEARING CONDITIONS

<table>
<thead>
<tr>
<th>Conditions</th>
<th>WDT</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDTE&lt;1:0&gt; = 00</td>
<td>Cleared</td>
</tr>
<tr>
<td>WDTE&lt;1:0&gt; = 01 and SWDTEN = 0</td>
<td>Cleared until the end of OST</td>
</tr>
<tr>
<td>WDTE&lt;1:0&gt; = 10 and enter Sleep</td>
<td>Unaffected</td>
</tr>
<tr>
<td>CLRWDT Command</td>
<td>Cleared</td>
</tr>
<tr>
<td>Oscillator Fail Detected</td>
<td>Cleared</td>
</tr>
<tr>
<td>Exit Sleep + System Clock = T1OSC, EXTRC, INTOSC, EXTCLK</td>
<td>Cleared</td>
</tr>
<tr>
<td>Exit Sleep + System Clock = XT, HS, LP</td>
<td>Unaffected</td>
</tr>
<tr>
<td>Change INTOSC divider (IRCF bits)</td>
<td>Unaffected</td>
</tr>
</tbody>
</table>

11.3 Time-Out Period

The WDTPS bits of the WDTCON register set the time-out period from 1 ms to 256 seconds (nominal). After a Reset, the default time-out period is two seconds.

11.4 Clearing the WDT

The WDT is cleared when any of the following conditions occur:
- Any Reset
- CLRWDT instruction is executed
- Device enters Sleep
- Device wakes up from Sleep
- Oscillator fail
- WDT is disabled
- Oscillator Start-up Timer (OST) is running

See Table 11-2 for more information.

11.5 Operation During Sleep

When the device enters Sleep, the WDT is cleared. If the WDT is enabled during Sleep, the WDT resumes counting.

When the device exits Sleep, the WDT is cleared again. The WDT remains clear until the OST, if enabled, completes. See Section 6.0 “Oscillator Module (with Fail-Safe Clock Monitor)” for more information on the OST.

When a WDT time-out occurs while the device is in Sleep, no Reset is generated. Instead, the device wakes up and resumes operation. The TO and PD bits in the STATUS register are changed to indicate the event. See Section 3.0 “Memory Organization” and Status Register (Register 3-1) for more information.
11.6 Register Definitions: Watchdog Control

REGISTER 11-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-1/1</th>
<th>R/W-0/0</th>
<th>R/W-1/1</th>
<th>R/W-0/0</th>
<th>SWDTEN</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>WDTPS&lt;4:0&gt;</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

bit 7-6 Unimplemented: Read as ‘0’
bit 5-1 WDTPS<4:0>: Watchdog Timer Period Select bits\(^{(1)}\)

<table>
<thead>
<tr>
<th>Bit Value</th>
<th>Prescale Rate</th>
<th>Interval (nominal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>11111</td>
<td>Reserved</td>
<td>Results in minimum interval (1:32)</td>
</tr>
<tr>
<td>10011</td>
<td>1:262144</td>
<td>(Interval 2s nominal)</td>
</tr>
<tr>
<td>10010</td>
<td>1:131072</td>
<td>(Interval 4s nominal)</td>
</tr>
<tr>
<td>10001</td>
<td>1:65536</td>
<td>(Interval 2s nominal)</td>
</tr>
<tr>
<td>10000</td>
<td>1:32768</td>
<td>(Interval 1s nominal)</td>
</tr>
<tr>
<td>01101</td>
<td>1:16384</td>
<td>(Interval 512 ms nominal)</td>
</tr>
<tr>
<td>01100</td>
<td>1:8192</td>
<td>(Interval 256 ms nominal)</td>
</tr>
<tr>
<td>01111</td>
<td>1:4096</td>
<td>(Interval 128 ms nominal)</td>
</tr>
<tr>
<td>01110</td>
<td>1:2048</td>
<td>(Interval 64 ms nominal)</td>
</tr>
<tr>
<td>01101</td>
<td>1:1024</td>
<td>(Interval 32 ms nominal)</td>
</tr>
<tr>
<td>01100</td>
<td>1:512</td>
<td>(Interval 16 ms nominal)</td>
</tr>
<tr>
<td>01011</td>
<td>1:256</td>
<td>(Interval 8 ms nominal)</td>
</tr>
<tr>
<td>01100</td>
<td>1:128</td>
<td>(Interval 4 ms nominal)</td>
</tr>
<tr>
<td>01001</td>
<td>1:64</td>
<td>(Interval 2 ms nominal)</td>
</tr>
<tr>
<td>00111</td>
<td>1:32</td>
<td>(Interval 1 ms nominal)</td>
</tr>
</tbody>
</table>

bit 0 SWDTEN: Software Enable/Disable for Watchdog Timer bit

- If WDTE<1:0> = 1x:
  - This bit is ignored.
- If WDTE<1:0> = 01:
  - 1 = WDT is turned on
  - 0 = WDT is turned off
- If WDTE<1:0> = 00:
  - This bit is ignored.

**Note 1:** Times are approximate. WDT time is based on 31 kHz LFINTOSC.
TABLE 11-3: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSCCON</td>
<td>SPLLEN</td>
<td>IRCF&lt;3:0&gt;</td>
<td>—</td>
<td>—</td>
<td>SCS&lt;1:0&gt;</td>
<td>82</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>STATUS</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TO</td>
<td>PD</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
<td>27</td>
</tr>
<tr>
<td>WDTCON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WDTPS&lt;4:0&gt;</td>
<td>SWDTEN</td>
<td>110</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: × = unknown, u = unchanged, – = unimplemented locations read as ‘0’. Shaded cells are not used by Watchdog Timer.

TABLE 11-4: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER

<table>
<thead>
<tr>
<th>Name</th>
<th>Bits</th>
<th>Bit -/7</th>
<th>Bit -/6</th>
<th>Bit 13/5</th>
<th>Bit 12/4</th>
<th>Bit 11/3</th>
<th>Bit 10/2</th>
<th>Bit 9/1</th>
<th>Bit 8/0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG1</td>
<td>13:8</td>
<td>—</td>
<td>—</td>
<td>FCMEN</td>
<td>IESO</td>
<td>CLKOUTEN</td>
<td>BOREN&lt;1:0&gt;</td>
<td>CPD</td>
<td>54</td>
<td></td>
</tr>
<tr>
<td>7:0</td>
<td>CP</td>
<td>MCLRE</td>
<td>PWRT</td>
<td>WDTE&lt;1:0&gt;</td>
<td>FOSC&lt;2:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by Watchdog Timer.
12.0 DATA EEPROM AND FLASH PROGRAM MEMORY CONTROL

The data EEPROM and Flash program memory are readable and writable during normal operation (full VDD range). These memories are not directly mapped in the register file space. Instead, they are indirectly addressed through the Special Function Registers (SFRs). There are six SFRs used to access these memories:

- EECON1
- EECON2
- EEDATL
- EEDATH
- EEADRL
- EEADRH

When interfacing the data memory block, EEDATL holds the 8-bit data for read/write, and EEADRL holds the address of the EEDATL location being accessed. These devices have 256 bytes of data EEPROM with an address range from 0h to 0FFh.

When accessing the program memory block, the EEDATH:EEDATL register pair forms a 2-byte word that holds the 14-bit data for read/write, and the EEADRL and EEADRH registers form a 2-byte word that holds the 15-bit address of the program memory location being read.

The EEPROM data memory allows byte read and write. An EEPROM byte write automatically erases the location and writes the new data (erase before write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the voltage range of the device for byte or word operations.

Depending on the setting of the Flash Program Memory Self Write Enable bits WRT<1:0> of the Configuration Words, the device may or may not be able to write certain blocks of the program memory. However, reads from the program memory are always allowed.

When the device is code-protected, the device programmer can no longer access data or program memory. When code-protected, the CPU may continue to read and write the data EEPROM memory and Flash program memory.

12.1 EADRL and EEADRH Registers

The EEADRH:EEADRL register pair can address up to a maximum of 256 bytes of data EEPROM or up to a maximum of 32K words of program memory.

When selecting a program address value, the MSB of the address is written to the EEADRH register and the LSB is written to the EEADRL register. When selecting an EEPROM address value, only the LSB of the address is written to the EEADRL register.

12.1.1 EECON1 AND EECON2 REGISTERS

EECON1 is the control register for EE memory accesses.

Control bit EEPGD determines if the access will be a program or data memory access. When clear, any subsequent operations will operate on the EEPROM memory. When set, any subsequent operations will operate on the program memory. On Reset, EEPROM is selected by default.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation to occur. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and execute the appropriate error handling routine.

Interrupt flag bit EEIF of the PIR2 register is set when write is complete. It must be cleared in the software.

Reading EECON2 will read all ‘0’s. The EECON2 register is used exclusively in the data EEPROM write sequence. To enable writes, a specific pattern must be written to EECON2.
12.2 Using the Data EEPROM

The data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). When variables in one section change frequently, while variables in another section do not change, it is possible to exceed the total number of write cycles to the EEPROM without exceeding the total number of write cycles to a single byte. Refer to Section 30.0 “Electrical Specifications”. If this is the case, then a refresh of the array must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in Flash program memory.

12.2.1 READING THE DATA EEPROM MEMORY

To read a data memory location, the user must write the address to the EEADRL register, clear the EEPGD and CFGS control bits of the EECON1 register, and then set control bit RD. The data is available at the very next cycle, in the EEDATL register; therefore, it can be read in the next instruction. EEDATL will hold this value until another read or until it is written to by the user (during a write operation).

**EXAMPLE 12-1: DATA EEPROM READ**

```asm
BANKSEL EEADRL ;
MOVLW DATA_EE_ADDR ;
MOVWF EEADRL ;Address to read
BCF EECON1, CFGS ;Deselect Config space
BCF EECON1, EEPGD;Point to DATA memory
BSF EECON1, RD ;EE Read
MOVF EEDATL, W ;W = EEDATL
```

**Note:** Data EEPROM can be read regardless of the setting of the CPD bit.

12.2.2 WRITING TO THE DATA EEPROM MEMORY

To write an EEPROM data location, the user must first write the address to the EEADRL register and the data to the EEDATL register. Then the user must follow a specific sequence to initiate the write for each byte.

The write will not initiate if the above sequence is not followed exactly (write 55h to EECON2, write AAh to EECON2, then set the WR bit) for each byte. Interrupts should be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. EEIF must be cleared by software.

12.2.3 PROTECTION AGAINST SPURIOUS WRITE

There are conditions when the user may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built-in. On power-up, WREN is cleared. Also, the Power-up Timer (64 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during:
- Brown-out
- Power Glitch
- Software Malfunction

12.2.4 DATA EEPROM OPERATION DURING CODE-PROTECT

Data memory can be code-protected by programming the CPD bit in the Configuration Words to '0'.

When the data memory is code-protected, only the CPU is able to read and write data to the data EEPROM. It is recommended to code-protect the program memory when code-protecting data memory. This prevents anyone from replacing your program with a program that will access the contents of the data EEPROM.
EXAMPLE 12-2: DATA EEPROM WRITE

```
BANKSEL EEADRL ;
MOVLW DATA_EE_ADDR ;
MOVWF EEADRL ; Data Memory Address to write
MOVLW DATA_EE_DATA ;
MOVWF EEDATL ; Data Memory Value to write
BCF EECON1, CFGS ; Deselect Configuration space
BCF EECON1, EEPGD ; Point to DATA memory
BSF EECON1, WREN ; Enable writes

BCF INTCON, GIE ; Disable INTs.
MOVLW 55h ;
MOVWF EECON2 ; Write 55h
MOVLW 0AAh ;
MOVWF EECON2 ; Write AAh
BSF EECON1, WR ; Set WR bit to begin write
BSF INTCON, GIE ; Enable Interrupts
BCF EECON1, WREN ; Disable writes
BTFSC EECON1, WR ; Wait for write to complete
GOTO $-2 ; Done
```

FIGURE 12-1: FLASH PROGRAM MEMORY READ CYCLE EXECUTION
12.3 Flash Program Memory Overview

It is important to understand the Flash program memory structure for erase and programming operations. Flash program memory is arranged in rows. A row consists of a fixed number of 14-bit program memory words. A row is the minimum block size that can be erased by user software.

Flash program memory may only be written or erased if the destination address is in a segment of memory that is not write-protected, as defined in bits WRT<1:0> of Configuration Words.

After a row has been erased, the user can reprogram all or a portion of this row. Data to be written into the program memory row is written to 14-bit wide data write latches. These write latches are not directly accessible to the user, but may be loaded via sequential writes to the EEDATH:EEDATL register pair.

The number of data write latches may not be equivalent to the number of row locations. During programming, user software may need to fill the set of write latches and initiate a programming operation multiple times in order to fully reprogram an erased row. For example, a device with a row size of 32 words and eight write latches will need to load the write latches with data and initiate a programming operation four times.

The size of a program memory row and the number of program memory write latches may vary by device. See Table 12-1 for details.

12.3.1 READING THE FLASH PROGRAM MEMORY

To read a program memory location, the user must:
1. Write the Least and Most Significant address bits to the EEADR<4:0> register pair.
2. Clear the CFGS bit of the EECON1 register.
3. Set the EEPGD control bit of the EECON1 register.
4. Then, set control bit RD of the EECON1 register.

Once the read control bit is set, the program memory Flash controller will use the second instruction cycle to read the data. This causes the second instruction immediately following the "BSF EECON1,RD" instruction to be ignored. The data is available in the very next cycle, in the EEDATH:EEDATL register pair; therefore, it can be read as two bytes in the following instructions.

EEDATH:EEDATL register pair will hold this value until another read or until it is written to by the user.

Note: If the user wants to modify only a portion of a previously programmed row, then the contents of the entire row must be read and saved in RAM prior to the erase.

The two instructions following a program memory read are required to be NOPs. This prevents the user from executing a two-cycle instruction on the next instruction after the RD bit is set.

2: Flash program memory can be read regardless of the setting of the CP bit.

TABLE 12-1: FLASH MEMORY ORGANIZATION BY DEVICE

<table>
<thead>
<tr>
<th>Device</th>
<th>Erase Block (Row) Size/Boundary</th>
<th>Number of Write Latches/Boundary</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC16(L)F1784/6/7</td>
<td>32 words, EEADRL&lt;4:0&gt; = 00000</td>
<td>32 words, EEADRL&lt;4:0&gt; = 00000</td>
</tr>
</tbody>
</table>
EXAMPLE 12-3: FLASH PROGRAM MEMORY READ

* This code block will read 1 word of program memory at the memory address:
PROG_ADDR_HI : PROG_ADDR_LO
* data will be returned in the variables;
* PROG_DATA_HI, PROG_DATA_LO

BANKSEL EEADRL ; Select Bank for EEPROM registers
MOVLW PROG_ADDR_LO ;
MOVWF EEADRL ; Store LSB of address
MOVLW PROG_ADDR_HI ;
MOVWL EEADRH ; Store MSB of address
BCF EECON1,CFGS ; Do not select Configuration Space
BSF EECON1,EEPGD ; Select Program Memory
BCF INTCON,GIE ; Disable interrupts
BSF EECON1,RD ; Initiate read
NOP ; Executed (Figure 12-1)
NOP ; Ignored (Figure 12-1)
BSF INTCON,GIE ; Restore interrupts
MOVF EEDATL,W ; Get LSB of word
MOVWF PROG_DATA_LO ; Store in user location
MOVF EEDATH,W ; Get MSB of word
MOVWF PROG_DATA_HI ; Store in user location
12.3.2 ERASING FLASH PROGRAM MEMORY

While executing code, program memory can only be erased by rows. To erase a row:

1. Load the EEADRH:EEADRL register pair with the address of new row to be erased.
2. Clear the CFGS bit of the EECON1 register.
3. Set the EEPGD, FREE, and WREN bits of the EECON1 register.
4. Write 55h, then AAh, to EECON2 (Flash programming unlock sequence).
5. Set control bit WR of the EECON1 register to begin the erase operation.
6. Poll the FREE bit in the EECON1 register to determine when the row erase has completed.

See Example 12-4.

After the "BSF EECON1,WR" instruction, the processor requires two cycles to set up the erase operation. The user must place two NOP instructions after the WR bit is set. The processor will halt internal operations for the typical 2 ms erase time. This is not Sleep mode as the clocks and peripherals will continue to run. After the erase cycle, the processor will resume operation with the third instruction after the EECON1 write instruction.

12.3.3 WRITING TO FLASH PROGRAM MEMORY

Program memory is programmed using the following steps:

1. Load the starting address of the word(s) to be programmed.
2. Load the write latches with data.
3. Initiate a programming operation.
4. Repeat steps 1 through 3 until all data is written.

Before writing to program memory, the word(s) to be written must be erased or previously unwritten. Program memory can only be erased one row at a time. No automatic erase occurs upon the initiation of the write.

Program memory can be written one or more words at a time. The maximum number of words written at one time is equal to the number of write latches. See Figure 12-2 (block writes to program memory with 32 write latches) for more details. The write latches are aligned to the address boundary defined by EEADRL as shown in Table 12-1. Write operations do not cross these boundaries. At the completion of a program memory write operation, the write latches are reset to contain 0x3FFF.

The following steps should be completed to load the write latches and program a block of program memory. These steps are divided into two parts. First, all write latches are loaded with data except for the last program memory location. Then, the last write latch is loaded and the programming sequence is initiated. A special unlock sequence is required to load a write latch with data or initiate a Flash programming operation. This unlock sequence should not be interrupted.

1. Set the EEPGD and WREN bits of the EECON1 register.
2. Clear the CFGS bit of the EECON1 register.
3. Set the LWLO bit of the EECON1 register. When the LWLO bit of the EECON1 register is '1', the write sequence will only load the write latches and will not initiate the write to Flash program memory.
4. Load the EEADRH:EEADRL register pair with the address of the location to be written.
5. Load the EEDATH:EEDATL register pair with the program memory data to be written.
6. Write 55h, then AAh, to EECON2, then set the WR bit of the EECON1 register (Flash programming unlock sequence). The write latch is now loaded.
7. Increment the EEADRH:EEADRL register pair to point to the next location.
8. Repeat steps 5 through 7 until all but the last write latch has been loaded.
9. Clear the LWLO bit of the EECON1 register. When the LWLO bit of the EECON1 register is '0', the write sequence will initiate the write to Flash program memory.
10. Load the EEDATH:EEDATL register pair with the program memory data to be written.
11. Write 55h, then AAh, to EECON2, then set the WR bit of the EECON1 register (Flash programming unlock sequence). The entire latch block is now written to Flash program memory.

It is not necessary to load the entire write latch block with user program data. However, the entire write latch block will be written to program memory.

An example of the complete write sequence for eight words is shown in Example 12-5. The initial address is loaded into the EEADRH:EEADRL register pair; the eight words of data are loaded using indirect addressing.

After the "BSF EECON1,WR" instruction, the processor requires two cycles to set up the write operation. The user must place two NOP instructions after the WR bit is set. The processor will halt internal operations for the typical 2 ms, only during the cycle in which the write takes place (i.e., the last word of the block write). This is not Sleep mode as the clocks and peripherals will continue to run. The processor does not stall when LWLO = 1, loading the write latches. After the write cycle, the processor will resume operation with the third instruction after the EECON1 WRITE instruction.
EXAMPLE 12-4:  ERASING ONE ROW OF PROGRAM MEMORY

This row erase routine assumes the following:
1. A valid address within the erase block is loaded in ADDRH:ADDRL
2. ADDRH and ADDRL are located in shared data memory 0x70 - 0x7F (common RAM)

```
BCF INTCON,GIE ; Disable ints so required sequences will execute properly
BANKSEL EEAADR
MOVF ADDRL,W ; Load lower 8 bits of erase address boundary
MOVWF EEAADR
MOVF ADDRH,W ; Load upper 6 bits of erase address boundary
MOVWF EEAADRH
BSF EECO1,EEPGD ; Point to program memory
BCF EECO1,CFGS ; Not configuration space
BSF EECO1,FREE ; Specify an erase operation
BSF EECO1,WREN ; Enable writes
MOVLW 55h ; Start of required sequence to initiate erase
MOVWF EECO2 ; Write 55h
MOVLW 0AAh ;
MOVWF EECO2 ; Write AAh
BSF EECO1,WR ; Set WR bit to begin erase
NOP ; Any instructions here are ignored as processor halts to begin erase sequence
NOP ; Processor will stop here and wait for erase complete.
BCF EECO1,WREN ; Disable writes
BSF INTCON,GIE ; Enable interrupts
```
EXAMPLE 12-5: WRITING TO FLASH PROGRAM MEMORY

; This write routine assumes the following:
; 1. The 16 bytes of data are loaded, starting at the address in DATA_ADDR
; 2. Each word of data to be written is made up of two adjacent bytes in DATA_ADDR,
;    stored in little endian format
; 3. A valid starting address (the least significant bits = 0000) is loaded in ADDRH:ADDRL
; 4. ADDRH and ADDRL are located in shared data memory 0x70 - 0x7F (common RAM)

BCF INTCON,GIE ; Disable ints so required sequences will execute properly
BANKSEL EEADRH ; Bank 3
MOVF ADDRH,W ; Load initial address
MOVF EEADRH ;
MOVF ADDRL,W ;
MOVF EEADRL ;
MOVLW LOW DATA_ADDR ; Load initial data address
MOVF ESR0L ;
MOVLW HIGH DATA_ADDR ; Load initial data address
MOVF ESR0H ;
BSF EECON1,EEPGD ; Point to program memory
BCF EECON1,CFGS ; Not configuration space
BSF EECON1,WREN ; Enable writes
BSF EECON1,LWLO ; Only Load Write Latches
LOOP
 MOVIW FSR0++ ; Load first data byte into lower
 MOVF EEDATL ;
 MOVIW FSR0++ ; Load second data byte into upper
 MOVF EEDATH ;
 MOVF EEADRL,W ; Check if lower bits of address are '000'
 XORLW 0x0F ; Check if we're on the last of 16 addresses
 ANDLW 0x0F ;
 BTFSC STATUS,Z ; Exit if last of 16 words,
 GOTO START_WRITE ;

START_WRITE
 BCF EECON1,LWLO ; No more loading latches - Actually start Flash program
                     ; memory write

Required Sequence

BCF EECON1,LWLO ; No more loading latches - Actually start Flash program
                     ; memory write

MOVIW 55h ; Start of required write sequence:
 MOVF EECON2 ; Write 55h
 MOVLW 0Ah ;
 MOVF EECON2 ; Write AAh
 BSF EECON1,WR ; Set WR bit to begin write
 NOP ; Any instructions here are ignored as processor
                     ; halts to begin write sequence
 NOP ; Processor will stop here and wait for write to complete.
                     ; After write processor continues with 3rd instruction.
 INCF EEADRL,F ; Still loading latches Increment address
 GOTO LOOP ; Write next latches

 Cost

MOVIW 55h ; Start of required write sequence:
 MOVF EECON2 ; Write 55h
 MOVLW 0Ah ;
 MOVF EECON2 ; Write AAh
 BSF EECON1,WR ; Set WR bit to begin write
 NOP ; Any instructions here are ignored as processor
                     ; halts to begin write sequence
 NOP ; Processor will stop here and wait for write complete.
                     ; After write processor continues with 3rd instruction.
 BCF EECON1,WREN ; Disable writes
 BSF INTCON,GIE ; Enable interrupts
12.4 Modifying Flash Program Memory

When modifying existing data in a program memory row, and data within that row must be preserved, it must first be read and saved in a RAM image. Program memory is modified using the following steps:

1. Load the starting address of the row to be modified.
2. Read the existing data from the row into a RAM image.
3. Modify the RAM image to contain the new data to be written into program memory.
4. Load the starting address of the row to be rewritten.
5. Erase the program memory row.
6. Load the write latches with data from the RAM image.
7. Initiate a programming operation.
8. Repeat steps 6 and 7 as many times as required to reprogram the erased row.

12.5 User ID, Device ID and Configuration Word Access

Instead of accessing program memory or EEPROM data memory, the User ID’s, Device ID/Revision ID and Configuration Words can be accessed when CFGS = 1 in the EECON1 register. This is the region that would be pointed to by PC<15> = 1, but not all addresses are accessible. Different access may exist for reads and writes. Refer to Table 12-2.

When read access is initiated on an address outside the parameters listed in Table 12-2, the EEDATH:EEDATL register pair is cleared.

<table>
<thead>
<tr>
<th>Address</th>
<th>Function</th>
<th>Read Access</th>
<th>Write Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>8000h-8003h</td>
<td>User IDs</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>8006h</td>
<td>Device ID/Revision ID</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>8007h-8008h</td>
<td>Configuration Words 1 and 2</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

**EXAMPLE 12-6:  CONFIGURATION WORD AND DEVICE ID ACCESS**

* This code block will read 1 word of program memory at the memory address:
* PROG_ADDR_LO (must be 00h-08h) data will be returned in the variables;
* PROG_DATA_HI, PROG_DATA_LO

```assembly
BANKSEL EEADRL ; Select correct Bank
MOVLW PROG_ADDR_LO ;
MOVF EEADRL,W ; Store LSB of address
CLRF EEADRH ; Clear MSB of address
BSF EECON1,CFGS ; Select Configuration Space
BCF INTCON,GIE ; Disable interrupts
BSF EECON1,RD ; Initiate read
NOP ; Executed (See Figure 12-1)
NOP ; Ignored (See Figure 12-1)
BSF INTCON,GIE ; Restore interrupts
MOVF EEDATL,W ; Get LSB of word
MOVF EEDATH,W ; Get MSB of word
MOVF PROG_DATA_HI ; Store in user location
MOVF PROG_DATA_LO ; Store in user location
```
12.6 Write Verify

Depending on the application, good programming practice may dictate that the value written to the data EEPROM or program memory should be verified (see Example 12-7) to the desired value to be written. Example 12-7 shows how to verify a write to EEPROM.

**EXAMPLE 12-7: EEPROM WRITE VERIFY**

```
BANKSEL EEDATL ;
MOVF EEDATL, W ;EEDATL not changed
               ;from previous write
BSF EECON1, RD ;YES, Read the
               ;value written
XORWF EEDATL, W ;
BTFSS STATUS, Z ;Is data the same
GOTO WRITE_ERR ;No, handle error
               ;Yes, continue
```
12.7 Register Definitions: EEPROM and Flash Control

REGISTER 12-1: EEDATL: EEPROM DATA LOW BYTE REGISTER

<table>
<thead>
<tr>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEDAT&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

bit 7-0 EEDAT<7:0>: Read/write value for EEPROM data byte or Least Significant bits of program memory

REGISTER 12-2: EEDATH: EEPROM DATA HIGH BYTE REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEDAT&lt;13:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

bit 7-6 Unimplemented: Read as ‘0’
bit 5-0 EEDAT<13:8>: Read/write value for Most Significant bits of program memory

REGISTER 12-3: EEADR: EEPROM ADDRESS REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEADR&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

bit 7-0 EEADR<7:0>: Specifies the Least Significant bits for program memory address or EEPROM address

REGISTER 12-4: EEADR: EEPROM ADDRESS HIGH BYTE REGISTER

<table>
<thead>
<tr>
<th>U-1</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEADR&lt;14:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

bit 7-0 EEADR<14:8>: Specifies the Most Significant bits for program memory address or EEPROM address

**Note 1:** Unimplemented, read as ‘1’.
## REGISTER 12-5: EECON1: EEPROM CONTROL 1 REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-x/q</th>
<th>R/W-0/0</th>
<th>R/S/HC-0/0</th>
<th>R/S/HC-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEPGD</td>
<td>CFGS</td>
<td>LWLO</td>
<td>FREE</td>
<td>WRERR</td>
<td>WREN</td>
<td>WR</td>
<td>RD</td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **S** = Bit can only be set
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **HC** = Bit is cleared by hardware

#### bit 7
**EEPGD**: Flash Program/Data EEPROM Memory Select bit
- 1 = Accesses program space Flash memory
- 0 = Accesses data EEPROM memory

#### bit 6
**CFGS**: Flash Program/Data EEPROM or Configuration Select bit
- 1 = Accesses Configuration, User ID and Device ID registers
- 0 = Accesses Flash program or data EEPROM memory

#### bit 5
**LWLO**: Load Write Latches Only bit
- If CFGS = 1 (Configuration space) OR CFGS = 0 and EEPGD = 1 (program Flash):
  - 1 = The next WR command does not initiate a write; only the program memory latches are updated.
  - 0 = The next WR command writes a value from EEDATH:EEDATL into program memory latches and initiates a write of all the data stored in the program memory latches.
- If CFGS = 0 and EEPGD = 0: (Accessing data EEPROM)
  - LWLO is ignored. The next WR command initiates a write to the data EEPROM.

#### bit 4
**FREE**: Program Flash Erase Enable bit
- If CFGS = 1 (Configuration space) OR CFGS = 0 and EEPGD = 1 (program Flash):
  - 1 = Performs an erase operation on the next WR command (cleared by hardware after completion of erase).
  - 0 = Performs a write operation on the next WR command.
- If EEPGD = 0 and CFGS = 0: (Accessing data EEPROM)
  - FREE is ignored. The next WR command will initiate both a erase cycle and a write cycle.

#### bit 3
**WRERR**: EEPROM Error Flag bit
- 1 = Condition indicates an improper program or erase sequence attempt or termination (bit is set automatically on any set attempt (write ‘1’) of the WR bit).
- 0 = The program or erase operation completed normally.

#### bit 2
**WREN**: Program/Erase Enable bit
- 1 = Allows program/erase cycles
- 0 = Inhibits programming/erasing of program Flash and data EEPROM

#### bit 1
**WR**: Write Control bit
- 1 = Initiates a program Flash or data EEPROM program/erase operation.
  - The operation is self-timed and the bit is cleared by hardware once operation is complete.
  - The WR bit can only be set (not cleared) in software.
- 0 = Program/erase operation to the Flash or data EEPROM is complete and inactive.

#### bit 0
**RD**: Read Control bit
- 1 = Initiates an program Flash or data EEPROM read. Read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software.
- 0 = Does not initiate a program Flash or data EEPROM data read.
REGISTER 12-6:  EECON2: EEPROM CONTROL 2 REGISTER

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEPROM Control Register 2</td>
<td>W-0/0</td>
<td>W-0/0</td>
<td>W-0/0</td>
<td>W-0/0</td>
<td>W-0/0</td>
<td>W-0/0</td>
<td>W-0/0</td>
<td>W-0/0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
S = Bit can only be set  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set  '0' = Bit is cleared

bit 7-0  Data EEPROM Unlock Pattern bits
To unlock writes, a 55h must be written first, followed by an AAh, before setting the WR bit of the EECON1 register. The value written to this register is used to unlock the writes. There are specific timing requirements on these writes. Refer to Section 12.2.2 “Writing to the Data EEPROM Memory” for more information.

TABLE 12-3:  SUMMARY OF REGISTERS ASSOCIATED WITH DATA EEPROM

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>EECON1</td>
<td>EEPGD</td>
<td>CFGS</td>
<td>LWLO</td>
<td>FREE</td>
<td>WRERR</td>
<td>WREN</td>
<td>WR</td>
<td>RD</td>
<td>123</td>
</tr>
<tr>
<td>EECON2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>124*</td>
</tr>
<tr>
<td>EEADRL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>122</td>
</tr>
<tr>
<td>EEADRH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>122</td>
</tr>
<tr>
<td>EEDATL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>122</td>
</tr>
<tr>
<td>EEDATH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>122</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>93</td>
</tr>
<tr>
<td>PIE2</td>
<td>OSFIE</td>
<td>C2IE</td>
<td>C1IE</td>
<td>EEIE</td>
<td>BCL1IE</td>
<td>C4IE</td>
<td>C3IE</td>
<td>CCP2IE</td>
<td>95</td>
</tr>
<tr>
<td>PIR2</td>
<td>OSFIF</td>
<td>C2IF</td>
<td>C1IF</td>
<td>EEIF</td>
<td>BCL1IF</td>
<td>C4IF</td>
<td>C3IF</td>
<td>CCP2IF</td>
<td>99</td>
</tr>
</tbody>
</table>

Legend:
— = unimplemented location, read as ‘0’. Shaded cells are not used by data EEPROM module.
* Page provides register information.
2: Unimplemented, read as ‘1’.
13.0 I/O PORTS

Each port has three standard registers for its operation. These registers are:

- TRISx registers (data direction)
- PORTx registers (reads the levels on the pins of the device)
- LATx registers (output latch)

Some ports may have one or more of the following additional registers. These registers are:

- ANSELx (analog select)
- WPUx (weak pull-up)

In general, when a peripheral is enabled on a port pin, that pin cannot be used as a general purpose output. However, the pin can still be read.

**TABLE 13-1: PORT AVAILABILITY PER DEVICE**

<table>
<thead>
<tr>
<th>Device</th>
<th>PORTA</th>
<th>PORTB</th>
<th>PORTC</th>
<th>PORTD</th>
<th>PORTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC16(L)F1786</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>PIC16(L)F1784/7</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
</tr>
</tbody>
</table>

The Data Latch (LATx registers) is useful for read-modify-write operations on the value that the I/O pins are driving.

A write operation to the LATx register has the same effect as a write to the corresponding PORTx register. A read of the LATx register reads of the values held in the I/O PORT latches, while a read of the PORTx register reads the actual I/O pin value.

Ports that support analog inputs have an associated ANSELx register. When an ANSEL bit is set, the digital input buffer associated with that bit is disabled. Disabling the input buffer prevents analog signal levels on the pin between a logic high and low from causing excessive current in the logic input circuitry. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 13-1.
13.1 Alternate Pin Function

The Alternate Pin Function Control (APFCON1 and APFCON2) registers are used to steer specific peripheral input and output functions between different pins. The APFCON1 and APFCON2 registers are shown in Register 13-1 and Register 13-2. For this device family, the following functions can be moved between different pins.

- C2OUT output
- CCP1 output
- SDO output
- SCL/SCK output
- SDA/SDI output
- TX/RX output
- CCP2 output
- CCP3 output

These bits have no effect on the values of any TRIS register. PORT and TRIS overrides will be routed to the correct pin. The unselected pin will be unaffected.
### Register Definitions: Alternate Pin Function Control

#### REGISTER 13-1: APFCON1: ALTERNATE PIN FUNCTION CONTROL 1 REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2OUTSEL</td>
<td>CCP1SEL</td>
<td>SDOSEL</td>
<td>SCKSEL</td>
<td>SDISEL</td>
<td>TXSEL</td>
<td>RXSEL</td>
<td>CCP2SEL</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

**bit 7**  
**C2OUTSEL:** C2OUT Pin Selection bit  
1 = C2OUT is on pin RA6  
0 = C2OUT is on pin RA5

**bit 6**  
**CCP1SEL:** CCP1 Input/Output Pin Selection bit  
1 = CCP1 is on pin RB0  
0 = CCP1 is on pin RC2

**bit 5**  
**SDOSEL:** MSSP SDO Pin Selection bit  
1 = SDO is on pin RB5  
0 = SDO is on pin RC5

**bit 4**  
**SCKSEL:** MSSP Serial Clock (SCL/SCK) Pin Selection bit  
1 = SCL/SCK is on pin RB7  
0 = SCL/SCK is on pin RC3

**bit 3**  
**SDISEL:** MSSP Serial Data (SDA/SDI) Output Pin Selection bit  
1 = SDA/SDI is on pin RB6  
0 = SDA/SDI is on pin RC4

**bit 2**  
**TXSEL:** TX Pin Selection bit  
1 = TX is on pin RB6  
0 = TX is on pin RC6

**bit 1**  
**RXSEL:** RX Pin Selection bit  
1 = RX is on pin RB7  
0 = RX is on pin RC7

**bit 0**  
**CCP2SEL:** CCP2 Input/Output Pin Selection bit  
1 = CCP2 is on pin RB3  
0 = CCP2 is on pin RC1
## REGISTER 13-2: APFCON2: ALTERNATE PIN FUNCTION CONTROL 2 REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>CCP3SEL</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

### bit 7-1
Unimplemented: Read as ‘0’

### bit 0
**CCP3SEL**: CCP3 Input/Output Pin Selection bit
- 1 = CCP3 is on pin RB5
- **PIC16(L)F1786 devices:**
  - 0 = CCP3 is on pin RC6
- **PIC16(L)F1784/7 devices:**
  - 0 = CCP3 is on pin RE0
13.3 PORTA Registers

13.3.1 DATA REGISTER
PORTA is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 13-4). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). Example 13-1 shows how to initialize PORTA.

Reading the PORTA register (Register 13-3) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATA).

13.3.2 DIRECTION CONTROL
The TRISA register (Register 13-4) controls the PORTA pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read ‘0’.

13.3.3 OPEN DRAIN CONTROL
The ODCONA register (Register 13-8) controls the open-drain feature of the port. Open drain operation is independently selected for each pin. When an ODCONA bit is set, the corresponding port output becomes an open drain driver capable of sinking current only. When an ODCONA bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

13.3.4 SLEW RATE CONTROL
The SLRCONA register (Register 13-9) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONA bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONA bit is cleared, the corresponding port pin drive slews at the maximum rate possible.

13.3.5 INPUT THRESHOLD CONTROL
The INLVLA register (Register 13-10) controls the input voltage threshold for each of the available PORTA input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTA register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Section TABLE 30-1: “Supply Voltage” for more information on threshold levels.

Note: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

13.3.6 ANALOG CONTROL
The ANSELA register (Register 13-6) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as ‘0’ and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note: The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to ‘0’ by user software.

EXAMPLE 13-1: INITIALIZING PORTA

; This code example illustrates
; initializing the PORTA register. The
; other ports are initialized in the same
; manner.

BANKSEL PORTA ;
CLRF PORTA ;Init PORTA
BANKSEL LATA ;Data Latch
CLRF LATA ;
BANKSEL ANSELA ;
CLRF ANSELA ;digital I/O
BANKSEL TRISA ;
MOVWF B’00111000’ ;Set RA<5:3> as inputs
MOVWF TRISA ;and set RA<2:0> as
;outputs
13.3.7 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 13-2.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority. Analog input functions, such as ADC, and comparator inputs, are not shown in the priority lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELx registers. Digital output functions may control the pin when it is in Analog mode with the priority shown in the priority list.

TABLE 13-2: PORTA OUTPUT PRIORITY

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Function Priority(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RA0</td>
<td>RA0</td>
</tr>
<tr>
<td>RA1</td>
<td>OPA1OUT</td>
</tr>
<tr>
<td></td>
<td>RA1</td>
</tr>
<tr>
<td>RA2</td>
<td>DAC1OUT1</td>
</tr>
<tr>
<td></td>
<td>RA2</td>
</tr>
<tr>
<td>RA3</td>
<td>RA3</td>
</tr>
<tr>
<td>RA4</td>
<td>C1OUT</td>
</tr>
<tr>
<td></td>
<td>RA4</td>
</tr>
<tr>
<td>RA5</td>
<td>C2OUT</td>
</tr>
<tr>
<td></td>
<td>RA5</td>
</tr>
<tr>
<td>RA6</td>
<td>CLKOUT</td>
</tr>
<tr>
<td></td>
<td>C2OUT</td>
</tr>
<tr>
<td></td>
<td>RA6</td>
</tr>
<tr>
<td>RA7</td>
<td>RA7</td>
</tr>
</tbody>
</table>

Note 1: Priority listed from highest to lowest.
13.4 Register Definitions: PORTA

REGISTER 13-3: PORTA: PORTA REGISTER

<table>
<thead>
<tr>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
<th>R/W-x/x</th>
</tr>
</thead>
<tbody>
<tr>
<td>RA7</td>
<td>RA6</td>
<td>RA5</td>
<td>RA4</td>
<td>RA3</td>
<td>RA2</td>
<td>RA1</td>
<td>RA0</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

bit 7-0 **RA<7:0>:** PORTA I/O Value bits
- **1** = Port pin is > ViH
- **0** = Port pin is < ViL

**Note 1:** Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

REGISTER 13-4: TRISA: PORTA TRI-STATE REGISTER

<table>
<thead>
<tr>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

bit 7-0 **TRISA<7:0>:** PORTA Tri-State Control bits
- **1** = PORTA pin configured as an input (tri-stated)
- **0** = PORTA pin configured as an output

REGISTER 13-5: LATA: PORTA DATA LATCH REGISTER

<table>
<thead>
<tr>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>LATA7</td>
<td>LATA6</td>
<td>LATA5</td>
<td>LATA4</td>
<td>LATA3</td>
<td>LATA2</td>
<td>LATA1</td>
<td>LATA0</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

bit 7-4 **LATA<7:0>:** PORTA Output Latch Value bits

**Note 1:** Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.
REGISTER 13-6: ANSELA: PORTA ANALOG SELECT REGISTER

<table>
<thead>
<tr>
<th>R/W-1/1</th>
<th>U-0</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSA7</td>
<td></td>
<td>ANSA5</td>
<td>ANSA4</td>
<td>ANSA3</td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **1/0/1/1/1/1/1** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

**bit 5**  ANSA7: Analog Select between Analog or Digital Function on pins RA7, respectively
- 0 = Digital I/O. Pin is assigned to port or digital special function.
- 1 = Analog input. Pin is assigned as analog input\(^{(1)}\). Digital input buffer disabled.

**bit 6**  Unimplemented: Read as ‘0’

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 13-7: WPUA: WEAK PULL-UP PORTA REGISTER

<table>
<thead>
<tr>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>WPUA7</td>
<td>WPUA6</td>
<td>WPUA5</td>
<td>WPUA4</td>
<td>WPUA3</td>
<td>WPUA2</td>
<td>WPUA1</td>
<td>WPUA0</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **1/0/1/1/1/1/1** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

**bit 7-0**  WPUA<7:0>: Weak Pull-up Register bits
- 1 = Pull-up enabled
- 0 = Pull-up disabled

Note 1: Global WPUEN bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in configured as an output.
## REGISTER 13-8: ODCONA: PORTA OPEN DRAIN CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ODA7</td>
<td>ODA6</td>
<td>ODA5</td>
<td>ODA4</td>
<td>ODA3</td>
<td>ODA2</td>
<td>ODA1</td>
<td>ODA0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **’1’** = Bit is set
- **’0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-0**

**ODA<7:0>:** PORTA Open Drain Enable bits
- 1 = Port pin operates as open-drain drive (sink current only)
- 0 = Port pin operates as standard push-pull drive (source and sink current)

## REGISTER 13-9: SLRCONA: PORTA SLEW RATE CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLRA7</td>
<td>SLRA6</td>
<td>SLRA5</td>
<td>SLRA4</td>
<td>SLRA3</td>
<td>SLRA2</td>
<td>SLRA1</td>
<td>SLRA0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **’1’** = Bit is set
- **’0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-0**

**SLRA<7:0>:** PORTA Slew Rate Enable bits
- 1 = Port pin slew rate is limited
- 0 = Port pin slews at maximum rate

## REGISTER 13-10: INLVLA: PORTA INPUT LEVEL CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>INLVLA7</td>
<td>INLVLA6</td>
<td>INLVLA5</td>
<td>INLVLA4</td>
<td>INLVLA3</td>
<td>INLVLA2</td>
<td>INLVLA1</td>
<td>INLVLA0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **’1’** = Bit is set
- **’0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-0**

**INLVLA<7:0>:** PORTA Input Level Select bits
- 1 = ST input used for PORT reads and interrupt-on-change
- 0 = TTL input used for PORT reads and interrupt-on-change
## TABLE 13-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSELA</td>
<td>ANSA7</td>
<td>—</td>
<td>ANSA5</td>
<td>ANSA4</td>
<td>ANSA3</td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
<td>132</td>
</tr>
<tr>
<td>INLVL A</td>
<td>INLVL A7</td>
<td>INLVL A6</td>
<td>INLVL A5</td>
<td>INLVL A4</td>
<td>INLVL A3</td>
<td>INLVL A2</td>
<td>INLVL A1</td>
<td>INLVL A0</td>
<td>133</td>
</tr>
<tr>
<td>LATA</td>
<td>LATA7</td>
<td>LATA6</td>
<td>LATA5</td>
<td>LATA4</td>
<td>LATA3</td>
<td>LATA2</td>
<td>LATA1</td>
<td>LATA0</td>
<td>131</td>
</tr>
<tr>
<td>ODCONA</td>
<td>ODA7</td>
<td>ODA6</td>
<td>ODA5</td>
<td>ODA4</td>
<td>ODA3</td>
<td>ODA2</td>
<td>ODA1</td>
<td>ODA0</td>
<td>133</td>
</tr>
<tr>
<td>OPTION_REG</td>
<td>WPUEN</td>
<td>INTEDG</td>
<td>TMR0CS</td>
<td>TMR0SE</td>
<td>PSA</td>
<td>PS&lt;2:0&gt;</td>
<td></td>
<td></td>
<td>198</td>
</tr>
<tr>
<td>PORTA</td>
<td>RA7</td>
<td>RA6</td>
<td>RA5</td>
<td>RA4</td>
<td>RA3</td>
<td>RA2</td>
<td>RA1</td>
<td>RA0</td>
<td>131</td>
</tr>
<tr>
<td>SLRCON A</td>
<td>SLRA7</td>
<td>SLRA6</td>
<td>SLRA5</td>
<td>SLRA4</td>
<td>SLRA3</td>
<td>SLRA2</td>
<td>SLRA1</td>
<td>SLRA0</td>
<td>133</td>
</tr>
<tr>
<td>TRISA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td>131</td>
</tr>
<tr>
<td>WPUA</td>
<td>WPUA7</td>
<td>WPUA6</td>
<td>WPUA5</td>
<td>WPUA4</td>
<td>WPUA3</td>
<td>WPUA2</td>
<td>WPUA1</td>
<td>WPUA0</td>
<td>132</td>
</tr>
</tbody>
</table>

Legend: \( \times \) = unknown, \( \_ \) = unchanged, \( - \) = unimplemented locations read as ‘0’. Shaded cells are not used by PORTA.

## TABLE 13-4: SUMMARY OF CONFIGURATION WORD WITH PORTA

<table>
<thead>
<tr>
<th>Name</th>
<th>Bits</th>
<th>Bit -7</th>
<th>Bit -6</th>
<th>Bit 13/5</th>
<th>Bit 12/4</th>
<th>Bit 11/3</th>
<th>Bit 10/2</th>
<th>Bit 9/1</th>
<th>Bit 8/0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG1</td>
<td>13:8</td>
<td>—</td>
<td>—</td>
<td>FCMEN</td>
<td>IESO</td>
<td>CLKOUTEN</td>
<td>BOREN&lt;1:0&gt;</td>
<td>CPD</td>
<td></td>
<td>54</td>
</tr>
<tr>
<td>CONFIG1</td>
<td>7:0</td>
<td>CP</td>
<td>MCLRE</td>
<td>PWRTEN</td>
<td>WDTE&lt;1:0&gt;</td>
<td>FOSC&lt;2:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: \( - \) = unimplemented location, read as ‘0’. Shaded cells are not used by PORTA.
13.5 PORTB Registers

13.5.1 DATA REGISTER
PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB (Register 13-12). Setting a TRISB bit (\(=1\)) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (\(=0\)) will make the corresponding PORTB pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 13-1 shows how to initialize an I/O port.

Reading the PORTB register (Register 13-11) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATB).

13.5.2 DIRECTION CONTROL
The TRISB register (Register 13-12) controls the PORTB pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISB register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read ‘0’.

13.5.3 OPEN DRAIN CONTROL
The ODCONB register (Register 13-16) controls the open-drain feature of the port. Open drain operation is independently selected for each pin. When an ODCONB bit is set, the corresponding port output becomes an open drain driver capable of sinking current only. When an ODCONB bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

13.5.4 SLEW RATE CONTROL
The SLRCONB register (Register 13-17) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONB bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONB bit is cleared, the corresponding port pin drive slews at the maximum rate possible.

13.5.5 INPUT THRESHOLD CONTROL
The INLVLB register (Register 13-18) controls the input voltage threshold for each of the available PORTB input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTB register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Section TABLE 30-1: “Supply Voltage” for more information on threshold levels.

Note: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

13.5.6 ANALOG CONTROL
The ANSELB register (Register 13-14) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELB bit high will cause all digital reads on the pin to be read as ‘0’ and allow analog functions on the pin to operate correctly.

The state of the ANSELB bits has no effect on digital output functions. A pin with TRIS clear and ANSELB set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note: The ANSELB bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to ‘0’ by user software.
13.5.7 PORTB FUNCTIONS AND OUTPUT PRIORITIES

Each PORTB pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 13-5.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority.

Analog input and some digital input functions are not included in the list below. These input functions can remain active when the pin is configured as an output. Certain digital input functions override other port functions and are included in the priority list.

TABLE 13-5: PORTB OUTPUT PRIORITY

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Function Priority(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RB0</td>
<td>CCP1</td>
</tr>
<tr>
<td></td>
<td>RB0</td>
</tr>
<tr>
<td>RB1</td>
<td>OPA2OUT</td>
</tr>
<tr>
<td></td>
<td>RB1</td>
</tr>
<tr>
<td>RB2</td>
<td>CLKR</td>
</tr>
<tr>
<td></td>
<td>RB2</td>
</tr>
<tr>
<td>RB3</td>
<td>CCP2</td>
</tr>
<tr>
<td></td>
<td>RB3</td>
</tr>
<tr>
<td>RB4</td>
<td>RB4</td>
</tr>
<tr>
<td>RB5</td>
<td>SDO</td>
</tr>
<tr>
<td></td>
<td>C3OUT</td>
</tr>
<tr>
<td></td>
<td>CCP3</td>
</tr>
<tr>
<td></td>
<td>RB5</td>
</tr>
<tr>
<td>RB6</td>
<td>ICSPCLK</td>
</tr>
<tr>
<td></td>
<td>SDA</td>
</tr>
<tr>
<td></td>
<td>TX/CK</td>
</tr>
<tr>
<td></td>
<td>RB6</td>
</tr>
<tr>
<td>RB7</td>
<td>ICSPDAT</td>
</tr>
<tr>
<td></td>
<td>DAC1OUT2</td>
</tr>
<tr>
<td></td>
<td>SCL/SCK</td>
</tr>
<tr>
<td></td>
<td>DT</td>
</tr>
<tr>
<td></td>
<td>RB7</td>
</tr>
</tbody>
</table>

Note 1: Priority listed from highest to lowest.
13.6 Register Definitions: PORTB

### REGISTER 13-11: PORTB: PORTB REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>RB7</th>
<th>RB6</th>
<th>RB5</th>
<th>RB4</th>
<th>RB3</th>
<th>RB2</th>
<th>RB1</th>
<th>RB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **1’** = Bit is set
- **0’** = Bit is cleared

**Note 1:** Writes to PORTB are actually written to corresponding LATB register. Reads from PORTB register is return of actual I/O pin values.

### REGISTER 13-12: TRISB: PORTB TRI-STATE REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>TRISB7</th>
<th>TRISB6</th>
<th>TRISB5</th>
<th>TRISB4</th>
<th>TRISB3</th>
<th>TRISB2</th>
<th>TRISB1</th>
<th>TRISB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
<td>R/W-1/1</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **1’** = Bit is set
- **0’** = Bit is cleared

**Note 1:** TRISB<7:0>: PORTB Tri-State Control bits
- **1** = PORTB pin configured as an input (tri-stated)
- **0** = PORTB pin configured as an output

### REGISTER 13-13: LATB: PORTB DATA LATCH REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>LATB7</th>
<th>LATB6</th>
<th>LATB5</th>
<th>LATB4</th>
<th>LATB3</th>
<th>LATB2</th>
<th>LATB1</th>
<th>LATB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
<td>R/W-x/u</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **1’** = Bit is set
- **0’** = Bit is cleared

**Note 1:** LATB<7:0>: PORTB Output Latch Value bits

**Note 1:** Writes to PORTB are actually written to corresponding LATB register. Reads from PORTB register is return of actual I/O pin values.
REGISTER 13-14: ANSELB: PORTB ANALOG SELECT REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>U-0</td>
</tr>
<tr>
<td>ANSB6</td>
<td>ANSB5</td>
</tr>
<tr>
<td>ANSB4</td>
<td>ANSB3</td>
</tr>
<tr>
<td>ANSB2</td>
<td>ANSB1</td>
</tr>
<tr>
<td>ANSB0</td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

bit 7: **Unimplemented**: Read as '0'

bit 6-0: **ANSB<6:0>:** Analog Select between Analog or Digital Function on pins RB<6:0>, respectively

- 0 = Digital I/O. Pin is assigned to port or digital special function.
- 1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.

**Note 1:** When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 13-15: WPUB: WEAK PULL-UP PORTB REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>WPUB7</td>
<td>WPUB6</td>
</tr>
<tr>
<td>WPUB5</td>
<td>WPUB4</td>
</tr>
<tr>
<td>WPUB3</td>
<td>WPUB2</td>
</tr>
<tr>
<td>WPUB1</td>
<td>WPUB0</td>
</tr>
</tbody>
</table>

Legend:

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

bit 7-0: **WPUB<7:0>:** Weak Pull-up Register bits

- 1 = Pull-up enabled
- 0 = Pull-up disabled

**Note 1:** Global WPUEN bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.

**Note 2:** The weak pull-up device is automatically disabled if the pin is in configured as an output.
### REGISTER 13-16: ODCONB: PORTB OPEN DRAIN CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ODB7</td>
<td>ODB6</td>
<td>ODB5</td>
<td>ODB4</td>
<td>ODB3</td>
<td>ODB2</td>
<td>ODB1</td>
<td>ODB0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-0 ODB<7:0>: PORTB Open Drain Enable bits**
- **1** = Port pin operates as open-drain drive (sink current only)
- **0** = Port pin operates as standard push-pull drive (source and sink current)

### REGISTER 13-17: SLRCONB: PORTB SLEW RATE CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLRB7</td>
<td>SLRB6</td>
<td>SLRB5</td>
<td>SLRB4</td>
<td>SLRB3</td>
<td>SLRB2</td>
<td>SLRB1</td>
<td>SLRB0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-0 SLRB<7:0>: PORTB Slew Rate Enable bits**
- **1** = Port pin slew rate is limited
- **0** = Port pin slews at maximum rate

### REGISTER 13-18: INLVLB: PORTB INPUT LEVEL CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>INLVLB7</td>
<td>INLVLB6</td>
<td>INLVLB5</td>
<td>INLVLB4</td>
<td>INLVLB3</td>
<td>INLVLB2</td>
<td>INLVLB1</td>
<td>INLVLB0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-0 INLVLB<7:0>: PORTB Input Level Select bits**
- **1** = ST input used for PORT reads and interrupt-on-change
- **0** = TTL input used for PORT reads and interrupt-on-change
### TABLE 13-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSELB</td>
<td>—</td>
<td>ANSB6</td>
<td>ANSB5</td>
<td>ANSB4</td>
<td>ANSB3</td>
<td>ANSB2</td>
<td>ANSB1</td>
<td>ANSB0</td>
<td>138</td>
</tr>
<tr>
<td>INVLB</td>
<td>INVLB7</td>
<td>INVLB6</td>
<td>INVLB5</td>
<td>INVLB4</td>
<td>INVLB3</td>
<td>INVLB2</td>
<td>INVLB1</td>
<td>INVLB0</td>
<td>139</td>
</tr>
<tr>
<td>LATB</td>
<td>LATB7</td>
<td>LATB6</td>
<td>LATB5</td>
<td>LATB4</td>
<td>LATB3</td>
<td>LATB2</td>
<td>LATB1</td>
<td>LATB0</td>
<td>137</td>
</tr>
<tr>
<td>ODCONB</td>
<td>ODB7</td>
<td>ODB6</td>
<td>ODB5</td>
<td>ODB4</td>
<td>ODB3</td>
<td>ODB2</td>
<td>ODB1</td>
<td>ODB0</td>
<td>139</td>
</tr>
<tr>
<td>PORTB</td>
<td>RB7</td>
<td>RB6</td>
<td>RB5</td>
<td>RB4</td>
<td>RB3</td>
<td>RB2</td>
<td>RB1</td>
<td>RB0</td>
<td>137</td>
</tr>
<tr>
<td>SLRCONB</td>
<td>SLRB7</td>
<td>SLRB6</td>
<td>SLRB5</td>
<td>SLRB4</td>
<td>SLRB3</td>
<td>SLRB2</td>
<td>SLRB1</td>
<td>SLRB0</td>
<td>139</td>
</tr>
<tr>
<td>TRISB</td>
<td>TRISB7</td>
<td>TRISB6</td>
<td>TRISB5</td>
<td>TRISB4</td>
<td>TRISB3</td>
<td>TRISB2</td>
<td>TRISB1</td>
<td>TRISB0</td>
<td>137</td>
</tr>
<tr>
<td>WPUB</td>
<td>WPUB7</td>
<td>WPUB6</td>
<td>WPUB5</td>
<td>WPUB4</td>
<td>WPUB3</td>
<td>WPUB2</td>
<td>WPUB1</td>
<td>WPUB0</td>
<td>138</td>
</tr>
</tbody>
</table>

**Legend:**  
- `x` = unknown  
- `u` = unchanged  
- `-` = unimplemented locations read as ‘0’.  
Shaded cells are not used by PORTB.
13.7 PORTC Registers

13.7.1 DATA REGISTER

PORTC is an 8-bit wide bidirectional port. The corresponding data direction register is TRISC (Register 13-20). Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 13-1 shows how to initialize an I/O port.

Reading the PORTC register (Register 13-19) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATC).

13.7.2 DIRECTION CONTROL

The TRISC register (Register 13-20) controls the PORTC pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISC register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read ‘0’.

13.7.3 OPEN DRAIN CONTROL

The ODCONC register (Register 13-23) controls the open-drain feature of the port. Open drain operation is independently selected for each pin. When an ODCONC bit is set, the corresponding port output becomes an open drain driver capable of sinking current only. When an ODCONC bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

13.7.4 SLEW RATE CONTROL

The SLRCONC register (Register 13-24) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONC bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONC bit is cleared, the corresponding port pin drive slews at the maximum rate possible.

13.7.5 INPUT THRESHOLD CONTROL

The INLVLC register (Register 13-25) controls the input voltage threshold for each of the available PORTC input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTC register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Section TABLE 30-1: "Supply Voltage" for more information on threshold levels.

Note: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

13.7.6 PORTC FUNCTIONS AND OUTPUT PRIORITIES

Each PORTC pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 13-7.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority. Analog input and some digital input functions are not included in the list below. These input functions can remain active when the pin is configured as an output. Certain digital input functions override other port functions and are included in the priority list.

### TABLE 13-7: PORTC OUTPUT PRIORITY

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Function Priority$^{(1)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>RC0</td>
<td>T1OSO, PSMC1A, RC0</td>
</tr>
<tr>
<td>RC1</td>
<td>PSMC1B, CCP2, RC1</td>
</tr>
<tr>
<td>RC2</td>
<td>PSMC1C, CCP1, RC2</td>
</tr>
<tr>
<td>RC3</td>
<td>PSMC1D, SCL, SCK, RC3</td>
</tr>
<tr>
<td>RC4</td>
<td>PSMC1E, SDA, RC4</td>
</tr>
<tr>
<td>RC5</td>
<td>PSMC1F, SDO, RC5</td>
</tr>
<tr>
<td>RC6</td>
<td>PSMC2A, TX/CK, CCP3, RC6</td>
</tr>
<tr>
<td>RC7</td>
<td>PSMC2B, DT, RC7</td>
</tr>
</tbody>
</table>

Note 1: Priority listed from highest to lowest.
13.8 Register Definitions: PORTC

**REGISTER 13-19: PORTC: PORTC REGISTER**

<table>
<thead>
<tr>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>RC7</td>
<td>RC6</td>
<td>RC5</td>
<td>RC4</td>
<td>RC3</td>
<td>RC2</td>
<td>RC1</td>
<td>RC0</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit 0</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- \(-n/n\) = Value at POR and BOR/Value at all other Resets

**bit 7-0**: RC<7:0>: PORTC General Purpose I/O Pin bits

   - 1 = Port pin is \( \geq \) \( \text{V}_\text{IH} \)
   - 0 = Port pin is \( \leq \) \( \text{V}_\text{IL} \)

**Note 1:** Writes to PORTC are actually written to corresponding LATC register. Reads from PORTC register is return of actual I/O pin values.

**REGISTER 13-20: TRISC: PORTC TRI-STATE REGISTER**

<table>
<thead>
<tr>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRISC7</td>
<td>TRISC6</td>
<td>TRISC5</td>
<td>TRISC4</td>
<td>TRISC3</td>
<td>TRISC2</td>
<td>TRISC1</td>
<td>TRISC0</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit 0</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- \(-n/n\) = Value at POR and BOR/Value at all other Resets

**bit 7-0**: TRISC<7:0>: PORTC Tri-State Control bits

   - 1 = PORTC pin configured as an input (tri-stated)
   - 0 = PORTC pin configured as an output

**REGISTER 13-21: LATC: PORTC DATA LATCH REGISTER**

<table>
<thead>
<tr>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>LATC7</td>
<td>LATC6</td>
<td>LATC5</td>
<td>LATC4</td>
<td>LATC3</td>
<td>LATC2</td>
<td>LATC1</td>
<td>LATC0</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit 0</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- \(-n/n\) = Value at POR and BOR/Value at all other Resets

**bit 7-0**: LATC<7:0>: PORTC Output Latch Value bits

**Note 1:** Writes to PORTC are actually written to corresponding LATC register. Reads from PORTC register is return of actual I/O pin values.
REGISTER 13-22: WPUC: WEAK PULL-UP PORTC REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>WPUC7</td>
<td>WPUC6</td>
<td>WPUC5</td>
<td>WPUC4</td>
<td>WPUC3</td>
<td>WPUC2</td>
<td>WPUC1</td>
<td>WPUC0</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

Bit 7-0: WPUC<7:0>: Weak Pull-up Register bits

- 1 = Pull-up enabled
- 0 = Pull-up disabled

Note 1: Global WPUE bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.

Note 2: The weak pull-up device is automatically disabled if the pin is in configured as an output.

REGISTER 13-23: ODC0NC: PORTC OPEN DRAIN CONTROL REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ODC7</td>
<td>ODC6</td>
<td>ODC5</td>
<td>ODC4</td>
<td>ODC3</td>
<td>ODC2</td>
<td>ODC1</td>
<td>ODC0</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

Bit 7-0: ODC<7:0>: PORTC Open Drain Enable bits

For RC<7:0> pins, respectively

- 1 = Port pin operates as open-drain drive (sink current only)
- 0 = Port pin operates as standard push-pull drive (source and sink current)

REGISTER 13-24: SLRC0NC: PORTC SLEW RATE CONTROL REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLRC7</td>
<td>SLRC6</td>
<td>SLRC5</td>
<td>SLRC4</td>
<td>SLRC3</td>
<td>SLRC2</td>
<td>SLRC1</td>
<td>SLRC0</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

Bit 7-0: SLRC<7:0>: PORTC Slew Rate Enable bits

For RC<7:0> pins, respectively

- 1 = Port pin slew rate is limited
- 0 = Port pin slews at maximum rate
### TABLE 13-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>LATC</td>
<td>LATC7</td>
<td>LATC6</td>
<td>LATC5</td>
<td>LATC4</td>
<td>LATC3</td>
<td>LATC2</td>
<td>LATC1</td>
<td>LATC0</td>
<td>142</td>
</tr>
<tr>
<td>PORTC</td>
<td>RC7</td>
<td>RC6</td>
<td>RC5</td>
<td>RC4</td>
<td>RC3</td>
<td>RC2</td>
<td>RC1</td>
<td>RC0</td>
<td>142</td>
</tr>
<tr>
<td>TRISC</td>
<td>TRISC7</td>
<td>TRISC6</td>
<td>TRISC5</td>
<td>TRISC4</td>
<td>TRISC3</td>
<td>TRISC2</td>
<td>TRISC1</td>
<td>TRISC0</td>
<td>142</td>
</tr>
<tr>
<td>WPUC</td>
<td>WPUC7</td>
<td>WPUC6</td>
<td>WPUC5</td>
<td>WPUC4</td>
<td>WPUC3</td>
<td>WPUC2</td>
<td>WPUC1</td>
<td>WPUC0</td>
<td>143</td>
</tr>
<tr>
<td>INLVLC</td>
<td>INLVLC7</td>
<td>INLVLC6</td>
<td>INLVLC5</td>
<td>INLVLC4</td>
<td>INLVLC3</td>
<td>INLVLC2</td>
<td>INLVLC1</td>
<td>INLVLC0</td>
<td>144</td>
</tr>
<tr>
<td>LATC</td>
<td>LATC7</td>
<td>LATC6</td>
<td>LATC5</td>
<td>LATC4</td>
<td>LATC3</td>
<td>LATC2</td>
<td>LATC1</td>
<td>LATC0</td>
<td>142</td>
</tr>
<tr>
<td>ODCONC</td>
<td>ODC7</td>
<td>ODC6</td>
<td>ODC5</td>
<td>ODC4</td>
<td>ODC3</td>
<td>ODC2</td>
<td>ODC1</td>
<td>ODC0</td>
<td>143</td>
</tr>
<tr>
<td>PORTC</td>
<td>RC7</td>
<td>RC6</td>
<td>RC5</td>
<td>RC4</td>
<td>RC3</td>
<td>RC2</td>
<td>RC1</td>
<td>RC0</td>
<td>142</td>
</tr>
<tr>
<td>SLRCONC</td>
<td>SLRC7</td>
<td>SLRC6</td>
<td>SLRC5</td>
<td>SLRC4</td>
<td>SLRC3</td>
<td>SLRC2</td>
<td>SLRC1</td>
<td>SLRC0</td>
<td>143</td>
</tr>
</tbody>
</table>

**Legend:**
- x = unknown
- u = unchanged
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared
- 'R' = Readable bit
- 'W' = Writable bit
- 'U' = Unimplemented bit, read as '0'

For RC<7:0> pins, respectively:
- 1 = ST input used for PORT reads and interrupt-on-change
- 0 = TTL input used for PORT reads and interrupt-on-change

---

**REGISTER 13-25: INLVLC: PORTC INPUT LEVEL CONTROL REGISTER**

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>INLVLC&lt;7:0&gt;: PORTC Input Level Select bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7-0</td>
<td>For RC&lt;7:0&gt; pins, respectively</td>
</tr>
<tr>
<td></td>
<td>1 = ST input used for PORT reads and interrupt-on-change</td>
</tr>
<tr>
<td></td>
<td>0 = TTL input used for PORT reads and interrupt-on-change</td>
</tr>
</tbody>
</table>

Legend:
- x = unknown, u = unchanged, -n/n = unimplemented locations read as ‘0’. Shaded cells are not used by PORTC.
13.9 PORTD Registers
(PIC16(L)F1784/7 only)

13.9.1 DATA REGISTER
PORTD is an 8-bit wide bidirectional port. The corresponding data direction register is TRISD (Register 13-27). Setting a TRISD bit (\(=1\)) will make the corresponding PORTD pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISD bit (\(=0\)) will make the corresponding PORTD pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 13-1 shows how to initialize an I/O port.

Reading the PORTD register (Register 13-26) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATD).

13.9.2 DIRECTION CONTROL
The TRISD register (Register 13-27) controls the PORTD pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISD register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read ‘0’.

13.9.3 OPEN DRAIN CONTROL
The ODCOND register (Register 13-31) controls the open-drain feature of the port. Open drain operation is independently selected for each pin. When an ODCOND bit is set, the corresponding port output becomes an open drain driver capable of sinking current only. When an ODCOND bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

13.9.4 SLEW RATE CONTROL
The SLRCOND register (Register 13-32) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCOND bit is set, the corresponding port pin drive is slew rate limited. When an SLRCOND bit is cleared, the corresponding port pin drive slews at the maximum rate possible.

13.9.5 INPUT THRESHOLD CONTROL
The INLVLD register (Register 13-33) controls the input voltage threshold for each of the available PORTD input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTD register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Section TABLE 30-1: “Supply Voltage” for more information on threshold levels.

Note: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

13.9.6 PORTD FUNCTIONS AND OUTPUT PRIORITIES

Each PORTD pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 13-9.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority. Analog input and some digital input functions are not included in the list below. These input functions can remain active when the pin is configured as an output. Certain digital input functions override other port functions and are included in the priority list.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Function Priority(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RD0</td>
<td>RD0</td>
</tr>
<tr>
<td>RD1</td>
<td>OPA3OUT</td>
</tr>
<tr>
<td></td>
<td>RD1</td>
</tr>
<tr>
<td>RD2</td>
<td>RD2</td>
</tr>
<tr>
<td>RD3</td>
<td>RD3</td>
</tr>
<tr>
<td>RD4</td>
<td>PSMC3F</td>
</tr>
<tr>
<td></td>
<td>RD4</td>
</tr>
<tr>
<td>RD5</td>
<td>PSMC3E</td>
</tr>
<tr>
<td></td>
<td>RD5</td>
</tr>
<tr>
<td>RD6</td>
<td>PSMC3D</td>
</tr>
<tr>
<td></td>
<td>C3OUT</td>
</tr>
<tr>
<td></td>
<td>RD6</td>
</tr>
<tr>
<td>RD7</td>
<td>PSMC3C</td>
</tr>
<tr>
<td></td>
<td>C4OUT</td>
</tr>
<tr>
<td></td>
<td>RD7</td>
</tr>
</tbody>
</table>

Note 1: Priority listed from highest to lowest.
13.10 Register Definitions: PORTD

REGISTER 13-26: PORTD: PORTD REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>RD7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RD6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RD5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RD4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RD3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RD2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RD1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RD0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **1** = Port pin is > $V_{IH}$
- **0** = Port pin is < $V_{IL}$

Note 1: Writes to PORTD are actually written to corresponding LATD register. Reads from PORTD register is return of actual I/O pin values.

REGISTER 13-27: TRISD: PORTD TRI-STATE REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRISD7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TRISD6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TRISD5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TRISD4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TRISD3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TRISD2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TRISD1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TRISD0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

Note 1: PORTD pin configured as an input (tri-stated)
- **1** = PORTD pin configured as an output

REGISTER 13-28: LATD: PORTD DATA LATCH REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>LATD7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LATD6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LATD5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LATD4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LATD3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LATD2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LATD1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LATD0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

Note 1: Writes to PORTD are actually written to corresponding LATD register. Reads from PORTD register is return of actual I/O pin values.
### REGISTER 13-29: ANSELD: PORTD ANALOG SELECT REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ANSD2</td>
<td>ANSD1</td>
<td>ANSD0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-3**  
**Unimplemented:** Read as ‘0’

**bit 2-0**  
**ANSD<2:0>**: Analog Select between Analog or Digital Function on pins RD<2:0>, respectively
- **0** = Digital I/O. Pin is assigned to port or digital special function.
- **1** = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.

**Note 1:** When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

### REGISTER 13-30: WPUD: WEAK PULL-UP PORTD REGISTER

<table>
<thead>
<tr>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>WPUD7</td>
<td>WPUD6</td>
<td>WPUD5</td>
<td>WPUD4</td>
<td>WPUD3</td>
<td>WPUD2</td>
<td>WPUD1</td>
<td>WPUD0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-0**  
**WPUD<7:0>**: Weak Pull-up Register bits
- **1** = Pull-up enabled
- **0** = Pull-up disabled

**Note 1:** Global **WPUEN** bit of the **OPTION_REG** register must be cleared for individual pull-ups to be enabled.

**2:** The weak pull-up device is automatically disabled if the pin is in configured as an output.
### REGISTER 13-31: ODCOND: PORTD OPEN DRAIN CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>ODD7</th>
<th>ODD6</th>
<th>ODD5</th>
<th>ODD4</th>
<th>ODD3</th>
<th>ODD2</th>
<th>ODD1</th>
<th>ODD0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W</td>
<td>0/0</td>
<td>0/0</td>
<td>0/0</td>
<td>0/0</td>
<td>0/0</td>
<td>0/0</td>
<td>0/0</td>
<td>0/0</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

Bit 7-0 **ODD<7:0>:** PORTD Open Drain Enable bits
- For RD<7:0> pins, respectively
- 1 = Port pin operates as open-drain drive (sink current only)
- 0 = Port pin operates as standard push-pull drive (source and sink current)

### REGISTER 13-32: SLRCOND: PORTD SLEW RATE CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>SLRD7</th>
<th>SLRD6</th>
<th>SLRD5</th>
<th>SLRD4</th>
<th>SLRD3</th>
<th>SLRD2</th>
<th>SLRD1</th>
<th>SLRD0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W</td>
<td>1/1</td>
<td>1/1</td>
<td>1/1</td>
<td>1/1</td>
<td>1/1</td>
<td>1/1</td>
<td>1/1</td>
<td>1/1</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

Bit 7-0 **SLRD<7:0>:** PORTD Slew Rate Enable bits
- For RD<7:0> pins, respectively
- 1 = Port pin slew rate is limited
- 0 = Port pin slews at maximum rate

### REGISTER 13-33: INLVLD: PORTD INPUT LEVEL CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>INLVLD7</th>
<th>INLVLD6</th>
<th>INLVLD5</th>
<th>INLVLD4</th>
<th>INLVLD3</th>
<th>INLVLD2</th>
<th>INLVLD1</th>
<th>INLVLD0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W</td>
<td>1/1</td>
<td>1/1</td>
<td>1/1</td>
<td>1/1</td>
<td>1/1</td>
<td>1/1</td>
<td>1/1</td>
<td>1/1</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

Bit 7-0 **INLVLD<7:0>:** PORTD Input Level Select bits
- For RD<7:0> pins, respectively
- 1 = ST input used for PORT reads and interrupt-on-change
- 0 = TTL input used for PORT reads and interrupt-on-change
## TABLE 13-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSELD</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ANSD2</td>
<td>ANSD1</td>
<td>ANSD0 147</td>
</tr>
<tr>
<td>INLVLD</td>
<td>INLVLD7</td>
<td>INLVLD6</td>
<td>INLVLD5</td>
<td>INLVLD4</td>
<td>INLVLD3</td>
<td>INLVLD2</td>
<td>INLVLD1</td>
<td>INLVLD0</td>
<td>148</td>
</tr>
<tr>
<td>LATD</td>
<td>LATD7</td>
<td>LATD6</td>
<td>LATD5</td>
<td>LATD4</td>
<td>LATD3</td>
<td>LATD2</td>
<td>LATD1</td>
<td>LATD0</td>
<td>146</td>
</tr>
<tr>
<td>ODCOND</td>
<td>ODD7</td>
<td>ODD6</td>
<td>ODD5</td>
<td>ODD4</td>
<td>ODD3</td>
<td>ODD2</td>
<td>ODD1</td>
<td>ODD0</td>
<td>148</td>
</tr>
<tr>
<td>PORTD</td>
<td>RD7</td>
<td>RD6</td>
<td>RD5</td>
<td>RD4</td>
<td>RD3</td>
<td>RD2</td>
<td>RD1</td>
<td>RD0</td>
<td>146</td>
</tr>
<tr>
<td>SLRCOND</td>
<td>SLRD7</td>
<td>SLRD6</td>
<td>SLRD5</td>
<td>SLRD4</td>
<td>SLRD3</td>
<td>SLRD2</td>
<td>SLRD1</td>
<td>SLRD0</td>
<td>148</td>
</tr>
<tr>
<td>TRISD</td>
<td>TRISD7</td>
<td>TRISD6</td>
<td>TRISD5</td>
<td>TRISD4</td>
<td>TRISD3</td>
<td>TRISD2</td>
<td>TRISD1</td>
<td>TRISD0</td>
<td>146</td>
</tr>
<tr>
<td>WPUD</td>
<td>WPUD7</td>
<td>WPUD6</td>
<td>WPUD5</td>
<td>WPUD4</td>
<td>WPUD3</td>
<td>WPUD2</td>
<td>WPUD1</td>
<td>WPUD0</td>
<td>147</td>
</tr>
</tbody>
</table>

**Legend:**  
- \( \times \) = unknown, \( u \) = unchanged, \(-\) = unimplemented locations read as ‘0’. Shaded cells are not used by PORTD.
13.11 PORTE Registers

RE3 is input only, and also functions as MCLR. The MCLR feature can be disabled via a configuration fuse. RE3 also supplies the programming voltage. The TRIS bit for RE3 (TRISE3) always reads ‘1’.

13.11.1 DATA REGISTER

PORTE is an 8-bit wide bidirectional port. The corresponding data direction register is TRISE (Register 13-35). Setting a TRISE bit (= 1) will make the corresponding PORTE pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISE bit (= 0) will make the corresponding PORTE pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 13-1 shows how to initialize an I/O port.

Reading the PORTE register (Register 13-34) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATE).

13.11.2 DIRECTION CONTROL

The TRISE register (Register 13-35) controls the PORTE pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISE register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read ‘0’.

13.11.3 OPEN DRAIN CONTROL

The ODCONE register (Register 13-31) controls the open-drain feature of the port. Open drain operation is independently selected for each pin. When an ODCONE bit is set, the corresponding port output becomes an open drain driver capable of sinking current only. When an ODCONE bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

13.11.4 SLEW RATE CONTROL

The SLRCOND register (Register 13-32) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCOND bit is set, the corresponding port pin drive is slew rate limited. When an SLRCOND bit is cleared, the corresponding port pin drive slews at the maximum rate possible.

13.11.5 INPUT THRESHOLD CONTROL

The INLVLD register (Register 13-33) controls the input voltage threshold for each of the available PORTD input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTD register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Section 30.1 “DC Characteristics: PIC16(L)F1784/6/7-I/E (Industrial, Extended)” for more information on threshold levels.

Note: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

13.11.6 INPUT THRESHOLD CONTROL

The INLVLE register (Register 13-41) controls the input voltage threshold for each of the available PORTE input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTE register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Section TABLE 30-1: “Supply Voltage” for more information on threshold levels.

Note: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.
13.11.7 PORTE FUNCTIONS AND OUTPUT PRIORITIES(1)

Each PORTE pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 13-11.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority. Analog input and some digital input functions are not included in the list below. These input functions can remain active when the pin is configured as an output. Certain digital input functions override other port functions and are included in the priority list.

Note 1: Applies to 40/44-pin devices only.

TABLE 13-11: PORTE OUTPUT PRIORITY

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Function Priority(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RE0</td>
<td>CCP3 RE0</td>
</tr>
<tr>
<td>RE1</td>
<td>PSMC3B RE1</td>
</tr>
<tr>
<td>RE2</td>
<td>PSMC3A RE2</td>
</tr>
</tbody>
</table>

Note 1: Priority listed from highest to lowest.
13.12 Register Definitions: PORTE

REGISTER 13-34: PORTE: PORTE REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>RE3(1)</td>
<td>RE2(1)</td>
<td>RE1(1)</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared

bit 7-4  Unimplemented: Read as ‘0’
bit 3-0  RE<3:0>: PORTE Input Pin bit(1)

1 = Port pin is > VIH
0 = Port pin is < VIL

Note 1:  RE<2:0> are available on PIC16(L)F1784/7 only.

REGISTER 13-35: TRISE: PORTE TRI-STATE REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-1(1)</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TRISE2(2)</td>
<td>TRISE1(2)</td>
<td>TRISE0(2)</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set  ‘0’ = Bit is cleared

bit 7-4  Unimplemented: Read as ‘0’
bit 3  Unimplemented: Read as ‘1’
bit 2-0  TRISA<2:0>: PORTA Tri-State Control bit(2)

1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

Note 1:  Unimplemented, read as ‘1’.

2:  TRISE<2:0> are available on PIC16(L)F1784/7 only.
REGISTER 13-36: LATE: PORTE DATA LATCH REGISTER(2)

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>LATE2</td>
<td>LATE1</td>
<td>LATE0</td>
</tr>
</tbody>
</table>

bit 7

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

bit 7-3 **Unimplemented**: Read as '0'

bit 2-0 **LATE<2:0>:** PORTE Output Latch Value bits(2)

**Note 1:** Writes to PORTE are actually written to corresponding LATE register. Reads from PORTE register is return of actual I/O pin values.

**Note 2:** LATE<2:0> are available on PIC16(L)F1784/7 only.

REGISTER 13-37: ANSELE: PORTE ANALOG SELECT REGISTER(2)

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ANSE2</td>
<td>ANSE1</td>
<td>ANSE0</td>
</tr>
</tbody>
</table>

bit 7

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

bit 7-3 **Unimplemented**: Read as '0'

bit 2-0 **ANSE<2:0>:** Analog Select between Analog or Digital Function on pins RE<2:0>, respectively

- 0 = Digital I/O. Pin is assigned to port or digital special function.
- 1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.

**Note 1:** When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

**Note 2:** ANSE<2:0> are available on PIC16(L)F1784/7 only.
### REGISTER 13-38: WPUE: WEAK PULL-UP PORT E REGISTER

| bit 7-4 | Unimplemented: Read as '0' |
| bit 3-0 | WPUE<3:0>: Weak Pull-up Register bit(3) |
|         | 1 = Pull-up enabled |
|         | 0 = Pull-up disabled |

#### Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

#### Note 1:

- Global WPUEN bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
- The weak pull-up device is automatically disabled if the pin is in configured as an output.
- WPUSE<2:0> are available on PIC16(L)F1784/7 only.

### REGISTER 13-39: ODCONE: PORT E OPEN DRAIN CONTROL REGISTER(1)

| bit 7-3 | Unimplemented: Read as '0' |
| bit 2-0 | ODE<2:0>: PORT E Open Drain Enable bits |
|         | For RE<2:0> pins, respectively |
|         | 1 = Port pin operates as open-drain drive (sink current only) |
|         | 0 = Port pin operates as standard push-pull drive (source and sink current) |

#### Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

#### Note 1:

- ODCONE<2:0> are available on PIC16(L)F1784/7 only.
### REGISTER 13-40: SLRCONE: PORTE SLEW RATE CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7-3</th>
<th>Bit 2-0</th>
<th>Unimplemented: Read as '0'</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLRE&lt;2:0&gt;: PORTE Slew Rate Enable bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td>For RE&lt;2:0&gt; pins, respectively</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 = Port pin slew rate is limited</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = Port pin slews at maximum rate</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** SLRE<2:0> are available on PIC16(L)F1784/7 only.

### REGISTER 13-41: INLVLE: PORTE INPUT LEVEL CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7-4</th>
<th>Bit 3-0</th>
<th>Unimplemented: Read as '0'</th>
</tr>
</thead>
<tbody>
<tr>
<td>INLVLE&lt;3:0&gt;: PORTE Input Level Select bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 = ST input used for PORT reads and interrupt-on-change</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = TTL input used for PORT reads and interrupt-on-change</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** INLVLE<2:0> are available on PIC16(L)F1784/7 only.

### TABLE 13-12: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADCON0</td>
<td>ADRMD</td>
<td>CHS&lt;4:0&gt;</td>
<td>GO/DONE</td>
<td>ADON</td>
<td>172</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ANSELE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ANSE2</td>
<td>ANSE1</td>
<td>ANSE0</td>
<td>153</td>
</tr>
<tr>
<td>INLVLE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>INLVLE3</td>
<td>INLVLE2(1)</td>
<td>INLVLE1(1)</td>
<td>INLVLE0(1)</td>
</tr>
<tr>
<td>LATE&lt;2(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LATE2</td>
<td>LATE1</td>
<td>LATE0</td>
<td>153</td>
</tr>
<tr>
<td>ODCONE&lt;2(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ODE2</td>
<td>ODE1</td>
<td>ODE0</td>
<td>154</td>
</tr>
<tr>
<td>PORTE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RE3</td>
<td>RE1(2)</td>
<td>RE0(2)</td>
<td>152</td>
</tr>
<tr>
<td>SLRCONE&lt;2(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SLRE2</td>
<td>SLRE1</td>
<td>SLRE0</td>
<td>155</td>
</tr>
<tr>
<td>TRISE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TRISE2(2)</td>
<td>TRISE1(2)</td>
<td>TRISE0(2)</td>
<td>152</td>
</tr>
<tr>
<td>WPUE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>WPUE3</td>
<td>WPUE2(2)</td>
<td>WPUE1(2)</td>
<td>WPUE0(2)</td>
</tr>
</tbody>
</table>

**Legend:**
- x = unknown, u = unchanged, – = unimplemented locations read as ‘0’. Shaded cells are not used by PORTE.

**Note 1:** Unimplemented, read as ‘1’.

**Note 2:** PIC16(L)F1784/7 only
14.0 INTERRUPT-ON-CHANGE

All pins on all ports can be configured to operate as Interrupt-On-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual pin, or combination of pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- Rising and falling edge detection
- Individual pin interrupt flags

Figure 14-1 is a block diagram of the IOC module.

14.1 Enabling the Module

To allow individual pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

14.2 Individual Pin Configuration

For each pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCxP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCxN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting the associated bits in both of the IOCxP and IOCxN registers.

14.3 Interrupt Flags

The bits located in the IOCxF registers are status flags that correspond to the Interrupt-on-change pins of each port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCxF bits.

14.4 Clearing Interrupt Flags

The individual status flags, (IOCxF register bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

**EXAMPLE 14-1: CLEARING INTERRUPT FLAGS (PORTA EXAMPLE)**

```
MOVLW 0xff
XORWF IOCAF, W
ANDWF IOCAF, F
```

14.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set. If an edge is detected while in Sleep mode, the affected IOCxF register will be updated prior to the first instruction executed out of Sleep.
FIGURE 14-1: INTERRUPT-ON-CHANGE BLOCK DIAGRAM

- Data bus = 0 or 1
- Write IOCBFx edge detect
- Edge detect from all other IOCBFx individual pin detectors
- IOC interrupt to CPU core
14.6 Register Definitions: Interrupt-on-Change Control

REGISTER 14-1: IOCxP: INTERRUPT-ON-CHANGE POSITIVE EDGE REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOCxP7</td>
<td>IOCxP6</td>
<td>IOCxP5</td>
<td>IOCxP4</td>
<td>IOCxP3</td>
<td>IOCxP2</td>
<td>IOCxP1</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
u = Bit is unchanged
x = Bit is unknown
-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set
‘0’ = Bit is cleared

bit 7-0 IOCxP<7:0>: Interrupt-on-Change Positive Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a positive going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin.

Note 1: For IOCEP register, bit 3 (IOCEP3) is the only implemented bit in the register.

REGISTER 14-2: IOCxN: INTERRUPT-ON-CHANGE NEGATIVE EDGE REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOCxN7</td>
<td>IOCxN6</td>
<td>IOCxN5</td>
<td>IOCxN4</td>
<td>IOCxN3</td>
<td>IOCxN2</td>
<td>IOCxN1</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
u = Bit is unchanged
x = Bit is unknown
-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set
‘0’ = Bit is cleared

bit 7-0 IOCxN<7:0>: Interrupt-on-Change Negative Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a negative going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin.

Note 1: For IOCEN register, bit 3 (IOCEN3) is the only implemented bit in the register.
REGISTERS 14-3: IOCxF: INTERRUPT-ON-CHANGE FLAG REGISTER

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>IOCxF&lt;7:0&gt;: Interrupt-on-Change Flag bits(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>An enabled change was detected on the associated pin. Set when IOCxPx = 1 and a rising edge was detected RBx, or when IOCxNx = 1 and a falling edge was detected on RBx.</td>
</tr>
<tr>
<td>0</td>
<td>No change was detected, or the user cleared the detected change.</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **HS** - Bit is set in hardware

Note 1: For IOCEF register, bit 3 (IOCEF3) is the only implemented bit in the register.

TABLE 14-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPT-ON-CHANGE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSELB</td>
<td>—</td>
<td>ANSB6</td>
<td>ANSB5</td>
<td>ANSB4</td>
<td>ANSB3</td>
<td>ANSB2</td>
<td>ANSB1</td>
<td>ANSB0</td>
<td>138</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMROIE</td>
<td>INTF</td>
<td>IOCIF</td>
<td>93</td>
</tr>
<tr>
<td>IOCAF</td>
<td>IOCAF7</td>
<td>IOCAF6</td>
<td>IOCAF5</td>
<td>IOCAF4</td>
<td>IOCAF3</td>
<td>IOCAF2</td>
<td>IOCAF1</td>
<td>IOCAF0</td>
<td>159</td>
</tr>
<tr>
<td>IOCAN</td>
<td>IOCAN7</td>
<td>IOCAN6</td>
<td>IOCAN5</td>
<td>IOCAN4</td>
<td>IOCAN3</td>
<td>IOCAN2</td>
<td>IOCAN1</td>
<td>IOCAN0</td>
<td>158</td>
</tr>
<tr>
<td>IOCAP</td>
<td>IOCAP7</td>
<td>IOCAP6</td>
<td>IOCAP5</td>
<td>IOCAP4</td>
<td>IOCAP3</td>
<td>IOCAP2</td>
<td>IOCAP1</td>
<td>IOCAP0</td>
<td>158</td>
</tr>
<tr>
<td>IOCBF</td>
<td>IOCBF7</td>
<td>IOCBF6</td>
<td>IOCBF5</td>
<td>IOCBF4</td>
<td>IOCBF3</td>
<td>IOCBF2</td>
<td>IOCBF1</td>
<td>IOCBF0</td>
<td>159</td>
</tr>
<tr>
<td>IOCBN</td>
<td>IOCBN7</td>
<td>IOCBN6</td>
<td>IOCBN5</td>
<td>IOCBN4</td>
<td>IOCBN3</td>
<td>IOCBN2</td>
<td>IOCBN1</td>
<td>IOCBN0</td>
<td>158</td>
</tr>
<tr>
<td>IOCBP</td>
<td>IOCBP7</td>
<td>IOCBP6</td>
<td>IOCBP5</td>
<td>IOCBP4</td>
<td>IOCBP3</td>
<td>IOCBP2</td>
<td>IOCBP1</td>
<td>IOCBP0</td>
<td>158</td>
</tr>
<tr>
<td>IOCCF</td>
<td>IOCCF7</td>
<td>IOCCF6</td>
<td>IOCCF5</td>
<td>IOCCF4</td>
<td>IOCCF3</td>
<td>IOCCF2</td>
<td>IOCCF1</td>
<td>IOCCF0</td>
<td>159</td>
</tr>
<tr>
<td>IOCCN</td>
<td>IOCCN7</td>
<td>IOCCN6</td>
<td>IOCCN5</td>
<td>IOCCN4</td>
<td>IOCCN3</td>
<td>IOCCN2</td>
<td>IOCCN1</td>
<td>IOCCN0</td>
<td>158</td>
</tr>
<tr>
<td>IOCCP</td>
<td>IOCCP7</td>
<td>IOCCP6</td>
<td>IOCCP5</td>
<td>IOCCP4</td>
<td>IOCCP3</td>
<td>IOCCP2</td>
<td>IOCCP1</td>
<td>IOCCP0</td>
<td>158</td>
</tr>
<tr>
<td>IOCEF</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>159</td>
</tr>
<tr>
<td>IOCEN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>158</td>
</tr>
<tr>
<td>IOCEP</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>158</td>
</tr>
<tr>
<td>TRISB</td>
<td>TRISB7</td>
<td>TRISB6</td>
<td>TRISB5</td>
<td>TRISB4</td>
<td>TRISB3</td>
<td>TRISB2</td>
<td>TRISB1</td>
<td>TRISB0</td>
<td>137</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by interrupt-on-change.
15.0 FIXED VOLTAGE REFERENCE (FVR)

The Fixed Voltage Reference, or FVR, is a stable voltage reference, independent of VDD, with 1.024V, 2.048V or 4.096V selectable output levels. The output of the FVR can be configured to supply a reference voltage to the following:

• ADC input channel
• ADC positive reference
• Comparator positive input
• Digital-to-Analog Converter (DAC)

The FVR can be enabled by setting the FVREN bit of the FVRCON register.

15.1 Independent Gain Amplifiers

The output of the FVR supplied to the ADC, Comparators, and DAC is routed through two independent programmable gain amplifiers. Each amplifier can be programmed for a gain of 1x, 2x or 4x, to produce the three possible voltage levels.

The ADFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the ADC module. Reference Section 17.0 “Analog-to-Digital Converter (ADC) Module” for additional information.

The CDAFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the DAC and comparator module. Reference Section 19.0 “Digital-to-Analog Converter (DAC) Module” and Section 20.0 “Comparator Module” for additional information.

15.2 FVR Stabilization Period

When the Fixed Voltage Reference module is enabled, it requires time for the reference and amplifier circuits to stabilize. Once the circuits stabilize and are ready for use, the FVRRDY bit of the FVRCON register will be set. See Section 30.0 “Electrical Specifications” for the minimum delay requirement.

15.3 FVR Buffer Stabilization Period

When either FVR Buffer1 or FVR Buffer 2 is enabled, the buffer amplifier circuits require 30 μs to stabilize. This stabilization time is required even when the FVR is already operating and stable.
FIGURE 15-1: VOLTAGE REFERENCE BLOCK DIAGRAM

TABLE 15-1: PERIPHERALS REQUIRING THE FIXED VOLTAGE REFERENCE (FVR)

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Conditions</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HFINTOSC</td>
<td>FOSC&lt;2:0&gt; = 100 and IRCF&lt;3:0&gt; ≠ 000x</td>
<td>INTOSC is active and device is not in Sleep</td>
</tr>
<tr>
<td></td>
<td>BOREN&lt;1:0&gt; = 11</td>
<td>BOR always enabled</td>
</tr>
<tr>
<td></td>
<td>BOREN&lt;1:0&gt; = 10 and BORFS = 1</td>
<td>BOR disabled in Sleep mode, BOR Fast Start enabled.</td>
</tr>
<tr>
<td></td>
<td>BOREN&lt;1:0&gt; = 01 and BORFS = 1</td>
<td>BOR under software control, BOR Fast Start enabled</td>
</tr>
<tr>
<td>BOR</td>
<td>All PIC16F1784/6/7 devices, when VREGPM = 1 and not in Sleep</td>
<td>The device runs off of the ULP regulator when in Sleep mode.</td>
</tr>
<tr>
<td>LDO</td>
<td>PxC SRC&lt;1:0&gt;</td>
<td>64 MHz clock forces HFINTOSC on during Sleep.</td>
</tr>
</tbody>
</table>
15.4 Register Definitions: FVR Control

**REGISTER 15-1:  FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>FVREN</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fixed Voltage Reference Enable bit</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Fixed Voltage Reference is enabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Fixed Voltage Reference is disabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>FVRRDY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fixed Voltage Reference Ready Flag bit</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Fixed Voltage Reference output is ready for use</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Fixed Voltage Reference output is not ready or not enabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TSEN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Temperature Indicator Enable bit</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Temperature Indicator is enabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Temperature Indicator is disabled</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TSRNG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Temperature Indicator Range Selection bit</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = VOUT = VDD - 4VT (High Range)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = VOUT = VDD - 2VT (Low Range)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CDAFVR&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Comparator and DAC Fixed Voltage Reference Selection bit</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>11 = Comparator and DAC Fixed Voltage Reference Peripheral output is 4x (4.096V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10 = Comparator and DAC Fixed Voltage Reference Peripheral output is 2x (2.048V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>01 = Comparator and DAC Fixed Voltage Reference Peripheral output is 1x (1.024V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>00 = Comparator and DAC Fixed Voltage Reference Peripheral output is off.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ADFVR&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ADC Fixed Voltage Reference Selection bit</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>11 = ADC Fixed Voltage Reference Peripheral output is 4x (4.096V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10 = ADC Fixed Voltage Reference Peripheral output is 2x (2.048V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>01 = ADC Fixed Voltage Reference Peripheral output is 1x (1.024V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>00 = ADC Fixed Voltage Reference Peripheral output is off.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- q = Value depends on condition
- q = Value depends on condition

Note 1: FVRRDY is always ‘1’ on “F” devices only.
Note 2: Fixed Voltage Reference output cannot exceed VDD.
Note 3: See Section 16.0 “Temperature Indicator Module” for additional information.

**TABLE 15-2: SUMMARY OF REGISTERS ASSOCIATED WITH FIXED VOLTAGE REFERENCE**

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>FVRCON</td>
<td>FVREN</td>
<td>FVRRDY</td>
<td>TSEN</td>
<td>TSRNG</td>
<td>CDAFVR&lt;1:0&gt;</td>
<td>ADFVR&lt;1:0&gt;</td>
<td></td>
<td></td>
<td>162</td>
</tr>
</tbody>
</table>

**Legend:** Shaded cells are not used with the Fixed Voltage Reference.
16.0 TEMPERATURE INDICATOR MODULE

This family of devices is equipped with a temperature circuit designed to measure the operating temperature of the silicon die. The circuit’s range of operating temperature falls between -40°C and +85°C. The output is a voltage that is proportional to the device temperature. The output of the temperature indicator is internally connected to the device ADC.

The circuit may be used as a temperature threshold detector or a more accurate temperature indicator, depending on the level of calibration performed. A one-point calibration allows the circuit to indicate a temperature closely surrounding that point. A two-point calibration allows the circuit to sense the entire range of temperature more accurately. Reference Application Note AN1333, “Use and Calibration of the Internal Temperature Indicator” (DS01333) for more details regarding the calibration process.

16.1 Circuit Operation

Figure 16-1 shows a simplified block diagram of the temperature circuit. The proportional voltage output is achieved by measuring the forward voltage drop across multiple silicon junctions.

Equation 16-1 describes the output characteristics of the temperature indicator.

**EQUATION 16-1: VOUT RANGES**

<table>
<thead>
<tr>
<th>Range</th>
<th>Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Range</td>
<td>VOUT = VDD - 4VT</td>
</tr>
<tr>
<td>Low Range</td>
<td>VOUT = VDD - 2VT</td>
</tr>
</tbody>
</table>

The temperature sense circuit is integrated with the Fixed Voltage Reference (FVR) module. See Section 15.0 “Fixed Voltage Reference (FVR)” for more information.

The circuit is enabled by setting the TSEN bit of the FVRCON register. When disabled, the circuit draws no current.

The circuit operates in either high or low range. The high range, selected by setting the TSRNG bit of the FVRCON register, provides a wider output voltage. This provides more resolution over the temperature range, but may be less consistent from part to part. This range requires a higher bias voltage to operate and thus, a higher VDD is needed.

The low range is selected by clearing the TSRNG bit of the FVRCON register. The low range generates a lower voltage drop and thus, a lower bias voltage is needed to operate the circuit. The low range is provided for low-voltage operation.

16.2 Minimum Operating VDD

When the temperature circuit is operated in low range, the device may be operated at any operating voltage that is within specifications.

When the temperature circuit is operated in high range, the device operating voltage, VDD, must be high enough to ensure that the temperature circuit is correctly biased.

Table 16-1 shows the recommended minimum VDD vs. range setting.

**TABLE 16-1: RECOMMENDED VDD VS. RANGE**

<table>
<thead>
<tr>
<th>Min. VDD, TSRNG = 1</th>
<th>Min. VDD, TSRNG = 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.6V</td>
<td>1.8V</td>
</tr>
</tbody>
</table>

16.3 Temperature Output

The output of the circuit is measured using the internal Analog-to-Digital Converter. A channel is reserved for the temperature circuit output. Refer to Section 17.0 “Analog-to-Digital Converter (ADC) Module” for detailed information.

16.4 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait at least 200 μs after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200 μs between sequential conversions of the temperature indicator output.
### TABLE 16-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE TEMPERATURE INDICATOR

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>FVRCON</td>
<td></td>
<td>FVREN</td>
<td>FVRDY</td>
<td>TSEN</td>
<td>TSRNG</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ADFVR&lt;1:0&gt; 161</td>
</tr>
</tbody>
</table>

**Legend:** Shaded cells are unused by the temperature indicator module.
17.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of a single-ended and differential analog input signals to a 12-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 12-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESH:ADRESL register pair). Figure 17-1 shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

**Note 1:** When ADON = 0, all multiplexer inputs are disconnected. PIC16(L)F1784/7 only.

**Note 2:** See ADCON0 register (Register 17-1) and ADCON2 register (Register 17-3) for detailed analog channel selection per device.
17.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port configuration
- Channel selection
  - Single-ended
  - Differential
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Result formatting

17.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. Refer to Section 13.0 “I/O Ports” for more information.

17.1.2 CHANNEL SELECTION

There are up to 18 channel selections available:

- AN<13:8, 4:0> pins (PIC16(L)F1786 only)
- AN<21, 13:0> pins (PIC16(L)F1784/7 only)
- Temperature Indicator
- DAC_output
- FVR (Fixed Voltage Reference) Output

Refer to Section 15.0 “Fixed Voltage Reference (FVR)” and Section 16.0 “Temperature Indicator Module” for more information on these channel selections.

When converting differential signals, the negative input for the channel is selected with the CHSN<3:0> bits of the ADCON2 register. Any positive input can be paired with any negative input to determine the differential channel.

The CHS<4:0> bits of the ADCON0 register determine which positive channel is selected.

When CHSN<3:0> = 1111 then the ADC is effectively a single ended ADC converter.

When changing channels, a delay is required before starting the next conversion.

17.1.3 ADC VOLTAGE REFERENCE

The ADPREF bits of the ADCON1 register provide control of the positive voltage reference. The positive voltage reference can be:

- VREF+
- VDD
- FVR Buffer1

The ADNREF bits of the ADCON1 register provide control of the negative voltage reference. The negative voltage reference can be:

- VREF- pin
- VSS

See Section 15.0 “Fixed Voltage Reference (FVR)” for more details on the Fixed Voltage Reference.

17.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ADCON1 register. There are seven possible clock options:

- FOSC/2
- FOSC/4
- FOSC/8
- FOSC/16
- FOSC/32
- FOSC/64
- FRC (dedicated internal FRC oscillator)

The time to complete one bit conversion is defined as TAD. One full 12-bit conversion requires 15 TAD periods as shown in Figure 17-2.

For correct conversion, the appropriate TAD specification must be met. Refer to the ADC conversion requirements in Section 30.0 “Electrical Specifications” for more information. Table 17-1 gives examples of appropriate ADC clock selections.

Note: Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.
## TABLE 17-1: ADC CLOCK PERIOD (TAD) VS. DEVICE OPERATING FREQUENCIES

<table>
<thead>
<tr>
<th>ADC Clock Source</th>
<th>ADCS&lt;2:0&gt;</th>
<th>32 MHz</th>
<th>20 MHz</th>
<th>16 MHz</th>
<th>8 MHz</th>
<th>4 MHz</th>
<th>1 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>FOSC/2</td>
<td>000</td>
<td>62.5 ns</td>
<td>100 ns</td>
<td>125 ns</td>
<td>250 ns</td>
<td>500 ns</td>
<td>2.0 μs</td>
</tr>
<tr>
<td>FOSC/4</td>
<td>100</td>
<td>125 ns</td>
<td>200 ns</td>
<td>250 ns</td>
<td>500 ns</td>
<td>1.0 μs</td>
<td>4.0 μs</td>
</tr>
<tr>
<td>FOSC/8</td>
<td>001</td>
<td>0.5 μs</td>
<td>400 ns</td>
<td>0.5 μs</td>
<td>1.0 μs</td>
<td>2.0 μs</td>
<td>8.0 μs</td>
</tr>
<tr>
<td>FOSC/16</td>
<td>101</td>
<td>800 ns</td>
<td>800 ns</td>
<td>1.0 μs</td>
<td>2.0 μs</td>
<td>4.0 μs</td>
<td>16.0 μs</td>
</tr>
<tr>
<td>FOSC/32</td>
<td>010</td>
<td>1.0 μs</td>
<td>1.6 μs</td>
<td>2.0 μs</td>
<td>4.0 μs</td>
<td>8.0 μs</td>
<td>32.0 μs</td>
</tr>
<tr>
<td>FOSC/64</td>
<td>110</td>
<td>2.0 μs</td>
<td>3.2 μs</td>
<td>4.0 μs</td>
<td>8.0 μs</td>
<td>16.0 μs</td>
<td>64.0 μs</td>
</tr>
<tr>
<td>FRC</td>
<td>x11</td>
<td>1.0-6.0 μs</td>
<td>1.0-6.0 μs</td>
<td>1.0-6.0 μs</td>
<td>1.0-6.0 μs</td>
<td>1.0-6.0 μs</td>
<td></td>
</tr>
</tbody>
</table>

Legend: Shaded cells are outside of recommended range.

Note 1: The FRC source has a typical TAD time of 1.6 μs for VDD.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

4: The ADC clock period (TAD) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock FOSC. However, the FRC oscillator source must be used when conversions are to be performed with the device in Sleep mode.

## FIGURE 17-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES

On the following cycle:
GO bit is cleared, ADIF bit is set, holding capacitor is connected to analog input.
17.1.5 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC Interrupt Flag is the ADIF bit in the PIR1 register. The ADC Interrupt Enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

**Note 1:** The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.

**Note 2:** The ADC operates during Sleep only when the FRC oscillator is selected.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the GIE and PEIE bits of the INTCON register must be disabled. If the GIE and PEIE bits of the INTCON register are enabled, execution will switch to the Interrupt Service Routine.

17.1.6 RESULT FORMATTING

The 10-bit and 12-bit ADC conversion results can be supplied in two formats: 2's complement or sign-magnitude. The ADFM bit of the ADCON1 register controls the output format. Sign magnitude is left justified with the sign bit in the LSb position. Negative numbers are indicated when the sign bit is '1'. Two's complement is right justified with the sign extended into the Most Significant bits.

Figure 17-3 shows the two output formats. Table 17-2 shows conversion examples.
### TABLE 17-2: ADC OUTPUT RESULTS FORMAT

<table>
<thead>
<tr>
<th>Absolute ADC Value (decimal)</th>
<th>Sign and Magnitude Result ADFM = 0, ADRMD = 0</th>
<th>2’s Compliment Result ADFM = 1, ADRMD = 0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ADRESH (ADRES&lt;15:8&gt;)</td>
<td>ADRESL (ADRES&lt;7:0&gt;)</td>
</tr>
<tr>
<td>+ 4095</td>
<td>1111 1111</td>
<td>1111 0000</td>
</tr>
<tr>
<td>+ 2355</td>
<td>1001 0011</td>
<td>0011 0000</td>
</tr>
<tr>
<td>+ 0001</td>
<td>0000 0000</td>
<td>0001 0000</td>
</tr>
<tr>
<td>0000</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>- 0001</td>
<td>0000 0000</td>
<td>0001 0011</td>
</tr>
<tr>
<td>- 4095</td>
<td>1111 1111</td>
<td>1111 0001</td>
</tr>
<tr>
<td>- 4096</td>
<td>0000 0000</td>
<td>0000 0001</td>
</tr>
</tbody>
</table>

**Note 1:** For the RSD ADC, the raw 13-bits from the ADC is presented in 2’s compliment format, so no data translation is required for 2’s compliment results.

**Note 2:** For the SAR ADC, the raw 13-bits from the ADC is presented in sign and magnitude format, so no data translation is required for sign and magnitude results.
17.2 ADC Operation

17.2.1 STARTING A CONVERSION
To enable the ADC module, the ADON bit of the ADCON0 register must be set to a ‘1’. Setting the GO/DONE bit of the ADCON0 register to a ‘1’ will clear the ADRESH and ADRESL registers and start the Analog-to-Digital conversion.

Note: The GO/DONE bit should not be set in the same instruction that turns on the ADC. Refer to Section 17.2.6 “A/D Conversion Procedure”.

17.2.2 COMPLETION OF A CONVERSION
When the conversion is complete, the ADC module will:
• Clear the GO/DONE bit
• Set the ADIF Interrupt Flag bit

17.2.3 TERMINATING A CONVERSION
When a conversion is terminated before completion by clearing the GO/DONE bit then the partial results are discarded and the results in the ADRESH and ADRESL registers from the previous conversion remain unchanged.

Note: A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

17.2.4 ADC OPERATION DURING SLEEP
The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC oscillator source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

17.2.5 AUTO-CONVERSION TRIGGER
The Auto-conversion Trigger allows periodic ADC measurements without software intervention. When a rising edge of the selected source occurs, the GO/DONE bit is set by hardware.

The Auto-conversion Trigger source is selected with the TRIGSEL<3:0> bits of the ADCON2 register.

Using the Auto-conversion Trigger does not assure proper ADC timing. It is the user’s responsibility to ensure that the ADC timing requirements are met.

Auto-conversion sources are:
• CCP1
• CCP2
• CCP3
• PSMC1(1)
• PSMC2(1)

Note: The PSMC clock frequency, after the prescaler, must be less than Fosc/4 to ensure that the ADC detects the auto-conversion trigger. This limitation can be overcome by synchronizing a slave PSMC, running at the required slower clock frequency, to the first PSMC and triggering the conversion from the slave PSMC.

• PSMC3
17.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
   - Disable pin output driver (Refer to the TRIS register)
   - Configure pin as analog (Refer to the ANSEL register)

2. Configure the ADC module:
   - Select ADC conversion clock
   - Configure voltage reference
   - Select ADC input channel
   - Turn on ADC module

3. Configure ADC interrupt (optional):
   - Clear ADC interrupt flag
   - Enable ADC interrupt
   - Enable peripheral interrupt
   - Enable global interrupt(1)

4. Wait the required acquisition time(2).

5. Start conversion by setting the GO/DONE bit.

6. Wait for ADC conversion to complete by one of the following:
   - Polling the GO/DONE bit
   - Waiting for the ADC interrupt (interrupts enabled)

7. Read ADC Result.

8. Clear the ADC interrupt flag (required if interrupt is enabled).

---

**EXAMPLE 17-1: A/D CONVERSION**

```asm
; This code block configures the ADC for polling, Vdd and Vss references, Frc clock and AN0 input.
; Conversion start & polling for completion are included.
; BANKSEL ADCON1 ;
MOVLW B'11110000' ; 2's complement, Frc clock
MOVWF ADCON1 ;
MOVLW B'00001111' ; set negative input
MOVWF ADCON2 ; to negative reference
BANKSEL TRISA ;
BSF TRISA,0 ; Set RA0 to input
BANKSEL ANSEL ;
BSF ANSEL,0 ; Set RA0 to analog
BANKSEL ADCON0 ;
MOVLW B'00000001' ; Select channel AN0
MOVWF ADCON0 ; Turn ADC on
CALL SampleTime ; Acquisition delay
BSF ADCON0,ADGO ; Start conversion
BTFSC ADCON0,ADGO ; Is conversion done?
GOTO $-1 ; No, test again
BANKSEL ADRESH ;
MOVF ADRESH,W ; Read upper 2 bits
MOVWF RESULTHI ; Store in GPR space
```

---

**Note 1:** The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

**Note 2:** Refer to Section 17.4 “ADC Acquisition Requirements”.
17.3 Register Definitions: ADC Control

REGISTER 17-1: ADCON0: ADC CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6-2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADRMD: ADC Result Mode bit</td>
<td>CHS&lt;4:0&gt;: Positive Differential Input Channel Select bits</td>
<td>GO/DONE: ADC Conversion Status bit</td>
<td>ADON: ADC Enable bit</td>
</tr>
<tr>
<td>1 = ADRESL and ADRESH provide data formatted for a 10-bit result</td>
<td>111111 = FVR (Fixed Voltage Reference) Buffer 1 Output(3)</td>
<td>1 = ADC conversion cycle in progress. Setting this bit starts an ADC conversion cycle. This bit is automatically cleared by hardware when the ADC conversion has completed.</td>
<td>1 = ADC is enabled</td>
</tr>
<tr>
<td>0 = ADRESL and ADRESH provide data formatted for a 12-bit result</td>
<td>111110 = DAC_output(2)</td>
<td>0 = ADC conversion completed/not in progress</td>
<td>0 = ADC is disabled and consumes no operating current</td>
</tr>
<tr>
<td>See Figure 17-3 for details</td>
<td>11101 = Temperature Indicator(4)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>11100 = Reserved. No channel connected.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>•</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10110 = Reserved. No channel connected</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10101 = AN21(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10100 = Reserved. No channel connected</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>•</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>01110 = Reserved. No channel connected.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>01101 = AN13</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>01100 = AN12</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>01011 = AN11</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>01010 = AN10</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>01001 = AN9</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>01000 = AN8</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>00111 = AN7(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>00110 = AN6(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>00101 = AN5(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>00100 = AN4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>00011 = AN3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>00010 = AN2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>00001 = AN1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>00000 = AN0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Note 1: PIC16(L)F1784/7 only.</td>
<td>Note 2: See Section 19.0 &quot;Digital-to-Analog Converter (DAC) Module&quot; for more information.</td>
<td>Note 3: See Section 15.0 “Fixed Voltage Reference (FVR)” for more information.</td>
<td>Note 4: See Section 16.0 “Temperature Indicator Module” for more information.</td>
</tr>
</tbody>
</table>
### REGISTER 17-2: ADCON1: ADC CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td><strong>ADFM</strong>: ADC Result Format Select bit (see Figure 17-3)</td>
</tr>
<tr>
<td></td>
<td>1 = 2’s complement format.</td>
</tr>
<tr>
<td></td>
<td>0 = Sign-magnitude result format.</td>
</tr>
<tr>
<td>6-4</td>
<td><strong>ADCS&lt;2:0&gt;</strong>: ADC Conversion Clock Select bits</td>
</tr>
<tr>
<td></td>
<td>111 = FRC (clock supplied from a dedicated FRC oscillator)</td>
</tr>
<tr>
<td></td>
<td>110 = Fosc/64</td>
</tr>
<tr>
<td></td>
<td>101 = Fosc/16</td>
</tr>
<tr>
<td></td>
<td>100 = Fosc/4</td>
</tr>
<tr>
<td></td>
<td>011 = FRC (clock supplied from a dedicated FRC oscillator)</td>
</tr>
<tr>
<td></td>
<td>010 = Fosc/32</td>
</tr>
<tr>
<td></td>
<td>001 = Fosc/8</td>
</tr>
<tr>
<td></td>
<td>000 = Fosc/2</td>
</tr>
<tr>
<td>3</td>
<td>&quot;Unimplemented&quot;: Read as '0'</td>
</tr>
<tr>
<td>2</td>
<td><strong>ADNREF</strong>: ADC Negative Voltage Reference Configuration bit</td>
</tr>
<tr>
<td></td>
<td>1 = VREF- is connected to external VREF- pin(f)</td>
</tr>
<tr>
<td></td>
<td>0 = VREF- is connected to VSS</td>
</tr>
<tr>
<td>1-0</td>
<td><strong>ADPREF&lt;1:0&gt;</strong>: ADC Positive Voltage Reference Configuration bits</td>
</tr>
<tr>
<td></td>
<td>11 = VREF+ is connected internally to FVR Buffer 1</td>
</tr>
<tr>
<td></td>
<td>10 = Reserved</td>
</tr>
<tr>
<td></td>
<td>01 = VREF+ is connected to VREF+ pin</td>
</tr>
<tr>
<td></td>
<td>00 = VREF+ is connected to VDD</td>
</tr>
</tbody>
</table>

**Note 1:** When selecting the FVR or VREF+ pin as the source of the positive reference, be aware that a minimum voltage specification exists. See Section 30.0 “Electrical Specifications” for details.
**REGISTER 17-3: ADCON2: ADC CONTROL REGISTER 2**

<table>
<thead>
<tr>
<th>bit 7-4</th>
<th>bit 3-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRIGSEL&lt;3:0&gt;</td>
<td>CHSN&lt;3:0&gt;</td>
</tr>
</tbody>
</table>

**Legend:**

<table>
<thead>
<tr>
<th>R</th>
<th>W</th>
<th>U</th>
<th>u</th>
<th>x</th>
<th>-n/n</th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>R = Readable bit</td>
<td>W = Writable bit</td>
<td>U = Unimplemented bit, read as ‘0’</td>
<td>u = Bit is unchanged</td>
<td>x = Bit is unknown</td>
<td>-n/n = Value at POR and BOR/Value at all other Resets</td>
<td>V = Value</td>
</tr>
</tbody>
</table>

**bit 7-4**

- TRIGSEL<3:0>: ADC Auto-conversion Trigger Source Selection bits
  - 1111 = Reserved. Auto-conversion Trigger disabled.
  - 1110 = Reserved. Auto-conversion Trigger disabled.
  - 1101 = Reserved. Auto-conversion Trigger disabled.
  - 1100 = PSMC3 Falling Match Event<sup>(1)</sup>
  - 1011 = PSMC3 Rising Edge Event<sup>(1)</sup>
  - 1010 = PSMC3 Period Edge Event<sup>(1)</sup>
  - 1001 = PSMC2 Falling Edge Event
  - 1000 = PSMC2 Rising Edge Event
  - 0111 = PSMC2 Period Match Event
  - 0110 = PSMC1 Falling Edge Event
  - 0101 = PSMC1 Rising Edge Event
  - 0100 = PSMC1 Period Match Event
  - 0011 = Reserved. Auto-conversion Trigger disabled.
  - 0010 = CCP2, Auto-conversion Trigger
  - 0001 = CCP1, Auto-conversion Trigger
  - 0000 = Disabled

**bit 3-0**

- CHSN<3:0>: Negative Differential Input Channel Select bits
  - When ADON = 0, all multiplexer inputs are disconnected.
  - 1111 = ADC Negative reference - selected by ADNREF
  - 1110 = AN21<sup>(1)</sup>
  - 1101 = AN13
  - 1100 = AN12
  - 1011 = AN11
  - 1010 = AN10
  - 1001 = AN9
  - 1000 = AN8
  - 0111 = AN7<sup>(1)</sup>
  - 0110 = AN6<sup>(1)</sup>
  - 0101 = AN5<sup>(1)</sup>
  - 0100 = AN4
  - 0011 = AN3
  - 0010 = AN2
  - 0001 = AN1
  - 0000 = AN0

**Note 1:** PIC16(L)F1784/7 only. For PIC16(L)F1786, “Reserved. No channel connected.”
REGISTER 17-4:  ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0

<table>
<thead>
<tr>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>AD&lt;11:4&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared

bit 7-0  **AD<11:4>:** ADC Result Register bits
Upper 8 bits of 12-bit conversion result

REGISTER 17-5:  ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0

<table>
<thead>
<tr>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>AD&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>ADSIGN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared

bit 7-4  **AD<3:0>:** ADC Result Register bits
Lower 4 bits of 12-bit conversion result

bit 3-1  **Extended LSb bits:** These are cleared to zero by DC conversion.

bit 0    **ADSIGN:** ADC Result Sign bit
### REGISTER 17-6: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ADSIGN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6-4</td>
<td>AD&lt;11:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3-0</td>
<td>AD&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

- **bit 7-4**: ADSIGN: Extended AD Result Sign bit
- **bit 3-0**: AD<11:8>: ADC Result Register bits
  - Most Significant 4 bits of 12-bit conversion result

### REGISTER 17-7: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
<th>R/W-x/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>AD&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6-0</td>
<td>AD&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- -n/n = Value at POR and BOR/Value at all other Resets

- **bit 7-0**: AD<7:0>: ADC Result Register bits
  - Least Significant 8 bits of 12-bit conversion result
17.4 ADC Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (C_{HOLD}) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 17-4. The source impedance (R_s) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor C_{HOLD}. The sampling switch (RSS) impedance varies over the device voltage (V_{DD}), refer to Figure 17-4. The maximum recommended impedance for analog sources is 10 kΩ. As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an ADC acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 17-1 may be used. This equation assumes that 1/2 LSb error is used (4,096 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

**EQUATION 17-1: ACQUISITION TIME EXAMPLE**

**Assumptions:** Temperature = 50°C and external impedance of 10kΩ 5.0V V_{DD}

\[ T_{ACQ} = \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \]
\[ = T_{AMP} + T_c + T_{COFF} \]
\[ = 2\mu s + T_c + [(Temperature - 25°C)(0.05\mu s/°C)] \]

The value for \( T_c \) can be approximated with the following equations:

\[ V_{APPLIED}\left(1 - \frac{1}{\left(\frac{V_{CHOLD}}{V_{APPLIED}}\right) - 1}\right) = V_{CHOLD} \quad \text{;}[1] \ \text{V}_{CHOLD} \text{ charged to within } 1/2 \text{ lsb} \]

\[ V_{APPLIED}\left(1 - e^{-\frac{T_c}{RC}}\right) = V_{CHOLD} \quad \text{;}[2] \ \text{V}_{CHOLD} \text{ charge response to } V_{APPLIED} \]

\[ V_{APPLIED}\left(1 - e^{-\frac{T_c}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{\left(\frac{V_{CHOLD}}{V_{APPLIED}}\right) - 1}\right) \quad \text{;combining } [1] \text{ and } [2] \]

**Note:** Where \( n \) = number of bits of the ADC.

**Solving for \( T_c \):**

\[ T_c = -C_{HOLD}(R_{IC} + RSS + RS) \ln(1/8191) \]
\[ = -10pF(1kΩ + 7kΩ + 10kΩ) \ln(0.000122) \]
\[ = 1.62\mu s \]

Therefore:

\[ T_{ACQ} = 2\mu s + 1.62\mu s + [(50°C - 25°C)(0.05\mu s/°C)] \]
\[ = 4.87\mu s \]

**Note 1:** The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

**2:** Maximum source impedance feeding the input pin should be considered so that the pin leakage does not cause a voltage divider, thereby limiting the absolute accuracy.
FIGURE 17-4: ANALOG INPUT MODEL

Legend:
- **CHOLD** = Sample/Hold Capacitance
- **CPIN** = Input Capacitance
- **I LEAKAGE** = Leakage current at the pin due to various junctions
- **Ric** = Interconnect Resistance
- **RSS** = Resistance of Sampling Switch
- **SS** = Sampling Switch
- **VT** = Threshold Voltage

Note 1: Refer to Section 30.0 “Electrical Specifications”.

FIGURE 17-5: ADC TRANSFER FUNCTION

Legend:
- **ADC Output Code**: Various ADC output codes are shown with their respective ADC input voltages.

Note 2: Each code corresponds to a specific range of input voltages, with 00h representing the zero-scale transition and FFFh representing the full-scale transition.
TABLE 17-3: SUMMARY OF REGISTERS ASSOCIATED WITH ADC

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADCON0</td>
<td>ADRMD</td>
<td>CHS&lt;4:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>GO/DONE</td>
<td>ADON 172</td>
</tr>
<tr>
<td>ADCON1</td>
<td>ADFM</td>
<td>ADCS&lt;2:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ADNREF</td>
<td>ADPREF&lt;1:0&gt;</td>
<td>173</td>
</tr>
<tr>
<td>ADCON2</td>
<td>TRIGSEL&lt;3:0&gt;</td>
<td>CHSN&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>174</td>
</tr>
<tr>
<td>ADRESH</td>
<td>A/D Result Register High</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>175, 176</td>
</tr>
<tr>
<td>ADRESL</td>
<td>A/D Result Register Low</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>175, 176</td>
</tr>
<tr>
<td>ANSELA</td>
<td>ANSA7</td>
<td>—</td>
<td>ANSA5</td>
<td>ANSA4</td>
<td>ANSA3</td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
<td>132</td>
</tr>
<tr>
<td>ANSELB</td>
<td>—</td>
<td>ANSB6</td>
<td>ANSB5</td>
<td>ANSB4</td>
<td>ANSB3</td>
<td>ANSB2</td>
<td>ANSB1</td>
<td>ANSB0</td>
<td>138</td>
</tr>
<tr>
<td>INTCN</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>93</td>
</tr>
<tr>
<td>PIE1</td>
<td>TMR1GIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSP1IE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>94</td>
</tr>
<tr>
<td>PIR1</td>
<td>TMR1GIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1IF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>98</td>
</tr>
<tr>
<td>TRISA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td>131</td>
</tr>
<tr>
<td>TRISB</td>
<td>TRISB7</td>
<td>TRISB6</td>
<td>TRISB5</td>
<td>TRISB4</td>
<td>TRISB3</td>
<td>TRISB2</td>
<td>TRISB1</td>
<td>TRISB0</td>
<td>137</td>
</tr>
<tr>
<td>FVRCON</td>
<td>FVREN</td>
<td>FVRRDY</td>
<td>TSEN</td>
<td>TSRNG</td>
<td>CDAFVR&lt;1:0&gt;</td>
<td>ADFVR&lt;1:0&gt;</td>
<td>162</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: x = unknown, u = unchanged, — = unimplemented read as '0', q = value depends on condition. Shaded cells are not used for the ADC module.
18.0 OPERATIONAL AMPLIFIER (OPA) MODULES

The Operational Amplifier (OPA) is a standard three-terminal device requiring external feedback to operate. The OPA module has the following features:

- External connections to I/O ports
- Low leakage inputs
- Factory Calibrated Input Offset Voltage

**FIGURE 18-1: OPAx MODULE BLOCK DIAGRAM**

**Note 1:** The OPAxSP bit must be set to ‘1’. Low-Power mode is not supported.
18.1 Effects of Reset

A device Reset forces all registers to their Reset state. This disables the OPA module.

18.2 OPA Module Performance

Common AC and DC performance specifications for the OPA module:

- Common Mode Voltage Range
- Leakage Current
- Input Offset Voltage
- Open Loop Gain
- Gain Bandwidth Product

**Common mode voltage range** is the specified voltage range for the OPA+ and OPA- inputs, for which the OPA module will perform to within its specifications. The OPA module is designed to operate with input voltages between VSS and VDD. Behavior for Common mode voltages greater than VDD, or below VSS, are not guaranteed.

**Leakage current** is a measure of the small source or sink currents on the OPA+ and OPA- inputs. To minimize the effect of leakage currents, the effective impedances connected to the OPA+ and OPA- inputs should be kept as small as possible and equal.

**Input offset voltage** is a measure of the voltage difference between the OPA+ and OPA- inputs in a closed loop circuit with the OPA in its linear region. The offset voltage will appear as a DC offset in the output equal to the input offset voltage, multiplied by the gain of the circuit. The input offset voltage is also affected by the Common mode voltage. The OPA is factory calibrated to minimize the input offset voltage of the module.

**Open loop gain** is the ratio of the output voltage to the differential input voltage, \((OPA+) - (OPA-)\). The gain is greatest at DC and falls off with frequency.

**Gain Bandwidth Product** or GBWP is the frequency at which the open loop gain falls off to 0 dB.

18.3 OPAxCON Control Register

The OPAxCON register, shown in Register 18-1, controls the OPA module.

The OPA module is enabled by setting the OPAxEN bit of the OPAxCON register. When enabled, the OPA forces the output driver of OPAxOUT pin into tri-state to prevent contention between the driver and the OPA output.

**Note:** When the OPA module is enabled, the OPAxOUT pin is driven by the op amp output, not by the PORT digital driver. Refer to the Electrical specifications for the op amp output drive capability.
18.4 Register Definitions: Op Amp Control

REGISTER 18-1: OPAxCON: OPERATIONAL AMPLIFIERS (OPAx) CONTROL REGISTERS

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPAxEN</td>
<td>OPAxSP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit   W = Writable bit   U = Unimplemented bit, read as ‘0’
= Bit is unchanged x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set    ‘0’ = Bit is cleared  q = Value depends on condition

bit 7    OPAxEN: Op Amp Enable bit
         1 = Op amp is enabled
         0 = Op amp is disabled and consumes no active power

bit 6    OPAxSP: Op Amp Speed/Power Select bit
         1 = Comparator operates in high GBWP mode
         0 = Reserved. Do not use.

bit 5-2  Unimplemented: Read as ‘0’

bit 1-0  OPAxCH<1:0>: Non-inverting Channel Selection bits
         11 = Non-inverting input connects to FVR Buffer 2 output
         10 = Non-inverting input connects to DAC output
         0x = Non-inverting input connects to OPAxIN+ pin

TABLE 18-1: SUMMARY OF REGISTERS ASSOCIATED WITH OP AMPS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSELA</td>
<td>ANSA7</td>
<td>—</td>
<td>ANSA5</td>
<td>ANSA4</td>
<td>ANSA3</td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
<td>132</td>
</tr>
<tr>
<td>ANSELB</td>
<td>—</td>
<td>ANSB6</td>
<td>ANSB5</td>
<td>ANSB4</td>
<td>ANSB3</td>
<td>ANSB2</td>
<td>ANSB1</td>
<td>ANSB0</td>
<td>138</td>
</tr>
<tr>
<td>DAC1CON0</td>
<td>DAC1EN</td>
<td>—</td>
<td>DAC1OE1</td>
<td>DAC1OE2</td>
<td>DAC1PSS&lt;1:0&gt;</td>
<td>—</td>
<td>DAC1NSS</td>
<td>186</td>
<td></td>
</tr>
<tr>
<td>DAC1CON1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>186</td>
</tr>
<tr>
<td>OPA1CON</td>
<td>OPA1EN</td>
<td>OPA1SP</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>182</td>
</tr>
<tr>
<td>OPA2CON</td>
<td>OPA2EN</td>
<td>OPA2SP</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>182</td>
</tr>
<tr>
<td>TRISA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td>131</td>
</tr>
<tr>
<td>TRISB</td>
<td>TRISB7</td>
<td>TRISB6</td>
<td>TRISB5</td>
<td>TRISB4</td>
<td>TRISB3</td>
<td>TRISB2</td>
<td>TRISB1</td>
<td>TRISB0</td>
<td>137</td>
</tr>
<tr>
<td>TRISC</td>
<td>TRISC7</td>
<td>TRISC6</td>
<td>TRISC5</td>
<td>TRISC4</td>
<td>TRISC3</td>
<td>TRISC2</td>
<td>TRISC1</td>
<td>TRISC0</td>
<td>142</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by op amps.

Note 1: PIC16(L)F1784/7 only
19.0 DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 256 selectable output levels.

The input of the DAC can be connected to:
- External VREF pins
- VDD supply voltage
- FVR (Fixed Voltage Reference)

The output of the DAC can be configured to supply a reference voltage to the following:
- Comparator positive input
- OpAmp positive input
- ADC input channel
- DAC1OUT1 pin
- DAC1OUT2 pin

The Digital-to-Analog Converter (DAC) is enabled by setting the DAC1EN bit of the DAC1CON0 register.

19.1 Output Voltage Selection

The DAC has 256 voltage level ranges. The 256 levels are set with the DAC1R<7:0> bits of the DAC1CON1 register.

The DAC output voltage is determined by \textit{Equation 19-1}:

\begin{equation}
\text{IF} \quad \text{DACxEN} = 1 \\
\text{VOUT} = \left( (V_{\text{SOURCE}+} - V_{\text{SOURCE}-}) \times \frac{\text{DACxR}[7:0]}{2^{8}} \right) + V_{\text{SOURCE}-} \\
V_{\text{SOURCE}+} = V_{\text{DD}}, \text{VREF, or FVR BUFFER 2} \\
V_{\text{SOURCE}-} = V_{\text{SS}}
\end{equation}

19.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

The value of the individual resistors within the ladder can be found in \textit{Section 30.0 “Electrical Specifications”}.

19.3 DAC Voltage Reference Output

The DAC voltage can be output to the DAC1OUT1 and DAC1OUT2 pins by setting the respective DAC1OE1 and DAC1OE2 pins of the DAC1CON0 register.

Selecting the DAC reference voltage for output on either DAC1OUTx pin automatically overrides the digital output buffer and digital input threshold detector functions of that pin. Reading the DAC1OUTx pin when it has been configured for DAC reference voltage output will always return a ‘0’.

Due to the limited current drive capability, a buffer must be used on the DAC voltage reference output for external connections to either DAC1OUTx pin. \textit{Figure 19-2} shows an example buffering technique.
FIGURE 19-1: DIGITAL-TO-ANALOG CONVERTER BLOCK DIAGRAM

FIGURE 19-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE
19.4 Operation During Sleep
When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the DAC1CON0 register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

19.5 Effects of a Reset
A device Reset affects the following:
• DAC is disabled.
• DAC output voltage is removed from the DAC1OUT pin.
• The DAC1R<7:0> range select bits are cleared.
19.6 Register Definitions: DAC Control

REGISTER 19-1: DAC1CON0: VOLTAGE REFERENCE CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC1EN</td>
<td>—</td>
<td>DAC1OE1</td>
<td>DAC1OE2</td>
<td>DAC1PSS&lt;1:0&gt;</td>
<td>—</td>
<td>DAC1NSS</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

bit 7 DAC1EN: DAC1 Enable bit
1 = DAC1 is enabled
0 = DAC1 is disabled

bit 6 Unimplemented: Read as ‘0’

bit 5 DAC1OE1: DAC1 Voltage Output 1 Enable bit
1 = DAC1 voltage level is also an output on the DAC1OUT1 pin
0 = DAC1 voltage level is disconnected from the DAC1OUT1 pin

bit 4 DAC1OE2: DAC1 Voltage Output 2 Enable bit
1 = DAC1 voltage level is also an output on the DAC1OUT2 pin
0 = DAC1 voltage level is disconnected from the DAC1OUT2 pin

bit 3-2 DAC1PSS<1:0>: DAC1 Positive Source Select bits
11 = Reserved, do not use
10 = FVR Buffer2 output
01 = VREF+ pin
00 = VDD

bit 1 Unimplemented: Read as ‘0’

bit 0 DAC1NSS: DAC1 Negative Source Select bits
1 = VREF- pin
0 = VSS

REGISTER 19-2: DAC1CON1: VOLTAGE REFERENCE CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC1R&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

bit 7-0 DAC1R<7:0>: DAC1 Voltage Output Select bits

TABLE 19-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE DAC MODULE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on page</th>
</tr>
</thead>
<tbody>
<tr>
<td>FVRCON</td>
<td>FVREN</td>
<td>FVRRDY</td>
<td>TSEN</td>
<td>TSRNG</td>
<td>CDAFVR&lt;1:0&gt;</td>
<td>ADFVR&lt;1:0&gt;</td>
<td></td>
<td></td>
<td>162</td>
</tr>
<tr>
<td>DAC1CON0</td>
<td>DAC1EN</td>
<td>—</td>
<td>DAC1OE1</td>
<td>DAC1OE2</td>
<td>DAC1PSS&lt;1:0&gt;</td>
<td>—</td>
<td>DAC1NSS</td>
<td></td>
<td>186</td>
</tr>
<tr>
<td>DAC1CON1</td>
<td>DAC1R&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>186</td>
</tr>
</tbody>
</table>

Legend:
- — = Unimplemented location, read as ‘0’. Shaded cells are not used with the DAC module.
20.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a
digital circuit by comparing two analog voltages and
providing a digital indication of their relative magnitudes.
Comparators are very useful mixed signal building
blocks because they provide analog functionality
independent of program execution. The analog
comparator module includes the following features:
• Independent comparator control
• Programmable input selection
• Comparator output is available internally/externally
• Programmable output polarity
• Interrupt-on-change
• Wake-up from Sleep
• Programmable Speed/Power optimization
• PWM shutdown
• Programmable and fixed voltage reference

20.1 Comparator Overview

A single comparator is shown in Figure 20-1 along with
the relationship between the analog input levels and
the digital output. When the analog voltage at VIN+ is
less than the analog voltage at VIN-, the output of the
comparator is a digital low level. When the analog
voltage at VIN+ is greater than the analog voltage at
VIN-, the output of the comparator is a digital high level.

The comparators available for this device are located in
Table 20-1.

| TABLE 20-1: COMPARATOR AVAILABILITY PER DEVICE |
|-----------------|----|----|----|----|
| Device          | C1 | C2 | C3 | C4 |
| PIC16(L)F1784/6/7 | ●  | ●  | ●  | ●  |

 Note: The black areas of the output of the comparator represents the uncertainty
due to input offsets and response time.
FIGURE 20-2: COMPARATOR MODULE SIMPLIFIED BLOCK DIAGRAM

Note 1: When CxON = 0, the comparator will produce a '0' at the output.
2: When CxON = 0, all multiplexer inputs are disconnected.
3: PIC16(L)F1784/7 only.
20.2 Comparator Control

Each comparator has two control registers: CMxCON0 and CMxCON1.
The CMxCON0 register (see Register 20-1) contains Control and Status bits for the following:
• Enable
• Output selection
• Output polarity
• Speed/Power selection
• Hysteresis enable
• Output synchronization

The CMxCON1 register (see Register 20-2) contains Control bits for the following:
• Interrupt enable
• Interrupt edge polarity
• Positive input channel selection
• Negative input channel selection

20.2.1 COMPARATOR ENABLE
Setting the CxON bit of the CMxCON0 register enables the comparator for operation. Clearing the CxON bit disables the comparator resulting in minimum current consumption.

20.2.2 COMPARATOR OUTPUT SELECTION
The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the MCxOUT bit of the CMOUT register. In order to make the output available for an external connection, the following conditions must be true:
• CxOE bit of the CMxCON0 register must be set
• Corresponding TRIS bit must be cleared
• CxON bit of the CMxCON0 register must be set

20.2.3 COMPARATOR OUTPUT POLARITY
Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

Table 20-2 shows the output state versus input conditions, including polarity control.

<table>
<thead>
<tr>
<th>Input Condition</th>
<th>CxPOL</th>
<th>CxOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CxVN &gt; CxVP</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CxVN &lt; CxVP</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>CxVN &gt; CxVP</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>CxVN &lt; CxVP</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

20.2.4 COMPARATOR SPEED/POWER SELECTION
The trade-off between speed or power can be optimized during program execution with the CxSP control bit. The default state for this bit is ‘1’ which selects the normal speed mode. Device power consumption can be optimized at the cost of slower comparator propagation delay by clearing the CxSP bit to ‘0’.

Note 1: The CxOE bit of the CMxCON0 register overrides the PORT data latch. Setting the CxON bit of the CMxCON0 register has no impact on the port override.

2: The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.
20.3 Comparator Hysteresis

A selectable amount of separation voltage can be added to the input pins of each comparator to provide a hysteresis function to the overall operation. Hysteresis is enabled by setting the CxHYS bit of the CMxCON0 register.

See Section 30.0 “Electrical Specifications” for more information.

20.4 Timer1 Gate Operation

The output resulting from a comparator operation can be used as a source for gate control of Timer1. See Section 22.6 “Timer1 Gate” for more information. This feature is useful for timing the duration or interval of an analog event.

It is recommended that the comparator output be synchronized to Timer1. This ensures that Timer1 does not increment while a change in the comparator is occurring.

20.4.1 COMPARATOR OUTPUT SYNCHRONIZATION

The output from a comparator can be synchronized with Timer1 by setting the CxSYNC bit of the CMxCON0 register.

Once enabled, the comparator output is latched on the falling edge of the Timer1 source clock. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 20-2) and the Timer1 Block Diagram (Figure 22-1) for more information.

20.5 Comparator Interrupt

An interrupt can be generated upon a change in the output value of the comparator for each comparator, a rising edge detector and a falling edge detector are present.

When either edge detector is triggered and its associated enable bit is set (CxINTP and/or CxINTN bits of the CMxCON1 register), the Corresponding Interrupt Flag bit (CxIF bit of the PIR2 register) will be set.

To enable the interrupt, you must set the following bits:

- CxON, CxPOL and CxSP bits of the CMxCON0 register
- CxIE bit of the PIE2 register
- CxINTP bit of the CMxCON1 register (for a rising edge detection)
- CxINTN bit of the CMxCON1 register (for a falling edge detection)
- PEIE and GIE bits of the INTCON register

The associated interrupt flag bit, CxIF bit of the PIR2 register, must be cleared in software. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

20.6 Comparator Positive Input Selection

Configuring the CxPCH<2:0> bits of the CMxCON1 register directs an internal voltage reference or an analog pin to the non-inverting input of the comparator:

- CxIN+ analog pin
- DAC output
- FVR (Fixed Voltage Reference)
- Vss (Ground)

See Section 15.0 “Fixed Voltage Reference (FVR)” for more information on the Fixed Voltage Reference module.

See Section 19.0 “Digital-to-Analog Converter (DAC) Module” for more information on the DAC input signal.

Any time the comparator is disabled (CxON = 0), all comparator inputs are disabled.
20.7 Comparator Negative Input Selection

The CxNCH<2:0> bits of the CMxCON0 register direct an analog input pin or analog ground to the inverting input of the comparator:

- CxIN- pin
- Analog Ground

Some inverting input selections share a pin with the operational amplifier output function. Enabling both functions at the same time will direct the operational amplifier output to the comparator inverting input.

Note: To use CxINy+ and CxINy- pins as analog input, the appropriate bits must be set in the ANSEL register and the corresponding TRIS bits must also be set to disable the output drivers.

20.8 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference.

Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in Section 30.0 “Electrical Specifications” for more details.

20.9 Zero Latency Filter

In high-speed operation, and under proper circuit conditions, it is possible for the comparator output to oscillate. This oscillation can have adverse effects on the hardware and software relying on this signal. Therefore, a digital filter has been added to the comparator output to suppress the comparator output oscillation. Once the comparator output changes, the output is prevented from reversing the change for a nominal time of 20 ns. This allows the comparator output to stabilize without affecting other dependent devices. Refer to Figure 20-3.

FIGURE 20-3: COMPARATOR ZERO LATENCY FILTER OPERATION

Output waiting for TZLF to expire before an output change is allowed
TZLF has expired so output change of ZLF is immediate based on comparator output change
20.10 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 20-4. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of 10 k\(\Omega\) is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

Note 1: When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.

2: Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 20-4: ANALOG INPUT MODEL

Legend:  
C\text{PIN} = Input Capacitance  
I\text{LEAKAGE} = Leakage Current at the pin due to various junctions  
R\text{IC} = Interconnect Resistance  
R\text{S} = Source Impedance  
V\text{A} = Analog Voltage  
V\text{T} = Threshold Voltage

Note 1: See Section 30.0 “Electrical Specifications”
20.11 Register Definitions: Comparator Control

REGISTER 20-1: CMxCON0: COMPARATOR Cx CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CxON</td>
<td>CxOUT</td>
<td>CxOE</td>
<td>CxPOL</td>
<td>CxZLF</td>
<td>CxSP</td>
<td>CxHYS</td>
<td>CxSYNC</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

- **CxON**: Comparator Enable bit
  - 1 = Comparator is enabled
  - 0 = Comparator is disabled and consumes no active power

- **CxOUT**: Comparator Output bit
  - If CxPOL = 1 (inverted polarity):
    - 1 = CxVP < CxVN
    - 0 = CxVP > CxVN
  - If CxPOL = 0 (non-inverted polarity):
    - 1 = CxVP > CxVN
    - 0 = CxVP < CxVN

- **CxOE**: Comparator Output Enable bit
  - 1 = CxOUT is present on the CxOUT pin. Requires that the associated TRIS bit be cleared to actually drive the pin. Not affected by CxON.
  - 0 = CxOUT is internal only

- **CxPOL**: Comparator Output Polarity Select bit
  - 1 = Comparator output is inverted
  - 0 = Comparator output is not inverted

- **CxZLF**: Comparator Zero Latency Filter Enable bit
  - 1 = Comparator output is filtered
  - 0 = Comparator output is unfiltered

- **CxSP**: Comparator Speed/Power Select bit
  - 1 = Comparator operates in normal power, higher speed mode
  - 0 = Comparator operates in low-power, low-speed mode

- **CxHYS**: Comparator Hysteresis Enable bit
  - 1 = Comparator hysteresis enabled
  - 0 = Comparator hysteresis disabled

- **CxSYNC**: Comparator Output Synchronous Mode bit
  - 1 = Comparator output to Timer1 and I/O pin is synchronous to changes on Timer1 clock source. Output updated on the falling edge of Timer1 clock source.
  - 0 = Comparator output to Timer1 and I/O pin is asynchronous.
## REGISTER 20-2: CMxCON1: COMPARATOR Cx CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CxINTP</td>
<td>CxINTN</td>
<td>CxPCH&lt;2:0&gt;</td>
<td>CxNCH&lt;2:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

#### bit 7
- **CxINTP**: Comparator Interrupt on Positive Going Edge Enable bits
  - 1 = The CxIF interrupt flag will be set upon a positive going edge of the CxOUT bit
  - 0 = No interrupt flag will be set on a positive going edge of the CxOUT bit

#### bit 6
- **CxINTN**: Comparator Interrupt on Negative Going Edge Enable bits
  - 1 = The CxIF interrupt flag will be set upon a negative going edge of the CxOUT bit
  - 0 = No interrupt flag will be set on a negative going edge of the CxOUT bit

#### bit 5-3
- **CxPCH<2:0>**: Comparator Positive Input Channel Select bits
  - 111 = CxVP connects to AGND
  - 110 = CxVP connects to FVR Buffer 2
  - 101 = CxVP connects to DAC1_output
  - 100 = CxVP unconnected, input floating
  - 011 = CxVP unconnected, input floating
  - 010 = CxVP unconnected, input floating
  - 001 = CxVP connects to CxIN1+ pin
  - 000 = CxVP connects to CxIN0+ pin

#### bit 2-0
- **CxNCH<2:0>**: Comparator Negative Input Channel Select bits
  - 111 = CxVN connects to AGND
  - 110 = CxVN unconnected, input floating
  - 101 = Reserved, input floating
  - 100 = CxVN connects to CxIN4- pin\(^{(2)}\)
  - 011 = CxVN connects to CxIN3- pin
  - 010 = CxVN connects to CxIN2- pin
  - 001 = CxVN connects to CxIN1- pin
  - 000 = CxVN connects to CxIN0- pin

### Note:
1. PIC16(L)F1784/7 only.
2. “Reserved, input floating” for PIC16(L)F1786 only.
TABLE 20-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARATOR MODULE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSELA</td>
<td>ANSA7</td>
<td>—</td>
<td>ANSA5</td>
<td>ANSA4</td>
<td>ANSA3</td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
<td>132</td>
</tr>
<tr>
<td>ANSELB</td>
<td>ANSB6</td>
<td>ANSB5</td>
<td>ANSB4</td>
<td>ANSB3</td>
<td>ANSB2</td>
<td>ANSB1</td>
<td>ANSB0</td>
<td></td>
<td>138</td>
</tr>
<tr>
<td>CM1CON0</td>
<td>C1ON</td>
<td>C1OUT</td>
<td>C1OE</td>
<td>C1POL</td>
<td>C1ZLF</td>
<td>C1SP</td>
<td>C1HYS</td>
<td>C1SYNC</td>
<td>193</td>
</tr>
<tr>
<td>CM2CON0</td>
<td>C2ON</td>
<td>C2OUT</td>
<td>C2OE</td>
<td>C2POL</td>
<td>C2ZLF</td>
<td>C2SP</td>
<td>C2HYS</td>
<td>C2SYNC</td>
<td>193</td>
</tr>
<tr>
<td>CM1CON1</td>
<td>C1NTP</td>
<td>C1INTN</td>
<td>C1PCH&lt;2:0&gt;</td>
<td>—</td>
<td>—</td>
<td>C1NCH&lt;2:0&gt;</td>
<td></td>
<td></td>
<td>194</td>
</tr>
<tr>
<td>CM2CON1</td>
<td>C2NTP</td>
<td>C2INTN</td>
<td>C2PCH&lt;2:0&gt;</td>
<td>—</td>
<td>—</td>
<td>C2NCH&lt;2:0&gt;</td>
<td></td>
<td></td>
<td>194</td>
</tr>
<tr>
<td>CM3CON0</td>
<td>C3ON</td>
<td>C3OUT</td>
<td>C3OE</td>
<td>C3POL</td>
<td>C3ZLF</td>
<td>C3SP</td>
<td>C3HYS</td>
<td>C3SYNC</td>
<td>193</td>
</tr>
<tr>
<td>CM3CON1</td>
<td>C3NTP</td>
<td>C3INTN</td>
<td>C3PCH&lt;2:0&gt;</td>
<td>—</td>
<td>—</td>
<td>C3NCH&lt;2:0&gt;</td>
<td></td>
<td></td>
<td>194</td>
</tr>
<tr>
<td>CMOUT</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>MC4OUT&lt;1&gt;</td>
<td>MC3OUT</td>
<td>MC2OUT</td>
<td>MC1OUT</td>
</tr>
<tr>
<td>FVRCON</td>
<td>FVREN</td>
<td>FVRDDY</td>
<td>TSEN</td>
<td>TSRNG</td>
<td>CDAFVR&lt;1:0&gt;</td>
<td>ADFVR&lt;1:0&gt;</td>
<td></td>
<td></td>
<td>162</td>
</tr>
<tr>
<td>DAC1CON0</td>
<td>DAC1EN</td>
<td>—</td>
<td>DAC1OE1</td>
<td>DAC1OE2</td>
<td>DAC1PSS&lt;1:0&gt;</td>
<td>—</td>
<td>DAC1NSS</td>
<td></td>
<td>186</td>
</tr>
<tr>
<td>DAC1CON1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DAC1&lt;7:0&gt;</td>
<td></td>
<td></td>
<td>186</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>93</td>
</tr>
<tr>
<td>PIE2</td>
<td>OSFIE</td>
<td>C2IE</td>
<td>C1IE</td>
<td>EEIE</td>
<td>BCL1IE</td>
<td>C4IE</td>
<td>C3IE</td>
<td>CCP2IE</td>
<td>95</td>
</tr>
<tr>
<td>PIR2</td>
<td>OSFIF</td>
<td>C2IF</td>
<td>C1IF</td>
<td>EEIF</td>
<td>BCL1IF</td>
<td>C4IF</td>
<td>C3IF</td>
<td>CCP2IF</td>
<td>99</td>
</tr>
<tr>
<td>TRISA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td>132</td>
</tr>
<tr>
<td>TRISB</td>
<td>TRISB7</td>
<td>TRISB6</td>
<td>TRISB5</td>
<td>TRISB4</td>
<td>TRISB3</td>
<td>TRISB2</td>
<td>TRISB1</td>
<td>TRISB0</td>
<td>138</td>
</tr>
<tr>
<td>TRISC</td>
<td>TRISC7</td>
<td>TRISC6</td>
<td>TRISC5</td>
<td>TRISC4</td>
<td>TRISC3</td>
<td>TRISC2</td>
<td>TRISC1</td>
<td>TRISC0</td>
<td>142</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as '0'. Shaded cells are unused by the comparator module.

Note 1: PIC16(L)F1784/7 only.
21.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (independent of Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Interrupt on overflow
- TMR0 can be used to gate Timer1

Figure 21-1 is a block diagram of the Timer0 module.

21.1 Timer0 Operation

The Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

21.1.1 8-BIT TIMER MODE

The Timer0 module will increment every instruction cycle, if used without a prescaler. 8-bit Timer mode is selected by clearing the TMR0CS bit of the OPTION_REG register.

When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note: The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written.

21.1.2 8-BIT COUNTER MODE

In 8-Bit Counter mode, the Timer0 module will increment on every rising or falling edge of the T0CKI pin.

8-Bit Counter mode using the T0CKI pin is selected by setting the TMR0CS bit in the OPTION_REG register to ‘1’.

The rising or falling transition of the incrementing edge for either input source is determined by the TMR0SE bit in the OPTION_REG register.
21.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A software programmable prescaler is available for exclusive use with Timer0. The prescaler is enabled by clearing the PSA bit of the OPTION_REG register.

| Note: | The Watchdog Timer (WDT) uses its own independent prescaler. |

There are eight prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION_REG register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be disabled by setting the PSA bit of the OPTION_REG register.

The prescaler is not readable or writable. All instructions writing to the TMR0 register will clear the prescaler.

21.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The TMR0IF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The TMR0IF bit can only be cleared in software. The Timer0 interrupt enable is the TMR0IE bit of the INTCON register.

| Note: | The Timer0 interrupt cannot wake the processor from Sleep since the timer is frozen during Sleep. |

21.1.5 8-BIT COUNTER MODE SYNCHRONIZATION

When in 8-Bit Counter mode, the incrementing edge on the T0CKI pin must be synchronized to the instruction clock. Synchronization can be accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the instruction clock. The high and low periods of the external clocking source must meet the timing requirements as shown in Section 30.0 “Electrical Specifications”.

21.1.6 OPERATION DURING SLEEP

Timer0 cannot operate while the processor is in Sleep mode. The contents of the TMR0 register will remain unchanged while the processor is in Sleep mode.
21.2 Register Definitions: Option Register

**REGISTER 21-1: OPTION_REG: OPTION REGISTER**

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>WPUEN</td>
<td>INTEDG</td>
<td>TMR0CS</td>
<td>TMR0SE</td>
<td>PSA</td>
<td>PS&lt;2:0&gt;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

- **WPUEN**: Weak Pull-Up Enable bit
  - 1 = All weak pull-ups are disabled (except MCLR, if it is enabled)
  - 0 = Weak pull-ups are enabled by individual WPUx latch values

- **INTEDG**: Interrupt Edge Select bit
  - 1 = Interrupt on rising edge of INT pin
  - 0 = Interrupt on falling edge of INT pin

- **TMR0CS**: Timer0 Clock Source Select bit
  - 1 = Transition on T0CKI pin
  - 0 = Internal instruction cycle clock (FOSC/4)

- **TMR0SE**: Timer0 Source Edge Select bit
  - 1 = Increment on high-to-low transition on T0CKI pin
  - 0 = Increment on low-to-high transition on T0CKI pin

- **PSA**: Prescaler Assignment bit
  - 1 = Prescaler is not assigned to the Timer0 module
  - 0 = Prescaler is assigned to the Timer0 module

- **PS<2:0>**: Prescaler Rate Select bits

<table>
<thead>
<tr>
<th>Bit Value</th>
<th>Timer0 Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>1 : 2</td>
</tr>
<tr>
<td>001</td>
<td>1 : 4</td>
</tr>
<tr>
<td>010</td>
<td>1 : 8</td>
</tr>
<tr>
<td>011</td>
<td>1 : 16</td>
</tr>
<tr>
<td>100</td>
<td>1 : 32</td>
</tr>
<tr>
<td>101</td>
<td>1 : 64</td>
</tr>
<tr>
<td>110</td>
<td>1 : 128</td>
</tr>
<tr>
<td>111</td>
<td>1 : 256</td>
</tr>
</tbody>
</table>

**TABLE 21-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0**

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IO CIF</td>
<td>93</td>
</tr>
<tr>
<td>OPTION_REG</td>
<td>WPUEN</td>
<td>INTEDG</td>
<td>TMR0CS</td>
<td>TMR0SE</td>
<td>PSA</td>
<td>PS&lt;2:0&gt;</td>
<td></td>
<td></td>
<td>198</td>
</tr>
<tr>
<td>TRISA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td>131</td>
</tr>
</tbody>
</table>

**Legend:**
- — = Unimplemented location, read as ‘0’. Shaded cells are not used by the Timer0 module.
- * Page provides register information.
22.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:
• 16-bit timer/counter register pair (TMR1H:TMR1L)
• Programmable internal or external clock source
• 2-bit prescaler
• Dedicated 32 kHz oscillator circuit
• Optionally synchronized comparator out
• Multiple Timer1 gate (count enable) sources
• Interrupt on overflow
• Wake-up on overflow (external clock, Asynchronous mode only)
• Time base for the Capture/Compare function
• Auto-conversion Trigger (with CCP)
• Selectable Gate Source Polarity

Figure 22-1 is a block diagram of the Timer1 module.

FIGURE 22-1: TIMER1 BLOCK DIAGRAM

Note 1: ST Buffer is high speed type when using T1CKI.
2: Timer1 register increments on rising edge.
3: Synchronize does not operate while in Sleep.
22.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

When used with an internal clock source, the module is a timer and increments on every instruction cycle. When used with an external clock source, the module can be used as either a timer or counter and increments on every selected edge of the external source.

Timer1 is enabled by configuring the TMR1ON and TMR1GE bits in the T1CON and T1GCON registers, respectively. Table 22-1 displays the Timer1 enable selections.

<table>
<thead>
<tr>
<th>TMR1ON</th>
<th>TMR1GE</th>
<th>Timer1 Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Off</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Off</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Always On</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Count Enabled</td>
</tr>
</tbody>
</table>

22.2 Clock Source Selection

The TMR1CS<1:0> and T1OSCEN bits of the T1CON register are used to select the clock source for Timer1. Table 22-2 displays the clock source selections.

22.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, the TMR1H:TMR1L register pair will increment on multiples of Fosc as determined by the Timer1 prescaler.

When the FOSC internal clock source is selected, the Timer1 register value will increment by four counts every instruction clock cycle. Due to this condition, a 2 LSB error in resolution will occur when reading the Timer1 value. To utilize the full resolution of Timer1, an asynchronous input signal must be used to gate the Timer1 clock input.

The following asynchronous sources may be used:

- Asynchronous event on the T1G pin to Timer1 gate
- C1 or C2 comparator input to Timer1 gate

22.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1 module may work as a timer or a counter.

When enabled to count, Timer1 is incremented on the rising edge of the external clock input T1CKI, which can be synchronized to the microcontroller system clock or can run asynchronously.

When used as a timer with a clock oscillator, an external 32.768 kHz crystal can be used in conjunction with the dedicated internal oscillator circuit.

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after any one or more of the following conditions:

- Timer1 enabled after POR
- Write to TMR1H or TMR1L
- Timer1 is disabled
- Timer1 is disabled (TMR1ON = 0) when T1CKI is high then Timer1 is enabled (TMR1ON=1) when T1CKI is low.
22.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

22.4 Timer1 Oscillator

A dedicated low-power 32.768 kHz oscillator circuit is built-in between pins T1OSI (input) and T1OSO (amplifier output). This internal circuit is to be used in conjunction with an external 32.768 kHz crystal.

The oscillator circuit is enabled by setting the T1OSCEN bit of the T1CON register. The oscillator will continue to run during Sleep.

Note: The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to using Timer1. A suitable delay similar to the OST delay can be implemented in software by clearing the TMR1IF bit then presetting the TMR1H:TMR1L register pair to FC00h. The TMR1IF flag will be set when 1024 clock cycles have elapsed, thereby indicating that the oscillator is running and reasonably stable.

22.5 Timer1 Operation in Asynchronous Counter Mode

If the control bit T1SYNC of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If the external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see Section 22.5.1 “Reading and Writing Timer1 in Asynchronous Counter Mode”).

Note: When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

22.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

22.6 Timer1 Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using Timer1 gate circuitry. This is also referred to as Timer1 Gate Enable. Timer1 gate can also be driven by multiple selectable sources.

22.6.1 TIMER1 GATE ENABLE

The Timer1 Gate Enable mode is enabled by setting the TMR1GE bit of the T1GCON register. The polarity of the Timer1 Gate Enable mode is configured using the T1GPOL bit of the T1GCON register.

When Timer1 Gate Enable mode is enabled, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 Gate Enable mode is disabled, no incrementing will occur and Timer1 will hold the current count. See Figure 22-3 for timing details.

### TABLE 22-3: TIMER1 GATE ENABLE SELECTIONS

<table>
<thead>
<tr>
<th>T1CLK</th>
<th>T1GPOL</th>
<th>T1G</th>
<th>Timer1 Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>↑</td>
<td>0</td>
<td>0</td>
<td>Counts</td>
</tr>
<tr>
<td>↑</td>
<td>0</td>
<td>1</td>
<td>Holds Count</td>
</tr>
<tr>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>Holds Count</td>
</tr>
<tr>
<td>↑</td>
<td>1</td>
<td>1</td>
<td>Counts</td>
</tr>
</tbody>
</table>
22.6.2 Timer1 Gate Source Selection

Timer1 gate source selections are shown in Table 22-4. Source selection is controlled by the T1GSS bits of the T1GCON register. The polarity for each available source is also selectable. Polarity selection is controlled by the T1GPOL bit of the T1GCON register.

### TABLE 22-4: Timer1 Gate Sources

<table>
<thead>
<tr>
<th>T1GSS</th>
<th>Timer1 Gate Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Timer1 Gate Pin</td>
</tr>
<tr>
<td>01</td>
<td>Overflow of Timer0 (TMR0 increments from FFh to 00h)</td>
</tr>
<tr>
<td>10</td>
<td>Comparator 1 Output sync_C1OUT (optionally Timer1 synchronized output)</td>
</tr>
<tr>
<td>11</td>
<td>Comparator 2 Output sync_C2OUT (optionally Timer1 synchronized output)</td>
</tr>
</tbody>
</table>

22.6.2.1 T1G Pin Gate Operation

The T1G pin is one source for Timer1 gate control. It can be used to supply an external source to the Timer1 gate circuitry.

22.6.2.2 Timer0 Overflow Gate Operation

When Timer0 increments from FFh to 00h, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 gate circuitry.

22.6.2.3 Comparator C1 Gate Operation

The output resulting from a Comparator 1 operation can be selected as a source for Timer1 gate control. The Comparator 1 output (sync_C1OUT) can be synchronized to the Timer1 clock or left asynchronous. For more information see Section 20.4.1 “Comparator Output Synchronization”.

22.6.2.4 Comparator C2 Gate Operation

The output resulting from a Comparator 2 operation can be selected as a source for Timer1 gate control. The Comparator 2 output (sync_C2OUT) can be synchronized to the Timer1 clock or left asynchronous. For more information see Section 20.4.1 “Comparator Output Synchronization”.

22.6.3 Timer1 Gate Toggle Mode

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal, as opposed to the duration of a single level pulse. The Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. See Figure 22-4 for timing details.

Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When the T1GTM bit is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

**Note:** Enabling Toggle mode at the same time as changing the gate polarity may result in indeterminate operation.

22.6.4 Timer1 Gate Single-Pulse Mode

When Timer1 Gate Single-Pulse mode is enabled, it is possible to capture a single-pulse gate event. Timer1 Gate Single-Pulse mode is enabled by first setting the T1GSPM bit in the T1GCON register. Next, the T1GGO/DONE bit in the T1GCON register must be set. The Timer1 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the T1GGO/DONE bit will automatically be cleared. No other gate events will be allowed to increment Timer1 until the T1GGO/DONE bit is once again set in software. See Figure 22-5 for timing details.

If the Single-Pulse Gate mode is disabled by clearing the T1GSPM bit in the T1GCON register, the T1GGO/DONE bit should also be cleared.

Enabling the Toggle mode and the Single-Pulse mode simultaneously will permit both sections to work together. This allows the cycle times on the Timer1 gate source to be measured. See Figure 22-6 for timing details.

22.6.5 Timer1 Gate Value

When Timer1 Gate Value Status is utilized, it is possible to read the most current level of the gate control value. The value is accessible by reading the T1GVAL bit in the T1GCON register. The T1GVAL bit is valid even when the Timer1 gate is not enabled (TMR1GE bit is cleared).

22.6.6 Timer1 Gate Event Interrupt

When Timer1 Gate Event Interrupt is enabled, it is possible to generate an interrupt upon the completion of a gate event. When the falling edge of T1GVAL occurs, the TMR1GIF flag bit in the PIR1 register will be set. If the TMR1GIE bit in the PIE1 register is set, then an interrupt will be recognized.

The TMR1GIF flag bit operates even when the Timer1 gate is not enabled (TMR1GE bit is cleared).
22.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- TMR1ON bit of the T1CON register
- TMR1IE bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note: The TMR1H:TMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

22.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set
- T1SYNC bit of the T1CON register must be set
- TMR1CS bits of the T1CON register must be configured
- T1OSCEN bit of the T1CON register must be configured

The device will wake-up on an overflow and execute the next instructions. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine.

Timer1 oscillator will continue to operate in Sleep regardless of the T1SYNC bit setting.

FIGURE 22-2: TIMER1 INCREMENTING EDGE

Note:

- Arrows indicate counter increments.
- In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

22.9 CCP Capture/Compare Time Base

The CCP modules use the TMR1H:TMR1L register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMR1H:TMR1L register pair is copied into the CCPR1H:CCPR1L register pair on a configured event.

In Compare mode, an event is triggered when the value CCPR1H:CCPR1L register pair matches the value in the TMR1H:TMR1L register pair. This event can be an Auto-conversion Trigger.

For more information, see Section 25.0 “Capture/Compare/PWM Modules”.

22.10 CCP Auto-Conversion Trigger

When any of the CCP’s are configured to trigger a auto-conversion, the trigger will clear the TMR1H:TMR1L register pair. This auto-conversion does not cause a Timer1 interrupt. The CCP module may still be configured to generate a CCP interrupt.

In this mode of operation, the CCPR1H:CCPR1L register pair becomes the period register for Timer1.

Timer1 should be synchronized and FOSC/4 should be selected as the clock source in order to utilize the Auto-conversion Trigger. Asynchronous operation of Timer1 can cause a Auto-conversion Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Auto-conversion Trigger from the CCP, the write will take precedence.

For more information, see Section 25.2.4 “Auto-Conversion Trigger”.

Note 1: Arrows indicate counter increments.

Note 2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.
FIGURE 22-3:  TIMER1 GATE ENABLE MODE

FIGURE 22-4:  TIMER1 GATE TOGGLE MODE
FIGURE 22-5: TIMER1 GATE SINGLE-PULSE MODE

- **TMR1GE**: Set by software.
- **T1GPOL**: Cleared by hardware on falling edge of T1GVAL.
- **T1GSPM**: Counting enabled on rising edge of T1G.
- **T1GGO/DONE**: Set by software, cleared by hardware on falling edge of T1GVAL.
- **T1g_in**: Cleared by software.
- **T1CKI**: Set by hardware on falling edge of T1GVAL.
- **T1GVAL**: Cleared by software.
- **Timer1**: N, N + 1, N + 2.
FIGURE 22-6: TIMER1 GATE SINGLE-PULSE AND TOGGLE COMBINED MODE

- **TMR1GE**: Set by software
- **T1GVAL**: Cleared by hardware on falling edge of T1GVAL
- **T1GGO/DONE**: Counting enabled on rising edge of T1G
- **T1Gin**: Cleared by software
- **T1CKI**: Set by hardware on falling edge of T1GVAL
- **Timer1**: Cleared by software
- **TMR1GIF**: Set by hardware on falling edge of T1GVAL

Diagram showing the timing and logic of various signals and flags related to Timer1 in single-pulse and toggle combined mode.
22.11 Register Definitions: Timer1 Control

REGISTER 22-1: T1CON: TIMER1 CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7-6</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMR1CS&lt;1:0&gt;</td>
<td>Timer1 Clock Source Select bits</td>
</tr>
<tr>
<td>11</td>
<td>Reserved, do not use.</td>
</tr>
<tr>
<td>10</td>
<td>Timer1 clock source is pin or oscillator:</td>
</tr>
<tr>
<td></td>
<td>If T1OSCEN = 0: External clock from T1CKI pin (on the rising edge)</td>
</tr>
<tr>
<td></td>
<td>If T1OSCEN = 1: Crystal oscillator on T1OSI/T1OSO pins</td>
</tr>
<tr>
<td>01</td>
<td>Timer1 clock source is system clock (Fosc)</td>
</tr>
<tr>
<td>00</td>
<td>Timer1 clock source is instruction clock (Fosc/4)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 5-4</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1CKPS&lt;1:0&gt;</td>
<td>Timer1 Input Clock Prescale Select bits</td>
</tr>
<tr>
<td>11</td>
<td>1:8 Prescale value</td>
</tr>
<tr>
<td>10</td>
<td>1:4 Prescale value</td>
</tr>
<tr>
<td>01</td>
<td>1:2 Prescale value</td>
</tr>
<tr>
<td>00</td>
<td>1:1 Prescale value</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 3</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1OSCEN</td>
<td>LP Oscillator Enable Control bit</td>
</tr>
<tr>
<td>1</td>
<td>Dedicated Timer1 oscillator circuit enabled</td>
</tr>
<tr>
<td>0</td>
<td>Dedicated Timer1 oscillator circuit disabled</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 2</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1SYNC</td>
<td>Timer1 Synchronization Control bit</td>
</tr>
<tr>
<td>1</td>
<td>Do not synchronize asynchronous clock input</td>
</tr>
<tr>
<td>0</td>
<td>Synchronize asynchronous clock input with system clock (Fosc)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 1</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unimplemented</td>
<td>Read as '0'</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 0</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMR1ON</td>
<td>Timer1 On bit</td>
</tr>
<tr>
<td>1</td>
<td>Enables Timer1</td>
</tr>
<tr>
<td>0</td>
<td>Stops Timer1 and clears Timer1 gate flip-flop</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
u = Bit is unchanged  x = Bit is unknown  -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set  '0' = Bit is cleared
**REGISTER 22-2: ** **T1GCON: TIMER1 GATE CONTROL REGISTER**

<table>
<thead>
<tr>
<th>R/W-0/u</th>
<th>R/W-0/u</th>
<th>R/W-0/u</th>
<th>R/W-0/u</th>
<th>R/W/HC-0/u</th>
<th>R-x/x</th>
<th>R/W-0/u</th>
<th>R/W-0/u</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMR1GE</td>
<td>T1GPOl</td>
<td>T1GTM</td>
<td>T1GSPM</td>
<td>T1GO/DONE</td>
<td>T1GVAL</td>
<td>T1GSS&lt;1:0&gt;</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- '-n/n' = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared
- **HC** = Bit is cleared by hardware

**bit 7**  
**TMR1GE:** Timer1 Gate Enable bit

- If **TMR1ON = 0:**
  - This bit is ignored
- If **TMR1ON = 1:**
  - 1 = Timer1 counting is controlled by the Timer1 gate function
  - 0 = Timer1 counts regardless of Timer1 gate function

**bit 6**  
**T1GPOl:** Timer1 Gate Polarity bit

- 1 = Timer1 gate is active-high (Timer1 counts when gate is high)
- 0 = Timer1 gate is active-low (Timer1 counts when gate is low)

**bit 5**  
**T1GTM:** Timer1 Gate Toggle Mode bit

- 1 = Timer1 Gate Toggle mode is enabled
- 0 = Timer1 Gate Toggle mode is disabled and toggle flip-flop is cleared

**bit 4**  
**T1GSPM:** Timer1 Gate Single-Pulse Mode bit

- 1 = Timer1 Gate Single-Pulse mode is enabled and is controlling Timer1 gate
- 0 = Timer1 Gate Single-Pulse mode is disabled

**bit 3**  
**T1GO/DONE:** Timer1 Gate Single-Pulse Acquisition Status bit

- 1 = Timer1 gate single-pulse acquisition is ready, waiting for an edge
- 0 = Timer1 gate single-pulse acquisition has completed or has not been started

**bit 2**  
**T1GVAL:** Timer1 Gate Current State bit

Indicates the current state of the Timer1 gate that could be provided to TMR1H:TMR1L. Unaffected by Timer1 Gate Enable (TMR1GE).

**bit 1-0**  
**T1GSS<1:0>:** Timer1 Gate Source Select bits

- 11 = Comparator 2 optionally synchronized output (sync_C2OUT)
- 10 = Comparator 1 optionally synchronized output (sync_C1OUT)
- 01 = Timer0 overflow output
- 00 = Timer1 gate pin
## TABLE 22-5: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSELB</td>
<td>—</td>
<td>—</td>
<td>ANSB6</td>
<td>ANSB5</td>
<td>ANSB4</td>
<td>ANSB3</td>
<td>ANSB2</td>
<td>ANSB1</td>
<td>ANSB0</td>
</tr>
<tr>
<td>CCP1CON</td>
<td>—</td>
<td>—</td>
<td>DC1B&lt;1:0&gt;</td>
<td></td>
<td></td>
<td>CCP1M&lt;3:0&gt;</td>
<td></td>
<td></td>
<td>280</td>
</tr>
<tr>
<td>CCP2CON</td>
<td>—</td>
<td>—</td>
<td>DC2B&lt;1:0&gt;</td>
<td></td>
<td></td>
<td>CCP2M&lt;3:0&gt;</td>
<td></td>
<td></td>
<td>280</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>93</td>
</tr>
<tr>
<td>PIE1</td>
<td>TMR1GE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSP1IE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>94</td>
</tr>
<tr>
<td>PIR1</td>
<td>TMR1GIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1IF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>98</td>
</tr>
<tr>
<td>TMR1H</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Holding Register for the Most Significant Byte of the 16-bit TMR1 Register</td>
</tr>
<tr>
<td>TMR1L</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Holding Register for the Least Significant Byte of the 16-bit TMR1 Register</td>
</tr>
<tr>
<td>TRISB</td>
<td>TRISB7</td>
<td>TRISB6</td>
<td>TRISB5</td>
<td>TRISB4</td>
<td>TRISB3</td>
<td>TRISB2</td>
<td>TRISB1</td>
<td>TRISB0</td>
<td>137</td>
</tr>
<tr>
<td>TRISC</td>
<td>TRISC7</td>
<td>TRISC6</td>
<td>TRISC5</td>
<td>TRISC4</td>
<td>TRISC3</td>
<td>TRISC2</td>
<td>TRISC1</td>
<td>TRISC0</td>
<td>142</td>
</tr>
<tr>
<td>T1CON</td>
<td>TMR1CS&lt;1:0&gt;</td>
<td>T1CKPS&lt;1:0&gt;</td>
<td>T1OSCEN</td>
<td>T1SYNC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TMR1ON</td>
</tr>
<tr>
<td>T1GCON</td>
<td>TMR1GE</td>
<td>T1GPOL</td>
<td>T1GTM</td>
<td>T1GSPM</td>
<td>T1GGO/</td>
<td>T1GVAL</td>
<td></td>
<td>T1GSS&lt;1:0&gt;</td>
<td>208</td>
</tr>
</tbody>
</table>

**Legend:**  
— = unimplemented location, read as '0'. Shaded cells are not used by the Timer1 module.  
*Page provides register information.*
23.0 TIMER2 MODULE

The Timer2 module incorporates the following features:

- 8-bit Timer and Period registers (TMR2 and PR2, respectively)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4, 1:16, and 1:64)
- Software programmable postscaler (1:1 to 1:16)
- Interrupt on TMR2 match with PR2
- Optional use as the shift clock for the MSSP module

See Figure 23-1 for a block diagram of Timer2.

FIGURE 23-1: TIMER2 BLOCK DIAGRAM
23.1 Timer2 Operation

The clock input to the Timer2 modules is the system instruction clock (Fosc/4).

A 4-bit counter/prescaler on the clock input allows direct input, divide-by-4 and divide-by-16 prescale options. These options are selected by the prescaler control bits, T2CKPS<1:0> of the T2CON register. The value of TMR2 is compared to that of the Period register, PR2, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal also resets the value of TMR2 to 00h on the next cycle and drives the output counter/postscaler (see Section 23.2 “Timer2 Interrupt”).

The TMR2 and PR2 registers are both directly readable and writable. The TMR2 register is cleared on any device Reset, whereas the PR2 register initializes to FFh. Both the prescaler and postscaler counters are cleared on the following events:

- a write to the TMR2 register
- a write to the T2CON register
- Power-on Reset (POR)
- Brown-out Reset (BOR)
- MCLR Reset
- Watchdog Timer (WDT) Reset
- Stack Overflow Reset
- Stack Underflow Reset
- \texttt{RESET} Instruction

\textbf{Note: TMR2 is not cleared when T2CON is written.}

23.3 Timer2 Output

The unscaled output of TMR2 is available primarily to the CCP modules, where it is used as a time base for operations in PWM mode. Timer2 can be optionally used as the shift clock source for the MSSP module operating in SPI mode. Additional information is provided in Section 26.0 “Master Synchronous Serial Port (MSSP) Module”

23.4 Timer2 Operation During Sleep

The Timer2 timers cannot be operated while the processor is in Sleep mode. The contents of the TMR2 and PR2 registers will remain unchanged while the processor is in Sleep mode.
23.5 Register Definitions: Timer2 Control

REGISTER 23-1: T2CON: TIMER2 CONTROL REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6-3</th>
<th>bit 2</th>
<th>bit 1-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>T2OUTPS&lt;3:0&gt;</td>
<td>TMR2ON</td>
<td>T2CKPS&lt;1:0&gt;</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7**
- **Unimplemented**: Read as ‘0’

**bit 6-3**
- **T2OUTPS<3:0>**: Timer2 Output Postscaler Select bits
  - 1111 = 1:16 Postscaler
  - 1110 = 1:15 Postscaler
  - 1101 = 1:14 Postscaler
  - 1100 = 1:13 Postscaler
  - 1011 = 1:12 Postscaler
  - 1010 = 1:11 Postscaler
  - 1001 = 1:10 Postscaler
  - 1000 = 1:9 Postscaler
  - 0111 = 1:8 Postscaler
  - 0110 = 1:7 Postscaler
  - 0101 = 1:6 Postscaler
  - 0100 = 1:5 Postscaler
  - 0011 = 1:4 Postscaler
  - 0010 = 1:3 Postscaler
  - 0001 = 1:2 Postscaler
  - 0000 = 1:1 Postscaler

**bit 2**
- **TMR2ON**: Timer2 On bit
  - 1 = Timer2 is on
  - 0 = Timer2 is off

**bit 1-0**
- **T2CKPS<1:0>**: Timer2 Clock Prescale Select bits
  - 11 = Prescaler is 64
  - 10 = Prescaler is 16
  - 01 = Prescaler is 4
  - 00 = Prescaler is 1
### TABLE 23-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCP2CON</td>
<td>—</td>
<td>—</td>
<td>DC2B&lt;1:0&gt;</td>
<td></td>
<td></td>
<td>CCP2M&lt;3:0&gt;</td>
<td></td>
<td></td>
<td>280</td>
</tr>
<tr>
<td>INTCON</td>
<td></td>
<td></td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOIE</td>
<td>TMR0IF</td>
<td>TMR0IF</td>
</tr>
<tr>
<td>PIE1</td>
<td></td>
<td></td>
<td></td>
<td>TMR1GIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSP1IE</td>
<td>CCP1IE</td>
</tr>
<tr>
<td>PIR1</td>
<td></td>
<td></td>
<td></td>
<td>TMR1GIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1IF</td>
<td>CCP1IF</td>
</tr>
<tr>
<td>PR2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T2CON</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>T2OUTPS&lt;3:0&gt;</td>
<td></td>
<td></td>
<td>TMR2ON</td>
<td>T2CKPS&lt;1:0&gt;</td>
</tr>
<tr>
<td>TMR2</td>
<td></td>
<td></td>
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</tbody>
</table>

**Legend:**
- — = unimplemented location, read as '0'. Shaded cells are not used for Timer2 module.
- * Page provides register information.
24.0 PROGRAMMABLE SWITCH MODE CONTROL (PSMC)

The Programmable Switch Mode Controller (PSMC) is a high-performance Pulse Width Modulator (PWM) that can be configured to operate in one of several modes to support single or multiple phase applications.

A simplified block diagram indicating the relationship between inputs, outputs, and controls is shown in Figure 24-1.

This section begins with the fundamental aspects of the PSMC operation. A more detailed description of operation for each mode is located later in Section 24.3 “Modes of Operation”

Modes of operation include:
- Single-phase
- Complementary Single-phase
- Push-Pull
- Push-Pull 4-Bridge
- Complementary Push-Pull 4-Bridge
- Pulse Skipping
- Variable Frequency Fixed Duty Cycle
- Complementary Variable Frequency Fixed Duty Cycle
- ECCP Compatible modes
  - Full-Bridge
  - Full-Bridge Reverse
- 3-Phase 6-Step PWM
24.1 Fundamental Operation

PSMC operation is based on the sequence of three events:

- Period Event – Determines the frequency of the active signal.
- Rising Edge Event – Determines start of the active pulse. This is also referred to as the phase.
- Falling Edge Event – Determines the end of the active pulse. This is also referred to as the duty cycle.

The basic waveform generated from these events is shown in Figure 24-2.

FIGURE 24-2: BASIC PWM WAVEFORM GENERATION

Each of the three types of events is triggered by a user selectable combination of synchronous timed and asynchronous external inputs.

Asynchronous event inputs may come directly from an input pin or through the comparators.

Synchronous timed events are determined from the PSMCxTMR counter, which is derived from internal clock sources. See Section 24.2.5 “PSMC Time Base Clock Sources” for more detail.

The active pulse stream can be further modulated by one of several internal or external sources:

- Register control bit
- Comparator output
- CCP output
- Input pin

User selectable deadtime can be inserted in the drive outputs to prevent shoot through of configurations with two devices connected in series between the supply rails.

Applications requiring very small frequency granularity control when the PWM frequency is large can do so with the fractional frequency control available in the variable frequency fixed Duty Cycle modes.

PSMC operation can be quickly terminated without software intervention by the auto-shutdown control. Auto-shutdown can be triggered by any combination of the following:

- PSMCxIN pin
- sync_C1OUT
- sync_C2OUT
- sync_C3OUT
- sync_C4OUT
24.1.1 PERIOD EVENT
The period event determines the frequency of the active pulse. Period event sources include any combination of the following:
- PSMCxTMR counter match
- PSMC input pin
- sync_C1OUT
- sync_C2OUT
- sync_C3OUT
- sync_C4OUT
Period event sources are selected with the PSMC Period Source (PSMCxPRS) register (Register 24-14).
Section 24.2.1.2 “16-bit Period Register” contains details on configuring the PSMCxTMR counter match for synchronous period events.

All period events cause the PSMCxTMR counter to reset on the counting clock edge immediately following the period event. The PSMCxTMR counter resumes counting from zero on the counting clock edge after the period event Reset.
During a period, the rising event and falling event are each permitted to occur only once. Subsequent rising or falling events that may occur within the period are suppressed, thereby preventing output chatter from spurious inputs.

24.1.2 RISING EDGE EVENT
The rising edge event determines the start of the active drive period. The rising edge event is also referred to as the phase because two synchronized PSMC peripherals may have different rising edge events relative to the period start, thereby creating a phase relationship between the two PSMC peripheral outputs.
Depending on the PSMC mode, one or more of the PSMC outputs will change in immediate response to the rising edge event. Rising edge event sources include any combination of the following:
- Synchronous:
  - PSMCxTMR time base counter match
- Asynchronous:
  - PSMC input pin
  - sync_C1OUT
  - sync_C2OUT
  - sync_C3OUT
  - sync_C4OUT
Rising edge event sources are selected with the PSMC Phase Source (PSMCxPHS) register (Register 24-12).
For configuring the PSMCxTMR time base counter match for synchronous rising edge events, see Section 24.2.1.3 “16-bit Phase Register”.
The first rising edge event in a cycle period is the only one permitted to cause action. All subsequent rising edge events in the same period are suppressed to prevent the PSMC output from chattering in the presence of spurious event inputs. A rising edge event is also suppressed when it occurs after a falling edge event in the same period.
The rising edge event also triggers the start of two other timers when needed: falling edge blanking and dead-band period. For more detail refer to Section 24.2.8 “Input Blanking” and Section 24.4 “Dead-Band Control”.
When the rising edge event is delayed from the period start, the amount of delay subtracts from the total amount of time available for the drive duty cycle. For example, if the rising edge event is delayed by 10% of the period time, the maximum duty cycle for that period is 90%. A 100% duty cycle is still possible in this example, but duty cycles from 90% to 100% are not possible.

24.1.3 FALLING EDGE EVENT
The falling edge event determines the end of the active drive period. The falling edge event is also referred to as the duty cycle because varying the falling edge event, while keeping the rising edge event and period events fixed, varies the active drive duty cycle.
Depending on the PSMC mode, one or more of the PSMC outputs will change in immediate response to the falling edge event. Falling edge event sources include any combination of the following:
- Synchronous:
  - PSMCxTMR time base counter match
- Asynchronous:
  - PSMC input pin
  - sync_C1OUT
  - sync_C2OUT
  - sync_C3OUT
  - sync_C4OUT
Falling edge event sources are selected with PSMC Duty Cycle Source (PSMCxDCS) register (Register 24-13).
For configuring the PSMCxTMR time base counter match for synchronous falling edge events, see Section 24.2.1.4 “16-bit Duty Cycle Register”.
The first falling edge event in a cycle period is the only one permitted to cause action. All subsequent falling edge events in the same period are suppressed to prevent the PSMC output from chattering in the presence of spurious event inputs.
A falling edge event suppresses any subsequent rising edges that may occur in the same period. In other words, if an asynchronous falling edge input should come late and occur early in the period, following that for which it was intended, the rising edge in that period will be suppressed. This will have a similar effect as pulse skipping.
The falling edge event also triggers the start of two other timers: rising edge blanking and dead-band period. For more detail refer to Section 24.2.8 “Input Blanking” and Section 24.4 “Dead-Band Control”.

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24.2 Event Sources

There are two main sources for the period, rising edge and falling edge events:

- Synchronous input
  - Time base
- Asynchronous Inputs
  - Digital Inputs
  - Analog inputs

24.2.1 TIME BASE

The Time Base section consists of several smaller pieces.

- 16-bit time base counter
- 16-bit Period register
- 16-bit Phase register (rising edge event)
- 16-bit Duty Cycle register (falling edge event)
- Clock control
- Interrupt Generator

An example of a fully synchronous PWM waveform generated with the time base is shown in Figure 24-2. The PSMCxLD bit of the PSMCxCON register is provided to synchronize changes to the event Count registers. Changes are withheld from taking action until the first period event Reset after the PSMCxLD bit is set. For example, to change the PWM frequency, while maintaining the same effective duty cycle, the Period and Duty Cycle registers need to be changed. The changes to all four registers take effect simultaneously on the period event Reset after the PSMCxLD bit is set.

24.2.1.1 16-bit Counter (Time Base)

The PSMCxTMR is the counter used as a timing reference for each synchronous PWM period. The counter starts at 0000h and increments to FFFFh on the rising edge of the psmc_clk signal.

When the counter rolls over from FFFFh to 0000h without a period event occurring, the overflow interrupt will be generated, thereby setting the PxTOVIF bit of the PSMC Time Base Interrupt Control (PSMCxINT) register (Register 24-33).

The PSMCxTMR counter is reset on both synchronous and asynchronous period events.

The PSMCxTMR is accessible to software as two 8-bit registers:

- PSMC Time Base Counter Low (PSMCxTMRL) register (Register 24-18)
- PSMC PSMC Time Base Counter High (PSMCxTMRH) register (Register 24-19)

PSMCxTMR is reset to the default POR value when the PSMCxEN bit is cleared.

24.2.1.2 16-bit Period Register

The PSMCxPR Period register is used to determine a synchronous period event referenced to the 16-bit PSMCxTMR digital counter. A match between the PSMCxTMR and PSMCxPR register values will generate a period event.

The match will generate a period match interrupt, thereby setting the PxTPRIF bit of the PSMC Time Base Interrupt Control (PSMCxINT) register (Register 24-33).

The 16-bit period value is accessible to software as two 8-bit registers:

- PSMC Period Count Low Byte (PSMCxPRL) register (Register 24-24)
- PSMC Period Count High Byte (PSMCxPRH) register (Register 24-25)

The 16-bit period value is double-buffered before it is presented to the 16-bit time base for comparison. The buffered registers are updated on the first period event Reset after the PSMCxLD bit of the PSMCxCON register is set.

The synchronous PWM period time can be determined from Equation 24-1.

\[
\text{Period} = \frac{\text{PSMCxPR}[15:0] + 1}{F_{\text{psmc clk}}}
\]

24.2.1.3 16-bit Phase Register

The PSMCxPH Phase register is used to determine a synchronous rising edge event referenced to the 16-bit PSMCxTMR digital counter. A match between the PSMCxTMR and the PSMCxPH register values will generate a rising edge event.

The match will generate a phase match interrupt, thereby setting the PxTPHIF bit of the PSMC Time Base Interrupt Control (PSMCxINT) register (Register 24-33).

The 16-bit phase value is accessible to software as two 8-bit registers:

- PSMC Phase Count Low Byte (PSMCxPHL) register (Register 24-33)
- PSMC Phase Count High Byte (PSMCxPHH) register (Register 24-33)

The 16-bit phase value is double-buffered before it is presented to the 16-bit PSMCxTMR for comparison. The buffered registers are updated on the first period event Reset after the PSMCxLD bit of the PSMCxCON register is set.
24.2.1.4 16-bit Duty Cycle Register

The PSMCxDC Duty Cycle register is used to determine a synchronous falling edge event referenced to the 16-bit PSMCxTMR digital counter. A match between the PSMCxTMR and PSMCxDC register values will generate a falling edge event.

The match will generate a duty cycle match interrupt, thereby setting the PxTDCIF bit of the PSMC Time Base Interrupt Control (PSMCxINT) register (Register 24-33). The 16-bit duty cycle value is accessible to software as two 8-bit registers:

- PSMC Duty Cycle Count Low Byte (PSMCxDCL) register (Register 24-22)
- PSMC Duty Cycle Count High Byte (PSMCxDCH) register (Register 24-23)

The 16-bit duty cycle value is double-buffered before it is presented to the 16-bit base for comparison. The buffered registers are updated on the first period event Reset after the PSMCxLD bit of the PSMCxCON register is set.

When the period, phase, and duty cycle are all determined from the time base, the effective PWM duty cycle can be expressed as shown in Equation 24-2.

EQUATION 24-2: PWM DUTY CYCLE

\[
\text{DUTYCYCLE} = \frac{\text{PSMCxDC}[15:0] - \text{PSMCxPH}[15:0]}{(\text{PSMCxPR}[15:0] + 1)}
\]

24.2.2 0% DUTY CYCLE OPERATION USING TIME BASE

To configure the PWM for 0% duty cycle set PSMCxDC<15:0> = PSMCxPH<15:0>. This will trigger a falling edge event simultaneous with the rising edge event and prevent the PWM from being asserted.

24.2.3 100% DUTY CYCLE OPERATION USING TIME BASE

To configure the PWM for 100% duty cycle set PSMCxDC<15:0> > PSMCxPR<15:0>. This will prevent a falling edge event from occurring as the PSMCxDC<15:0> value and the time base value PSMCxTMR<15:0> will never be equal.

24.2.4 TIME BASE INTERRUPT GENERATION

The Time Base section can generate four unique interrupts:

- Time Base Counter Overflow Interrupt
- Time Base Phase Register Match Interrupt
- Time Base Duty Cycle Register Match Interrupt
- Time Base Period Register Match Interrupt

Each interrupt has an interrupt flag bit and an interrupt enable bit. The interrupt flag bit is set anytime a given event occurs, regardless of the status of the enable bit.

Time base interrupt enables and flags are located in the PSMC Time Base Interrupt Control (PSMCxINT) register (Register 24-33).

PSMC time base interrupts also require that the PSMCxTIE bit in the PIE4 register and the PEIE and GIE bits in the INTCON register be set in order to generate an interrupt. The PSMCxTIF interrupt flag in the PIR4 register will only be set by a time base interrupt when one or more of the enable bits in the PSMCxINT register is set.

The interrupt flag bits need to be cleared in software. However, all PSMCx time base interrupt flags, except PSMCxTIF, are cleared when the PSMCxEN bit is cleared.

Interrupt bits that are set by software will generate an interrupt provided that the corresponding interrupt is enabled.

Note: Interrupt flags in both the PIE4 and PSMCxINT registers must be cleared to clear the interrupt. The PSMCxINT flags must be cleared first.

24.2.5 PSMC TIME BASE CLOCK SOURCES

There are three clock sources available to the module:

- Internal 64 MHz clock
- Fosc system clock
- External clock input pin

The clock source is selected with the PxCSRC<1:0> bits of the PSMCx Clock Control (PSMCxCLK) register (Register 24-6).

When the Internal 64 MHz clock is selected as the source, the HFINTOSC continues to operate and clock the PSMC circuitry in Sleep. However, the system clock to other peripherals and the CPU is suppressed.

Note: When the 64 MHz clock is selected, the clock continues to operate in Sleep, even when the PSMC is disabled (PSMCxEN = 0). Select a clock other than the 64 MHz clock to minimize power consumption when the PSMC is not enabled.

The Internal 64 MHz clock utilizes the system clock 4x PLL. When the system clock source is external and the PSMC is using the Internal 64 MHz clock, the 4x PLL should not be used for the system clock.
24.2.6 CLOCK PRESCALER

There are four prescaler choices available to be applied to the selected clock:

- Divide by 1
- Divide by 2
- Divide by 4
- Divide by 8

The clock source is selected with the PxCPRE<1:0> bits of the PSMCx Clock Control (PSMCxCLK) register (Register 24-6).

The prescaler output is psmc_clk, which is the clock used by all of the other portions of the PSMC module.

**FIGURE 24-3: TIME BASE WAVEFORM GENERATION**
24.2.7 ASYNCHRONOUS INPUTS
The PSMC module supports asynchronous inputs alone or in combination with the synchronous inputs. Asynchronous inputs include:

- Analog
  - sync_C1OUT
  - sync_C2OUT
  - sync_C3OUT
  - sync_C4OUT
- Digital
  - PSMCxIN pin

24.2.7.1 Comparator Inputs
The outputs of any combination of the synchronized comparators may be used to trigger any of the three events as well as auto-shutdown. The event triggers on the rising edge of the comparator output. Except for auto-shutdown, the event input is not level sensitive.

24.2.7.2 PSMCxIN Pin Input
The PSMCxIN pin may be used to trigger PSMC events. Data is passed through straight to the PSMC module without any synchronization to a system clock. This is so that input blanking may be applied to any external circuit using the module. The event triggers on the rising edge of the PSMCxIN signal.

24.2.7.3 Asynchronous Polarity
Polarity control is available for the period and duty-cycle asynchronous event inputs. Polarity control is necessary when the same signal is used as the source for both events. Inverting the polarity of one event relative to the other enables starting the period on one edge of the signal and terminating the duty-cycle on the opposite edge. Polarity is controlled with the PxPRPOL and PxDCPOL bits of the PSMCxSYNC register. Inverting the asynchronous input with these controls inverts all enabled asynchronous inputs for the corresponding event.

24.2.8 INPUT BLANKING
Input blanking is a function whereby the inputs from any selected asynchronous input may be driven inactive for a short period of time. This is to prevent electrical transients from the turn-on/off of power components from generating a false event. Blankering is initiated by either or both:

- Rising event
- Falling event

Blanked inputs are suppressed from causing all asynchronous events, including:

- Rising
- Falling
- Period
- Shutdown

Rising edge and falling edge blanking are controlled independently. The following features are available for blanking:

- Blankering enable
- Blankering time counters
- Blankering mode

The following Blankering modes are available:

- Blankering disabled
- Immediate blanking

The Falling Edge Blankering mode is set with the PxFEBM<1:0> bits of the PSMCx Blankering Control (PSMCxBLNK) register (Register 24-9).

The Rising Edge Blankering mode is set with the PxREBM<1:0> bits of the PSMCx Blankering Control (PSMCxBLNK) register (Register 24-9).

24.2.8.1 Blankering Disabled
With blankering disabled, the asynchronous inputs are passed to the PSMC module without any intervention.

24.2.8.2 Immediate Blankering
With Immediate blankering, a counter is used to determine the blanking period. The desired blanking time is measured in psmc_clk periods. A rising edge event will start incrementing the rising edge blanking counter. A falling edge event will start incrementing the falling edge blanking counter.

The rising edge blanking time is set with the PSMC Rising Edge Blankering Time (PSMCxBLKR) register (Register 24-29). The inputs to be blanked are selected with the PSMC Rising Edge Blanked Source (PSMCxREBS) register (Register 24-10). During rising edge blanking, the selected blanked sources are suppressed for falling edge as well as rising edge, auto-shutdown and period events.

The falling edge blanking time is set with the PSMC Falling Edge Blankering Time (PSMCxBLKF) register (Register 24-30). The inputs to be blanked are selected with the PSMC Falling Edge Blanked Source (PSMCxFEBS) register (Register 24-11). During falling edge blanking, the selected blanked sources are suppressed for falling edge, as well as falling edge, auto-shutdown, and period events.

The blanking counters are incremented on the rising edge of psmc_clk. Blanked sources are suppressed until the counter value equals the blanking time register causing the blanking to terminate.

As the rising and falling edge events are from asynchronous inputs, there may be some uncertainty in the actual blanking time implemented in each cycle. The maximum uncertainty is equal to one psmc_clk period.
24.2.9 OUTPUT WAVEFORM GENERATION

The PSMC PWM output waveform is generated based upon the different input events. However, there are several other factors that affect the PWM waveshapes:

- Output Control
  - Output Enable
  - Output Polarity
- Waveform Mode Selection
- Dead-band Control
- Steering control

24.2.10 OUTPUT CONTROL

24.2.10.1 Output Pin Enable

Each PSMC PWM output pin has individual output enable control.

When the PSMC output enable control is disabled, the module asserts no control over the pin. In this state, the pin can be used for general purpose I/O or other associate peripheral use.

When the PSMC output enable is enabled, the active PWM waveform is applied to the pin per the port priority selection.

PSMC output enable selections are made with the PSMC Output Enable Control (PSMCxOEN) register (Register 24-7).

24.2.10.2 Output Steering

PWM output will be presented only on pins for which output steering is enabled. The PSMC has up to six PWM outputs. The PWM signal in some modes can be steered to one or more of these outputs.

Steering differs from output enable in the following manner: When the output is enabled but the PWM steering to the corresponding output is not enabled, then general purpose output to the pin is disabled and the pin level will remain constantly in the inactive PWM state. Output steering is controlled with the PSMCS Steering Control 0 (PSMCxSTR0) register (Register 24-31).

Steering operates only in the following modes:

- Single-phase
- Complementary Single-phase
- 3-phase 6-step PWM

24.2.10.3 Polarity Control

Each PSMC output has individual output polarity control. Polarity is set with the PSMC Polarity Control (PSMCxPOL) register (Register 24-8).

24.3 Modes of Operation

All modes of operation use the period, rising edge, and falling edge events to generate the various PWM output waveforms.

The 3-phase 6-step PWM mode makes special use of the software controlled steering to generate the required waveform.

Modes of operation are selected with the PSMC Control (PSMCxCON) register (Register 24-1).

24.3.1 SINGLE-PHASE MODE

The single PWM is the most basic of all the waveshapes generated by the PSMC module. It consists of a single output that uses all three events (rising edge, falling edge and period events) to generate the waveform.

24.3.1.1 Mode Features

- No dead-band control available
- PWM can be steered to any combination of the following PSMC outputs:
  - PSMCxA
  - PSMCxB
  - PSMCxC
  - PSMCxD
  - PSMCxE
  - PSMCxF
- Identical PWM waveform is presented to all pins for which steering is enabled.

24.3.1.2 Waveform Generation

Rising Edge Event

- All outputs with PxSTR enabled are set to the active state

Falling Edge Event

- All outputs with PxSTR enabled are set to the inactive state

Code for setting up the PSMC generate the single-phase waveform shown in Figure 24-4, and given in Example 24-1.
EXAMPLE 24-1: SINGLE-PHASE SETUP

; Single-phase PWM PSMC setup
; Fully synchronous operation
; Period = 10 us
; Duty cycle = 50%
  BANKSEL PSMC1CON
  MOVLM 0x02 ; set period
  MOVWF PSMC1PRH
  MOVLM 0x7F
  MOVWF PSMC1PRL
  MOVLM 0x01 ; set duty cycle
  MOVWF PSMC1DCH
  MOVLM 0x3F
  MOVWF PSMC1DCL
  CLRF PSMC1PHH ; no phase offset
  CLRF PSMC1PHL
  MOVLM 0x01 ; PSMC clock=64 MHz
  MOVWF PSMC1CLK

; output on A, normal polarity
  BSF PSMC1STR0,P1STRA
  BCF PSMC1POL, P1POLA
  BSF PSMC1OEN, P1OEA

; set time base as source for all events
  BSF PSMC1PRS, P1PRST
  BSF PSMC1PHS, P1PHST
  BSF PSMC1DCS, P1DCST

; enable PSMC in Single-Phase Mode
; this also loads steering and time buffers
  MOVLM B’11000000’
  MOVWF PSMC1CON
  BANKSEL TRISC
  BCF TRISC, 0 ; enable pin driver

FIGURE 24-4: SINGLE PWM WAVEFORM – PSMCXSTR0 = 01H

<table>
<thead>
<tr>
<th>PWM Period Number</th>
<th>1</th>
<th>2</th>
<th>3</th>
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<tbody>
<tr>
<td><strong>Period Event</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Rising Edge Event</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Falling Edge Event</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PSMCxa</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
24.3.2 COMPLEMENTARY PWM

The complementary PWM uses the same events as the single PWM, but two waveforms are generated instead of only one.

The two waveforms are opposite in polarity to each other. The two waveforms may also have dead-band control as well.

24.3.2.1 Mode Features and Controls

- Dead-band control available
- PWM primary output can be steered to the following pins:
  - PSMCxA
  - PSMCxC
  - PSMCxE
- PWM complementary output can be steered to the following pins:
  - PSMCxB
  - PSMCxD
  - PSMCxE

24.3.2.2 Waveform Generation

**Rising Edge Event**

- Complementary output is set inactive
- Optional rising edge dead band is activated
- Primary output is set active

**Falling Edge Event**

- Primary output is set inactive
- Optional falling edge dead band is activated
- Complementary output is set active

Code for setting up the PSMC generates the complementary single-phase waveform shown in Figure 24-5, and given in Example 24-2.

**EXAMPLE 24-2: COMPLEMENTARY SINGLE-PHASE SETUP**

```assembly
; Complementary Single-phase PWM PSMC setup
; Fully synchronous operation
; Period = 10 us
; Duty cycle = 50%
; Deadband = 93.75 ±15.6/-0 ns
BANKSEL PSMC1CON
MOVLW 0x02 ; set period
MOVWF PSMC1PRH
MOVLW 0x7F
MOVWF PSMC1PRL
MOVLW 0x01 ; set duty cycle
MOVWF PSMC1DCH
MOVLW 0x3F
MOVWF PSMC1DCL
CLRF PSMC1PHH ; no phase offset
CLRF PSMC1PHL
MOVLW 0x01 ; PSMC clock=64 MHz
MOVWF PSMC1CLK
; output on A, normal polarity
MOVLW B'00000001'; A and B enables
MOVWF PSMC1OEN
MOVWF PSMC1STR0
CLRF PSMC1POL
; set time base as source for all events
BSF PSMC1PRS, P1PRST
BSF PSMC1PHS, P1PHST
BSF PSMC1DCS, P1DCST
; set rising and falling dead-band times
MOVLW D'6'
MOVWF PSMC1DBR
MOVWF PSMC1DBF
; enable PSMC in Complementary Single Mode
; this also loads steering and time buffers
; and enables rising and falling deadbands
MOVLW B'11110001'
MOVWF PSMC1CON
BANKSEL TRISC
BCF TRISC, 0 ; enable pin drivers
BCF TRISC, 1
```

**FIGURE 24-5: COMPLEMENTARY PWM WAVEFORM – PSMCXSTR0 = 03H**

<table>
<thead>
<tr>
<th>PWM Period Number</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Period Event</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Rising Edge Event</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Falling Edge Event</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PSMCxA</strong> (Primary Output)</td>
<td></td>
<td>Rising Edge</td>
<td>Dead Band</td>
</tr>
<tr>
<td><strong>PSMCxB</strong> (Complementary Output)</td>
<td></td>
<td>Falling Edge</td>
<td>Dead Band</td>
</tr>
</tbody>
</table>
24.3.3  PUSH-PULL PWM

The push-pull PWM is used to drive transistor bridge circuits. It uses at least two outputs and generates PWM signals that alternate between the two outputs in even and odd cycles.

Variations of the push-pull waveform include four outputs with two outputs being complementary or two sets of two identical outputs. Refer to Sections 24.3.4 through 24.3.6 for the other Push-Pull modes.

24.3.3.1  Mode Features

- No dead-band control available
- No steering control available
- Output is on the following two pins only:
  - PSMCxA
  - PSMCxB

Note: This is a subset of the 6-pin output of the push-pull PWM output, which is why pin functions are fixed in these positions, so they are compatible with that mode. See Section 24.3.6 “Push-Pull PWM with Four Full-Bridge and Complementary Outputs”

24.3.3.2  Waveform Generation

Odd numbered period rising edge event:
- PSMCxA is set active
Odd numbered period falling edge event:
- PSMCxA is set inactive
Even numbered period rising edge event:
- PSMCxB is set active
Even numbered period falling edge event:
- PSMCxB is set inactive

EXAMPLE 24-3:  PUSH-PULL SETUP

Code for setting up the PSMC generate the complementary single-phase waveform shown in Figure 24-6, and given in Example 24-3.

BANKSEL PSMC1CON
MOVLW 0x02 ; set period
MOVWF PSMC1PRH
MOVLW 0x7F
MOVWF PSMC1PRL
MOVLW 0x01 ; set duty cycle
MOVWF PSMC1DCH
MOVLW 0x3F
MOVWF PSMC1DCL
CLRF PSMC1PHH ; no phase offset
CLRF PSMC1PHL
MOVLW 0x01 ; PSMC clock=64 MHz
MOVWF PSMC1CLK
BANKSEL PSMC1CON
MOVLW B’00000011’
MOVWF PSMC1OEN
CLRF PSMC1POL
BANKSEL PSMC1CON
BANKSEL TRISC
BCF TRISC, 0 ; enable pin drivers
BCF TRISC, 1

FIGURE 24-6:  PUSH-PULL PWM WAVEFORM

<table>
<thead>
<tr>
<th>PWM Period Number</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Period Event</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rising Edge Event</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Falling Edge Event</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSMCxA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSMCxB</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>A Output</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B Output</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: This is a subset of the 6-pin output of the push-pull PWM output, which is why pin functions are fixed in these positions, so they are compatible with that mode. See Section 24.3.6 “Push-Pull PWM with Four Full-Bridge and Complementary Outputs”
24.3.4 PULL-PULL PWM WITH COMPLEMENTARY OUTPUTS

The complementary push-pull PWM is used to drive transistor bridge circuits as well as synchronous switches on the secondary side of the bridge. The PWM waveform is output on four pins presented as two pairs of two-output signals with a normal and complementary output in each pair. Dead band can be inserted between the normal and complementary outputs at the transition times.

24.3.4.1 Mode Features

- Dead-band control is available
- No steering control available
- Primary PWM output is only on:
  - PSMCxA
  - PSMCxB
- Complementary PWM output is only on:
  - PSMCxE
  - PSMCxF

Note: This is a subset of the 6-pin output of the push-pull PWM output, which is why pin functions are fixed in these positions, so they are compatible with that mode. See Section 24.3.6 “Push-Pull PWM with Four Full-Bridge and Complementary Outputs”.

24.3.4.2 Waveform Generation

Push-Pull waveforms generate alternating outputs on the output pairs. Therefore, there are two sets of rising edge events and two sets of falling edge events.

Odd numbered period rising edge event:
- PSMCxE is set inactive
- Dead-band rising is activated (if enabled)
- PSMCxA is set active

Odd numbered period falling edge event:
- PSMCxA is set inactive
- Dead-band falling is activated (if enabled)
- PSMCxE is set active

Even numbered period rising edge event:
- PSMCxF is set inactive
- Dead-band rising is activated (if enabled)
- PSMCxB is set active

Even numbered period falling edge event:
- PSMCxB is set inactive
- Dead-band falling is activated (if enabled)
- PSMCxF is set active

FIGURE 24-7: PUSH-PULL WITH COMPLEMENTARY OUTPUTS PWM WAVEFORM
24.3.5 PUSH-PULL PWM WITH FOUR FULL-BRIDGE OUTPUTS

The full-bridge push-pull PWM is used to drive transistor bridge circuits as well as synchronous switches on the secondary side of the bridge.

24.3.5.1 Mode Features

- No Dead-band control
- No Steering control available
- PWM is output on the following four pins only:
  - PSMCxA
  - PSMCxB
  - PSMCxC
  - PSMCxD

Note: PSMCxA and PSMCxC are identical waveforms, and PSMCxB and PSMCxD are identical waveforms.

24.3.5.2 Waveform generation

Push-pull waveforms generate alternating outputs on the output pairs. Therefore, there are two sets of rising edge events and two sets of falling edge events.

Odd numbered period rising edge event:
  - PSMCxOUT0 and PSMCxOUT2 is set active
Odd numbered period falling edge event:
  - PSMCxOUT0 and PSMCxOUT2 is set inactive
Even numbered period rising edge event:
  - PSMCxOUT1 and PSMCxOUT3 is set active
Even numbered period falling edge event:
  - PSMCxOUT1 and PSMCxOUT3 is set inactive

Note: This is a subset of the 6-pin output of the push-pull PWM output, which is why pin functions are fixed in these positions, so they are compatible with that mode. See Section 24.3.6 “Push-Pull PWM with Four Full-Bridge and Complementary Outputs”.

FIGURE 24-8: PUSH-PULL PWM WITH 4 FULL-BRIDGE OUTPUTS
24.3.6  PUSH-PULL PWM WITH FOUR FULL-BRIDGE AND COMPLEMENTARY OUTPUTS

The push-pull PWM is used to drive transistor bridge circuits as well as synchronous switches on the secondary side of the bridge. It uses six outputs and generates PWM signals with dead band that alternate between the six outputs in even and odd cycles.

24.3.6.1  Mode Features and Controls

- Dead-band control is available
- No steering control available
- Primary PWM is output on the following four pins:
  - PSMCxA
  - PSMCxB
  - PSMCxC
  - PSMCxD
- Complementary PWM is output on the following two pins:
  - PSMCxE
  - PSMCxF

Note: PSMCxA and PSMCxC are identical waveforms, and PSMCxB and PSMCxD are identical waveforms.

24.3.6.2  Waveform Generation

Push-pull waveforms generate alternating outputs on two sets of pin. Therefore, there are two sets of rising edge events and two sets of falling edge events.

Odd numbered period rising edge event:
- PSMCxE is set inactive
- Dead-band rising is activated (if enabled)
- PSMCxA and PSMCxC are set active

Odd numbered period falling edge event:
- PSMCxA and PSMCxC are set inactive
- Dead-band falling is activated (if enabled)
- PSMCxE is set active

Even numbered period rising edge event:
- PSMCxF is set inactive
- Dead-band rising is activated (if enabled)
- PSMCxB and PSMCxD are set active

Even numbered period falling edge event:
- PSMCxB and PSMCxOUT3 are set inactive
- Dead-band falling is activated (if enabled)
- PSMCxF is set active

FIGURE 24-9:  PUSH-PULL 4 FULL-BRIDGE AND COMPLEMENTARY PWM
24.3.7 PULSE-SKIPPING PWM

The pulse-skipping PWM is used to generate a series of fixed-length pulses that can be triggered at each period event. A rising edge event will be generated when any enabled asynchronous rising edge input is active when the period event occurs, otherwise no event will be generated.

The rising edge event occurs based upon the value in the PSMCxPH register pair.

The falling edge event always occurs according to the enabled event inputs without qualification between any two inputs.

24.3.7.1 Mode Features
- No dead-band control available
- No steering control available
- PWM is output to only one pin: PSMCxA

24.3.7.2 Waveform Generation

Rising Edge Event
If any enabled asynchronous rising edge event = 1 when there is a period event, then upon the next synchronous rising edge event:
- PSMCxA is set active

Falling Edge Event
- PSMCxA is set inactive

Note: To use this mode, an external source must be used for the determination of whether or not to generate the set pulse. If the phase time base is used, it will either always generate a pulse or never generate a pulse based on the PSMCxPH value.

FIGURE 24-10: PULSE-SKIPPING PWM WAVEFORM
24.3.8 PULSE-SKIPPING PWM WITH COMPLEMENTARY OUTPUTS

The pulse-skipping PWM is used to generate a series of fixed-length pulses that may or may not be triggered at each period event. If any of the sources enabled to generate a rising edge event are high when a period event occurs, a pulse will be generated. If the rising edge sources are low at the period event, no pulse will be generated.

The rising edge occurs based upon the value in the PSMCxPH register pair.

The falling edge event always occurs according to the enabled event inputs without qualification between any two inputs.

24.3.8.1 Mode Features

- Dead-band control is available
- No steering control available
- Primary PWM is output on only PSMCxA.
- Complementary PWM is output on only PSMCxB.

24.3.8.2 Waveform Generation

### Rising Edge Event

- Complementary output is set inactive
- Dead-band rising is activated (if enabled)
- Primary output is set active

### Falling Edge Event

- Primary output is set inactive
- Dead-band falling is activated (if enabled)
- Complementary output is set active

**Note:** To use this mode, an external source must be used for the determination of whether or not to generate the set pulse. If the phase time base is used, it will either always generate a pulse or never generate a pulse based on the PSMCxPH value.

**FIGURE 24-11: PULSE-SKIPPING WITH COMPLEMENTARY OUTPUT PWM WAVEFORM**

<table>
<thead>
<tr>
<th>PWM Period Number</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Period Event</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
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<td></td>
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<td>Asynchronous</td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>Synchronous</td>
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<td></td>
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</tr>
<tr>
<td>PSMCxA</td>
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<td></td>
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<td></td>
<td></td>
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<tr>
<td>PSMxCB</td>
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</tr>
</tbody>
</table>

- Rising Edge Dead Band
- Falling Edge Dead Band
24.3.9 ECCP COMPATIBLE FULL-BRIDGE PWM

This mode of operation is designed to match the Full-Bridge mode from the ECCP module. It is called ECCP compatible as the term “full-bridge” alone has different connotations in regards to the output waveforms.

Full-Bridge Compatible mode uses the same waveform events as the single PWM mode to generate the output waveforms.

There are both Forward and Reverse modes available for this operation, again to match the ECCP implementation. Direction is selected with the mode control bits.

24.3.9.1 Mode Features

- Dead-band control available on direction switch
  - Changing from forward to reverse uses the falling edge dead-band counters.
  - Changing from reverse to forward uses the rising edge dead-band counters.
- No steering control available
- PWM is output on the following four pins only:
  - PSMCxA
  - PSMCxB
  - PSMCxC
  - PSMCxD

24.3.9.2 Waveform Generation - Forward

In this mode of operation, three of the four pins are static. PSMCxA is the only output that changes based on rising edge and falling edge events.

Static Signal Assignment
- Outputs set to active state
  - PSMCxD
- Outputs set to inactive state
  - PSMCxB
  - PSMCxC

Rising Edge Event
- PSMCxA is set active

Falling Edge Event
- PSMCxA is set inactive

24.3.9.3 Waveform Generation – Reverse

In this mode of operation, three of the four pins are static. Only PSMCxB toggles based on rising edge and falling edge events.

Static Signal Assignment
- Outputs set to active state
  - PSMCxC
- Outputs set to inactive state
  - PSMCxA
  - PSMCxD

Rising Edge Event
- PSMCxB is set active

Falling Edge Event
- PSMCxB is set inactive

---

FIGURE 24-12: ECCP COMPATIBLE FULL-BRIDGE PWM WAVEFORM – PSMCXSTR0 = 0FH

<table>
<thead>
<tr>
<th>PWM Period Number</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
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<tr>
<td>Forward Event</td>
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</tr>
<tr>
<td>Falling Edge Event</td>
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<td></td>
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</tr>
<tr>
<td>PSMCxA</td>
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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>PSMCxB</td>
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<td></td>
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<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>PSMCxC</td>
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<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>PSMCxD</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>
24.3.10 VARIABLE FREQUENCY – FIXED DUTY CYCLE PWM

This mode of operation is quite different from all of the other modes. It uses only the period event for waveform generation. At each period event, the PWM output is toggled.

The rising edge and falling edge events are unused in this mode.

24.3.10.1 Mode Features

• No dead-band control available
• No steering control available
• Fractional Frequency Adjust
  - Fine period adjustments are made with the PSMC Fractional Frequency Adjust (PSMCxFFA) register (Register 24-28)
• PWM is output on the following pin only:
  - PSMCxA

24.3.10.2 Waveform Generation

Period Event

• Output of PSMCxA is toggled
• FFA counter is incremented by the 4-bit value in PSMCxF FA

FIGURE 24-13: VARIABLE FREQUENCY – FIXED DUTY CYCLE PWM WAVEFORM
24.3.11 VARIABLE FREQUENCY - FIXED DUTY CYCLE PWM WITH COMPLEMENTARY OUTPUTS

This mode is the same as the single output Fixed Duty Cycle mode except a complementary output with dead-band control is generated.

The rising edge and falling edge events are unused in this mode. Therefore, a different triggering mechanism is required for the dead-band counters.

A period events that generate a rising edge on PSMCxA use the rising edge dead-band counters.

A period events that generate a falling edge on PSMCxA use the falling edge dead-band counters.

24.3.11.1 Mode Features

- Dead-band control is available
- No steering control available
- Fractional Frequency Adjust
  - Fine period adjustments are made with the PSMC Fractional Frequency Adjust (PSMCxFFA) register (Register 24-28)
- Primary PWM is output to the following pin:
  - PSMCxA
- Complementary PWM is output to the following pin:
  - PSMCxB

24.3.11.2 Waveform Generation

**Period Event**

When output is going inactive to active:
- Complementary output is set inactive
- FFA counter is incremented by the 4-bit value in PSMCFFA register.
- Dead-band rising is activated (if enabled)
- Primary output is set active

When output is going active to inactive:
- Primary output is set inactive
- FFA counter is incremented by the 4-bit value in PSMCFFA register
- Dead-band falling is activated (if enabled)
- Complementary output is set active

**FIGURE 24-14: VARIABLE FREQUENCY – FIXED DUTY CYCLE PWM WITH COMPLEMENTARY OUTPUTS WAVEFORM**

<table>
<thead>
<tr>
<th>PWM Period Number</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
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<th>7</th>
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<tbody>
<tr>
<td>period_event</td>
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<td></td>
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<td>Rising Edge Event</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Unused in this mode</td>
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<tr>
<td>Falling Edge Event</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Unused in this mode</td>
</tr>
<tr>
<td>PSMCxA</td>
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<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>PSMCxB</td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Falling Edge Dead Band</td>
</tr>
</tbody>
</table>

Unused in this mode
24.3.12 3-PHASE PWM

The 3-Phase mode of operation is used in 3-phase power supply and motor drive applications configured as three half-bridges. A half-bridge configuration consists of two power driver devices in series, between the positive power rail (high side) and negative power rail (low side). The three outputs come from the junctions between the two drivers in each half-bridge. When the steering control selects a phase drive, power flows from the positive rail through a high-side power device to the load and back to the power supply through a low-side power device.

In this mode of operation, all six PSMC outputs are used, but only two are active at a time.

The two active outputs consist of a high-side driver and low-side driver output.

24.3.12.1 Mode Features

- No dead-band control is available
- PWM can be steered to the following six pairs:
  - PSMCxA and PSMCxD
  - PSMCxA and PSMCxF
  - PSMCxC and PSMCxF
  - PSMCxC and PSMxCB
  - PSMxE and PSMxCB
  - PSMxE and PSMxD

24.3.12.2 Waveform Generation

3-phase steering has a more complex waveform generation scheme than the other modes. There are several factors which go into what waveforms are created.

The PSMC outputs are grouped into three sets of drivers: one for each phase. Each phase has two associated PWM outputs: one for the high-side drive and one for the low-side drive.

High Side drives are indicated by 1H, 2H and 3H.
Low Side drives are indicated by 1L, 2L, 3L.

Phase grouping is mapped as shown in Table 24-1. There are six possible phase drive combinations. Each phase drive combination activates two of the six outputs and deactivates the other four. Phase drive is selected with the steering control as shown in Table 24-2.

### TABLE 24-1: PHASE GROUPING

<table>
<thead>
<tr>
<th>PSMC grouping</th>
<th>1H</th>
<th>1L</th>
<th>2H</th>
<th>2L</th>
<th>3H</th>
<th>3L</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSMCxA</td>
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<td>PSMxCB</td>
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<tr>
<td>PSMxCC</td>
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</tr>
<tr>
<td>PSMxCD</td>
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<td></td>
</tr>
<tr>
<td>PSMxCE</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSMxCF</td>
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<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

### TABLE 24-2: 3-PHASE STEERING CONTROL

<table>
<thead>
<tr>
<th>PSMC outputs</th>
<th>00h</th>
<th>01h</th>
<th>02h</th>
<th>04h</th>
<th>08h</th>
<th>10h</th>
<th>20h</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSMCxA</td>
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<td>inactive</td>
<td>active</td>
<td>active</td>
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<tr>
<td>PSMxCB</td>
<td>1L</td>
<td>inactive</td>
<td>inactive</td>
<td>inactive</td>
<td>active</td>
<td>active</td>
<td>inactive</td>
</tr>
<tr>
<td>PSMxCC</td>
<td>2H</td>
<td>inactive</td>
<td>inactive</td>
<td>inactive</td>
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<td>active</td>
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<tr>
<td>PSMxCD</td>
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<tr>
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<td>inactive</td>
<td>inactive</td>
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<td>active</td>
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<tr>
<td>PSMxCF</td>
<td>3L</td>
<td>inactive</td>
<td>inactive</td>
<td>active</td>
<td>inactive</td>
<td>inactive</td>
<td>inactive</td>
</tr>
</tbody>
</table>

Note 1: Steering for any value other than those shown will default to the output combination of the Least Significant steering bit that is set.

High/Low Side Modulation Enable

It is also possible to enable the PWM output on the low side or high side drive independently using the PxLSMEN and PxHSMEN bits of the PSMC Steering Control 1 (PSMCxSTR1) register (Register 24-32).

When the PxHSMEN bit is set, the active-high side output listed in Table 24-2 is modulated using the normal rising edge and falling edge events.

When the PxLSMEN bit is set, the active-low side output listed in Table 24-2 is modulated using the normal rising edge and falling edge events.

When both the PxHSMEN and PxLSMEN bits are cleared, the active outputs listed in Table 24-2 go immediately to the rising edge event states and do not change.

Rising Edge Event

- Active outputs are set to their active states

Falling Edge Event

- Active outputs are set to their inactive state
FIGURE 24-15: 3-PHASE PWM STEERING WAVEFORM (PXHSMEN = 0 AND PXLSMEN = 1)
24.4 Dead-Band Control

The dead-band control provides non-overlapping PWM signals to prevent shoot-through current in series connected power switches. Dead-band control is available only in modes with complementary drive and when changing direction in the ECCP compatible Full-Bridge modes.

The module contains independent 8-bit dead-band counters for rising edge and falling edge dead-band control.

24.4.1 DEAD-BAND TYPES

There are two separate dead-band generators available, one for rising edge events and the other for falling edge events.

24.4.1.1 Rising Edge Dead Band

Rising edge dead-band control is used to delay the turn-on of the primary switch driver from when the complementary switch driver is turned off.

Rising edge dead band is initiated with the rising edge event.

Rising edge dead-band time is adjusted with the PSMC Rising Edge Dead-Band Time (PSMCxDBR) register (Register 24-26).

If the PSMCxDBR register value is changed when the PSMC is enabled, the new value does not take effect until the first period event after the PSMCxLD bit is set.

24.4.1.2 Falling Edge Dead Band

Falling edge dead-band control is used to delay the turn-on of the complementary switch driver from when the primary switch driver is turned off.

Falling edge dead band is initiated with the falling edge event.

Falling edge dead-band time is adjusted with the PSMC Falling Edge Dead-Band Time (PSMCxDBF) register (Register 24-27).

If the PSMCxDBF register value is changed when the PSMC is enabled, the new value does not take effect until the first period event after the PSMCxLD bit is set.

24.4.2 DEAD-BAND ENABLE

When a mode is selected that may use dead-band control, dead-band timing is enabled by setting one of the enable bits in the PSMC Control (PSMCxCON) register (Register 24-1).

Rising edge dead band is enabled with the PxDBRE bit.

Rising edge dead band is enabled with the PxDBFE bit.

Enable changes take effect immediately.

24.4.3 DEAD-BAND CLOCK SOURCE

The dead-band counters are incremented on every rising edge of the psmc_clk signal.

24.4.4 DEAD-BAND UNCERTAINTY

When the rising and falling edge events that trigger the dead-band counters come from asynchronous inputs, there will be uncertainty in the actual dead-band time of each cycle. The maximum uncertainty is equal to one psmc_clk period. The one clock of uncertainty may still be introduced, even when the dead-band count time is cleared to zero.

24.4.5 DEAD-BAND OVERLAP

There are two cases of dead-band overlap and each is treated differently due to system requirements.

24.4.5.1 Rising to Falling Overlap

In this case, the falling edge event occurs while the rising edge dead-band counter is still counting. The following sequence occurs:

1. Dead-band rising count is terminated.
2. Dead-band falling count is initiated.
3. Primary output is suppressed.

24.4.5.2 Falling to Rising Overlap

In this case, the rising edge event occurs while the falling edge dead-band counter is still counting. The following sequence occurs:

1. Dead-band falling count is terminated.
2. Dead-band rising count is initiated.
3. Complementary output is suppressed.

24.4.5.3 Rising Edge-to-Rising Edge or Falling Edge-to-Falling Edge

In cases where one of the two dead-band counters is set for a short period, or disabled all together, it is possible to get rising-to-rising or falling-to-falling overlap. When this is the case, the following sequence occurs:

1. Dead-band count is terminated.
2. Dead-band count is restarted.
3. Output waveform control freezes in the present state.
4. Restarted dead-band count completes.
5. Output control resumes normally.
24.5 Output Steering

Output steering allows for PWM signals generated by the PSMC module to be placed on different pins under software control. Synchronized steering will hold steering changes until the first period event after the PSMCxLD bit is set. Unsynchronized steering changes will take place immediately.

Output steering is available in the following modes:
- 3-phase PWM
- Single PWM
- Complementary PWM

24.5.1 3-PHASE STEERING

3-phase steering is available in the 3-Phase Modulation mode only. For more details on 3-phase steering refer to Section 24.3.12 “3-Phase PWM”.

24.5.2 SINGLE PWM STEERING

In Single PWM Steering mode, the single PWM signal can be routed to any combination of the PSMC output pins. Examples of unsynchronized single PWM steering are shown in Figure 24-16.

FIGURE 24-16: SINGLE PWM STEERING WAVEFORM (NO SYNCHRONIZATION)

With synchronization disabled, it is possible to get glitches on the PWM outputs.
24.5.3 COMPLEMENTARY PWM STEERING

In Complementary PWM Steering mode, the primary PWM signal (non-complementary) and complementary signal can be steered according to their respective type.

Primary PWM signal can be steered to any of the following outputs:
- PSMCxA
- PSMCxC
- PSMCxE

The complementary PWM signal can be steered to any of the following outputs:
- PSMCxB
- PSMCxD
- PSMCxE

Examples of unsynchronized complementary steering are shown in Figure 24-17.

FIGURE 24-17: COMPLEMENTARY PWM STEERING WAVEFORM (NO SYNCHRONIZATION, ZERO DEAD-BAND TIME)
24.5.4 SYNCHRONIZED PWM STEERING

In Single, Complementary and 3-phase PWM modes, it is possible to synchronize changes to steering selections with the period event. This is so that PWM outputs do not change in the middle of a cycle and therefore, disrupt operation of the application.

Steering synchronization is enabled by setting the PxSSYNC bit of the PSMC Steering Control 1 (PSMCxSTR1) register (Register 24-32).

When synchronized steering is enabled while the PSMC module is enabled, steering changes do not take effect until the first period event after the PSMCxLD bit is set.

Examples of synchronized steering are shown in Figure 24-18.

24.5.5 INITIALIZING SYNCHRONIZED STEERING

If synchronized steering is to be used, special care should be taken to initialize the PSMC Steering Control 0 (PSMCxSTR0) register (Register 24-31) in a safe configuration before setting either the PSMCxEN or PSMCxLD bits. When either of those bits are set, the PSMCxSTR0 value at that time is loaded into the synchronized steering output buffer. The buffer load occurs even if the PxSSYNC bit is low. When the PxSSYNC bit is set, the outputs will immediately go to the drive states in the preloaded buffer.

FIGURE 24-18: PWM STEERING WITH SYNCHRONIZATION WAVEFORM
24.6  PSMC Modulation (Burst Mode)

PSMC modulation is a method to stop/start PWM operation of the PSMC without having to disable the module. It also allows other modules to control the operational period of the PSMC. This is also referred to as Burst mode.

This is a method to implement PWM dimming.

24.6.1 MODULATION ENABLE

The modulation function is enabled by setting the PxMDLEN bit of PSMC Modulation Control (PSMCxMDL) register (Register 24-2).

When modulation is enabled, the modulation source controls when the PWM signals are active and inactive.

When modulation is disabled, the PWM signals operate continuously, regardless of the selected modulation source.

24.6.2 MODULATION SOURCES

There are multiple sources that can be used for modulating the PSMC. However, unlike the PSMC input sources, only one modulation source can be selected at a time. Modulation sources include:

- PSMCxIN pin
- Any CCP output
- Any Comparator output
- PxMDLBIT of the PSMCxMDL register

24.6.2.1 PxMDLBIT Bit

The PxMDLBIT bit of the PSMC Modulation Control (PSMCxMDL) register (Register 24-2) allows for software modulation control without having to enable/disable other module functions.

24.6.3 MODULATION EFFECT ON PWM SIGNALS

When modulation starts, the PSMC begins operation on a new period, just as if it had rolled over from one period to another during continuous operation.

When modulation stops, its operation depends on the type of waveform being generated.

In operation modes other than Fixed Duty Cycle, the PSMC completes its current PWM period and then freezes the module. The PSMC output pins are forced into the default inactive state ready for use when modulation starts.

In Fixed Duty Cycle mode operation, the PSMC continues to operate until the period event changes the PWM to its inactive state, at which point the PSMC module is frozen. The PSMC output pins are forced into the default inactive state ready for use when modulation starts.

---

**FIGURE 24-19: PSMC MODULATION WAVEFORM**

![PSMC Modulation Waveform Diagram]
24.7 Auto-Shutdown
Auto-shutdown is a method to immediately override the PSMC output levels with specific overrides that allow for safe shutdown of the application.
Auto-shutdown includes a mechanism to allow the application to restart under different conditions.
Auto-shutdown is enabled with the PxASDEN bit of the PSMC Auto-shutdown Control (PSMCxASDC) register (Register 24-15). All auto-shutdown features are enabled when PxASDEN is set and disabled when cleared.

24.7.1 SHUTDOWN
There are two ways to generate a shutdown event:
- Manual
- External Input

24.7.1.1 Manual Override
The auto-shutdown control register can be used to manually override the pin functions. Setting the PxASE bit of the PSMC Auto-shutdown Control (PSMCxASDC) register (Register 24-15) generates a software shut-down event.
The auto-shutdown override will persist as long as PxASE remains set.

24.7.1.2 External Input Source
Any of the given sources that are available for event generation are also available for system shut-down. This is so that external circuitry can monitor and force a shutdown without any software overhead. Auto-shutdown sources are selected with the PSMC Auto-shutdown Source (PSMCxASDS) register (Register 24-17).
When any of the selected external auto-shutdown sources go high, the PxASE bit is set and an auto-shutdown interrupt is generated.

Note: The external shutdown sources are level sensitive, not edge sensitive. The shutdown condition will persist as long as the circuit is driving the appropriate logic level.

24.7.2 PIN OVERRIDE LEVELS
The logic levels driven to the output pins during an auto-shutdown event are determined by the PSMC Auto-shutdown Output Level (PSMCxASDL) register (Register 24-16).

24.7.2.1 PIN Override Enable
Setting the PxASDOV bit of the PSMC Auto-shutdown Control (PSMCxASDC) register (Register 24-15) will also force the override levels onto the pins, exactly like what happens when the auto-shutdown is used. However, whereas setting PxASE causes an auto-shutdown interrupt, setting PxASDOV does not generate an interrupt.

24.7.3 RESTART FROM AUTO-SHUTDOWN
After an auto-shutdown event has occurred, there are two ways for the module to resume operation:
- Manual restart
- Automatic restart
The restart method is selected with the PxARSEN bit of the PSMC Auto-shutdown Control (PSMCxASDC) register (Register 24-15).

24.7.3.1 Manual Restart
When PxARSEN is cleared, and once the PxASDE bit is set, it will remain set until cleared by software. The PSMC will restart on the period event after PxASDE bit is cleared in software.

24.7.3.2 Auto-Restart
When PxARSEN is set, the PxASDE bit will clear automatically when the source causing the Reset and no longer asserts the shut-down condition. The PSMC will restart on the next period event after the auto-shutdown condition is removed.
Examples of manual and automatic restart are shown in Figure 24-20.

Note: Whether manual or auto-restart is selected, the PxASDE bit cannot be cleared in software when the auto-shutdown condition is still present.
FIGURE 24-20: AUTO-SHUTDOWN AND RESTART WAVEFORM

- **Base PWM signal**
- **PxARSEN**
- **Auto-Shutdown Source**
- **PSMCx Auto-shutdown int flag bit**
- **PxASE**
- **PSMCxA**
- **PSMCxB**

Operational States:
- **Normal Output**
- **Auto-shutdown**
- **Manual Restart**
- **Auto-restart**

Event Timeline:
- **1:** Initial state
- **2:** Auto-shutdown event
- **3:** Cleared in software
- **4:** Cleared in hardware
- **5:** Next Period Event
24.8 PSMC Synchronization

It is possible to synchronize the periods of two or more PSMC modules together, provided that all modules are on the same device.

Synchronization is achieved by sending a sync signal from the master PSMC module to the desired slave modules. This sync signal generates a period event in each slave module, thereby aligning all slaves with the master. This is useful when an application requires different PWM signal generation from each module but the waveforms must be consistent within a PWM period.

24.8.1 SYNCHRONIZATION SOURCES

The synchronization source can be any PSMC module on the same device. For example, in a device with two PSMC modules, the possible sources for each device is as shown below:

- Sources for PSMC1
  - PSMC2
- Sources for PSMC2
  - PSMC1

24.8.1.1 PSMC Internal Connections

The sync signal from the master PSMC module is essentially that modules period event trigger. The slave PSMC modules reset their PSMCxTMR with the sync signal instead of their own period event.

Enabling a module as a slave recipient is done with the PxSYNC bits of the PSMC Synchronization Control (PSMCxSYNC) registers; registers 24-3 and 24-4.

24.8.1.2 Phase Offset Synchronization

The synchronization output signal from the PSMC module is selectable. The sync_out source may be either:

- Period Event
- Rising Event

Source selection is made with the PxPOFST bit of the PSMCxSYNC registers, registers 24-3, 24-4 and 24-6.

When the PxPOFST bit is set, the sync_out signal comes from the rising event and the period event replaces the rising event as the start of the active drive period. When PxPOFST is set, duty cycles of up to 100% are achievable in both the slave and master.

When PXPOFST is clear, the sync_out signal comes from the period event. When PxPOFST is clear, rising events that start after the period event remove the equivalent start delay percentage from the maximum 100% duty cycle.

24.8.1.3 Synchronization Skid

When the sync_out source is the Period Event, the slave synchronous rising and falling events will lag by one psmc_clk period. When the sync_out source is the Rising Event, the synchronous events will lag by two clock periods. To compensate for this, the values in PHH:PHL and DCH:DCL registers can be reduced by the number of lag cycles.
24.9 Fractional Frequency Adjust (FFA)

FFA is a method by which PWM resolution can be improved on 50% fixed duty cycle signals. Higher resolution is achieved by altering the PWM period by a single count for calculated intervals. This increased resolution is based upon the PWM frequency averaged over a large number of PWM periods. For example, if the period event time is increased by one psmc_clk period (TPSMC_CLK) every N events, then the effective resolution of the average event period is TPSMC_CLK/N.

When active, after every period event the FFA hardware adds the PSMCxxFFA value with the previously accumulated result. Each time the addition causes an overflow, the period event time is increased by one. Refer to Figure 24-22.

FIGURE 24-22: FFA BLOCK DIAGRAM.

The FFA function is only available when using one of the two Fixed Duty Cycle modes of operation. In fixed duty cycle operation each PWM period is comprised of two period events. That is why the PWM periods in Table 24-3 example calculations are multiplied by two as opposed to the normal period calculations for normal mode operation.

The extra resolution gained by the FFA is based upon the number of bits in the FFA register and the psmc_clk frequency. The parameters of interest are:

- **TPWM** – this is the lower bound of the PWM period that will be adjusted
- **TPWM+1** – this is the upper bound of the PWM period that will be adjusted. This is used to help determine the step size for each increment of the FFA register
- **TRESOLUTION** – each increment of the FFA register will add this amount of period to average PWM frequency

### TABLE 24-3: FRACTIONAL FREQUENCY ADJUST CALCULATIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPSMC_CLK</td>
<td>64 MHz</td>
</tr>
<tr>
<td>TPSMC_CLK</td>
<td>15.625 ns</td>
</tr>
<tr>
<td>PSMC&lt;15:0&gt;</td>
<td>00FFh = 255</td>
</tr>
<tr>
<td>TPWM</td>
<td>= (PSMC&lt;15:0&gt;+1)<em>2</em>TPSMC_CLK = 256<em>2</em>15.625ns = 8 us</td>
</tr>
<tr>
<td>FPWM</td>
<td>125 kHz</td>
</tr>
<tr>
<td>TPWM+1</td>
<td>= (PSMC&lt;15:0&gt;+2)<em>2</em>TPSMC_CLK = 257<em>2</em>15.625ns = 8.03125 us</td>
</tr>
<tr>
<td>FPWM+1</td>
<td>= 124.513 kHz</td>
</tr>
<tr>
<td>TRESOLUTION</td>
<td>= (TPWM+1-TPWM)/2^FFA-Bits = (8.03125us - 8.0 us)/16 = 0.03125us/16 ~ 1.95 ns</td>
</tr>
<tr>
<td>FRESOLUTION</td>
<td>(FPWM+1-FPWM)/2^FFA-Bits ~ -30.4 Hz</td>
</tr>
</tbody>
</table>
### TABLE 24-4: SAMPLE FFA OUTPUT PERIODS/FREQUENCIES

<table>
<thead>
<tr>
<th>FFA number</th>
<th>Output Frequency (kHz)</th>
<th>Step Size (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>125.000</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>124.970</td>
<td>-30.4</td>
</tr>
<tr>
<td>2</td>
<td>124.939</td>
<td>-60.8</td>
</tr>
<tr>
<td>3</td>
<td>124.909</td>
<td>-91.2</td>
</tr>
<tr>
<td>4</td>
<td>124.878</td>
<td>-121.6</td>
</tr>
<tr>
<td>5</td>
<td>124.848</td>
<td>-152.0</td>
</tr>
<tr>
<td>6</td>
<td>124.818</td>
<td>-182.4</td>
</tr>
<tr>
<td>7</td>
<td>124.787</td>
<td>-212.8</td>
</tr>
<tr>
<td>8</td>
<td>124.757</td>
<td>-243.2</td>
</tr>
<tr>
<td>9</td>
<td>124.726</td>
<td>-273.6</td>
</tr>
<tr>
<td>10</td>
<td>124.696</td>
<td>-304.0</td>
</tr>
<tr>
<td>11</td>
<td>124.666</td>
<td>-334.4</td>
</tr>
<tr>
<td>12</td>
<td>124.635</td>
<td>-364.8</td>
</tr>
<tr>
<td>13</td>
<td>124.605</td>
<td>-395.2</td>
</tr>
<tr>
<td>14</td>
<td>124.574</td>
<td>-425.6</td>
</tr>
<tr>
<td>15</td>
<td>124.544</td>
<td>-456.0</td>
</tr>
</tbody>
</table>
24.10 Register Updates

There are 10 double-buffered registers that can be updated “on the fly”. However, due to the asynchronous nature of the potential updates, a special hardware system is used for the updates.

There are two operating cases for the PSMC:
• module is enabled
• module is disabled

24.10.1 DOUBLE BUFFERED REGISTERS

The double-buffered registers that are affected by the special hardware update system are:
• PSMCxPRL
• PSMCxPRH
• PSMCxDCL
• PSMCxDCH
• PSMCxPHL
• PSMCxPHH
• PSMCxDBR
• PSMCxDBF
• PSMCxBLKR
• PSMCxBLKF
• PSMCxSTR0 (when the PxSSYNCE bit is set)

24.10.2 MODULE DISABLED UPDATES

When the PSMC module is disabled (PSMCxEN = 0), any write to one of the buffered registers will also write directly to the buffer. This means that all buffers are loaded and ready for use when the module is enabled.

24.10.3 MODULE ENABLED UPDATES

When the PSMC module is enabled (PSMCxEN = 1), the PSMCxLD bit of the PSMC Control (PSMCxCON) register (Register 24-1) must be used.

When the PSMCxLD bit is set, the transfer from the register to the buffer occurs on the next period event. The PSMCxLD bit is automatically cleared by hardware after the transfer to the buffers is complete.

The reason that the PSMCxLD bit is required is that depending on the customer application and operation conditions, all 10 registers may not be updated in one PSMC period. If the buffers are loaded at different times (i.e., DCL gets updated, but DCH does not OR DCL and DCL are updated by PRH and PRL are not), then unintended operation may occur.

The sequence for loading the buffer registers when the PSMC module is enabled is as follows:
1. Software updates all registers.
2. Software sets the PSMCxLD bit.
3. Hardware updates all buffers on the next period event.
4. Hardware clears PSMCxLD bit.

24.11 Operation During Sleep

The PSMC continues to operate in Sleep with the following clock sources:
• Internal 64 MHz
• External clock
### 24.12 Register Definitions: PSMC Control

#### REGISTER 24-1: PSMCxCON: PSMC CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PSMCxEN: PSMC Module Enable bit</td>
<td>1 = PSMCx module is enabled, 0 = PSMCx module is disabled</td>
</tr>
<tr>
<td>6</td>
<td>PSMCxLD: PSMC Load Buffer Enable bit</td>
<td>1 = PSMCx registers are ready to be updated with the appropriate register contents, 0 = PSMCx buffer update complete</td>
</tr>
<tr>
<td>5</td>
<td>PxDBFE: PSMC Falling Edge Dead-Band Enable bit</td>
<td>1 = PSMCx falling edge dead band enabled, 0 = PSMCx falling edge dead band disabled</td>
</tr>
<tr>
<td>4</td>
<td>PxDBRE: PSMC Rising Edge Dead-Band Enable bit</td>
<td>1 = PSMCx rising edge dead band enabled, 0 = PSMCx rising edge dead band disabled</td>
</tr>
<tr>
<td>3-0</td>
<td>PxMODE&lt;3:0&gt;: PSMC Operating Mode bits</td>
<td>1111 = Reserved, 1110 = Reserved, 1101 = Reserved, 1100 = 3-phase steering PWM, 1011 = Fixed duty cycle, variable frequency, complementary PWM, 1010 = Fixed duty cycle, variable frequency, single PWM, 1001 = ECCP compatible Full-Bridge forward output, 1000 = ECCP compatible Full-Bridge reverse output, 0111 = Pulse-skipping with complementary output, 0110 = Pulse-skipping PWM output, 0101 = Push-pull with four full-bridge outputs and complementary outputs, 0100 = Push-pull with four full-bridge outputs, 0011 = Push-pull with complementary outputs, 0010 = Push-pull output, 0001 = Single PWM with complementary output (with PWM steering capability), 0000 = Single PWM waveform generation (with PWM steering capability)</td>
</tr>
</tbody>
</table>
## REGISTER 24-2: PSMCxMDL: PSMC MODULATION CONTROL REGISTER

| R/W-0/0 | R/W-0/0 | R/W-0/0 | U-0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | — | — |
|---|---|---|---|---|---|---|---|---|
| PxMDLEN | PxMDLPOL | PxMDLBIT | — | — | — | — | — | PxMSRC<3:0> |

### bit 7
**PxMDLEN**: PSMC Periodic Modulation Mode Enable bit

- **1**: PSMCx is active when input signal selected by PxMSRC<3:0> is in its active state (see PxMPOL)
- **0**: PSMCx module is always active

### bit 6
**PxMDLPOL**: PSMC Periodic Modulation Polarity bit

- **1**: PSMCx is active when the PSMCx Modulation source output equals logic ‘0’ (active-low)
- **0**: PSMCx is active when the PSMCx Modulation source output equals logic ‘1’ (active-high)

### bit 5
**PxMDLBIT**: PSMC Periodic Modulation Software Control bit

- PxMDLEN = 1 AND PxMSRC<3:0> = 0000
- **1**: PSMCx is active when the PxMDLPOL equals logic ‘0’
- **0**: PSMCx is active when the PxMDLPOL equals logic ‘1’

PxMDLEN = 0 OR (PxMDLEN = 1 and PxMSRC<3:0> <> ’0000’)

*Does not affect module operation*

### bit 4
**Unimplemented**: Read as ‘0’

### bit 3-0
**PxMSRC<3:0>**: PSMC Periodic Modulation Source Selection bits

- 1111 = Reserved
- 1110 = Reserved
- 1101 = Reserved
- 1100 = Reserved
- 1011 = Reserved
- 1010 = Reserved
- 1001 = Reserved
- 1000 = PSMCx Modulation Source is PSMCxIN pin
- 0111 = Reserved
- 0110 = PSMCx Modulation Source is CCP2
- 0101 = PSMCx Modulation Source is CCP1
- 0100 = Reserved
- 0011 = PSMCx Modulation Source is sync_C3OUT
- 0010 = PSMCx Modulation Source is sync_C2OUT
- 0001 = PSMCx Modulation Source is sync_C1OUT
- 0000 = PSMCx Modulation Source is PxMDLBIT register bit
### REGISTER 24-3: PSMC1SYNC: PSMC1 SYNCHRONIZATION CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td><strong>P1POFST: PSMC1 Phase Offset Control bit</strong></td>
<td>1 = sync_out source is phase event and latch set source is synchronous period event 0 = sync_out source is period event and latch set source is phase event</td>
</tr>
<tr>
<td>bit 6</td>
<td><strong>P1PRPOL: PSMC1 Period Polarity Event Control bit</strong></td>
<td>1 = Selected asynchronous period event inputs are inverted 0 = Selected asynchronous period event inputs are not inverted</td>
</tr>
<tr>
<td>bit 5</td>
<td><strong>P1DCPOL: PSMC1 Duty-cycle Event Polarity Control bit</strong></td>
<td>1 = Selected asynchronous duty-cycle event inputs are inverted 0 = Selected asynchronous duty-cycle event inputs are not inverted</td>
</tr>
<tr>
<td>bit 4-2</td>
<td><strong>Unimplemented</strong></td>
<td>Read as ‘0’</td>
</tr>
<tr>
<td>bit 1-0</td>
<td><strong>P1SYNC&lt;1:0&gt;: PSMC1 Period Synchronization Mode bits</strong></td>
<td>11 = PSMC1 is synchronized with the PSMC3 module (sync_in comes from PSMC3 sync_out) 10 = Reserved – Do not use 01 = PSMC1 is synchronized with the PSMC1 module (sync_in comes from PSMC1 sync_out) 00 = PSMC1 is synchronized with period event</td>
</tr>
</tbody>
</table>

### REGISTER 24-4: PSMC2SYNC: PSMC2 SYNCHRONIZATION CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td><strong>P2POFST: PSMC2 Phase Offset Control bit</strong></td>
<td>1 = sync_out source is phase event and latch set source is synchronous period event 0 = sync_out source is period event and latch set source is phase event</td>
</tr>
<tr>
<td>bit 6</td>
<td><strong>P2PRPOL: PSMC2 Period Polarity Event Control bit</strong></td>
<td>1 = Selected asynchronous period event inputs are inverted 0 = Selected asynchronous period event inputs are not inverted</td>
</tr>
<tr>
<td>bit 5</td>
<td><strong>P2DCPOL: PSMC2 Duty-cycle Event Polarity Control bit</strong></td>
<td>1 = Selected asynchronous duty-cycle event inputs are inverted 0 = Selected asynchronous duty-cycle event inputs are not inverted</td>
</tr>
<tr>
<td>bit 4-2</td>
<td><strong>Unimplemented</strong></td>
<td>Read as ‘0’</td>
</tr>
<tr>
<td>bit 1-0</td>
<td><strong>P2SYNC&lt;1:0&gt;: PSMC2 Period Synchronization Mode bits</strong></td>
<td>11 = PSMC2 is synchronized with the PSMC3 module (sync_in comes from PSMC3 sync_out) 10 = Reserved – Do not use 01 = PSMC2 is synchronized with the PSMC1 module (sync_in comes from PSMC1 sync_out) 00 = PSMC2 is synchronized with period event</td>
</tr>
</tbody>
</table>
### REGISTER 24-5: PSMC3SYNC: PSMC3 SYNCHRONIZATION CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4-2</th>
<th>Bit 1-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3POFST</td>
<td>P3PRPOL</td>
<td>P3DCPOL</td>
<td>_</td>
<td>P3SYNC&lt;1:0&gt;</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Legend:</th>
</tr>
</thead>
<tbody>
<tr>
<td>R = Readable bit</td>
</tr>
<tr>
<td>u = Bit is unchanged</td>
</tr>
<tr>
<td>'1' = Bit is set</td>
</tr>
</tbody>
</table>

- **bit 7**: **P3POFST**: PSMC3 Phase Offset Control bit
  - 1 = sync_out source is phase event and latch set source is synchronous period event
  - 0 = sync_out source is period event and latch set source is phase event

- **bit 6**: **P3PRPOL**: PSMC3 Period Polarity Event Control bit
  - 1 = Selected asynchronous period event inputs are inverted
  - 0 = Selected asynchronous period event inputs are not inverted

- **bit 5**: **P3DCPOL**: PSMC3 Duty-cycle Event Polarity Control bit
  - 1 = Selected asynchronous duty-cycle event inputs are inverted
  - 0 = Selected asynchronous duty-cycle event inputs are not inverted

- **bit 4-2**: **Unimplemented**: Read as '0'

- **bit 1-0**: **P3SYNC<1:0>**: PSMC3 Period Synchronization Mode bits
  - 11 = Reserved – Do not use
  - 10 = PSMC3 is synchronized with the PSMC2 module (sync_in comes from PSMC2 sync_out)
  - 01 = PSMC3 is synchronized with the PSMC1 module (sync_in comes from PSMC1 sync_out)
  - 00 = PSMC3 is synchronized with period event
## REGISTER 24-6: PSMCxCLK: PSMC CLOCK CONTROL REGISTER

<table>
<thead>
<tr>
<th>bit 7-6</th>
<th>Unimplemented: Read as ‘0’</th>
</tr>
</thead>
</table>

### bit 5-4

PxCPRE<1:0>: PSMCx Clock Prescaler Selection bits

- 11 = PSMCx Clock frequency/8
- 10 = PSMCx Clock frequency/4
- 01 = PSMCx Clock frequency/2
- 00 = PSMCx Clock frequency/1

### bit 3-2

Unimplemented: Read as ‘0’

### bit 1-0

PxCSRC<1:0>: PSMCx Clock Source Selection bits

- 11 = Reserved
- 10 = PSMCxCLK pin
- 01 = 64 MHz clock in from PLL
- 00 = FOSC system clock

## REGISTER 24-7: PSMCxOEN: PSMC OUTPUT ENABLE CONTROL REGISTER

<table>
<thead>
<tr>
<th>bit 7-6</th>
<th>Unimplemented: Read as ‘0’</th>
</tr>
</thead>
</table>

### bit 5-0

PxOEy: PSMCx Output y Enable bit

- 1 = PWM output is active on PSMCx output y pin
- 0 = PWM output is not active, normal port functions in control of pin

**Note 1:** These bits are not implemented on PSMC2.
**REGISTER 24-8: PSMCxPOL: PSMC POLARITY CONTROL REGISTER**

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PxPOLIN</td>
<td>PxPOLF(1)</td>
<td>PxPOLE(1)</td>
<td>PxPOLD(1)</td>
<td>PxPOLC(1)</td>
<td>PxPOLB</td>
<td>PxPOLA</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7** Unimplemented: Read as '0'

**bit 6** **PxPOLIN**: PSMCxIN Polarity bit
- **1** = PSMCxIN input is active-low
- **0** = PSMCxIN input is active-high

**bit 5-0** **PxPOLy**: PSMCx Output y Polarity bit(1)
- **1** = PWM PSMCx output y is active-low
- **0** = PWM PSMCx output y is active-high

**Note 1:** These bits are not implemented on PSMC2.

**REGISTER 24-9: PSMCxBLNK: PSMC BLANKING CONTROL REGISTER**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>PxFEBM1</td>
<td>PxFEBM0</td>
<td></td>
<td></td>
<td>PxREBM1</td>
<td>PxREBM0</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-6** Unimplemented: Read as '0'

**bit 5-4** **PxFEBM<1:0>** PSMC Falling Edge Blanking Mode bits
- **11** = Reserved – do not use
- **10** = Reserved – do not use
- **01** = Immediate blanking
- **00** = No blanking

**bit 3-2** Unimplemented: Read as '0'

**bit 1-0** **PxREBM<1:0>** PSMC Rising Edge Blanking Mode bits
- **11** = Reserved – do not use
- **10** = Reserved – do not use
- **01** = Immediate blanking
- **00** = No blanking
### REGISTER 24-10: PSMCxREBS: PSMC RISING EDGE BLANKED SOURCE REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>PxREBSIN</th>
<th>PxREBSC4</th>
<th>PxREBSC3</th>
<th>PxREBSC2</th>
<th>PxREBSC1</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets

- **1** = Bit is set
- **0** = Bit is cleared

- **PxREBSIN**: PSMCx Rising Edge Event Blanked from PSMCxIN pin
  - 1 = PSMCxIN pin cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
  - 0 = PSMCxIN pin is not blanked

- **bit 6-5**: Unimplemented: Read as ‘0’

- **bit 4**: PxREBSC4: PSMCx Rising Edge Event Blanked from sync_C4OUT
  - 1 = sync_C4OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
  - 0 = sync_C4OUT is not blanked

- **bit 3**: PxREBSC3: PSMCx Rising Edge Event Blanked from sync_C3OUT
  - 1 = sync_C3OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
  - 0 = sync_C3OUT is not blanked

- **bit 2**: PxREBSC2: PSMCx Rising Edge Event Blanked from sync_C2OUT
  - 1 = sync_C2OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
  - 0 = sync_C2OUT is not blanked

- **bit 1**: PxREBSC1: PSMCx Rising Edge Event Blanked from sync_C1OUT
  - 1 = sync_C1OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
  - 0 = sync_C1OUT is not blanked

- **bit 0**: Unimplemented: Read as ‘0’

### REGISTER 24-11: PSMCxFEBS: PSMC FALLING EDGE BLANKED SOURCE REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>PxFEBSIN</th>
<th>PxFEBSC4</th>
<th>PxFEBSC3</th>
<th>PxFEBSC2</th>
<th>PxFEBSC1</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets

- **1** = Bit is set
- **0** = Bit is cleared

- **PxFEBSIN**: PSMCx Falling Edge Event Blanked from PSMCxIN pin
  - 1 = PSMCxIN pin cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
  - 0 = PSMCxIN pin is not blanked

- **bit 6-5**: Unimplemented: Read as ‘0’

- **bit 4**: PxFEBSC4: PSMCx Falling Edge Event Blanked from sync_C4OUT
  - 1 = sync_C4OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
  - 0 = sync_C4OUT is not blanked

- **bit 3**: PxFEBSC3: PSMCx Falling Edge Event Blanked from sync_C3OUT
  - 1 = sync_C3OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
  - 0 = sync_C3OUT is not blanked

- **bit 2**: PxFEBSC2: PSMCx Falling Edge Event Blanked from sync_C2OUT
  - 1 = sync_C2OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
  - 0 = sync_C2OUT is not blanked

- **bit 1**: PxFEBSC1: PSMCx Falling Edge Event Blanked from sync_C1OUT
  - 1 = sync_C1OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
  - 0 = sync_C1OUT is not blanked

- **bit 0**: Unimplemented: Read as ‘0’
## REGISTER 24-12: PSMCxPHS: PSMC PHASE SOURCE REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value at POR and BOR</th>
<th>Value at all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PxPHSIN: PSMCx Rising Edge Event occurs on PSMCxIN pin</td>
<td>1</td>
<td>= Rising edge event will occur when PSMCxIN pin goes true</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>= PSMCxIN pin will not cause rising edge event</td>
</tr>
<tr>
<td>6-5</td>
<td>Unimplemented: Read as '0'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PxPHSC4: PSMCx Rising Edge Event occurs on sync_C4OUT output</td>
<td>1</td>
<td>= Rising edge event will occur when sync_C4OUT output goes true</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>= sync_C4OUT will not cause rising edge event</td>
</tr>
<tr>
<td>3</td>
<td>PxPHSC3: PSMCx Rising Edge Event occurs on sync_C3OUT output</td>
<td>1</td>
<td>= Rising edge event will occur when sync_C3OUT output goes true</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>= sync_C3OUT will not cause rising edge event</td>
</tr>
<tr>
<td>2</td>
<td>PxPHSC2: PSMCx Rising Edge Event occurs on sync_C2OUT output</td>
<td>1</td>
<td>= Rising edge event will occur when sync_C2OUT output goes true</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>= sync_C2OUT will not cause rising edge event</td>
</tr>
<tr>
<td>1</td>
<td>PxPHSC1: PSMCx Rising Edge Event occurs on sync_C1OUT output</td>
<td>1</td>
<td>= Rising edge event will occur when sync_C1OUT output goes true</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>= sync_C1OUT will not cause rising edge event</td>
</tr>
<tr>
<td>0</td>
<td>PxPHST: PSMCx Rising Edge Event occurs on Time Base match</td>
<td>1</td>
<td>= Rising edge event will occur when PSMCxTMR = PSMCxPH</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>= Time base will not cause rising edge event</td>
</tr>
</tbody>
</table>

### Note 1:
Sources are not mutually exclusive: more than one source can cause a rising edge event.
<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PxDCSIN: PSMCx Falling Edge Event occurs on PSMCxIN pin</td>
<td>1 = Falling edge event will occur when PSMCxIN pin goes true, 0 = PSMCxIN pin will not cause falling edge event</td>
</tr>
<tr>
<td>6-5</td>
<td>Unimplemented: Read as '0'</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PxDCSC4: PSMCx Falling Edge Event occurs on sync_C4OUT output</td>
<td>1 = Falling edge event will occur when sync_C4OUT output goes true, 0 = sync_C4OUT will not cause falling edge event</td>
</tr>
<tr>
<td>3</td>
<td>PxDCSC3: PSMCx Falling Edge Event occurs on sync_C3OUT output</td>
<td>1 = Falling edge event will occur when sync_C3OUT output goes true, 0 = sync_C3OUT will not cause falling edge event</td>
</tr>
<tr>
<td>2</td>
<td>PxDCSC2: PSMCx Falling Edge Event occurs on sync_C2OUT output</td>
<td>1 = Falling edge event will occur when sync_C2OUT output goes true, 0 = sync_C2OUT will not cause falling edge event</td>
</tr>
<tr>
<td>1</td>
<td>PxDCSC1: PSMCx Falling Edge Event occurs on sync_C1OUT output</td>
<td>1 = Falling edge event will occur when sync_C1OUT output goes true, 0 = sync_C1OUT will not cause falling edge event</td>
</tr>
<tr>
<td>0</td>
<td>PxDCST: PSMCx Falling Edge Event occurs on Time Base match</td>
<td>1 = Falling edge event will occur when PSMCxTMR = PSMCxDC, 0 = Time base will not cause falling edge event</td>
</tr>
</tbody>
</table>

Note 1: Sources are not mutually exclusive: more than one source can cause a falling edge event.
## REGISTER 24-14: PSMCxPRS: PSMC PERIOD SOURCE REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PxPRSIN</td>
<td>—</td>
<td>—</td>
<td>PxPRSC4</td>
<td>PxPRSC3</td>
<td>PxPRSC2</td>
<td>PxPRSC1</td>
<td>PxPRST</td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

### bit 7
- **PxPRSIN**: PSMC<sub>x</sub> Period Event occurs on PSMC<sub>x</sub>IN pin
  - **1** = Period event will occur and PSMC<sub>x</sub>TMR will reset when PSMC<sub>x</sub>IN pin goes true
  - **0** = PSMC<sub>x</sub>IN pin will not cause period event

### bit 6-5
- **Unimplemented**: Read as '0'

### bit 4
- **PxPRSC4**: PSMC<sub>x</sub> Period Event occurs on sync<sub>C4</sub>OUT output
  - **1** = Period event will occur and PSMC<sub>x</sub>TMR will reset when sync<sub>C4</sub>OUT output goes true
  - **0** = sync<sub>C4</sub>OUT will not cause period event

### bit 3
- **PxPRSC3**: PSMC<sub>x</sub> Period Event occurs on sync<sub>C3</sub>OUT output
  - **1** = Period event will occur and PSMC<sub>x</sub>TMR will reset when sync<sub>C3</sub>OUT output goes true
  - **0** = sync<sub>C3</sub>OUT will not cause period event

### bit 2
- **PxPRSC2**: PSMC<sub>x</sub> Period Event occurs on sync<sub>C2</sub>OUT output
  - **1** = Period event will occur and PSMC<sub>x</sub>TMR will reset when sync<sub>C2</sub>OUT output goes true
  - **0** = sync<sub>C2</sub>OUT will not cause period event

### bit 1
- **PxPRSC1**: PSMC<sub>x</sub> Period Event occurs on sync<sub>C1</sub>OUT output
  - **1** = Period event will occur and PSMC<sub>x</sub>TMR will reset when sync<sub>C1</sub>OUT output goes true
  - **0** = sync<sub>C1</sub>OUT will not cause period event

### bit 0
- **PxPRST**: PSMC<sub>x</sub> Period Event occurs on Time Base match
  - **1** = Period event will occur and PSMC<sub>x</sub>TMR will reset when PSMC<sub>x</sub>TMR = PSMC<sub>x</sub>PR
  - **0** = Time base will not cause period event

### Note 1:
Sources are not mutually exclusive: more than one source can force the period event and reset the PSMC<sub>x</sub>TMR.
REGISTER 24-15: PSMCxASDC: PSMC AUTO-SHUTDOWN CONTROL REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PxASE: PWM Auto-Shutdown Event Status bit&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>A shutdown event has occurred, PWM outputs are inactive and in their shutdown states</td>
</tr>
<tr>
<td>0</td>
<td>PWM outputs are operating normally</td>
</tr>
<tr>
<td>PxASDEN: PWM Auto-Shutdown Enable bit</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Auto-shutdown is enabled. If any of the sources in PSMCxASDS assert a logic ‘1’, then the outputs will go into their auto-shutdown state and PSMCxSIF flag will be set.</td>
</tr>
<tr>
<td>0</td>
<td>Auto-shutdown is disabled</td>
</tr>
<tr>
<td>PxARSEN: PWM Auto-Restart Enable bit</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>PWM restarts automatically when the shutdown condition is removed.</td>
</tr>
<tr>
<td>0</td>
<td>The PxASE bit must be cleared in firmware to restart PWM after the auto-shutdown condition is cleared.</td>
</tr>
<tr>
<td>Unimplemented: Read as ‘0’</td>
<td></td>
</tr>
<tr>
<td>PxASDOV: PWM Auto-Shutdown Override bit</td>
<td></td>
</tr>
<tr>
<td>PxASDEN = 1:</td>
<td>Force PxASDL[n] levels on the PSMCx[n] pins without causing a PSMCxSIF interrupt</td>
</tr>
<tr>
<td>1</td>
<td>Normal PWM and auto-shutdown execution</td>
</tr>
<tr>
<td>0</td>
<td>No effect</td>
</tr>
</tbody>
</table>

Note 1: PASE bit may be set in software. When this occurs the functionality is the same as that caused by hardware.
## REGISTER 24-16: PSMCxASDL: PSMC AUTO-SHUTDOWN OUTPUT LEVEL REGISTER

<table>
<thead>
<tr>
<th></th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>—</td>
<td>—</td>
<td>PxASDLF(1)</td>
<td>PxASDLE(1)</td>
<td>PxASDLD(1)</td>
<td>PxASDLC(1)</td>
<td>PxASDLB</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘-n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

### bit 7-6

**Unimplemented:** Read as ‘0’

### bit 5

**PxASDLF:** PSMCx Output F Auto-Shutdown Pin Level bit(1)

- **1** = When auto-shutdown is asserted, pin PSMCxF will drive logic ‘1’
- **0** = When auto-shutdown is asserted, pin PSMCxF will drive logic ‘0’

### bit 4

**PxASDLE:** PSMCx Output E Auto-Shutdown Pin Level bit(1)

- **1** = When auto-shutdown is asserted, pin PSMCxE will drive logic ‘1’
- **0** = When auto-shutdown is asserted, pin PSMCxE will drive logic ‘0’

### bit 3

**PxASDLD:** PSMCx Output D Auto-Shutdown Pin Level bit(1)

- **1** = When auto-shutdown is asserted, pin PSMCxD will drive logic ‘1’
- **0** = When auto-shutdown is asserted, pin PSMCxD will drive logic ‘0’

### bit 2

**PxASDLC:** PSMCx Output C Auto-Shutdown Pin Level bit(1)

- **1** = When auto-shutdown is asserted, pin PSMCxC will drive logic ‘1’
- **0** = When auto-shutdown is asserted, pin PSMCxC will drive logic ‘0’

### bit 1

**PxASDLB:** PSMCx Output B Auto-Shutdown Pin Level bit

- **1** = When auto-shutdown is asserted, pin PSMCxB will drive logic ‘1’
- **0** = When auto-shutdown is asserted, pin PSMCxB will drive logic ‘0’

### bit 0

**PxASDLA:** PSMCx Output A Auto-Shutdown Pin Level bit

- **1** = When auto-shutdown is asserted, pin PSMCxA will drive logic ‘1’
- **0** = When auto-shutdown is asserted, pin PSMCxA will drive logic ‘0’

**Note 1:** These bits are not implemented on PSMC2.
# PIC16(L)F1784/6/7

## REGISTER 24-17: PSMCxASDS: PSMC AUTO-SHUTDOWN SOURCE REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PxASDSIN: Auto-shutdown occurs on PSMCxIN pin</td>
<td>1 = Auto-shutdown will occur when PSMCxIN pin goes true, 0 = PSMCxIN pin will not cause auto-shutdown</td>
</tr>
<tr>
<td>6-5</td>
<td>Unimplemented: Read as '0'</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>PxASDSC4: Auto-shutdown occurs on sync_C4OUT output</td>
<td>1 = Auto-shutdown will occur when sync_C4OUT output goes true, 0 = sync_C4OUT will not cause auto-shutdown</td>
</tr>
<tr>
<td>4</td>
<td>PxASDSC3: Auto-shutdown occurs on sync_C3OUT output</td>
<td>1 = Auto-shutdown will occur when sync_C3OUT output goes true, 0 = sync_C3OUT will not cause auto-shutdown</td>
</tr>
<tr>
<td>3</td>
<td>PxASDSC2: Auto-shutdown occurs on sync_C2OUT output</td>
<td>1 = Auto-shutdown will occur when sync_C2OUT output goes true, 0 = sync_C2OUT will not cause auto-shutdown</td>
</tr>
<tr>
<td>2</td>
<td>PxASDSC1: Auto-shutdown occurs on sync_C1OUT output</td>
<td>1 = Auto-shutdown will occur when sync_C1OUT output goes true, 0 = sync_C1OUT will not cause auto-shutdown</td>
</tr>
<tr>
<td>1</td>
<td>Unimplemented: Read as '0'</td>
<td></td>
</tr>
</tbody>
</table>

### Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets
### REGISTER 24-18: PSMCxTMRL: PSMC TIME BASE COUNTER LOW REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- '-n/n' = Value at POR and BOR/Value at all other Resets

- **'1'** = Bit is set
- **'0'** = Bit is cleared

**bit 7-0**

- **PSMCxTMRL<7:0>: 16-bit PSMCx Time Base Counter Least Significant bits**
  - **= PSMCxTMR<7:0>**

### REGISTER 24-19: PSMCxTMRH: PSMC TIME BASE COUNTER HIGH REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-1/1</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- '-n/n' = Value at POR and BOR/Value at all other Resets

- **'1'** = Bit is set
- **'0'** = Bit is cleared

**bit 7-0**

- **PSMCxTMRH<7:0>: 16-bit PSMCx Time Base Counter Most Significant bits**
  - **= PSMCxTMR<15:8>**
**REGISTER 24-20: PSMCxPHL: PSMC PHASE COUNT LOW BYTE REGISTER**

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

\[
\text{bit 7-0} \quad \text{PSMCxPHL}<7:0>: \quad \text{16-bit Phase Count Least Significant bits}
\]
\[
\quad = \quad \text{PSMCxPH}<7:0>
\]

**REGISTER 24-21: PSMCxPHH: PSMC PHASE COUNT HIGH BYTE REGISTER**

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

\[
\text{bit 7-0} \quad \text{PSMCxPHH}<7:0>: \quad \text{16-bit Phase Count Most Significant bits}
\]
\[
\quad = \quad \text{PSMCxPH}<15:8>
\]
REGISTER 24-22: PSMCxDCL: PSMC DUTY CYCLE COUNT LOW BYTE REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSMCxDCL&lt;7:0&gt;</td>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

bit 7-0  
PSMCxDCL<7:0>: 16-bit Duty Cycle Count Least Significant bits  
= PSMCxDC<7:0>

REGISTER 24-23: PSMCxDCH: PSMC DUTY CYCLE COUNT HIGH REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSMCxDCH&lt;7:0&gt;</td>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

bit 7-0  
PSMCxDCH<7:0>: 16-bit Duty Cycle Count Most Significant bits  
= PSMCxDC<15:8>
**REGISTER 24-24: PSMCxPRL: PSMC PERIOD COUNT LOW BYTE REGISTER**

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>PSMCxPRL&lt;7:0&gt;</td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7-0**  
**PSMCxPRL<7:0>:** 16-bit Period Time Least Significant bits  
= **PSMCxPR<7:0>**

**REGISTER 24-25: PSMCxPRH: PSMC PERIOD COUNT HIGH BYTE REGISTER**

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
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<tbody>
<tr>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSMCxPRH&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7-0**  
**PSMCxPRH<7:0>:** 16-bit Period Time Most Significant bits  
= **PSMCxPR<15:8>**
REGISTER 24-26: PSMCxDBR: PSMC RISING EDGE DEAD-BAND TIME REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **’1’** = Bit is set
- **’0’** = Bit is cleared

bit 7-0  
**PSMCxDBR<7:0>:** Rising Edge Dead-Band Time bits
- Unsigned number of PSMCx psmc_clk clock periods in rising edge dead band

REGISTER 24-27: PSMCxDBF: PSMC FALLING EDGE DEAD-BAND TIME REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **’1’** = Bit is set
- **’0’** = Bit is cleared

bit 7-0  
**PSMCxDBF<7:0>:** Falling Edge Dead-Band Time bits
- Unsigned number of PSMCx psmc_clk clock periods in falling edge dead band

REGISTER 24-28: PSMCxFFA: PSMC FRACTIONAL FREQUENCY ADJUST REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PSMCxFFA&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **’1’** = Bit is set
- **’0’** = Bit is cleared

bit 7-4  
**Unimplemented:** Read as ‘0’

bit 3-0  
**PSMCxFFA<3:0>:** Fractional Frequency Adjustment bits
- Unsigned number of fractional PSMCx psmc_clk clock periods to add to each period event time.
  - The fractional time period = 1/(16*psmc_clk)

...
### REGISTER 24-29: PSMCxBLKR: PSMC RISING EDGE BLANKING TIME REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSMCxBLKR&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

**bit 7-0 PSMCxBLKR<7:0>:** Rising Edge Blanking Time bits

= Unsigned number of PSMCx psmc_clk clock periods in rising edge blanking

### REGISTER 24-30: PSMCxBLKF: PSMC FALLING EDGE BLANKING TIME REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSMCxBLKF&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

**bit 7-0 PSMCxBLKF<7:0>:** Falling Edge Blanking Time bits

= Unsigned number of PSMCx psmc_clk clock periods in falling edge blanking
**REGISTER 24-31: PSMCxSTR0: PSMC STEERING CONTROL REGISTER 0**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>PxSTRF(2)</td>
<td>PxSTRE(2)</td>
<td>PxSTRD(2)</td>
<td>PxSTRC(2)</td>
<td>PxSTRB</td>
<td>PxSTRA</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- U = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

**bit 7-6**
Unimplemented: Read as '0'

**bit 5**
**PxSTRF**: PWM Steering PSMCxF Output Enable bit(2)

If `PxMODE<3:0> = 0000` (Single-phase PWM):
1 = Single PWM output is active on pin PSMCxF
0 = Single PWM output is not active on pin PSMCxF. PWM drive is in inactive state

If `PxMODE<3:0> = 0001` (Complementary Single-phase PWM):
1 = Complementary PWM output is active on pin PSMCxF
0 = Complementary PWM output is not active on pin PSMCxF. PWM drive is in inactive state

If `PxMODE<3:0> = 1100` (3-phase Steering):
1 = `PxSTRF` and `PxSTRE` are high. PSMCxA, PSMCxB, PSMCxC and PSMCxD are low.
0 = 3-phase output combination is not active

**bit 4**
**PxSTRE**: PWM Steering PSMCxE Output Enable bit(2)

If `PxMODE<3:0> = 000x` (Single-phase PWM or Complementary PWM):
1 = Single PWM output is active on pin PSMCxE
0 = Single PWM output is not active on pin PSMCxE. PWM drive is in inactive state

If `PxMODE<3:0> = 1100` (3-phase Steering):
1 = PSMCxA and PSMCxD are high. PSMCxE, PSMCxC and PSMCxB are low.
0 = 3-phase output combination is not active

**bit 3**
**PxSTRD**: PWM Steering PSMCxD Output Enable bit(2)

If `PxMODE<3:0> = 0000` (Single-phase PWM):
1 = Single PWM output is active on pin PSMCxD
0 = Single PWM output is not active on pin PSMCxD. PWM drive is in inactive state

If `PxMODE<3:0> = 0001` (Complementary Single-phase PWM):
1 = Complementary PWM output is active on pin PSMCxD
0 = Complementary PWM output is not active on pin PSMCxD. PWM drive is in inactive state

If `PxMODE<3:0> = 1100` (3-phase Steering):
1 = PSMCxB and PSMCxC are high. PSMCxA, PSMCxD, PSMCxE and PSMCxF are low.
0 = 3-phase output combination is not active

**bit 2**
**PxSTRC**: PWM Steering PSMCxC Output Enable bit(2)

If `PxMODE<3:0> = 000x` (Single-phase PWM or Complementary PWM):
1 = Single PWM output is active on pin PSMCxC
0 = Single PWM output is not active on pin PSMCxC. PWM drive is in inactive state

If `PxMODE<3:0> = 1100` (3-phase Steering):
1 = PSMCxA and PSMCxF are high. PSMCxB, PSMCxD and PSMCxE are low.
0 = 3-phase output combination is not active
REGISTER 24-31: PSMCxSTR0: PSMC STEERING CONTROL REGISTER 0

bit 1  \textbf{PxSTRB}: PWM Steering PSMCxB Output Enable bit
\begin{itemize}
  \item If \textbf{PxMODE<3:0>} = \textit{0000} (Single-phase PWM):  
    \begin{itemize}
      \item 1 = Single PWM output is active on pin PSMCxOUT1
      \item 0 = Single PWM output is not active on pin PSMCxOUT1. PWM drive is in inactive state
    \end{itemize}
  \item If \textbf{PxMODE<3:0>} = \textit{0001} (Complementary Single-phase PWM):  
    \begin{itemize}
      \item 1 = Complementary PWM output is active on pin PSMCxB
      \item 0 = Complementary PWM output is not active on pin PSMCxB. PWM drive is in inactive state
    \end{itemize}
  \item If \textbf{PxMODE<3:0>} = \textit{1100} (3-phase Steering):\footnote{1}  
    \begin{itemize}
      \item 1 = PSMCxA and PSMCxB are high. PSMCxC, PSMCxD and PSMCxE are low.
      \item 0 = 3-phase output combination is not active
    \end{itemize}
\end{itemize}

bit 0  \textbf{PxSTRA}: PWM Steering PSMCxA Output Enable bit
\begin{itemize}
  \item If \textbf{PxMODE<3:0>} = \textit{000x} (Single-phase PWM or Complementary PWM):  
    \begin{itemize}
      \item 1 = Single PWM output is active on pin PSMCxA
      \item 0 = Single PWM output is not active on pin PSMCxA. PWM drive is in inactive state
    \end{itemize}
  \item If \textbf{PxMODE<3:0>} = \textit{1100} (3-phase Steering):\footnote{1}  
    \begin{itemize}
      \item 1 = PSMCxA and PSMCxD are high. PSMCxB, PSMCxC and PSMCxF are low.
      \item 0 = 3-phase output combination is not active
    \end{itemize}
\end{itemize}

\textbf{Note 1:} In 3-phase Steering mode, only one PSTRx bit should be set at a time. If more than one is set, then the lowest bit number steering combination has precedence.

\textbf{2:} These bits are not implemented on PSMC2.
REGISTER 24-32: PSMCxSTR1: PSMC STEERING CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
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<tr>
<td>PxSSYNC</td>
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<td>—</td>
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<td>PxLSMEN</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PxBHSMEN</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **'1'** = Bit is set
- **'0'** = Bit is cleared

**bit 7**  
**PxSSYNC**: PWM Steering Synchronization bit  
1 = PWM outputs are updated on period boundary  
0 = PWM outputs are updated immediately

**bit 6-2**  
**Unimplemented**: Read as '0'

**bit 1**  
**PxLSMEN**: 3-Phase Steering Low Side Modulation Enable bit  
**PxMODE = 1100**:
1 = Low side driver PSMCxB, PSMCxD and PSMCxF outputs are modulated according to PSMCxDL when the output is high and driven low without modulation when the output is low.  
0 = PSMCxB, PSMCxD, and PSMCxF outputs are driven high and low by PSMCxSTR0 control without modulation.
**PxMODE <> 1100**:  
No effect on output

**bit 0**  
**PxHSMEN**: 3-Phase Steering High Side Modulation Enable bit  
**PxMODE = 1100**:
1 = High side driver PSMCxA, PSMCxC and PSMCxE outputs are modulated according to PSMCxDL when the output is high and driven low without modulation when the output is low.  
0 = PSMCxA, PSMCxC and PSMCxE outputs are driven high and low by PSMCxSTR0 control without modulation.
**PxMODE <> 1100**:  
No effect on output
### REGISTER 24-33: PSMCxINT: PSMC TIME BASE INTERRUPT CONTROL REGISTER

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<thead>
<tr>
<th></th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
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<tbody>
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<tr>
<td>PxTPHIF</td>
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</tr>
<tr>
<td>PxTDCIF</td>
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<td></td>
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<tr>
<td>PxTPRIF</td>
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<td></td>
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<td></td>
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<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared

**bit 7**
- **PxTOVIE**: PSMC Time Base Counter Overflow Interrupt Enable bit
  - 1 = Time base counter overflow interrupts are enabled
  - 0 = Time base counter overflow interrupts are disabled

**bit 6**
- **PxTPHIE**: PSMC Time Base Phase Interrupt Enable bit
  - 1 = Time base phase match interrupts are enabled
  - 0 = Time base phase match interrupts are disabled

**bit 5**
- **PxTDCIE**: PSMC Time Base Duty Cycle Interrupt Enable bit
  - 1 = Time base duty cycle match interrupts are enabled
  - 0 = Time base duty cycle match interrupts are disabled

**bit 4**
- **PxTPRIE**: PSMC Time Base Period Interrupt Enable bit
  - 1 = Time base period match interrupts are enabled
  - 0 = Time base period match interrupts are disabled

**bit 3**
- **PxTOVIF**: PSMC Time Base Counter Overflow Interrupt Flag bit
  - 1 = The 16-bit PSMCxTMR has overflowed from FFFFh to 0000h
  - 0 = The 16-bit PSMCxTMR counter has not overflowed

**bit 2**
- **PxTPHIF**: PSMC Time Base Phase Interrupt Flag bit
  - 1 = The 16-bit PSMCxTMR counter has matched PSMCxPH<15:0>
  - 0 = The 16-bit PSMCxTMR counter has not matched PSMCxPH<15:0>

**bit 1**
- **PxTDCIF**: PSMC Time Base Duty Cycle Interrupt Flag bit
  - 1 = The 16-bit PSMCxTMR counter has matched PSMCxDC<15:0>
  - 0 = The 16-bit PSMCxTMR counter has not matched PSMCxDC<15:0>

**bit 0**
- **PxTPRIF**: PSMC Time Base Period Interrupt Flag bit
  - 1 = The 16-bit PSMCxTMR counter has matched PSMCxPR<15:0>
  - 0 = The 16-bit PSMCxTMR counter has not matched PSMCxPR<15:0>
## TABLE 24-5: SUMMARY OF REGISTERS ASSOCIATED WITH PSMC

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit7</th>
<th>Bit6</th>
<th>Bit5</th>
<th>Bit4</th>
<th>Bit3</th>
<th>Bit2</th>
<th>Bit1</th>
<th>Bit0</th>
<th>Register on Page</th>
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<td>PEIE</td>
<td>TMROI</td>
<td>INTE</td>
<td>IOCIE</td>
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<td>INT</td>
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<td>ODC7</td>
<td>ODC6</td>
<td>ODC5</td>
<td>ODC4</td>
<td>ODC3</td>
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<td>TRISC2</td>
<td>TRISC1</td>
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<td>142</td>
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</table>

**Legend:** — = unimplemented location, read as ‘0’. Shaded cells are not used by PSMC module.

**Note 1:** Unimplemented in PSMC2.
25.0 CAPTURE/COMPARE/PWM MODULES

The Capture/Compare/PWM module is a peripheral that allows the user to time and control different events, and to generate Pulse-Width Modulation (PWM) signals. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate Pulse-Width Modulated signals of varying frequency and duty cycle.

This family of devices contains two standard Capture/Compare/PWM modules (CCP1, CCP2 and CCP3).

The Capture and Compare functions are identical for all CCP modules.

**Note 1:** In devices with more than one CCP module, it is very important to pay close attention to the register names used. A number placed after the module acronym is used to distinguish between separate modules. For example, the CCP1CON and CCP2CON control the same operational aspects of two completely different CCP modules.

**2:** Throughout this section, generic references to a CCP module in any of its operating modes may be interpreted as being equally applicable to CCPx module. Register names, module signals, I/O pins, and bit names may use the generic designator ‘x’ to indicate the use of a numeral to distinguish a particular module, when required.
25.1 Capture Mode

The Capture mode function described in this section is available and identical for all CCP modules.

Capture mode makes use of the 16-bit Timer1 resource. When an event occurs on the CCPx pin, the 16-bit CCPRxH:CCPRxL register pair captures and stores the 16-bit value of the TMR1H:TMR1L register pair, respectively. An event is defined as one of the following and is configured by the CCPxM<3:0> bits of the CCPxCON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIRx register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH, CCPRxL register pair is read, the old captured value is overwritten by the new captured value.

Figure 25-1 shows a simplified diagram of the capture operation.

25.1.1 CCP PIN CONFIGURATION

In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit. Also, the CCP2 pin function can be moved to alternative pins using the APFCON register. Refer to Section 13.1 “Alternate Pin Function” for more details.

**Note:** If the CCPx pin is configured as an output, a write to the port can cause a capture condition.

Figure 25-1: Capture Mode Operation Block Diagram

25.1.2 TIMER1 MODE RESOURCE

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

See Section 22.0 “Timer1 Module with Gate Control” for more information on configuring Timer1.

25.1.3 SOFTWARE INTERRUPT MODE

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE interrupt enable bit of the PIEX register clear to avoid false interrupts. Additionally, the user should clear the CCPxIF interrupt flag bit of the PIRx register following any change in Operating mode.

**Note:** Clocking Timer1 from the system clock (Fosc) should not be used in Capture mode. In order for Capture mode to recognize the trigger event on the CCPx pin, Timer1 must be clocked from the instruction clock (Fosc/4) or from an external clock source.

25.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCPxM<3:0> bits of the CCPxCON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCPxCON register before changing the prescaler. Equation 25-1 demonstrates the code to perform this function.

**EXAMPLE 25-1: CHANGING BETWEEN CAPTURE PRESCALERS**

BANKSEL CCPxCON ;Set Bank bits to point to CCPxCON
CLRF CCPxCON ;Turn CCP module off
MOVLW NEW_CAPT_PS ;Load the W reg with the new prescaler
MOVF CCPxCON ;Load CCPxCON with this value

**Note:** The CCP module must be off before changing the prescaler.
25.1.5 CAPTURE DURING SLEEP

Capture mode depends upon the Timer1 module for proper operation. There are two options for driving the Timer1 module in Capture mode. It can be driven by the instruction clock (Fosc/4), or by an external clock source.

When Timer1 is clocked by Fosc/4, Timer1 will not increment during Sleep. When the device wakes from Sleep, Timer1 will continue from its previous state.

Capture mode will operate during Sleep when Timer1 is clocked by an external clock source.

25.1.6 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see Section 13.1 “Alternate Pin Function” for more information.
25.2 Compare Mode

The Compare mode function described in this section is available and identical for all CCP modules.

Compare mode makes use of the 16-bit Timer1 resource. The 16-bit value of the CCPRxH:CCPRxL register pair is constantly compared against the 16-bit value of the TMR1H:TMR1L register pair. When a match occurs, one of the following events can occur:

- Toggle the CCPx output
- Set the CCPx output
- Clear the CCPx output
- Generate an Auto-conversion Trigger
- Generate a Software Interrupt

The action on the pin is based on the value of the CCPxM<3:0> control bits of the CCPxCON register. At the same time, the interrupt flag CCPxIF bit is set.

All Compare modes can generate an interrupt.

Figure 25-2 shows a simplified diagram of the compare operation.

**FIGURE 25-2: COMPARE MODE OPERATION BLOCK DIAGRAM**

![Diagram](image)

25.2.1 CCPX PIN CONFIGURATION

The user must configure the CCPx pin as an output by clearing the associated TRIS bit.

The CCP2 pin function can be moved to alternate pins using the APFCON register (Register 13-1). Refer to Section 13.1 “Alternate Pin Function” for more details.

**Note:** Clearing the CCPxCON register will force the CCPx compare output latch to the default low level. This is not the PORT I/O data latch.

25.2.2 TIMER1 MODE RESOURCE

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

Note: Clocking Timer1 from the system clock (Fosc) should not be used in Compare mode. In order for Compare mode to recognize the trigger event on the CCPx pin, Timer1 must be clocked from the instruction clock (Fosc/4) or from an external clock source.

25.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen (CCPxM<3:0> = 1010), the CCPx module does not assert control of the CCPx pin (see the CCPxCON register).

25.2.4 AUTO-CONVERSION TRIGGER

When Auto-conversion Trigger mode is chosen (CCPxM<3:0> = 1011), the CCPx module does the following:

- Resets Timer1
- Starts an ADC conversion if ADC is enabled

The CCPx module does not assert control of the CCPx pin in this mode.

The Auto-conversion Trigger output of the CCP occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPRxH, CCPRxL register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. The Auto-conversion Trigger output starts an ADC conversion (if the ADC module is enabled). This allows the CCPRxH, CCPRxL register pair to effectively provide a 16-bit programmable period register for Timer1.

Refer to Section 17.2.5 “Auto-Conversion Trigger” for more information.

**Note 1:** The Auto-conversion Trigger from the CCP module does not set interrupt flag bit TMR1IF of the PIR1 register.

2: Removing the match condition by changing the contents of the CCPRxH and CCPRxL register pair, between the clock edge that generates the Auto-conversion Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.

25.2.5 COMPARE DURING SLEEP

The Compare mode is dependent upon the system clock (Fosc) for proper operation. Since Fosc is shut down during Sleep mode, the Compare mode will not function properly during Sleep.
25.2.6 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see Section 13.1 “Alternate Pin Function” for more information.
25.3 PWM Overview

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the on state and the low portion of the signal is considered the off state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and in turn the power that is applied to the load.

The term duty cycle describes the proportion of the on time to the off time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

Figure 25-3 shows a typical waveform of the PWM signal.

25.3.1 STANDARD PWM OPERATION

The standard PWM function described in this section is available and identical for all CCP modules.

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCPx pin with up to 10 bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- PR2 registers
- T2CON registers
- CCPRxL registers
- CCPxCON registers

Figure 25-4 shows a simplified block diagram of PWM operation.

---

**Note 1:** The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin.

**2:** Clearing the CCPxCON register will relinquish control of the CCPx pin.
25.3.2 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for standard PWM operation:

1. Disable the CCPx pin output driver by setting the associated TRIS bit.
2. Load the PR2 register with the PWM period value.
3. Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
4. Load the CCPRxL register and the DCxBx bits of the CCPxCON register, with the PWM duty cycle value.
5. Configure and start Timer2:
   - Clear the TMR2IF interrupt flag bit of the PIRx register. See Note below.
   - Configure the T2CKPS bits of the T2CON register with the Timer prescale value.
   - Enable the Timer by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output pin:
   - Wait until the Timer overflows and the TMR2IF bit of the PIR1 register is set. See Note below.
   - Enable the CCPx pin output driver by clearing the associated TRIS bit.

Note: In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

25.3.3 TIMER2 TIMER RESOURCE

The PWM standard mode makes use of the 8-bit Timer2 timer resources to specify the PWM period.

25.3.4 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 25-1.

**EQUATION 25-1: PWM PERIOD**

\[
\text{PWM Period} = \frac{(PR2 + 1) \cdot 4 \cdot \text{Tosc}}{(\text{TMR2 Prescale Value})}
\]

**Note 1:** \(\text{Tosc} = 1/\text{Fosc}\)

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPRxL into CCPRxH.

Note: The Timer postscaler (see Section 23.1 “Timer2 Operation”) is not used in the determination of the PWM frequency.

25.3.5 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPRxL register and DCxB<1:0> bits of the CCPxCON register. The CCPRxL contains the eight MSbs and the DCxB<1:0> bits of the CCPxCON register contain the two LSbs. CCPRxL and DCxB<1:0> bits of the CCPxCON register can be written to at any time. The duty cycle value is not latched into CCPRxH until after the period completes (i.e., a match between PR2 and TMR2 registers occurs). While using the PWM, the CCPRxH register is read-only.

Equation 25-2 is used to calculate the PWM pulse width.

Equation 25-3 is used to calculate the PWM duty cycle ratio.

**EQUATION 25-2: PULSE WIDTH**

\[
\text{Pulse Width} = (\text{CCPRxL}.\text{CCPxCON<5:4>}) \cdot \frac{\text{Tosc} \cdot (\text{TMR2 Prescale Value})}{4(PR2 + 1)}
\]

**EQUATION 25-3: DUTY CYCLE RATIO**

\[
\text{Duty Cycle Ratio} = \frac{(\text{CCPRxL}.\text{CCPxCON<5:4>})}{4(PR2 + 1)}
\]

The CCPRxH register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.
The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (FOSC), or 2 bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH and 2-bit latch, then the CCPx pin is cleared (see Figure 25-4).

25.3.6 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 25-4.

\[
Resolution = \frac{\log[4(PR2 + 1)]}{\log(2)} \text{ bits}
\]

Note: If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

### Table 25-1: Example PWM Frequencies and Resolutions (Fosc = 20 MHz)

<table>
<thead>
<tr>
<th>PWM Frequency</th>
<th>1.22 kHz</th>
<th>4.88 kHz</th>
<th>19.53 kHz</th>
<th>78.12 kHz</th>
<th>156.3 kHz</th>
<th>208.3 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer Prescale</td>
<td>16</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>PR2 Value</td>
<td>0xFF</td>
<td>0xFF</td>
<td>0xFF</td>
<td>0x3F</td>
<td>0x1F</td>
<td>0x17</td>
</tr>
<tr>
<td>Maximum Resolution (bits)</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>8</td>
<td>7</td>
<td>6.6</td>
</tr>
</tbody>
</table>

### Table 25-2: Example PWM Frequencies and Resolutions (Fosc = 8 MHz)

<table>
<thead>
<tr>
<th>PWM Frequency</th>
<th>1.22 kHz</th>
<th>4.90 kHz</th>
<th>19.61 kHz</th>
<th>76.92 kHz</th>
<th>153.85 kHz</th>
<th>200.0 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer Prescale</td>
<td>16</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>PR2 Value</td>
<td>0x65</td>
<td>0x65</td>
<td>0x65</td>
<td>0x19</td>
<td>0x0C</td>
<td>0x09</td>
</tr>
<tr>
<td>Maximum Resolution (bits)</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>6</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>
25.3.7 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

25.3.8 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See Section 6.0 “Oscillator Module (with Fail-Safe Clock Monitor)” for additional details.

25.3.9 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

### TABLE 25-3: SUMMARY OF REGISTERS ASSOCIATED WITH STANDARD PWM

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>APFCON1</td>
<td>C2OUTSEL</td>
<td>CC1PSEL</td>
<td>SDOSEL</td>
<td>SCKSEL</td>
<td>SDSEL</td>
<td>TXSEL</td>
<td>RXSEL</td>
<td>CCP2SEL</td>
<td>127</td>
</tr>
<tr>
<td>APFCON2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CCP3SEL</td>
</tr>
<tr>
<td>CCP1CON</td>
<td></td>
<td></td>
<td></td>
<td>DC1B&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>CCP1M&lt;3:0&gt;</td>
<td>280</td>
</tr>
<tr>
<td>CCP2CON</td>
<td></td>
<td></td>
<td></td>
<td>DC2B&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>CCP2M&lt;3:0&gt;</td>
<td>280</td>
</tr>
<tr>
<td>CCP3CON</td>
<td></td>
<td></td>
<td></td>
<td>DC3B&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>CCP3M&lt;3:0&gt;</td>
<td>280</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMROIE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>93</td>
</tr>
<tr>
<td>PIE1</td>
<td>TMR1GIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSP1IE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>93</td>
</tr>
<tr>
<td>PIE2</td>
<td>OSFIE</td>
<td>C2IE</td>
<td>C1IE</td>
<td>EEIE</td>
<td>BCL1IE</td>
<td>C4IE</td>
<td>C3IE</td>
<td>CCP2IE</td>
<td>95</td>
</tr>
<tr>
<td>PIE3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CCP3IE</td>
<td></td>
<td></td>
<td>96</td>
</tr>
<tr>
<td>PIR1</td>
<td>TMR1GIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1IF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>98</td>
</tr>
<tr>
<td>PIR2</td>
<td>OSFIF</td>
<td>C2IF</td>
<td>C1IF</td>
<td>EEIF</td>
<td>BCL1IF</td>
<td>C4IF</td>
<td>C3IF</td>
<td>CCP2IF</td>
<td>99</td>
</tr>
<tr>
<td>PIR3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CCP3IF</td>
<td></td>
<td></td>
<td>100</td>
</tr>
<tr>
<td>PR2</td>
<td>Timer2 Period Register</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>210*</td>
</tr>
<tr>
<td>T2CON</td>
<td></td>
<td></td>
<td>T2OUTPS&lt;3:0&gt;</td>
<td>TMRO2N</td>
<td>T2CKPS&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>212</td>
</tr>
<tr>
<td>TMR2</td>
<td>Timer2 Module Register</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>210</td>
</tr>
<tr>
<td>TRISA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td>131</td>
</tr>
</tbody>
</table>

Legend: — Unimplemented location, read as ‘0’. Shaded cells are not used by the PWM.

* Page provides register information.
25.4 Register Definitions: CCP Control

REGISTER 25-1: CCPxCON: CCPx CONTROL REGISTER

<table>
<thead>
<tr>
<th>bit 7-6</th>
<th>bit 5-4</th>
<th>bit 3-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
<td>R/W-0/0</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>DCxB&lt;1:0&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CCPxM&lt;3:0&gt;</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- ‘-n/n’ = Value at POR and BOR/Value at all other Reset
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7-6**: Unimplemented: Read as ‘0’

**bit 5-4**: DCxB<1:0>: PWM Duty Cycle Least Significant bits
- **Capture mode**: Unused
- **Compare mode**: Unused
- **PWM mode**: These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPRxL.

**bit 3-0**: CCPxM<3:0>: CCPx Mode Select bits
- 11xx = PWM mode
  - 1011 = Compare mode: Auto-conversion Trigger (sets CCPxIF bit (CCP2), starts ADC conversion if ADC module is enabled)\(^1\)
  - 1010 = Compare mode: generate software interrupt only
  - 1001 = Compare mode: clear output on compare match (set CCPxIF)
  - 1000 = Compare mode: set output on compare match (set CCPxIF)
  - 0111 = Capture mode: every 16th rising edge
  - 0110 = Capture mode: every 4th rising edge
  - 0101 = Capture mode: every rising edge
  - 0100 = Capture mode: every falling edge
- 0011 = Reserved
- 0010 = Compare mode: toggle output on match
- 0001 = Reserved
- 0000 = Capture/Compare/PWM off (resets CCPx module)
26.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

26.1 Master SSP (MSSP) Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module can operate in one of two modes:
• Serial Peripheral Interface (SPI)
• Inter-Integrated Circuit (I²C™)

The SPI interface supports the following modes and features:
• Master mode
• Slave mode
• Clock Parity
• Slave Select Synchronization (Slave mode only)
• Daisy-chain connection of slave devices

Figure 26-1 is a block diagram of the SPI interface module.

FIGURE 26-1: MSSP BLOCK DIAGRAM (SPI MODE)
The I²C interface supports the following modes and features:

- Master mode
- Slave mode
- Byte NACKing (Slave mode)
- Limited multi-master support
- 7-bit and 10-bit addressing
- Start and Stop interrupts
- Interrupt masking
- Clock stretching
- Bus collision detection
- General call address matching
- Address masking
- Address Hold and Data Hold modes
- Selectable SDA hold times

Figure 26-2 is a block diagram of the I²C interface module in Master mode. Figure 26-3 is a diagram of the I²C interface module in Slave mode.

**FIGURE 26-2: MSSP BLOCK DIAGRAM (I²C™ MASTER MODE)**
FIGURE 26-3: MSSP BLOCK DIAGRAM (I²C™ SLAVE MODE)
26.2 SPI Mode Overview

The Serial Peripheral Interface (SPI) bus is a synchronous serial data communication bus that operates in Full-Duplex mode. Devices communicate in a master/slave environment where the master device initiates the communication. A slave device is controlled through a Chip Select known as Slave Select.

The SPI bus specifies four signal connections:
- Serial Clock (SCK)
- Serial Data Out (SDO)
- Serial Data In (SDI)
- Slave Select (SS)

Figure 26-1 shows the block diagram of the MSSP module when operating in SPI mode.

The SPI bus operates with a single master device and one or more slave devices. When multiple slave devices are used, an independent Slave Select connection is required from the master device to each slave device.

Figure 26-4 shows a typical connection between a master device and multiple slave devices.

The master selects only one slave at a time. Most slave devices have tri-state outputs so their output signal appears disconnected from the bus when they are not selected.

Transmissions involve two shift registers, 8 bits in size, one in the master and one in the slave. With either the master or the slave device, data is always shifted out one bit at a time, with the Most Significant bit (MSb) shifted out first. At the same time, a new Least Significant bit (LSb) is shifted into the same register.

Figure 26-5 shows a typical connection between two processors configured as master and slave devices.

Data is shifted out of both shift registers on the programmed clock edge and latched on the opposite edge of the clock.

The master device transmits information out on its SDO output pin which is connected to, and received by, the slave’s SDI input pin. The slave device transmits information out on its SDO output pin, which is connected to, and received by, the master’s SDI input pin.

To begin communication, the master device first sends out the clock signal. Both the master and the slave devices should be configured for the same clock polarity.

The master device starts a transmission by sending out the MSb from its shift register. The slave device reads this bit from that same line and saves it into the LSb position of its shift register.

During each SPI clock cycle, a full-duplex data transmission occurs. This means that while the master device is sending out the MSb from its shift register (on its SDO pin) and the slave device is reading this bit and saving it as the LSb of its shift register, that the slave device is also sending out the MSb from its shift register (on its SDO pin) and the master device is reading this bit and saving it as the LSb of its shift register.

After 8 bits have been shifted out, the master and slave have exchanged register values.

If there is more data to exchange, the shift registers are loaded with new data and the process repeats itself.

Whether the data is meaningful or not (dummy data), depends on the application software. This leads to three scenarios for data transmission:
- Master sends useful data and slave sends dummy data.
- Master sends useful data and slave sends useful data.
- Master sends dummy data and slave sends useful data.

Transmissions may involve any number of clock cycles. When there is no more data to be transmitted, the master stops sending the clock signal and it deselects the slave.

Every slave device connected to the bus that has not been selected through its slave select line must disregard the clock and transmission signals and must not transmit out any data of its own.
26.2.1 SPI MODE REGISTERS

The MSSP module has five registers for SPI mode operation. These are:

- MSSP STATUS register (SSPSTAT)
- MSSP Control register 1 (SSPCON1)
- MSSP Control register 3 (SSPCON3)
- MSSP Data Buffer register (SSPBUF)
- MSSP Address register (SSPADD)
- MSSP Shift register (SSPSR)
  (Not directly accessible)

SSPCON1 and SSPSTAT are the control and STATUS registers in SPI mode operation. The SSPCON1 register is readable and writable. The lower 6 bits of the SSPSTAT are read-only. The upper 2 bits of the SSPSTAT are read/write.

In one SPI master mode, SSPADD can be loaded with a value used in the Baud Rate Generator. More information on the Baud Rate Generator is available in Section 26.7 “Baud Rate Generator”.

SSPSR is the shift register used for shifting data in and out. SSPBUF provides indirect access to the SSPSR register. SSPBUF is the buffer register to which data bytes are written, and from which data bytes are read.

In receive operations, SSPSR and SSPBUF together create a buffered receiver. When SSPSR receives a complete byte, it is transferred to SSPBUF and the SSP1IF interrupt is set.

During transmission, the SSPBUF is not buffered. A write to SSPBUF will write to both SSPBUF and SSPSR.
26.2.2 SPI MODE OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSPCON<5:0> and SSPSTAT<7:6>). These control bits allow the following to be specified:

- Master mode (SCK is the clock output)
- Slave mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Data Input Sample Phase (middle or end of data output time)
- Clock Edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- Slave Select mode (Slave mode only)

To enable the serial port, SSP Enable bit, SSPEN of the SSPCON1 register, must be set. To reset or reconfigure SPI mode, clear the SSPEN bit, re-initialize the SSPCONx registers and then set the SSPEN bit. This configures the SDI, SDO, SCK and SS pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed as follows:

- SDI must have corresponding TRIS bit set
- SDO must have corresponding TRIS bit cleared
- SCK (Master mode) must have corresponding TRIS bit cleared
- SCK (Slave mode) must have corresponding TRIS bit set
- SS must have corresponding TRIS bit set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value.

The MSSP consists of a transmit/receive shift register (SSPSR) and a buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR until the received data is ready. Once the 8 bits of data have been received, that byte is moved to the SSPBUF register. Then, the Buffer Full Detect bit, BF of the SSPSTAT register, and the interrupt flag bit, SSP1IF, are set. This double-buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPBUF register during transmission/reception of data will be ignored and the write collision detect bit WCOL of the SSPCON1 register, will be set. User software must clear the WCOL bit to allow the following write(s) to the SSPBUF register to complete successfully.

When the application software is expecting to receive valid data, the SSPBUF should be read before the next byte of data to transfer is written to the SSPBUF. The Buffer Full bit, BF of the SSPSTAT register, indicates when SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally, the MSSP interrupt is used to determine when the transmission/reception has completed. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur.

The SSPSR is not directly readable or writable and can

FIGURE 26-5: SPI MASTER/SLAVE CONNECTION
26.2.3 SPI MASTER MODE

The master can initiate the data transfer at any time because it controls the SCK line. The master determines when the slave (Processor 2, Figure 26-5) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SDO output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and Status bits appropriately set).

The clock polarity is selected by appropriately programming the CKP bit of the SSPCON1 register and the CKE bit of the SSPSTAT register. This then, would give waveforms for SPI communication as shown in Figure 26-6, Figure 26-8 and Figure 26-9, where the MSB is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- Fosc/4 (or TCY)
- Fosc/16 (or 4 * TCY)
- Fosc/64 (or 16 * TCY)
- Timer2 output/2
- Fosc/(4 * (SSPADD + 1))

Figure 26-6 shows the waveforms for Master mode.

When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPBUF is loaded with the received data is shown.

**FIGURE 26-6: SPI MODE WAVEFORM (MASTER MODE)**
26.2.4 SPI SLAVE MODE

In Slave mode, the data is transmitted and received as external clock pulses appear on SCK. When the last bit is latched, the SSP1IF interrupt flag bit is set.

Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCK pin. The Idle state is determined by the CKP bit of the SSPCON1 register.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. The shift register is clocked from the SCK pin input and when a byte is received, the device will generate an interrupt. If enabled, the device will wake-up from Sleep.

26.2.4.1 Daisy-Chain Configuration

The SPI bus can sometimes be connected in a daisy-chain configuration. The first slave output is connected to the second slave input, the second slave output is connected to the third slave input, and so on. The final slave output is connected to the master input. Each slave sends out, during a second group of clock pulses, an exact copy of what was received during the first group of clock pulses. The whole chain acts as one large communication shift register. The daisy-chain feature only requires a single Slave Select line from the master device.

Figure 26-7 shows the block diagram of a typical daisy-chain connection when operating in SPI mode.

In a daisy-chain configuration, only the most recent byte on the bus is required by the slave. Setting the BOEN bit of the SSPCON3 register will enable writes to the SSPBUF register, even if the previous byte has not been read. This allows the software to ignore data that may not apply to it.

26.2.5 SLAVE SELECT SYNCHRONIZATION

The Slave Select can also be used to synchronize communication. The Slave Select line is held high until the master device is ready to communicate. When the Slave Select line is pulled low, the slave knows that a new transmission is starting.

If the slave fails to receive the communication properly, it will be reset at the end of the transmission, when the Slave Select line returns to a high state. The slave is then ready to receive a new transmission when the Slave Select line is pulled low again. If the Slave Select line is not used, there is a risk that the slave will eventually become out of sync with the master. If the slave misses a bit, it will always be one bit off in future transmissions. Use of the Slave Select line allows the slave and master to align themselves at the beginning of each transmission.

The SS pin allows a Synchronous Slave mode. The SPI must be in Slave mode with SS pin control enabled (SSPCON1<3:0> = 0100).

When the SS pin is low, transmission and reception are enabled and the SDO pin is driven. When the SS pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte and becomes a floating output. External pull-up/pull-down resistors may be desirable depending on the application.

Note 1: When the SPI is in Slave mode with SS pin control enabled (SSPCON1<3:0> = 0100), the SPI module will reset if the SS pin is set to VDD.

2: When the SPI is used in Slave mode with CKE set; the user must enable SS pin control.

3: While operated in SPI Slave mode the SMP bit of the SSPSTAT register must remain clear.

When the SPI module resets, the bit counter is forced to '0'. This can be done by either forcing the SS pin to a high level or clearing the SSPEN bit.
**FIGURE 26-7: SPI DAISY-CHAIN CONNECTION**

- SPI Master
  - SCK
  - SDO
  - SDI
  - General I/O

- SPI Slave #1
  - SCK
  - SDI
  - SDO
  - SS

- SPI Slave #2
  - SCK
  - SDI
  - SDO
  - SS

- SPI Slave #3
  - SCK
  - SDI
  - SDO
  - SS

**FIGURE 26-8: SLAVE SELECT SYNCHRONOUS WAVEFORM**

- SS
- SCK (CKP = 0, CKE = 0)
- SCK (CKP = 1, CKE = 0)
- Write to SSPBUF
- SSPBUF to SSPSR
- SDO (bit 7, bit 6, bit 7, bit 6, bit 0)
- SDI (bit 7)
- Input Sample
- SSP1IF Interrupt Flag
- SSPSR to SSPBUF

Shift register SSPSR and bit count are reset
FIGURE 26-9: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

FIGURE 26-10: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)
26.2.6 SPI OPERATION IN SLEEP MODE

In SPI Master mode, module clocks may be operating at a different speed than when in Full-Power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSP clock is much faster than the system clock.

In Slave mode, when MSSP interrupts are enabled, after the master completes sending data, an MSSP interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSP interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all 8 bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device.

### TABLE 26-1: SUMMARY OF REGISTERS ASSOCIATED WITH SPI OPERATION

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSELA</td>
<td>ANSA7</td>
<td>—</td>
<td>ANSA5</td>
<td>ANSA4</td>
<td>ANSA3</td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
<td>132</td>
</tr>
<tr>
<td>APFCON1</td>
<td>C2OUTSEL</td>
<td>CCP1SEL</td>
<td>SDOSEL</td>
<td>SCKSEL</td>
<td>SDISEL</td>
<td>TXSEL</td>
<td>RXSEL</td>
<td>CCP2SEL</td>
<td>127</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMROIE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMROIF</td>
<td>INTF</td>
<td>IOCF</td>
<td>93</td>
</tr>
<tr>
<td>PIE1</td>
<td>TMRIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSIIE</td>
<td>CCP1IE</td>
<td>TMRIE</td>
<td>TMRIE</td>
<td>94</td>
</tr>
<tr>
<td>PIR1</td>
<td>TMRIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSIIF</td>
<td>CCP1IF</td>
<td>TMRIF</td>
<td>TMRIF</td>
<td>98</td>
</tr>
<tr>
<td>SSP1BUF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>285*</td>
</tr>
<tr>
<td>SSP1CON1</td>
<td>WCOL</td>
<td>SSOV</td>
<td>SSPE</td>
<td>CKP</td>
<td>SSPM&lt;3:0&gt;</td>
<td>331</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSP1CON3</td>
<td>ACKTIM</td>
<td>PCIe</td>
<td>SCIE</td>
<td>BOEN</td>
<td>SDAHT</td>
<td>SBCDE</td>
<td>AHEN</td>
<td>DHEN</td>
<td>333</td>
</tr>
<tr>
<td>SSP1STAT</td>
<td>SMP</td>
<td>CKE</td>
<td>D/A</td>
<td>P</td>
<td>S</td>
<td>R/W</td>
<td>UA</td>
<td>BF</td>
<td>329</td>
</tr>
<tr>
<td>TRISA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td>131</td>
</tr>
<tr>
<td>TRISC</td>
<td>TRISC7</td>
<td>TRISC6</td>
<td>TRISC5</td>
<td>TRISC4</td>
<td>TRISC3</td>
<td>TRISC2</td>
<td>TRISC1</td>
<td>TRISA0</td>
<td>142</td>
</tr>
</tbody>
</table>

Legend: — = Unimplemented location, read as ‘0’. Shaded cells are not used by the MSSP in SPI mode.

Note 1: PIC16(L)F1784/7 only.
26.3 \(\text{i}^2\text{C} \) MODE OVERVIEW

The Inter-Integrated Circuit Bus (\(\text{i}^2\text{C}\)) is a multi-master serial data communication bus. Devices communicate in a master/slave environment where the master devices initiate the communication. A Slave device is controlled through addressing.

The \(\text{i}^2\text{C}\) bus specifies two signal connections:
- Serial Clock (SCL)
- Serial Data (SDA)

Figure 26-11 shows the block diagram of the MSSP module when operating in \(\text{i}^2\text{C}\) mode.

Both the SCL and SDA connections are bidirectional open-drain lines, each requiring pull-up resistors for the supply voltage. Pulling the line to ground is considered a logical zero and letting the line float is considered a logical one.

Figure 26-11 shows a typical connection between two processors configured as master and slave devices.

The \(\text{i}^2\text{C}\) bus can operate with one or more master devices and one or more slave devices.

There are four potential modes of operation for a given device:
- Master Transmit mode
  (master is transmitting data to a slave)
- Master Receive mode
  (master is receiving data from a slave)
- Slave Transmit mode
  (slave is transmitting data to a master)
- Slave Receive mode
  (slave is receiving data from the master)

To begin communication, a master device starts out in Master Transmit mode. The master device sends out a Start bit followed by the address byte of the slave it intends to communicate with. This is followed by a single Read/Write bit, which determines whether the master intends to transmit to or receive data from the slave device.

If the requested slave exists on the bus, it will respond with an Acknowledge bit, otherwise known as an \(\text{ACK}\). The master then continues in either Transmit mode or Receive mode and the slave continues in the complement, either in Receive mode or Transmit mode, respectively.

A Start bit is indicated by a high-to-low transition of the SDA line while the SCL line is held high. Address and data bytes are sent out, Most Significant bit (MSb) first. The Read/Write bit is sent out as a logical one when the master intends to read data from the slave, and is sent out as a logical zero when it intends to write data to the slave.

The Acknowledge bit (\(\text{ACK}\)) is an active-low signal, which holds the SDA line low to indicate to the transmitter that the slave device has received the transmitted data and is ready to receive more.

The transition of a data bit is always performed while the SCL line is held low. Transitions that occur while the SCL line is held high are used to indicate Start and Stop bits.

If the master intends to write to the slave, then it repeatedly sends out a byte of data, with the slave responding after each byte with an \(\text{ACK}\) bit. In this example, the master device is in Master Transmit mode and the slave is in Slave Receive mode.

If the master intends to read from the slave, then it repeatedly receives a byte of data from the slave, and responds after each byte with an \(\text{ACK}\) bit. In this example, the master device is in Master Receive mode and the slave is Slave Transmit mode.

On the last byte of data communicated, the master device may end the transmission by sending a Stop bit. If the master device is in Receive mode, it sends the Stop bit in place of the last \(\text{ACK}\) bit. A Stop bit is indicated by a low-to-high transition of the SDA line while the SCL line is held high.

In some cases, the master may want to maintain control of the bus and re-initiate another transmission. If so, the master device may send another Start bit in place of the Stop bit or last \(\text{ACK}\) bit when it is in receive mode.

The \(\text{i}^2\text{C}\) bus specifies three message protocols:
- Single message where a master writes data to a slave.
- Single message where a master reads data from a slave.
- Combined message where a master initiates a minimum of two writes, or two reads, or a combination of writes and reads, to one or more slaves.
When one device is transmitting a logical one, or letting the line float, and a second device is transmitting a logical zero, or holding the line low, the first device can detect that the line is not a logical one. This detection, when used on the SCL line, is called clock stretching. Clock stretching gives slave devices a mechanism to control the flow of data. When this detection is used on the SDA line, it is called arbitration. Arbitration ensures that there is only one master device communicating at any single time.

26.3.1 CLOCK STRETCHING

When a slave device has not completed processing data, it can delay the transfer of more data through the process of clock stretching. An addressed slave device may hold the SCL clock line low after receiving or sending a bit, indicating that it is not yet ready to continue. The master that is communicating with the slave will attempt to raise the SCL line in order to transfer the next bit, but will detect that the clock line has not yet been released. Because the SCL connection is open-drain, the slave has the ability to hold that line low until it is ready to continue communicating.

Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data.

26.3.2 ARBITRATION

Each master device must monitor the bus for Start and Stop bits. If the device detects that the bus is busy, it cannot begin a new message until the bus returns to an Idle state.

However, two master devices may try to initiate a transmission on or about the same time. When this occurs, the process of arbitration begins. Each transmitter checks the level of the SDA data line and compares it to the level that it expects to find. The first transmitter to observe that the two levels do not match, loses arbitration, and must stop transmitting on the SDA line.

For example, if one transmitter holds the SDA line to a logical one (lets it float) and a second transmitter holds it to a logical zero (pulls it low), the result is that the SDA line will be low. The first transmitter then observes that the level of the line is different than expected and concludes that another transmitter is communicating.

The first transmitter to notice this difference is the one that loses arbitration and must stop driving the SDA line. If this transmitter is also a master device, it also must stop driving the SCL line. It then can monitor the lines for a Stop condition before trying to reissue its transmission. In the meantime, the other device that has not noticed any difference between the expected and actual levels on the SDA line continues with its original transmission. It can do so without any complications, because so far, the transmission appears exactly as expected with no other transmitter disturbing the message.

Slave Transmit mode can also be arbitrated, when a master addresses multiple slaves, but this is less common.

If two master devices are sending a message to two different slave devices at the address stage, the master sending the lower slave address always wins arbitration. When two master devices send messages to the same slave address, and addresses can sometimes refer to multiple slaves, the arbitration process must continue into the data stage.

Arbitration usually occurs very rarely, but it is a necessary process for proper multi-master support.
26.4 I²C MODE OPERATION

All MSSP I²C communication is byte oriented and shifted out MSb first. Six SFR registers and two interrupt flags interface the module with the PIC® microcontroller and user software. Two pins, SDA and SCL, are exercised by the module to communicate with other external I²C devices.

26.4.1 BYTE FORMAT

All communication in I²C is done in 9-bit segments. A byte is sent from a master to a slave or vice-versa, followed by an Acknowledge bit sent back. After the 8th falling edge of the SCL line, the device outputting data on the SDA changes that pin to an input and reads in an acknowledge value on the next clock pulse.

The clock signal, SCL, is provided by the master. Data is valid to change while the SCL signal is low, and sampled on the rising edge of the clock. Changes on the SDA line while the SCL line is high define special conditions on the bus, explained below.

26.4.2 DEFINITION OF I²C TERMINOLOGY

There is language and terminology in the description of I²C communication that have definitions specific to I²C. That word usage is defined below and may be used in the rest of this document without explanation. This table was adapted from the Philips I²C specification.

26.4.3 SDA AND SCL PINS

Selection of any I²C mode with the SSPEN bit set, forces the SCL and SDA pins to be open-drain. These pins should be set by the user to inputs by setting the appropriate TRIS bits.

Note: Data is tied to output zero when an I²C mode is enabled.

26.4.4 SDA HOLD TIME

The hold time of the SDA pin is selected by the SDAHT bit of the SSPCON3 register. Hold time is the time SDA is held valid after the falling edge of SCL. Setting the SDAHT bit selects a longer 300 ns minimum hold time and may help on buses with large capacitance.

<table>
<thead>
<tr>
<th>TERM</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmitter</td>
<td>The device which shifts data out onto the bus.</td>
</tr>
<tr>
<td>Receiver</td>
<td>The device which shifts data in from the bus.</td>
</tr>
<tr>
<td>Master</td>
<td>The device that initiates a transfer, generates clock signals and terminates a transfer.</td>
</tr>
<tr>
<td>Slave</td>
<td>The device addressed by the master.</td>
</tr>
<tr>
<td>Multi-master</td>
<td>A bus with more than one device that can initiate data transfers.</td>
</tr>
<tr>
<td>Arbitration</td>
<td>Procedure to ensure that only one master at a time controls the bus. Winning arbitration ensures that the message is not corrupted.</td>
</tr>
<tr>
<td>Synchronization</td>
<td>Procedure to synchronize the clocks of two or more devices on the bus.</td>
</tr>
<tr>
<td>Idle</td>
<td>No master is controlling the bus, and both SDA and SCL lines are high.</td>
</tr>
<tr>
<td>Active</td>
<td>Any time one or more master devices are controlling the bus.</td>
</tr>
<tr>
<td>Addressed Slave</td>
<td>Slave device that has received a matching address and is actively being clocked by a master.</td>
</tr>
<tr>
<td>Matching Address</td>
<td>Address byte that is clocked into a slave that matches the value stored in SSPADD.</td>
</tr>
<tr>
<td>Write Request</td>
<td>Slave receives a matching address with R/W bit clear, and is ready to clock in data.</td>
</tr>
<tr>
<td>Read Request</td>
<td>Master sends an address byte with the R/W bit set, indicating that it wishes to clock data out of the Slave. This data is the next and all following bytes until a Restart or Stop.</td>
</tr>
<tr>
<td>Clock Stretching</td>
<td>When a device on the bus hold SCL low to stall communication.</td>
</tr>
<tr>
<td>Bus Collision</td>
<td>Any time the SDA line is sampled low by the module while it is outputting and expected high state.</td>
</tr>
</tbody>
</table>
26.4.5 START CONDITION

The \(^2\text{C}\) specification defines a Start condition as a transition of SDA from a high to a low state while SCL line is high. A Start condition is always generated by the master and signifies the transition of the bus from an Idle to an Active state. Figure 26-10 shows waveforms for Start and Stop conditions.

A bus collision can occur on a Start condition if the module samples the SDA line low before asserting it low. This does not conform to the \(^2\text{C}\) Specification that states no bus collision can occur on a Start.

26.4.6 STOP CONDITION

A Stop condition is a transition of the SDA line from low-to-high state while the SCL line is high.

Note: At least one SCL low time must appear before a Stop is valid, therefore, if the SDA line goes low then high again while the SCL line stays high, only the Start condition is detected.

26.4.7 RESTART CONDITION

A Restart is valid any time that a Stop would be valid. A master can issue a Restart if it wishes to hold the bus after terminating the current transfer. A Restart has the same effect on the slave that a Start would, resetting all slave logic and preparing it to clock in an address. The master may want to address the same or another slave.

In 10-bit Addressing Slave mode a Restart is required for the master to clock data out of the addressed slave. Once a slave has been fully addressed, matching both high and low address bytes, the master can issue a Restart and the high address byte with the R/W bit set. The slave logic will then hold the clock and prepare to clock out data.

After a full match with R/W clear in 10-bit mode, a prior match flag is set and maintained. Until a Stop condition, a high address with R/W clear, or high address match fails.

26.4.8 START/STOP CONDITION INTERRUPT MASKING

The SCIE and PCIE bits of the SSPCON3 register can enable the generation of an interrupt in Slave modes that do not typically support this function. Slave modes where interrupt on Start and Stop detect are already enabled, these bits will have no effect.

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FIGURE 26-12: \(^2\text{C}\) START AND STOP CONDITIONS

FIGURE 26-13: \(^2\text{C}\) RESTART CONDITION
26.4.9 ACKNOWLEDGE SEQUENCE

The 9th SCL pulse for any transferred byte in I²C is dedicated as an Acknowledge. It allows receiving devices to respond back to the transmitter by pulling the SDA line low. The transmitter must release control of the line during this time to shift in the response. The Acknowledge (ACK) is an active-low signal, pulling the SDA line low indicated to the transmitter that the device has received the transmitted data and is ready to receive more.

The result of an ACK is placed in the ACKSTAT bit of the SSPCON2 register.

Slave software, when the AHEN and DHEN bits are set, allow the user to set the ACK value sent back to the transmitter. The ACKDT bit of the SSPCON2 register is set/cleared to determine the response.

Slave hardware will generate an ACK response if the AHEN and DHEN bits of the SSPCON3 register are clear.

There are certain conditions where an ACK will not be sent by the slave. If the BF bit of the SSPSTAT register or the SSPOV bit of the SSPCON1 register are set when a byte is received.

When the module is addressed, after the 8th falling edge of SCL on the bus, the ACKTIM bit of the SSPCON3 register are set when a byte is received.

26.5 I²C SLAVE MODE OPERATION

The MSSP Slave mode operates in one of four modes selected in the SSPM bits of SSPCON1 register. The modes can be divided into 7-bit and 10-bit Addressing mode. 10-bit Addressing modes operate the same as 7-bit with some additional overhead for handling the larger addresses.

Modes with Start and Stop bit interrupts operated the same as the other modes with SSP1IF additionally getting set upon detection of a Start, Restart, or Stop condition.

26.5.1 SLAVE MODE ADDRESSES

The SSPADD register (Register 26-6) contains the Slave mode address. The first byte received after a Start or Restart condition is compared against the value stored in this register. If the byte matches, the value is loaded into the SSPBUF register and an interrupt is generated. If the value does not match, the module goes idle and no indication is given to the software that anything happened.

The SSP Mask register (Register 26-5) affects the address matching process. See Section 26.5.9 “SSP Mask Register” for more information.

26.5.1.1 I²C Slave 7-bit Addressing Mode

In 7-bit Addressing mode, the LSB of the received data byte is ignored when determining if there is an address match.

26.5.1.2 I²C Slave 10-bit Addressing Mode

In 10-bit Addressing mode, the first received byte is compared to the binary value of ‘1 1 1 1 0 A9 A8 0’. A9 and A8 are the two MSb of the 10-bit address and stored in bits 2 and 1 of the SSPADD register.

After the acknowledge of the high byte the UA bit is set and SCL is held low until the user updates SSPADD with the low address. The low address byte is clocked in and all 8 bits are compared to the low address value in SSPADD. Even if there is not an address match; SSP1IF and UA are set, and SCL is held low until SSPADD is updated to receive a high byte again. When SSPADD is updated the UA bit is cleared. This ensures the module is ready to receive the high address byte on the next communication.

A high and low address match as a write request is required at the start of all 10-bit addressing communication. A transmission can be initiated by issuing a Restart once the slave is addressed, and clocking in the high address with the R/W bit set. The slave hardware will then acknowledge the read request and prepare to clock out data. This is only valid for a slave after it has received a complete high and low address byte match.
26.5.2 SLAVE RECEPTION

When the R/W bit of a matching received address byte is clear, the R/W bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register and acknowledged.

When the overflow condition exists for a received address, then not Acknowledge is given. An overflow condition is defined as either bit BF of the SSPSTAT register is set, or bit SSPOV of the SSPCON1 register is set. The BOEN bit of the SSPCON3 register modifies this operation. For more information see Register 26-4.

An MSSP interrupt is generated for each transferred data byte. Flag bit, SSP1IF, must be cleared by software.

When the SEN bit of the SSPCON2 register is set, SCL will be held low (clock stretch) following each received byte. The clock must be released by setting the CKP bit of the SSPCON1 register, except sometimes in 10-bit mode. See Section 26.2.3 “SPI Master Mode” for more detail.

26.5.2.1 7-bit Addressing Reception

This section describes a standard sequence of events for the MSSP module configured as an I²C Slave in 7-bit Addressing mode. All decisions made by hardware or software and their effect on reception. Figure 26-13 and Figure 26-14 is used as a visual reference for this description.

This is a step by step process of what typically must be done to accomplish I²C communication.

1. Start bit detected.
2. S bit of SSPSTAT is set; SSP1IF is set if interrupt on Start detect is enabled.
3. Matching address with R/W bit clear is received.
4. The slave pulls SDA low sending an ACK to the master, and sets SSP1IF bit.
5. Software clears the SSP1IF bit.
6. Software reads received address from SSPBUF clearing the BF flag.
7. If SEN = 1; Slave software sets CKP bit to release the SCL line.
8. The master clocks out a data byte.
9. Slave drives SDA low sending an ACK to the master, and sets SSP1IF bit.
10. Software clears SSP1IF.
11. Software reads the received byte from SSPBUF clearing BF.
12. Steps 8-12 are repeated for all received bytes from the master.

26.5.2.2 7-bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operate the same as without these options with extra interrupts and clock stretching added after the 8th falling edge of SCL. These additional interrupts allow the slave software to decide whether it wants to ACK the receive address or data byte, rather than the hardware. This functionality adds support for PMBus™ that was not present on previous versions of this module.

This list describes the steps that need to be taken by slave software to use these options for I²C communication. Figure 26-15 displays a module using both address and data holding. Figure 26-16 includes the operation with the SEN bit of the SSPCON2 register set.

1. S bit of SSPSTAT is set; SSP1IF is set if interrupt on Start detect is enabled.
2. Matching address with R/W bit clear is clocked in. SSP1IF is set and CKP cleared after the 8th falling edge of SCL.
3. Slave clears the SSP1IF.
4. Slave can look at the ACKTIM bit of the SSPCON3 register to determine if the SSP1IF was after or before the ACK.
5. Slave reads the address value from SSPBUF, clearing the BF flag.
6. Slave sets ACK value clocked out to the master by setting ACKDT.
7. Slave releases the clock by setting CKP.
8. SSP1IF is set after an ACK, not after a NACK.
9. If SEN = 1, the slave hardware will stretch the clock after the ACK.
10. Slave clears SSP1IF.

Note: SSP1IF is still set after the 9th falling edge of SCL even if there is no clock stretching and BF has been cleared. Only if NACK is sent to master is SSP1IF not set
FIGURE 26-14: \( \text{I}^2\text{C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 0, DHEN = 0)} \)

Bus Master sends Stop condition

From Slave to Master

Receiving Address

ACK

Receiving Data

ACK

Receiving Data ACK

\( A7\) \( A6\) \( A5\) \( A4\) \( A3\) \( A2\) \( A1\) \( D7\) \( D6\) \( D5\) \( D4\) \( D3\) \( D2\) \( D1\) \( D0\)

SDA

SCL

SSP1IF

BF

SSPOV

First byte of data is available in SSPBUF

SSPBUF is read

Cleared by software

SSPOV set because SSPBUF is still full. ACR is not sent.

SSP1IF set on 9th falling edge of SCL

Cleared by software

From Slave to Master

SSPOV set because SSPBUF is still full.

P

Bus Master sends Stop condition

S

From Master to Slave

\( A7\) \( A6\) \( A5\) \( A4\) \( A3\) \( A2\) \( A1\) \( D7\) \( D6\) \( D5\) \( D4\) \( D3\) \( D2\) \( D1\) \( D0\)

SDA

SCL

SSP1IF

BF

SSPOV
FIGURE 26-15: I2C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)
FIGURE 26-16: \( \text{i}^2\text{C} \) SLAVE, 7-BIT ADDRESS, RECEPTION (\( \text{SEN} = 0, \text{AHEN} = 1, \text{DHEN} = 1 \))

- Master sends Stop condition
- No interrupt after not ACK from Slave
- Master releases SDA to slave for ACK sequence
- Data is read from SSPBUF
- ACKTIM cleared by hardware in 9th rising edge of SCL
- ACK set by software
- SCL is released
- Slave software clears ACKDT to not ACK
- ACKTIM cleared by hardware on 8th falling edge of SCL
- ACK = 1
- ACKDT
- ACKTIM
- SSP1IF
- If AHEN = 1:
  - SSP1IF is set on 9th falling edge of SCL after ACK
  - ACKTIM is set by hardware on 8th falling edge of SCL
  - ACKDT
  - ACKTIM cleared by hardware in 9th rising edge of SCL
FIGURE 26-17: 7-BIT ADDRESS, RECEPTION

- **Master releases SDA to slave for ACK sequence**
- **Slave sends not ACK**
- **CKP is not cleared if not ACK**
- **When AHEN = 1; on the 8th falling edge of SCL of an address byte, CKP is cleared**
- **When DHEN = 1; on the 8th falling edge of SCL of a received data byte, CKP is cleared**
- **ACKTIM is set by hardware on 8th falling edge of SCL**
- **ACKTIM is cleared by hardware on 8th rising edge of SCL**
- **ACKDT is cleared by software**
- **SSPBUF can be read any time before next byte is loaded**
- **ACKDT to ACK the received byte**
- **Slave sends not ACK**
- **CKP is not cleared if not ACK**
- **No interrupt after if not ACK from Slave**

**Reception**

**R/W = 0**

**Received address is loaded into SSPBUF**

**Received data is available on SSPBUF**

**ACKDT is cleared by software**

**Set by software, release SCL**

**ACKTIM is cleared by hardware on 8th rising edge of SCL**

**ACKDT is cleared by software**

**ACKTIM is cleared by hardware on 8th rising edge of SCL**

**Master sends Stop condition**
26.5.3 SLAVE TRANSMISSION

When the R/W bit of the incoming address byte is set and an address match occurs, the R/W bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register, and an ACK pulse is sent by the slave on the ninth bit.

Following the ACK, slave hardware clears the CKP bit and the SCL pin is held low (see Section 26.5.6 “Clock Stretching” for more detail). By stretching the clock, the master will be unable to assert another clock pulse until the slave is done preparing the transmit data.

The transmit data must be loaded into the SSPBUF register which also loads the SSPSR register. Then the SCL pin should be released by setting the CKP bit of the SSPCON1 register. The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time.

The ACK pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. This ACK value is copied to the ACKSTAT bit of the SSPCON2 register. If ACKSTAT is set (not ACK), then the data transfer is complete. In this case, when the not ACK is latched by the slave, the slave goes idle and waits for another occurrence of the Start bit. If the SDA line was low (AKC), the next transmit data must be loaded into the SSPBUF register. Again, the SCL pin must be released by setting bit CKP.

An MSSP interrupt is generated for each data transfer byte. The SSP1IF bit must be cleared by software and the SSPSTAT register is used to determine the status of the byte. The SSP1IF bit is set on the falling edge of the ninth clock pulse.

26.5.3.1 Slave Mode Bus Collision

A slave receives a Read request and begins shifting data out on the SDA line. If a bus collision is detected and the SBCDE bit of the SSPCON3 register is set, the BCL1IF bit of the PIR register is set. Once a bus collision is detected, the slave goes idle and waits to be addressed again. User software can use the BCL1IF bit to handle a slave bus collision.

26.5.3.2 7-bit Transmission

A master device can transmit a read request to a slave, and then clock data out of the slave. The list below outlines what software for a slave will need to do to accomplish a standard transmission. Figure 26-17 can be used as a reference to this list.

1. Master sends a Start condition on SDA and SCL.
2. S bit of SSPSTAT is set; SSP1IF is set if interrupt on Start detect is enabled.
3. Matching address with R/W bit set is received by the Slave setting SSP1IF bit.
4. Slave hardware generates an ACK and sets SSP1IF.
5. SSP1IF bit is cleared by user.
6. Software reads the received address from SSPBUF, clearing BF.
7. R/W is set so CKP was automatically cleared after the ACK.
8. The slave software loads the transmit data into SSPBUF.
9. CKP bit is set releasing SCL, allowing the master to clock the data out of the slave.
10. SSP1IF is set after the ACK response from the master is loaded into the ACKSTAT register.
11. SSP1IF bit is cleared.
12. The slave software checks the ACKSTAT bit to see if the master wants to clock out more data.

Note 1: If the master ACKs the clock will be stretched.
2: ACKSTAT is the only bit updated on the rising edge of SCL (9th) rather than the falling.

13. Steps 9-13 are repeated for each transmitted byte.
14. If the master sends a not ACK; the clock is not held, but SSP1IF is still set.
15. The master sends a Restart condition or a Stop.
16. The slave is no longer addressed.
FIGURE 26-18: \( \text{i}^2 \text{C SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 0)} \)

- **SDA**: Data line
- **SCL**: Clock line
- **SSP1IF**: SSP1 Interrupt Flag
- **BF**: Buffer Full
- **CKP**: Clock Stop
- **ACKSTAT**: Acknowledge Status
- **R/W**: Read/Write

**Master Sends Stop Condition**
- Master sends a stop condition to end the transmission.

**Receiving Address**
- The received address is stored in the SSPBUF register.
- The address is read from the SSPBUF register.
- SCL is always held low after the 9th SCL falling edge.
- When R/W is set, SCL is always held low after the 9th SCL falling edge.
- ACK is copied from the matching address byte.
- Indicates an address has been received.

**Data to Transmit**
- Data to transmit is loaded into SSPBUF.
- BF is automatically cleared after 8th falling edge of SCL.
- ACK is not held for not ACK.
- CKP is not held for not ACK.
- ACKSTAT is set by software.
- Data is set by software.

**Controller Actions**
- **ACK**: Acknowledgment
- **S**: Start condition
- **P**: Stop condition
26.5.3.3 7-bit Transmission with Address Hold Enabled

Setting the AHEN bit of the SSPCON3 register enables additional clock stretching and interrupt generation after the 8th falling edge of a received matching address. Once a matching address has been clocked in, CKP is cleared and the SSP1IF interrupt is set.

Figure 26-18 displays a standard waveform of a 7-bit Address Slave Transmission with AHEN enabled.

1. Bus starts Idle.
2. Master sends Start condition; the S bit of SSPSTAT is set; SSP1IF is set if interrupt on Start detect is enabled.
3. Master sends matching address with R/W bit set. After the 8th falling edge of the SCL line the CKP bit is cleared and SSP1IF interrupt is generated.
4. Slave software clears SSP1IF.
5. Slave software reads ACKTIM bit of SSPCON3 register, and R/W and D/A of the SSPSTAT register to determine the source of the interrupt.
6. Slave reads the address value from the SSPBUF register clearing the BF bit.
7. Slave software decides from this information if it wishes to ACK or not ACK and sets the ACKDT bit of the SSPCON2 register accordingly.
8. Slave sets the CKP bit releasing SCL.
9. Master clocks in the ACK value from the slave.
10. Slave hardware automatically clears the CKP bit and sets SSP1IF after the ACK if the R/W bit is set.
11. Slave software clears SSP1IF.
12. Slave loads value to transmit to the master into SSPBUF setting the BF bit.

**Note:** SSPBUF cannot be loaded until after the ACK.

13. Slave sets the CKP bit releasing the clock.
14. Master clocks out the data from the slave and sends an ACK value on the 9th SCL pulse.
15. Slave hardware copies the ACK value into the ACKSTAT bit of the SSPCON2 register.
16. Steps 10-15 are repeated for each byte transmitted to the master from the slave.
17. If the master sends a not ACK the slave releases the bus allowing the master to send a Stop and end the communication.

**Note:** Master must send a not ACK on the last byte to ensure that the slave releases the SCL line to receive a Stop.
FIGURE 26-19:  \( \text{I}^2\text{C SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 1)} \)

- Master sends \( \text{Stop condition} \)
- Master releases SDA to slave for \( \text{ACK} \) sequence
- \( \text{ACK} \)
- \( \text{BF} \) is automatically cleared after 8th falling edge of \( \text{SCL} \)
- Data to transmit is loaded into \( \text{SSPBUF} \)
- Slave clears \( \text{ACKDT} \) to \( \text{ACK} \)
- Master's \( \text{ACK} \) response is copied to \( \text{SSPSTAT} \)
- \( \text{CKP} \) not cleared after not \( \text{ACK} \)
- ACKTIM is cleared on 9th rising edge of \( \text{SCL} \)
- ACKTIM is set on 8th falling edge of \( \text{SCL} \)

When \( \text{AHEN} = 1 \):
- \( \text{CKP} \) is cleared by hardware after receiving matching address.

When \( \text{R/W} = 1 \):
- \( \text{CKP} \) is always cleared after \( \text{ACK} \)
26.5.4 SLAVE MODE 10-BIT ADDRESS RECEPTION

This section describes a standard sequence of events for the MSSP module configured as an I^2C slave in 10-bit Addressing mode.

Figure 26-19 is used as a visual reference for this description.

This is a step by step process of what must be done by slave software to accomplish I^2C communication.

1. Bus starts Idle.
2. Master sends Start condition; S bit of SSPSTAT is set; SSP1IF is set if interrupt on Start detect is enabled.
3. Master sends matching high address with R/W bit clear; UA bit of the SSPSTAT register is set.
4. Slave sends ACK and SSP1IF is set.
5. Software clears the SSP1IF bit.
6. Software reads received address from SSPBUF clearing the BF flag.
7. Slave loads low address into SSPADD, releasing SCL.
8. Master sends matching low address byte to the slave; UA bit is set.

9. Slave sends ACK and SSP1IF is set.

Note: If the low address does not match, SSP1IF and UA are still set so that the slave software can set SSPADD back to the high address. BF is not set because there is no match. CKP is unaffected.

10. Slave clears SSP1IF.
11. Slave reads the received matching address from SSPBUF clearing BF.
12. Slave loads high address into SSPADD.
13. Master clocks a data byte to the slave and clocks out the slaves ACK on the 9th SCL pulse; SSP1IF is set.
14. If SEN bit of SSPCON2 is set, CKP is cleared by hardware and the clock is stretched.
15. Slave clears SSP1IF.
16. Slave reads the received byte from SSPBUF clearing BF.
17. If SEN is set the slave sets CKP to release the SCL.
18. Steps 13-17 repeat for each received byte.
19. Master sends Stop to end the transmission.

26.5.5 10-BIT ADDRESSING WITH ADDRESS OR DATA HOLD

Reception using 10-bit addressing with AHEN or DHEN set is the same as with 7-bit modes. The only difference is the need to update the SSPADD register using the UA bit. All functionality, specifically when the CKP bit is cleared and SCL line is held low are the same. Figure 26-20 can be used as a reference of a slave in 10-bit addressing with AHEN set.

Figure 26-21 shows a standard waveform for a slave transmitter in 10-bit Addressing mode.
FIGURE 26-20: I2C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)
FIGURE 26-21: I2C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 1, DHEN = 0)
FIGURE 26-22: I²C SLAVE, 10-BIT ADDRESS, TRANSMISSION (SEN = 0, AHEN = 0, DHEN = 0)
26.5.6 CLOCK STRETCHING

Clock stretching occurs when a device on the bus holds the SCL line low effectively pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching as anytime it is active on the bus and not transferring data it is stretching. Any stretching done by a slave is invisible to the master software and handled by the hardware that generates SCL.

The CKP bit of the SSPCON1 register is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. Setting CKP will release SCL and allow more communication.

26.5.6.1 Normal Clock Stretching

Following an ACK if the R/W bit of SSPSTAT is set, a read request, the slave hardware will clear CKP. This allows the slave time to update SSPBUF with data to transfer to the master. If the SEN bit of SSPCON2 is set, the slave hardware will always stretch the clock after the ACK sequence. Once the slave is ready; CKP is set by software and communication resumes.

Note 1: The BF bit has no effect on if the clock will be stretched or not. This is different than previous versions of the module that would not stretch the clock, clear CKP, if SSPBUF was read before the 9th falling edge of SCL.

2: Previous versions of the module did not stretch the clock for a transmission if SSPBUF was loaded before the 9th falling edge of SCL. It is now always cleared for read requests.

26.5.6.2 10-bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set the clock is always stretched. This is the only time the SCL is stretched without CKP being cleared. SCL is released immediately after a write to SSPADD.

Note: Previous versions of the module did not stretch the clock if the second address byte did not match.

26.5.6.3 Byte NACKing

When AHEN bit of SSPCON3 is set; CKP is cleared by hardware after the 8th falling edge of SCL for a received matching address byte. When DHEN bit of SSPCON3 is set; CKP is cleared after the 8th falling edge of SCL for received data.

Stretching after the 8th falling edge of SCL allows the slave to look at the received address or data and decide if it wants to ACK the received data.

26.5.7 CLOCK SYNCHRONIZATION AND THE CKP BIT

Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. However, clearing the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external \(^{\text{\textregistered}}\)I\(^2\)C master device has already asserted the SCL line. The SCL output will remain low until the CKP bit is set and all other devices on the \(^{\text{\textregistered}}\)I\(^2\)C bus have released SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (see Figure 26-22).
26.5.8 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the $i^2$C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

The general call address is a reserved address in the $i^2$C protocol, defined as address 0x00. When the GCEN bit of the SSPCON2 register is set, the slave module will automatically ACK the reception of this address regardless of the value stored in SSPADD. After the slave clocks in an address of all zeros with the R/W bit clear, an interrupt is generated and slave software can read SSPBUF and respond. Figure 26-23 shows a general call reception sequence.

In 10-bit Address mode, the UA bit will not be set on the reception of the general call address. The slave will prepare to receive the second byte as data, just as it would in 7-bit mode.

If the AHEN bit of the SSPCON3 register is set, just as with any other address reception, the slave hardware will stretch the clock after the 8th falling edge of SCL. The slave must then set its ACKDT value and release the clock with communication progressing as it would normally.

26.5.9 SSP MASK REGISTER

An SSP Mask (SSPMSK) register (Register 26-5) is available in $i^2$C Slave mode as a mask for the value held in the SSPSR register during an address comparison operation. A zero (‘0’) bit in the SSPMSK register has the effect of making the corresponding bit of the received address a “don’t care”.

This register is reset to all ‘1’s upon any Reset condition and, therefore, has no effect on standard SSP operation until written with a mask value.

The SSP Mask register is active during:
- 7-bit Address mode: address compare of A<7:1>.
- 10-bit Address mode: address compare of A<7:0> only. The SSP mask has no effect during the reception of the first (high) byte of the address.
26.6  I²C Master Mode

Master mode is enabled by setting and clearing the appropriate SSPM bits in the SSPCON1 register and by setting the SSPEN bit. In Master mode, the SDA and SCK pins must be configured as inputs. The MSSP peripheral hardware will override the output driver TRIS controls when necessary to drive the pins low.

Master mode of operation is supported by interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit is set, or the bus is Idle.

In Firmware Controlled Master mode, user code conducts all I²C bus operations based on Start and Stop bit condition detection. Start and Stop condition detection is the only active circuitry in this mode. All other communication is done by the user software directly manipulating the SDA and SCL lines.

The following events will cause the SSP Interrupt Flag bit, SSP1IF, to be set (SSP interrupt, if enabled):

- Start condition detected
- Stop condition detected
- Data transfer byte transmitted/received
- Acknowledge transmitted/received
- Repeated Start generated

Note 1: The MSSP module, when configured in I²C Master mode, does not allow queuing of events. For instance, the user is not allowed to initiate a Start condition and immediately write the SSPBUF register to initiate transmission before the Start condition is complete. In this case, the SSPBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPBUF did not occur.

Note 2: When in Master mode, Start/Stop detection is masked and an interrupt is generated when the SEN/PEN bit is cleared and the generation is complete.

26.6.1  I²C MASTER MODE OPERATION

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDA, while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/W) bit. In this case, the R/W bit will be logic ‘0’. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an Acknowledge bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/W bit. In this case, the R/W bit will be logic ‘1’. Thus, the first byte transmitted is a 7-bit slave address followed by a ‘1’ to indicate the receive bit. Serial data is received via SDA, while SCL outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

A Baud Rate Generator is used to set the clock frequency output on SCL. See Section 26.7 “Baud Rate Generator” for more detail.
26.6.2 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit or Repeated Start/Stop condition, releases the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the Baud Rate Generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<7:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 26-25).

FIGURE 26-25: BAUD RATE GENERATOR TIMING WITH CLOCK ARBITRATION

26.6.3 WCOL STATUS FLAG

If the user writes the SSPBUF when a Start, Restart, Stop, Receive or Transmit sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write does not occur). Any time the WCOL bit is set it indicates that an action on SSPBUF was attempted while the module was not idle.

**Note:** Because queueing of events is not allowed, writing to the lower 5 bits of SSPCON2 is disabled until the Start condition is complete.
26.6.4 I\textsuperscript{2}C MASTER MODE START
CONDITION TIMING

To initiate a Start condition, the user sets the Start Enable bit, SEN bit of the SSPCON2 register. If the SDA and SCL pins are sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<7:0> and starts its count. If SCL and SDA are both sampled high when the Baud Rate Generator times out (TBRG), the SDA pin is driven low. The action of the SDA being driven low while SCL is high is the Start condition and causes the S bit of the SSPSTAT1 register to be set. Following this, the Baud Rate Generator is reloaded with the contents of SSPADD<7:0> and resumes its count. When the Baud Rate Generator times out (TBRG), the SEN bit of the SSPCON2 register will be automatically cleared by hardware; the Baud Rate Generator is suspended, leaving the SDA line held low and the Start condition is complete.

Note 1: If at the beginning of the Start condition, the SDA and SCL pins are already sampled low, or if during the Start condition, the SCL line is sampled low before the SDA line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCL1IF, is set, the Start condition is aborted and the I\textsuperscript{2}C module is reset into its Idle state.

2: The Philips I\textsuperscript{2}C specification states that a bus collision cannot occur on a Start.
26.6.5 \( ^2 \)C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition occurs when the RSEN bit of the SSPCON2 register is programmed high and the master state machine is no longer active. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. SCL is asserted low. Following this, the RSEN bit of the SSP-CON2 register will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit of the SSPSTAT register will be set. The SSP1IF bit will not be set until the Baud Rate Generator has timed out.

Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.

2: A bus collision during the Repeated Start condition occurs if:
   - SDA is sampled low when SCL goes from low-to-high.
   - SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data ‘1’.

**FIGURE 26-27: REPEAT START CONDITION WAVEFORM**

![Waveform Diagram](image-url)
26.6.6 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address is accomplished by simply writing a value to the SSPBUF register. This action will set the Buffer Full flag bit, BF and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted. SCL is held low for one Baud Rate Generator rollover count (TBRG). Data should be valid before SCL is released high. When the SCL pin is released high, it is held that way for TBRG. The data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA. This allows the slave device being addressed to respond with an ACK bit during the ninth bit time if an address match occurred, or if data was received properly. The status of ACK is written into the ACKSTAT bit on the rising edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared. If not, the bit is set. After the ninth clock, the SSP1IF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSPBUF, leaving SCL low and SDA unchanged (Figure 26-27).

After the write to the SSPBUF, each bit of the address will be shifted out on the falling edge of SCL until all seven address bits and the R/W bit are completed. On the falling edge of the eighth clock, the master will release the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of ACK is loaded into the ACKSTAT Status bit of the SSPCON2 register. Following the falling edge of the ninth clock transmission of the address, the SSP1IF is set, the BF flag is cleared and the Baud Rate Generator is turned off until another write to the SSPBUF takes place, holding SCL low and allowing SDA to float.

26.6.6.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit of the SSPCON2 register is cleared when the slave has sent an Acknowledge (ACK = 0) and is set when the slave does not Acknowledge (ACK = 1). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

26.6.6.4 Typical transmit sequence:

1. The user generates a Start condition by setting the SEN bit of the SSPCON2 register.
2. SSP1IF is set by hardware on completion of the Start.
3. SSP1IF is cleared by software.
4. The MSSP module will wait the required start time before any other operation takes place.
5. The user loads the SSPBUF with the slave address to transmit.
6. Address is shifted out the SDA pin until all 8 bits are transmitted. Transmission begins as soon as SSPBUF is written to.
7. The MSSP module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSPCON2 register.
8. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSP1IF bit.
9. The user loads the SSPBUF with eight bits of data.
10. Data is shifted out the SDA pin until all 8 bits are transmitted.
11. The MSSP module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSPCON2 register.
12. Steps 8-11 are repeated for all transmitted data bytes.
13. The user generates a Stop or Restart condition by setting the PEN or RSEN bits of the SSPCON2 register. Interrupt is generated once the Stop/Restart condition is complete.

26.6.6.1 BF Status Flag

In Transmit mode, the BF bit of the SSPSTAT register is set when the CPU writes to SSPBUF and is cleared when all 8 bits are shifted out.

26.6.6.2 WCOL Status Flag

If the user writes the SSPBUF when a transmit is already in progress (i.e., SSPSR is still shifting out a data byte), the WCOL is set and the contents of the buffer are unchanged (the write does not occur).

WCOL must be cleared by software before the next transmission.
FIGURE 26-28: I²C MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)
26.6.7 \textbf{I²C MASTER MODE RECEPTION}

Master mode reception is enabled by programming the Receive Enable bit, RCEN bit of the SSPCON2 register.

\begin{itemize}
  \item \textbf{Note:} The MSSP module must be in an Idle state before the RCEN bit is set or the RCEN bit will be disregarded.
\end{itemize}

The Baud Rate Generator begins counting and on each rollover, the state of the SCL pin changes (high-to-low/low-to-high) and data is shifted into the SSPSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag bit is set, the SSP1IF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSP is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable, ACKEN bit of the SSPCON2 register.

26.6.7.1 \textbf{BF Status Flag}

In receive operation, the BF bit is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when the SSPBUF register is read.

26.6.7.2 \textbf{SSPOV Status Flag}

In receive operation, the SSPOV bit is set when 8 bits are received into the SSPSR and the BF flag bit is already set from a previous reception.

26.6.7.3 \textbf{WCOL Status Flag}

If the user writes the SSPBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

26.6.7.4 \textbf{Typical Receive Sequence:}

1. The user generates a Start condition by setting the SEN bit of the SSPCON2 register.
2. SSP1IF is set by hardware on completion of the Start.
3. SSP1IF is cleared by software.
4. User writes SSPBUF with the slave address to transmit and the R/W bit set.
5. Address is shifted out the SDA pin until all 8 bits are transmitted. Transmission begins as soon as SSPBUF is written to.
6. The MSSP module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSPCON2 register.
7. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSP1IF bit.
8. User sets the RCEN bit of the SSPCON2 register and the master clocks in a byte from the slave.
9. After the 8th falling edge of SCL, SSP1IF and BF are set.
10. User clears the SSP1IF bit and reads the received byte from SSPUF, which clears the BF flag.
11. The user either clears the SSPCON2 register’s ACKDT bit to receive another byte or sets the ADKDT bit to suppress further data and then initiates the acknowledge sequence by setting the ACKEN bit.
12. Master’s ACK or \textit{ACK} is clocked out to the slave and SSP1IF is set.
13. User clears SSP1IF.
14. Steps 8-13 are repeated for each received byte from the slave.
15. If the ACKST bit was set in step 11 then the user can send a \textit{STOP} to release the bus.
FIGURE 26-29: \( \text{i}^2\text{C} \) MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)
26.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSPCON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts high, the SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into Idle mode (Figure 26-29).

26.6.8.1 WCOL Status Flag

If the user writes the SSPBUF when an Acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 26-30: ACKNOWLEDGE SEQUENCE WAVEFORM

Note: TBRG = one Baud Rate Generator period.

26.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSPCON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to ‘0’. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit of the SSPSTAT register is set. A TBRG later, the PEN bit is cleared and the SSP1IF bit is set (Figure 26-30).

26.6.9.1 WCOL Status Flag

If the user writes the SSPBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).
26.6.10 SLEEP OPERATION
While in Sleep mode, the I²C slave module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

26.6.11 EFFECTS OF A RESET
A Reset disables the MSSP module and terminates the current transfer.

26.6.12 MULTI-MASTER MODE
In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit of the SSPSTAT register is set, or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed by hardware with the result placed in the BCL1IF bit.

The states where arbitration can be lost are:
- Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

26.6.13 MULTI-MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION
Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a ‘1’ on SDA, by letting SDA float high and another master asserts a ‘0’. When the SCL pin floats high, data should be stable. If the expected data on SDA is a ‘1’ and the data sampled on the SDA pin is ‘0’, then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCL1IF and reset the I²C port to its Idle state (Figure 26-31).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are deasserted and the SSPBUF can be written to. When the user services the bus collision Interrupt Service Routine and if the I²C bus is free, the user can resume communication by asserting a Start condition.

If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are deasserted and the respective control bits in the SSPCON2 register are cleared. When the user services the bus collision Interrupt Service Routine and if the I²C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDA and SCL pins. If a Stop condition occurs, the SSP1IF bit will be set.

A write to the SSPBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I²C bus can be taken when the P bit is set in the SSPSTAT register, or the bus is Idle and the S and P bits are cleared.
FIGURE 26-32: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE

- Data changes while SCL = 0
- SDA line pulled low by another source
- SDA released by master
- Sample SDA. While SCL is high, data does not match what is driven by the master. Bus collision has occurred.
- Set bus collision interrupt (BCL1IF)
26.6.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

a) SDA or SCL are sampled low at the beginning of the Start condition (Figure 26-32).

b) SCL is sampled low before SDA is asserted low (Figure 26-33).

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

• the Start condition is aborted,
• the BCL1IF flag is set and
• the MSSP module is reset to its Idle state (Figure 26-32).

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data ‘1’ during the Start condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCL pin is sampled as ‘0’ during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

Note: The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.

FIGURE 26-33: BUS COLLISION DURING START CONDITION (SDA ONLY)
FIGURE 26-34: BUS COLLISION DURING START CONDITION (SCL = 0)

SDA = 0, SCL = 1

SDA

SCL

SEN

BCL1IF

Interrupt cleared by software

SDA = 0, SCL = 1

Set SEN, enable Start sequence if SDA = 1, SCL = 1

SCL = 0 before SDA = 0, bus collision occurs. Set BCL1IF.

SDA = 0, SCL = 1

Set SSP1IF

S

SSP1IF

'0'

'0'

FIGURE 26-35: BRG RESET DUE TO SDA ARBITRATION DURING START CONDITION

SDA = 0, SCL = 1

Less than TBRG

SDA pulled low by other master.
Reset BRG and assert SDA.

Set S

S

Set S

SSP1IF

SDA = 0, SCL = 1

Interruption cleared by software

Set SSP1IF

S

SSP1IF

'0'

'0'

SDA = 0, SCL = 1

Set SEN, enable Start sequence if SDA = 1, SCL = 1

SCL = 0 before SDA = 0, bus collision occurs. Set BCL1IF.

SDA = 0, SCL = 1

SCL pulled low after BRG time-out

Set SEN, enable Start sequence if SDA = 1, SCL = 1

'0'

SDA pulled low by other master.
Reset BRG and assert SDA.

SDA = 0, SCL = 1

Interruption cleared by software

Set SSP1IF

S

SSP1IF

'0'

'0'
26.6.13.2  Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDA when SCL goes from low level to high level.

b) SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data ‘1’.

When the user releases SDA and the pin is allowed to float high, the BRG is loaded with SSPADD and counts down to zero. The SCL pin is then deasserted and when sampled high, the SDA pin is sampled.

If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data ‘0’, Figure 26-35).

If SDA is sampled high, the BRG is reloaded and begins counting. If SDA goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

If SCL goes from high-to-low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data ‘1’ during the Repeated Start condition, see Figure 26-36.

If, at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated Start condition is complete.

**FIGURE 26-36: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)**

**FIGURE 26-37: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)**
26.6.13.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

a) After the SDA pin has been deasserted and allowed to float high, SDA is sampled low after the BRG has timed out.

b) After the SCL pin is deasserted, SCL is sampled low before SDA goes high.

The Stop condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSPADD and counts down to 0. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 26-37). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 26-38).

**FIGURE 26-38: BUS COLLISION DURING A STOP CONDITION (CASE 1)**

<table>
<thead>
<tr>
<th>SDA</th>
<th>TBRG</th>
<th>TBRG</th>
<th>TBRG</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SDA asserted low</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCL</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PEN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BCL1IF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P</td>
<td>'0'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSP1IF</td>
<td>'0'</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**FIGURE 26-39: BUS COLLISION DURING A STOP CONDITION (CASE 2)**

<table>
<thead>
<tr>
<th>SDA</th>
<th>TBRG</th>
<th>TBRG</th>
<th>TBRG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assert SDA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCL</td>
<td>SCL goes low before SDA goes high, set BCL1IF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PEN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BCL1IF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P</td>
<td>'0'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSP1IF</td>
<td>'0'</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
TABLE 26-3: SUMMARY OF REGISTERS ASSOCIATED WITH I²C™ OPERATION

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Reset Values on Page:</th>
</tr>
</thead>
<tbody>
<tr>
<td>APFCON1</td>
<td>C2OUTSEL</td>
<td>CCP1SEL</td>
<td>SDSEL</td>
<td>SCKSEL</td>
<td>SDSEL</td>
<td>TXSEL</td>
<td>RXSEL</td>
<td>CCP2SEL</td>
<td>127</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IE</td>
<td>INTF</td>
<td>IOCIF</td>
<td>93</td>
</tr>
<tr>
<td>PIE1</td>
<td>TMR1GIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSP1IE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>94</td>
</tr>
<tr>
<td>PIE2</td>
<td>OSFIE</td>
<td>C2IE</td>
<td>C1IE</td>
<td>EEIE</td>
<td>BCL1IE</td>
<td>C4IE</td>
<td>C3IE</td>
<td>CCP2IE</td>
<td>95</td>
</tr>
<tr>
<td>PIR1</td>
<td>TMR1GIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1IF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>98</td>
</tr>
<tr>
<td>PIR2</td>
<td>OSFIF</td>
<td>C2IF</td>
<td>C1IF</td>
<td>EEIF</td>
<td>BCL1IF</td>
<td>C4IF</td>
<td>C3IF</td>
<td>CCP2IF</td>
<td>99</td>
</tr>
<tr>
<td>SSP1ADD</td>
<td>ADD&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>334</td>
</tr>
<tr>
<td>SSP1BUF</td>
<td>Synchronous Serial Port Receive Buffer/Transmit Register</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>285*</td>
<td></td>
</tr>
<tr>
<td>SSP1CON1</td>
<td>WCOL</td>
<td>SSPOV</td>
<td>SSPEN</td>
<td>CKP</td>
<td>SSPM&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>331</td>
</tr>
<tr>
<td>SSP1CON2</td>
<td>GCEN</td>
<td>ACKSTAT</td>
<td>ACKDT</td>
<td>ACKEN</td>
<td>RCEN</td>
<td>PEN</td>
<td>RSEN</td>
<td>SEN</td>
<td>332</td>
</tr>
<tr>
<td>SSP1CON3</td>
<td>ACKTIM</td>
<td>PCIE</td>
<td>SCIE</td>
<td>BOEN</td>
<td>SDAHT</td>
<td>SBCDE</td>
<td>AHEN</td>
<td>DHEN</td>
<td>331</td>
</tr>
<tr>
<td>SSP1MSK</td>
<td>MSK&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>334</td>
</tr>
<tr>
<td>SSP1STAT</td>
<td>SMP</td>
<td>CKE</td>
<td>D/Å</td>
<td>P</td>
<td>S</td>
<td>R/W</td>
<td>UA</td>
<td>BF</td>
<td>329</td>
</tr>
<tr>
<td>TRISC</td>
<td>TRISC7</td>
<td>TRISC6</td>
<td>TRISC5</td>
<td>TRISC4</td>
<td>TRISC3</td>
<td>TRISC2</td>
<td>TRISC1</td>
<td>TRISA0</td>
<td>142</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by the MSSP module in I²C™ mode.
* Page provides register information.

Note 1: PIC16(L)F1784/7 only.
26.7 BAUD RATE GENERATOR

The MSSP module has a Baud Rate Generator available for clock generation in both I²C and SPI Master modes. The Baud Rate Generator (BRG) reload value is placed in the SSPADD register (Register 26-6). When a write occurs to SSPBUF, the Baud Rate Generator will automatically begin counting down.

Once the given operation is complete, the internal clock will automatically stop counting and the clock pin will remain in its last state.

An internal signal “Reload” in Figure 26-39 triggers the value from SSPADD to be loaded into the BRG counter. This occurs twice for each oscillation of the module clock line. The logic dictating when the reload signal is asserted depends on the mode the MSSP is being operated in.

Table 26-4 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPADD.

EQUATION 26-1:

\[
F_{\text{clock}} = \frac{F_{\text{osc}}}{(SSP\times\text{ADD} + 1)(4)}
\]

FIGURE 26-40: BAUD RATE GENERATOR BLOCK DIAGRAM

Note: Values of 0x00, 0x01 and 0x02 are not valid for SSPADD when used as a Baud Rate Generator for I²C. This is an implementation limitation.

TABLE 26-4: MSSP CLOCK RATE W/BRG

<table>
<thead>
<tr>
<th>Fosc</th>
<th>Fcy</th>
<th>BRG Value</th>
<th>F_{\text{clock}} (2 Rollovers of BRG)</th>
</tr>
</thead>
<tbody>
<tr>
<td>32 MHz</td>
<td>8 MHz</td>
<td>13h</td>
<td>400 kHz (^{(1)})</td>
</tr>
<tr>
<td>32 MHz</td>
<td>8 MHz</td>
<td>19h</td>
<td>308 kHz</td>
</tr>
<tr>
<td>32 MHz</td>
<td>8 MHz</td>
<td>4Fh</td>
<td>100 kHz</td>
</tr>
<tr>
<td>16 MHz</td>
<td>4 MHz</td>
<td>09h</td>
<td>400 kHz (^{(1)})</td>
</tr>
<tr>
<td>16 MHz</td>
<td>4 MHz</td>
<td>0Ch</td>
<td>308 kHz</td>
</tr>
<tr>
<td>16 MHz</td>
<td>4 MHz</td>
<td>27h</td>
<td>100 kHz</td>
</tr>
<tr>
<td>4 MHz</td>
<td>1 MHz</td>
<td>09h</td>
<td>100 kHz</td>
</tr>
</tbody>
</table>

Note 1: The I²C interface does not conform to the 400 kHz I²C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.
26.8 Register Definitions: MSSP Control

REGISTER 26-1: SSPSTAT: SSP STATUS REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>SMP</th>
<th>CKE</th>
<th>D/A</th>
<th>P</th>
<th>S</th>
<th>R/W</th>
<th>UA</th>
<th>BF</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
u = Bit is unchanged
x = Bit is unknown
-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set
'0' = Bit is cleared

bit 7
**SMP**: SPI Data Input Sample bit
SPI Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
SPI Slave mode:
SPI must be cleared when SPI is used in Slave mode
In **I^2C** Master or Slave mode:
1 = Slew rate control disabled for standard speed mode (100 kHz and 1 MHz)
0 = Slew rate control enabled for high speed mode (400 kHz)

bit 6
**CKE**: SPI Clock Edge Select bit (SPI mode only)
In SPI Master or Slave mode:
1 = Transmit occurs on transition from active to Idle clock state
0 = Transmit occurs on transition from Idle to active clock state
In **I^2C** mode only:
1 = Enable input logic so that thresholds are compliant with SMBus specification
0 = Disable SMBus specific inputs

bit 5
**D/A**: Data/Address bit (**I^2C** mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4
**P**: Stop bit
(**I^2C** mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a Stop bit has been detected last (this bit is ‘0’ on Reset)
0 = Stop bit was not detected last

bit 3
**S**: Start bit
(**I^2C** mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a Start bit has been detected last (this bit is ‘0’ on Reset)
0 = Start bit was not detected last

bit 2
**R/W**: Read/Write bit information (**I^2C** mode only)
This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit, or not ACK bit.
In **I^2C** Slave mode:
1 = Read
0 = Write
In **I^2C** Master mode:
1 = Transmit is in progress
0 = Transmit is not in progress
OR-ing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSP is in Idle mode.

bit 1
**UA**: Update Address bit (10-bit **I^2C** mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated
REGISTER 26-1: SSPSTAT: SSP STATUS REGISTER (CONTINUED)

bit 0  **BF:** Buffer Full Status bit

Receive (SPI and I²C modes):
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty

Transmit (I²C mode only):
1 = Data transmit in progress (does not include the ACK and Stop bits), SSPBUF is full
0 = Data transmit complete (does not include the ACK and Stop bits), SSPBUF is empty
REGISTER 26-2:  SSPCON1: SSP CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>R/C/HS-0/0</th>
<th>R/C/HS-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>bit 6</td>
<td>bit 5</td>
<td>bit 4</td>
<td>bit 3-0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- '1' = Bit is set
- '0' = Bit is cleared
- HS = Bit is set by hardware
- C = User cleared

bit 7  WCOL: Write Collision Detect bit
- Master mode:
  - 1 = A write to the SSPBUF register was attempted while the I2C conditions were not valid for a transmission to be started
  - 0 = No collision
- Slave mode:
  - 1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
  - 0 = No collision

bit 6  SSPOV: Receive Overflow Indicator bit(1)
- In SPI mode:
  - 1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost.
    Overflow can only occur in Slave mode. In Slave mode, the user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register (must be cleared in software).
  - 0 = No overflow
- In I2C mode:
  - 1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a “don’t care” in Transmit mode (must be cleared in software).
  - 0 = No overflow

bit 5  SSPEN: Synchronous Serial Port Enable bit
- In both modes, when enabled, these pins must be properly configured as input or output
- In SPI mode:
  - 1 = Enables serial port and configures SCK, SDI, SDO and SS as the source of the serial port pins(2)
  - 0 = Disables serial port and configures these pins as I/O port pins
- In I2C mode:
  - 1 = Enables the serial port and configures the SDA and SCL pins as the source of the serial port pins(3)
  - 0 = Disables serial port and configures these pins as I/O port pins

bit 4  CKP: Clock Polarity Select bit
- In SPI mode:
  - 1 = Idle state for clock is a high level
  - 0 = Idle state for clock is a low level
- In I2C Slave mode:
  - SCL release control
    - 1 = Enable clock
    - 0 = Holds clock low (clock stretch). (Used to ensure data setup time.)
- In I2C Master mode:
  - Unused in this mode

bit 3-0 SSPM<3:0>: Synchronous Serial Port Mode Select bits
- 0000 = SPI Master mode, clock = Fosc/4
- 0001 = SPI Master mode, clock = Fosc/16
- 0010 = SPI Master mode, clock = Fosc/64
- 0011 = SPI Slave mode, clock = TMR2 output/2
- 0100 = SPI Slave mode, clock = SCK pin, SS pin control enabled
- 0101 = SPI Slave mode, clock = SCK pin, SS pin control disabled, SS can be used as I/O pin
- 0110 = I2C Slave mode, 7-bit address
- 0111 = I2C Slave mode, 10-bit address
- 1000 = I2C Master mode, clock = Fosc / (4 * (SSPADD+1))(4)
- 1001 = Reserved
- 1010 = SPI Master mode, clock = Fosc/4 * (SSPADD+1))(5)
- 1011 = I2C firmware controlled Master mode (Slave idle)
- 1100 = Reserved
- 1101 = Reserved
- 1110 = I2C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
- 1111 = I2C Slave mode, 10-bit address with Start and Stop bit interrupts enabled

Note:
1: In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.
2: When enabled, these pins must be properly configured as input or output.
3: When enabled, the SDA and SCL pins must be configured as inputs.
4: SSPADD values of 0, 1 or 2 are not supported for I2C mode.
5: SSPADD value of ‘0’ is not supported. Use SSPM = 0000 instead.
REGISTER 26-3: SSPCON2: SSP CONTROL REGISTER 2

<table>
<thead>
<tr>
<th>GCEN</th>
<th>ACKSTAT</th>
<th>ACKDT</th>
<th>ACKEN</th>
<th>RCEN</th>
<th>PEN</th>
<th>RSEN</th>
<th>SEN</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0/0</td>
<td>R-0/0</td>
<td>R/W-0/0</td>
<td>R/S/HS-0/0</td>
<td>R/S/HS-0/0</td>
<td>R/S/HS-0/0</td>
<td>R/W/HS-0/0</td>
<td>bit 7</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **HC** = Cleared by hardware
- **S** = User set

<table>
<thead>
<tr>
<th>bit 7</th>
<th>GCEN: General Call Enable bit (in I²C Slave mode only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Enable interrupt when a general call address (0x00 or 00h) is received in the SSPSR</td>
</tr>
<tr>
<td>0</td>
<td>General call address disabled</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 6</th>
<th>ACKSTAT: Acknowledge Status bit (in I²C mode only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Acknowledge was not received</td>
</tr>
<tr>
<td>0</td>
<td>Acknowledge was received</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 5</th>
<th>ACKDT: Acknowledge Data bit (in I²C mode only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>In Receive mode:</td>
<td></td>
</tr>
<tr>
<td>Value transmitted when the user initiates an Acknowledge sequence at the end of a receive</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Not Acknowledge</td>
</tr>
<tr>
<td>0</td>
<td>Acknowledge</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 4</th>
<th>ACKEN: Acknowledge Sequence Enable bit (in I²C Master mode only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>In Master Receive mode:</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Initiate Acknowledge sequence on SDA and SCL pins, and transmit ACKDT data bit. Automatically cleared by hardware.</td>
</tr>
<tr>
<td>0</td>
<td>Acknowledge sequence idle</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 3</th>
<th>RCEN: Receive Enable bit (in I²C Master mode only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Enables Receive mode for I²C</td>
</tr>
<tr>
<td>0</td>
<td>Receive idle</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 2</th>
<th>PEN: Stop Condition Enable bit (in I²C Master mode only)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SCKMSSP Release Control:</strong></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Initiate Stop condition on SDA and SCL pins. Automatically cleared by hardware.</td>
</tr>
<tr>
<td>0</td>
<td>Stop condition idle</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 1</th>
<th>RSEN: Repeated Start Condition Enable bit (in I²C Master mode only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Initiate Repeated Start condition on SDA and SCL pins. Automatically cleared by hardware.</td>
</tr>
<tr>
<td>0</td>
<td>Repeated Start condition idle</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 0</th>
<th>SEN: Start Condition Enable/Stretch Enable bit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>In Master mode:</strong></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Initiate Start condition on SDA and SCL pins. Automatically cleared by hardware.</td>
</tr>
<tr>
<td>0</td>
<td>Start condition Idle</td>
</tr>
<tr>
<td><strong>In Slave mode:</strong></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Clock stretching is enabled for both slave transmit and slave receive (stretch enabled)</td>
</tr>
<tr>
<td>0</td>
<td>Clock stretching is disabled</td>
</tr>
</tbody>
</table>

**Note 1:** For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I²C module is not in the Idle mode, this bit may not be set (no spooling) and the SSPBUF may not be written (or writes to the SSPBUF are disabled).
## REGISTER 26-4: SSPCON3: SSP CONTROL REGISTER 3

<table>
<thead>
<tr>
<th>Bit</th>
<th>Read/Write</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7   | R/W-0/0    | ACKTIM: Acknowledge Time Status bit (I^2C mode only)\(^{(3)}\)  
1 = Indicates the I^2C bus is in an Acknowledge sequence, set on 8^th falling edge of SCL clock  
0 = Not an Acknowledge sequence, cleared on 9^th rising edge of SCL clock |
| 6   | R/W-0/0    | PCIE: Stop Condition Interrupt Enable bit (I^2C mode only)  
1 = Enable interrupt on detection of Stop condition  
0 = Stop detection interrupts are disabled\(^{(2)}\) |
| 5   | R/W-0/0    | SCIE: Start Condition Interrupt Enable bit (I^2C mode only)  
1 = Enable interrupt on detection of Start or Restart conditions  
0 = Start detection interrupts are disabled\(^{(2)}\) |
| 4   | R/W-0/0    | BOEN: Buffer Overwrite Enable bit  
In SPI Slave mode:  
1 = SSPBUF updates every time that a new data byte is shifted in ignoring the BF bit  
0 = If new byte is received with BF bit of the SSPSTAT register already set, SSPOV bit of the SSPCON1 register is set, and the buffer is not updated  
In I^2C Master mode and SPI Master mode:  
This bit is ignored.  
In I^2C Slave mode:  
1 = SSPBUF is updated and ACK is generated for a received address/data byte, ignoring the state of the SSPOV bit only if the BF bit = 0.  
0 = SSPBUF is only updated when SSPOV is clear |
| 3   | R/W-0/0    | SDAHT: SDA Hold Time Selection bit (I^2C mode only)  
1 = Minimum of 300 ns hold time on SDA after the falling edge of SCL  
0 = Minimum of 100 ns hold time on SDA after the falling edge of SCL |
| 2   | R/W-0/0    | SBCDE: Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)  
If on the rising edge of SCL, SDA is sampled low when the module is outputting a high state, the BCL1IF bit of the PIR2 register is set, and bus goes idle  
1 = Enable slave bus collision interrupts  
0 = Slave bus collision interrupts are disabled |
| 1   | R/W-0/0    | AHEN: Address Hold Enable bit (I^2C Slave mode only)  
1 = Following the 8th falling edge of SCL for a matching received address byte; CKP bit of the SSPCON1 register will be cleared and the SCL will be held low.  
0 = Address holding is disabled |
| 0   | R/W-0/0    | DHEN: Data Hold Enable bit (I^2C Slave mode only)  
1 = Following the 8th falling edge of SCL for a received data byte; slave hardware clears the CKP bit of the SSPCON1 register and SCL is held low.  
0 = Data holding is disabled |

**Legend:**
- **R** = Readable bit  
- **W** = Writable bit  
- **U** = Unimplemented bit, read as ‘0’  
- **u** = Bit is unchanged  
- **x** = Bit is unknown  
- **-n/n** = Value at POR and BOR/Value at all other Resets  
- ‘1’ = Bit is set  
- ‘0’ = Bit is cleared

**Note 1:** For daisy-chained SPI operation; allows the user to ignore all but the last received byte. SSPOV is still set when a new byte is received and BF = 1, but hardware continues to write the most recent byte to SSPBUF.

**Note 2:** This bit has no effect in Slave modes that Start and Stop condition detection is explicitly listed as enabled.

**Note 3:** The ACKTIM Status bit is only active when the AHEN bit or DHEN bit is set.
REGISTER 26-5:  SSPMSK: SSP MASK REGISTER

<table>
<thead>
<tr>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
<th>R/W-1/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSK&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**bit 7-1**  
**MSK<7:1>: Mask bits**  
1 = The received address bit n is compared to SSPADD<n> to detect I^2^C address match  
0 = The received address bit n is not used to detect I^2^C address match

**bit 0**  
**MSK<0>: Mask bit for I^2^C Slave mode, 10-bit Address**  
I^2^C Slave mode, 10-bit address (SSPM<3:0> = 0111 or 1111):  
1 = The received address bit 0 is compared to SSPADD<0> to detect I^2^C address match  
0 = The received address bit 0 is not used to detect I^2^C address match  
I^2^C Slave mode, 7-bit address, the bit is ignored

REGISTER 26-6:  SSPADD: MSSP ADDRESS AND BAUD RATE REGISTER (I^2^C MODE)

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **-n/n** = Value at POR and BOR/Value at all other Resets

**Master mode:**

**bit 7-0**  
**ADD<7:0>: Baud Rate Clock Divider bits**  
SCL pin clock period = ((ADD<7:0> + 1) * 4)/Fosc

**10-Bit Slave mode — Most Significant Address Byte:**

**bit 7-3**  
**Not used:** Unused for Most Significant Address byte. Bit state of this register is a “don’t care”. Bit pattern sent by master is fixed by I^2^C specification and must be equal to ‘11110’. However, those bits are compared by hardware and are not affected by the value in this register.

**bit 2-1**  
**ADD<2:1>: Two Most Significant bits of 10-bit address**

**bit 0**  
**Not used:** Unused in this mode. Bit state is a “don’t care”.

**10-Bit Slave mode — Least Significant Address Byte:**

**bit 7-0**  
**ADD<7:0>: Eight Least Significant bits of 10-bit address**

**7-Bit Slave mode:**

**bit 7-1**  
**ADD<7:1>: 7-bit address**

**bit 0**  
**Not used:** Unused in this mode. Bit state is a “don’t care”.
27.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The EUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The EUSART module includes the following capabilities:
- Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- Programmable 8-bit or 9-bit character length
- Address detection in 9-bit mode
- Input buffer overrun error detection
- Received character framing error detection
- Half-duplex synchronous master
- Half-duplex synchronous slave
- Programmable clock polarity in synchronous modes
- Sleep operation

The EUSART module implements the following additional features, making it ideally suited for use in Local Interconnect Network (LIN) bus systems:
- Automatic detection and calibration of the baud rate
- Wake-up on Break reception
- 13-bit Break character transmit

Block diagrams of the EUSART transmitter and receiver are shown in Figure 27-1 and Figure 27-2.
The operation of the EUSART module is controlled through three registers:

- **Transmit Status and Control (TXSTA)**
- **Receive Status and Control (RCSTA)**
- **Baud Rate Control (BAUDCON)**

These registers are detailed in **Register 27-1, Register 27-2 and Register 27-3**, respectively.

When the receiver or transmitter section is not enabled then the corresponding RX or TX pin may be used for general purpose input and output.
27.1 EUSART Asynchronous Mode

The EUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a VOH mark state which represents a '1' data bit, and a VOL space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the Mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is 8 bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit/16-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. See Table 27-5 for examples of baud rate configurations.

The EUSART transmits and receives the LSB first. The EUSART’s transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

27.1.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 27-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXREG register.

27.1.1.1 Enabling the Transmitter

The EUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXSTA register enables the transmitter circuitry of the EUSART. Clearing the SYNC bit of the TXSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the EUSART and automatically configures the TX/CK I/O pin as an output. If the TX/CK pin is shared with an analog peripheral, the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

Note: The TXIF Transmitter Interrupt flag is set when the TXEN enable bit is set.

27.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXREG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXREG until the Stop bit of the previous character has been transmitted. The pending character in the TXREG is then transferred to the TSR in one Tcy immediately following the Stop bit transmission. The transmission of the Start bit, data bits and Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXREG.

27.1.3 Transmit Data Polarity

The polarity of the transmit data can be controlled with the SCKP bit of the BAUDxCON register. The default state of this bit is '0' which selects high true transmit idle and data bits. Setting the SCKP bit to '1' will invert the transmit data resulting in low true idle and data bits. The SCKP bit controls transmit data polarity in Asynchronous mode only. In Synchronous mode, the SCKP bit has a different function. See Section 27.5.1.2 “Clock Polarity”.

27.1.4 Transmit Interrupt Flag

The TXIF interrupt flag bit of the PIR1 register is set whenever the EUSART transmitter is enabled and no character is being held for transmission in the TXREG. In other words, the TXIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXREG. The TXIF flag bit is not cleared immediately upon writing TXREG. TXIF becomes valid in the second instruction cycle following the write execution. Polling TXIF immediately following the TXREG write will return invalid results. The TXIF bit is read-only, it cannot be set or cleared by software.

The TXIF interrupt can be enabled by setting the TXIE interrupt enable bit of the PIE1 register. However, the TXIF flag bit will be set whenever the TXREG is empty, regardless of the state of TXIE enable bit.

To use interrupts when transmitting data, set the TXIE bit only when there is more data to send. Clear the TXIE interrupt enable bit upon writing the last character of the transmission to the TXREG.
27.1.1.5 TSR Status
The TRMT bit of the TXSTA register indicates the status of the TSR register. This is a read-only bit. The TRMT bit is set when the TSR register is empty and is cleared when a character is transferred to the TSR register from the TXREG. The TRMT bit remains clear until all bits have been shifted out of the TSR register. No interrupt logic is tied to this bit, so the user has to poll this bit to determine the TSR status.

Note: The TSR register is not mapped in data memory, so it is not available to the user.

27.1.1.6 Transmitting 9-Bit Characters
The EUSART supports 9-bit character transmissions. When the TX9 bit of the TXSTA register is set, the EUSART will shift nine bits out for each character transmitted. The TX9D bit of the TXSTA register is the ninth, and Most Significant, data bit. When transmitting 9-bit data, the TX9D data bit must be written before writing the eight Least Significant data bits into the TXREG. All nine bits of data will be transferred to the TSR shift register immediately after the TXREG is written.

A special 9-bit Address mode is available for use with multiple receivers. See Section 27.1.2.7 “Address Detection” for more information on the address mode.

27.1.1.7 Asynchronous Transmission Set-up:
1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 27.4 “EUSART Baud Rate Generator (BRG)”).
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If 9-bit transmission is desired, set the TX9 control bit. A set ninth data bit will indicate that the eight Least Significant data bits are an address when the receiver is set for address detection.
4. Set SCKP bit if inverted transmit is desired.
5. Enable the transmission by setting the TXEN control bit. This will cause the TXIF interrupt bit to be set.
6. If interrupts are desired, set the TXIE interrupt enable bit of the PIE1 register. An interrupt will occur immediately provided that the GIE and PEIE bits of the INTCON register are also set.
7. If 9-bit transmission is selected, the ninth bit should be loaded into the TX9D data bit.
8. Load 8-bit data into the TXREG register. This will start the transmission.
FIGURE 27-4: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)

Table 27-1: Summary of Registers Associated with Asynchronous Transmission

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>APFCON1</td>
<td>C2OUTSEL</td>
<td>CC1PSEL</td>
<td>SDOSEL</td>
<td>SCKSEL</td>
<td>SDISEL</td>
<td>TXSEL</td>
<td>RXSEL</td>
<td>CCP2SEL</td>
<td>127</td>
</tr>
<tr>
<td>BAUDCON</td>
<td>ABDOVF</td>
<td>RCIDL</td>
<td>—</td>
<td>SCKP</td>
<td>BRG16</td>
<td>—</td>
<td>WUE</td>
<td>ABDEN</td>
<td>347</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IO CIF</td>
<td>93</td>
</tr>
<tr>
<td>PIE1</td>
<td>TMR1GIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSP1IE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>94</td>
</tr>
<tr>
<td>PIR1</td>
<td>TMR1 GIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1IF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>98</td>
</tr>
<tr>
<td>RCSTA</td>
<td>SPEN</td>
<td>RX9</td>
<td>SREN</td>
<td>CREN</td>
<td>ADDEN</td>
<td>FERR</td>
<td>OERR</td>
<td>RX9D</td>
<td>346</td>
</tr>
<tr>
<td>SPBRGL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BRG&lt;7:0&gt;</td>
<td></td>
<td></td>
<td>348</td>
</tr>
<tr>
<td>SPBRGH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BRG&lt;15:8&gt;</td>
<td></td>
<td></td>
<td>348</td>
</tr>
<tr>
<td>TRISC</td>
<td>TRISC7</td>
<td>TRISC6</td>
<td>TRISC5</td>
<td>TRISC4</td>
<td>TRISC3</td>
<td>TRISC2</td>
<td>TRISC1</td>
<td>TRISC0</td>
<td>142</td>
</tr>
<tr>
<td>TXREG</td>
<td>EUSART Transmit Data Register</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>337*</td>
</tr>
<tr>
<td>TXSTA</td>
<td>CSRC</td>
<td>TX9</td>
<td>TXEN</td>
<td>SYNC</td>
<td>SENDB</td>
<td>BRGH</td>
<td>TRMT</td>
<td>TX9D</td>
<td>345</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used for asynchronous transmission.
* Page provides register information.
27.1.2 EUSART ASYNCHRONOUS RECEIVER

The Asynchronous mode is typically used in RS-232 systems. The receiver block diagram is shown in Figure 27-2. The data is received on the RX/DT pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at 16 times the baud rate, whereas the serial Receive Shift Register (RSR) operates at the bit rate. When all 8 or 9 bits of the character have been shifted in, they are immediately transferred to a two character First-In-First-Out (FIFO) memory. The FIFO buffering allows reception of two complete characters and the start of a third character before software must start servicing the EUSART receiver. The FIFO and RSR registers are not directly accessible by software. Access to the received data is via the RCREG register.

27.1.2.1 Enabling the Receiver

The EUSART receiver is enabled for asynchronous operation by configuring the following three control bits:

- CREN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the CREN bit of the RCSTA register enables the receiver circuitry of the EUSART. Clearing the SYNC bit of the TXSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the EUSART. The programmer must set the corresponding TRIS bit to configure the RX/DT I/O pin as an input.

27.1.2.2 Receiving Data

The receiver data recovery circuit initiates character reception on the falling edge of the first bit. The first bit, also known as the Start bit, is always a zero. The data recovery circuit counts one-half bit time to the center of the Start bit and verifies that the bit is still a zero. If it is not a zero then the data recovery circuit aborts character reception, without generating an error, and resumes looking for the falling edge of the Start bit. If the Start bit zero verification succeeds then the data recovery circuit counts a full bit time to the center of the next bit. The bit is then sampled by a majority detect circuit and the resulting ‘0’ or ‘1’ is shifted into the RSR.

This repeats until all data bits have been sampled and shifted into the RSR. One final bit time is measured and the level sampled. This is the Stop bit, which is always a ‘1’. If the data recovery circuit samples a ‘0’ in the Stop bit position then a framing error is set for this character, otherwise the framing error is cleared for this character. See Section 27.1.2.4 “Receive Framing Error” for more information on framing errors.

Immediately after all data bits and the Stop bit have been received, the character in the RSR is transferred to the EUSART receive FIFO and the RCIF interrupt flag bit of the PIR1 register is set. The top character in the FIFO is transferred out of the FIFO by reading the RCREG register.

27.1.2.3 Receive Interrupts

The RCIF interrupt flag bit of the PIR1 register is set whenever the EUSART receiver is enabled and there is an unread character in the receive FIFO. The RCIF interrupt flag bit is read-only, it cannot be set or cleared by software.

RCIF interrupts are enabled by setting all of the following bits:

- RCIE, Interrupt Enable bit of the PIE1 register
- PEIE, Peripheral Interrupt Enable bit of the INTCON register
- GIE, Global Interrupt Enable bit of the INTCON register

The RCIF interrupt flag bit will be set when there is an unread character in the FIFO, regardless of the state of interrupt enable bits.
27.1.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCSTA register which resets the EUSART. Clearing the CREN bit of the RCSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

Note: If all receive characters in the receive FIFO have framing errors, repeated reads of the RCREG will not clear the FERR bit.

27.1.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCSTA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCSTA register or by resetting the EUSART by clearing the SPEN bit of the RCSTA register.

27.1.2.6 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift 9 bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

27.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.
27.1.2.8 Asynchronous Reception Set-up:
1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 27.4 “EUSART Baud Rate Generator (BRG)”).
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
5. If 9-bit reception is desired, set the RX9 bit.
6. Enable reception by setting the CREN bit.
7. The RCIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
8. Read the RCSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
9. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register.
10. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

27.1.2.9 9-bit Address Detection Mode Set-up
This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:
1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 27.4 “EUSART Baud Rate Generator (BRG)”)
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
5. Enable 9-bit reception by setting the RX9 bit.
6. Enable address detection by setting the ADDEN bit.
7. Enable reception by setting the CREN bit.
8. The RCIF interrupt flag bit will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
9. Read the RCSTA register to get the error flags. The ninth data bit will always be set.
10. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register. Software determines if this is the device’s address.
11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
12. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.

**FIGURE 27-5:** ASYNCHRONOUS RECEPTION

Note: This timing diagram shows three words appearing on the RX input. The RCREG (receive buffer) is read after the third word, causing the OERR (overrun) bit to be set.
<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>APFCON1</td>
<td>C2OUTSEL</td>
<td>CC1PSEL</td>
<td>SDOSEL</td>
<td>SCKSEL</td>
<td>SDISEL</td>
<td>TXSEL</td>
<td>RXSEL</td>
<td>CCP2SEL</td>
<td>127</td>
</tr>
<tr>
<td>BAUDCON</td>
<td>ABDOVF</td>
<td>RCIDL</td>
<td>—</td>
<td>SCKP</td>
<td>BRG16</td>
<td>—</td>
<td>WUE</td>
<td>ABDEN</td>
<td>347</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>93</td>
</tr>
<tr>
<td>PIE1</td>
<td>TMR1GIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSP1IE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>94</td>
</tr>
<tr>
<td>PIR1</td>
<td>TMR1GIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1IF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>98</td>
</tr>
<tr>
<td>RCREG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>EUSART Receive Data Register</td>
</tr>
<tr>
<td>RCSTA</td>
<td>SPEN</td>
<td>RX9</td>
<td>SREN</td>
<td>CREN</td>
<td>ADDEN</td>
<td>FERR</td>
<td>OERR</td>
<td>RX9D</td>
<td>346</td>
</tr>
<tr>
<td>SPBRGL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BRG&lt;7:0&gt;</td>
<td></td>
<td></td>
<td>348</td>
</tr>
<tr>
<td>SPBRGH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BRG&lt;15:8&gt;</td>
<td></td>
<td></td>
<td>348</td>
</tr>
<tr>
<td>TRISC</td>
<td>TRISC7</td>
<td>TRISC6</td>
<td>TRISC5</td>
<td>TRISC4</td>
<td>TRISC3</td>
<td>TRISC2</td>
<td>TRISC1</td>
<td>TRISC0</td>
<td>142</td>
</tr>
<tr>
<td>TXSTA</td>
<td>CSRC</td>
<td>TX9</td>
<td>TXEN</td>
<td>SYNC</td>
<td>SENDB</td>
<td>BRGH</td>
<td>TRMT</td>
<td>TX9D</td>
<td>345</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as “0”. Shaded cells are not used for asynchronous reception.
* Page provides register information.
27.2 Clock Accuracy with Asynchronous Operation

The factory calibrates the internal oscillator block output (INTOSC). However, the INTOSC frequency may drift as VDD or temperature changes, and this directly affects the asynchronous baud rate. Two methods may be used to adjust the baud rate clock, but both require a reference clock source of some kind.

The first (preferred) method uses the OSCTUNE register to adjust the INTOSC output. Adjusting the value in the OSCTUNE register allows for fine resolution changes to the system clock source. See Section 6.2.2 “Internal Clock Sources” for more information.

The other method adjusts the value in the Baud Rate Generator. This can be done automatically with the Auto-Baud Detect feature (see Section 27.4.1 “Auto-Baud Detect”). There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change in the peripheral clock frequency.
27.3 Register Definitions: EUSART Control

REGISTER 27-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R-1/1</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSRC</td>
<td>TX9</td>
<td>TXEN(1)</td>
<td>SYNC</td>
<td>SENDB</td>
<td>BRGH</td>
<td>TRMT</td>
<td>TX9D</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit     W = Writable bit     U = Unimplemented bit, read as ‘0’
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set      ‘0’ = Bit is cleared

bit 7      CSRC: Clock Source Select bit
Asynchronous mode:
Don’t care
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)
bit 6      TX9: 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission
bit 5      TXEN: Transmit Enable bit(1)
1 = Transmit enabled
0 = Transmit disabled
bit 4      SYNC: EUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode
bit 3      SENDB: Send Break Character bit
Asynchronous mode:
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed
Synchronous mode:
Don’t care
bit 2      BRGH: High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode
bit 1      TRMT: Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full
bit 0      TX9D: Ninth bit of Transmit Data
Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Sync mode.
**REGISTER 27-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER**

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPEN</td>
<td>RX9</td>
<td>SREN</td>
<td>CREN</td>
<td>ADDEN</td>
<td>FERR</td>
<td>OERR</td>
<td>RX9D</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Legend:</th>
</tr>
</thead>
<tbody>
<tr>
<td>R = Readable bit</td>
</tr>
<tr>
<td>u = Bit is unchanged</td>
</tr>
<tr>
<td>‘1’ = Bit is set</td>
</tr>
</tbody>
</table>

- **bit 7 SPEN:** Serial Port Enable bit
  - 1 = Serial port enabled (configures RX/DT and TX/CK pins as serial port pins)
  - 0 = Serial port disabled (held in Reset)

- **bit 6 RX9:** 9-bit Receive Enable bit
  - 1 = Selects 9-bit reception
  - 0 = Selects 8-bit reception

- **bit 5 SREN:** Single Receive Enable bit
  - Asynchronous mode:
    - Don’t care
  - Synchronous mode – Master:
    - 1 = Enables single receive
    - 0 = Disables single receive
    - This bit is cleared after reception is complete.
  - Synchronous mode – Slave:
    - Don’t care

- **bit 4 CREN:** Continuous Receive Enable bit
  - Asynchronous mode:
    - 1 = Enables receiver
    - 0 = Disables receiver
  - Synchronous mode:
    - 1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
    - 0 = Disables continuous receive

- **bit 3 ADDEN:** Address Detect Enable bit
  - Asynchronous mode 9-bit (RX9 = 1):
    - 1 = Enables address detection, enable interrupt and load the receive buffer when RSR<8> is set
    - 0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit
  - Asynchronous mode 8-bit (RX9 = 0):
    - Don’t care

- **bit 2 FERR:** Framing Error bit
  - 1 = Framing error (can be updated by reading RCREG register and receive next valid byte)
  - 0 = No framing error

- **bit 1 OERR:** Overrun Error bit
  - 1 = Overrun error (can be cleared by clearing bit CREN)
  - 0 = No overrun error

- **bit 0 RX9D:** Ninth bit of Received Data
  - This can be address/data bit or a parity bit and must be calculated by user firmware.
REGISTER 27-3: BAUDCON: BAUD RATE CONTROL REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABDOVF</td>
<td>RCIDL</td>
<td>—</td>
<td>SCKP</td>
<td>BRG16</td>
<td>—</td>
<td>WUE</td>
<td>ABDEN</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W =Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7**  
**ABDOVF**: Auto-Baud Detect Overflow bit  
Asynchronous mode:  
1 = Auto-baud timer overflowed  
0 = Auto-baud timer did not overflow  
Synchronous mode:  
Don’t care

**bit 6**  
**RCIDL**: Receive Idle Flag bit  
Asynchronous mode:  
1 = Receiver is idle  
0 = Start bit has been received and the receiver is receiving  
Synchronous mode:  
Don’t care

**bit 5**  
**Unimplemented**: Read as ‘0’

**bit 4**  
**SCKP**: Synchronous Clock Polarity Select bit  
Asynchronous mode:  
1 = Transmit inverted data to the TX/CK pin  
0 = Transmit non-inverted data to the TX/CK pin  
Synchronous mode:  
1 = Data is clocked on rising edge of the clock  
0 = Data is clocked on falling edge of the clock

**bit 3**  
**BRG16**: 16-bit Baud Rate Generator bit  
1 = 16-bit Baud Rate Generator is used  
0 = 8-bit Baud Rate Generator is used

**bit 2**  
**Unimplemented**: Read as ‘0’

**bit 1**  
**WUE**: Wake-up Enable bit  
Asynchronous mode:  
1 = Receiver is waiting for a falling edge. No character will be received, byte RCIF will be set. WUE will automatically clear after RCIF is set.  
0 = Receiver is operating normally  
Synchronous mode:  
Don’t care

**bit 0**  
**ABDEN**: Auto-Baud Detect Enable bit  
Asynchronous mode:  
1 = Auto-Baud Detect mode is enabled (clears when auto-baud is complete)  
0 = Auto-Baud Detect mode is disabled  
Synchronous mode:  
Don’t care
27.4 EUSART Baud Rate Generator (BRG)

The Baud Rate Generator (BRG) is an 8-bit or 16-bit timer that is dedicated to the support of both the asynchronous and synchronous EUSART operation. By default, the BRG operates in 8-bit mode. Setting the BRG16 bit of the BAUDCON register selects 16-bit mode.

The SPBRGH, SPBRGL register pair determines the period of the free running baud rate timer. In Asynchronous mode the multiplier of the baud rate period is determined by both the BRGH bit of the TXSTA register and the BRG16 bit of the BAUDCON register. In Synchronous mode, the BRGH bit is ignored.

Table 27-3 contains the formulas for determining the baud rate. Example 27-1 provides a sample calculation for determining the baud rate and baud rate error.

Typical baud rates and error values for various asynchronous modes have been computed for your convenience and are shown in Table 27-3. It may be advantageous to use the high baud rate (BRGH = 1), or the 16-bit BRG (BRG16 = 1) to reduce the baud rate error. The 16-bit BRG mode is used to achieve slow baud rates for fast oscillator frequencies.

Writing a new value to the SPBRGH, SPBRGL register pair causes the BRG timer to be reset (or cleared). This ensures that the BRG does not wait for a timer overflow before outputting the new baud rate.

If the system clock is changed during an active receive operation, a receive error or data loss may result. To avoid this problem, check the status of the RCIDL bit to make sure that the receive operation is idle before changing the system clock.

---

**EXAMPLE 27-1: CALCULATING BAUD RATE ERROR**

For a device with Fosc of 16 MHz, desired baud rate of 9600, Asynchronous mode, 8-bit BRG:

\[
\text{Desired Baud Rate} = \frac{\text{Fosc}}{64(\text{SPBRGH:SPBRGL}) + 1}
\]

Solving for SPBRGH:SPBRGL:

\[
X = \frac{\text{Fosc}}{\text{Desired Baud Rate}} - 1
\]

\[
= \frac{16000000}{9600} - 1
\]

\[
= [25.042] = 25
\]

**Calculated Baud Rate**

\[
= \frac{16000000}{64(25 + 1)}
\]

\[
= 9615
\]

**Error**

\[
= \frac{\text{Calc. Baud Rate} - \text{Desired Baud Rate}}{\text{Desired Baud Rate}}
\]

\[
= \frac{(9615 - 9600)}{9600} = 0.16\%
\]
### TABLE 27-3: BAUD RATE FORMULAS

<table>
<thead>
<tr>
<th>Configuration Bits</th>
<th>BRG/EUSART Mode</th>
<th>Baud Rate Formula</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sync</td>
<td>BRG&lt;15:8&gt;</td>
<td>BRG&lt;7:0&gt;</td>
</tr>
<tr>
<td>000</td>
<td>8-bit/Asynchronous</td>
<td>Fosc/64 (n+1)</td>
</tr>
<tr>
<td>001</td>
<td>8-bit/Asynchronous</td>
<td>Fosc/16 (n+1)</td>
</tr>
<tr>
<td>010</td>
<td>16-bit/Asynchronous</td>
<td></td>
</tr>
<tr>
<td>011</td>
<td>16-bit/Asynchronous</td>
<td>Fosc/4 (n+1)</td>
</tr>
<tr>
<td>10x</td>
<td>8-bit/Synchronous</td>
<td></td>
</tr>
<tr>
<td>11x</td>
<td>16-bit/Synchronous</td>
<td></td>
</tr>
</tbody>
</table>

Legend:  
- x = Don’t care, n = value of SPBRGH, SPBRGL register pair

### TABLE 27-4: SUMMARY OF REGISTERS ASSOCIATED WITH THE BAUD RATE GENERATOR

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>BAUDCON</td>
<td>ABDOVF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>347</td>
</tr>
<tr>
<td>RCSTA</td>
<td>SPEN</td>
<td>RX9</td>
<td>SREN</td>
<td>CREN</td>
<td>ADDEN</td>
<td>FERR</td>
<td>OERR</td>
<td>RX9D</td>
<td>346</td>
</tr>
<tr>
<td>SPBRGL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>348</td>
</tr>
<tr>
<td>SPBRGH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>348</td>
</tr>
<tr>
<td>TXSTA</td>
<td>CSRC</td>
<td>TX9</td>
<td>TXEN</td>
<td>SYNC</td>
<td>SENDB</td>
<td>BRGH</td>
<td>TRMT</td>
<td>TX9D</td>
<td>345</td>
</tr>
</tbody>
</table>

Legend:  
- — = unimplemented location, read as ‘0’. Shaded cells are not used for the Baud Rate Generator.  
* Page provides register information.
### TABLE 27-5: BAUD RATES FOR ASYNCHRONOUS MODES

#### SYNC = 0, BRGH = 0, BRG16 = 0

<table>
<thead>
<tr>
<th>BAUD RATE</th>
<th>Fosc = 32.000 MHz</th>
<th>Fosc = 20.000 MHz</th>
<th>Fosc = 18.432 MHz</th>
<th>Fosc = 11.0592 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Actual Rate</td>
<td>% Error</td>
<td>SPBRG value (decimal)</td>
<td>Actual Rate</td>
</tr>
<tr>
<td>300</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>1200</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1200</td>
</tr>
<tr>
<td>2400</td>
<td>2404</td>
<td>0.16</td>
<td>207</td>
<td>2404</td>
</tr>
<tr>
<td>9600</td>
<td>9615</td>
<td>0.16</td>
<td>51</td>
<td>9470</td>
</tr>
<tr>
<td>10417</td>
<td>10417</td>
<td>0.00</td>
<td>47</td>
<td>10417</td>
</tr>
<tr>
<td>19.2k</td>
<td>19.23k</td>
<td>0.16</td>
<td>25</td>
<td>19.53k</td>
</tr>
<tr>
<td>57.6k</td>
<td>55.55k</td>
<td>-3.55</td>
<td>3</td>
<td>57.60k</td>
</tr>
<tr>
<td>115.2k</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

#### SYNC = 0, BRGH = 1, BRG16 = 0

<table>
<thead>
<tr>
<th>BAUD RATE</th>
<th>Fosc = 8.000 MHz</th>
<th>Fosc = 4.000 MHz</th>
<th>Fosc = 3.6864 MHz</th>
<th>Fosc = 1.000 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Actual Rate</td>
<td>% Error</td>
<td>SPBRG value (decimal)</td>
<td>Actual Rate</td>
</tr>
<tr>
<td>300</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>300</td>
</tr>
<tr>
<td>1200</td>
<td>1202</td>
<td>0.16</td>
<td>103</td>
<td>1202</td>
</tr>
<tr>
<td>2400</td>
<td>2404</td>
<td>0.16</td>
<td>51</td>
<td>2404</td>
</tr>
<tr>
<td>9600</td>
<td>9615</td>
<td>0.16</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>10417</td>
<td>10417</td>
<td>0.00</td>
<td>11</td>
<td>10417</td>
</tr>
<tr>
<td>19.2k</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>57.6k</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>115.2k</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

#### SYNC = 0, BRGH = 0, BRG16 = 1

<table>
<thead>
<tr>
<th>BAUD RATE</th>
<th>Fosc = 32.000 MHz</th>
<th>Fosc = 20.000 MHz</th>
<th>Fosc = 18.432 MHz</th>
<th>Fosc = 11.0592 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Actual Rate</td>
<td>% Error</td>
<td>SPBRG value (decimal)</td>
<td>Actual Rate</td>
</tr>
<tr>
<td>300</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>1200</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>2400</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>9600</td>
<td>9615</td>
<td>0.16</td>
<td>207</td>
<td>9615</td>
</tr>
<tr>
<td>10417</td>
<td>10417</td>
<td>0.00</td>
<td>191</td>
<td>10417</td>
</tr>
<tr>
<td>19.2k</td>
<td>19.23k</td>
<td>0.16</td>
<td>103</td>
<td>19.23k</td>
</tr>
<tr>
<td>57.6k</td>
<td>57.14k</td>
<td>-0.79</td>
<td>34</td>
<td>56.82k</td>
</tr>
<tr>
<td>115.2k</td>
<td>117.64k</td>
<td>2.12</td>
<td>16</td>
<td>113.64k</td>
</tr>
</tbody>
</table>
### TABLE 27-5: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

#### BAUD RATE

<table>
<thead>
<tr>
<th>BAUD RATE</th>
<th>Fosc = 8.000 MHz</th>
<th>Fosc = 4.000 MHz</th>
<th>Fosc = 3.6864 MHz</th>
<th>Fosc = 1.000 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Actual Rate</td>
<td>% Error</td>
<td>SPBRG value</td>
<td>Actual Rate</td>
</tr>
<tr>
<td>300</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>300</td>
</tr>
<tr>
<td>1200</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1202</td>
</tr>
<tr>
<td>2400</td>
<td>2404</td>
<td>0.16</td>
<td>207</td>
<td>2404</td>
</tr>
<tr>
<td>9600</td>
<td>9615</td>
<td>0.16</td>
<td>51</td>
<td>9615</td>
</tr>
<tr>
<td>10417</td>
<td>10417</td>
<td>0.00</td>
<td>47</td>
<td>10417</td>
</tr>
<tr>
<td>19.2k</td>
<td>19.23k</td>
<td>0.16</td>
<td>12</td>
<td>19.2k</td>
</tr>
<tr>
<td>57.6k</td>
<td>55556</td>
<td>-3.55</td>
<td>8</td>
<td>—</td>
</tr>
<tr>
<td>115.2k</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>115.2k</td>
</tr>
</tbody>
</table>

#### SYNC = 0, BRGH = 0, BRG16 = 1

<table>
<thead>
<tr>
<th>BAUD RATE</th>
<th>Fosc = 32.000 MHz</th>
<th>Fosc = 20.000 MHz</th>
<th>Fosc = 18.432 MHz</th>
<th>Fosc = 11.0592 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Actual Rate</td>
<td>% Error</td>
<td>SPBRG value</td>
<td>Actual Rate</td>
</tr>
<tr>
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<td>300.0</td>
<td>0.00</td>
<td>6666</td>
<td>300.0</td>
</tr>
<tr>
<td>1200</td>
<td>1200</td>
<td>-0.02</td>
<td>3332</td>
<td>1200</td>
</tr>
<tr>
<td>2400</td>
<td>2401</td>
<td>-0.04</td>
<td>832</td>
<td>2399</td>
</tr>
<tr>
<td>9600</td>
<td>9615</td>
<td>0.16</td>
<td>207</td>
<td>9615</td>
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<tr>
<td>10417</td>
<td>10417</td>
<td>0.00</td>
<td>191</td>
<td>10417</td>
</tr>
<tr>
<td>19.2k</td>
<td>19.23k</td>
<td>0.16</td>
<td>103</td>
<td>19.23k</td>
</tr>
<tr>
<td>57.6k</td>
<td>57.14k</td>
<td>-0.79</td>
<td>34</td>
<td>56.818</td>
</tr>
<tr>
<td>115.2k</td>
<td>117.6k</td>
<td>2.12</td>
<td>16</td>
<td>113.636</td>
</tr>
</tbody>
</table>

#### SYNC = 0, BRGH = 1, BRG16 = 0

<table>
<thead>
<tr>
<th>BAUD RATE</th>
<th>Fosc = 8.000 MHz</th>
<th>Fosc = 4.000 MHz</th>
<th>Fosc = 3.6864 MHz</th>
<th>Fosc = 1.000 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Actual Rate</td>
<td>% Error</td>
<td>SPBRG value</td>
<td>Actual Rate</td>
</tr>
<tr>
<td>300</td>
<td>299.9</td>
<td>-0.02</td>
<td>1666</td>
<td>300.1</td>
</tr>
<tr>
<td>1200</td>
<td>1199</td>
<td>-0.08</td>
<td>416</td>
<td>1202</td>
</tr>
<tr>
<td>2400</td>
<td>2404</td>
<td>0.16</td>
<td>207</td>
<td>2404</td>
</tr>
<tr>
<td>9600</td>
<td>9615</td>
<td>0.16</td>
<td>51</td>
<td>9615</td>
</tr>
<tr>
<td>10417</td>
<td>10417</td>
<td>0.00</td>
<td>47</td>
<td>10417</td>
</tr>
<tr>
<td>19.2k</td>
<td>19.23k</td>
<td>0.16</td>
<td>25</td>
<td>19.23k</td>
</tr>
<tr>
<td>57.6k</td>
<td>55556</td>
<td>-3.55</td>
<td>8</td>
<td>—</td>
</tr>
<tr>
<td>115.2k</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>
### TABLE 27-5: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

<table>
<thead>
<tr>
<th>BAUD RATE</th>
<th>( F_{OSC} = 32.000 \text{ MHz} )</th>
<th>( F_{OSC} = 20.000 \text{ MHz} )</th>
<th>( F_{OSC} = 18.432 \text{ MHz} )</th>
<th>( F_{OSC} = 11.0592 \text{ MHz} )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Actual Rate</td>
<td>% Error</td>
<td>SPBRG value (decimal)</td>
<td>Actual Rate</td>
</tr>
<tr>
<td>300</td>
<td>300.0</td>
<td>0.00</td>
<td>26666</td>
<td>300.0</td>
</tr>
<tr>
<td>1200</td>
<td>1200</td>
<td>0.00</td>
<td>6666</td>
<td>1200</td>
</tr>
<tr>
<td>2400</td>
<td>2400</td>
<td>0.01</td>
<td>3332</td>
<td>2400</td>
</tr>
<tr>
<td>9600</td>
<td>9604</td>
<td>0.04</td>
<td>832</td>
<td>9597</td>
</tr>
<tr>
<td>10417</td>
<td>10417</td>
<td>0.00</td>
<td>767</td>
<td>10417</td>
</tr>
<tr>
<td>19.2k</td>
<td>19.18k</td>
<td>-0.08</td>
<td>416</td>
<td>19.23k</td>
</tr>
<tr>
<td>57.6k</td>
<td>57.55k</td>
<td>-0.08</td>
<td>138</td>
<td>57.47k</td>
</tr>
<tr>
<td>115.2k</td>
<td>115.9k</td>
<td>0.64</td>
<td>68</td>
<td>116.3k</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>BAUD RATE</th>
<th>( F_{OSC} = 8.000 \text{ MHz} )</th>
<th>( F_{OSC} = 4.000 \text{ MHz} )</th>
<th>( F_{OSC} = 3.6864 \text{ MHz} )</th>
<th>( F_{OSC} = 1.000 \text{ MHz} )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Actual Rate</td>
<td>% Error</td>
<td>SPBRG value (decimal)</td>
<td>Actual Rate</td>
</tr>
<tr>
<td>300</td>
<td>300.0</td>
<td>0.00</td>
<td>6666</td>
<td>300.0</td>
</tr>
<tr>
<td>1200</td>
<td>1200</td>
<td>-0.02</td>
<td>1666</td>
<td>1200</td>
</tr>
<tr>
<td>2400</td>
<td>2401</td>
<td>0.04</td>
<td>832</td>
<td>2398</td>
</tr>
<tr>
<td>9600</td>
<td>9615</td>
<td>0.16</td>
<td>207</td>
<td>9615</td>
</tr>
<tr>
<td>10417</td>
<td>10417</td>
<td>0</td>
<td>191</td>
<td>10417</td>
</tr>
<tr>
<td>19.2k</td>
<td>19.23k</td>
<td>0.16</td>
<td>103</td>
<td>19.23k</td>
</tr>
<tr>
<td>57.6k</td>
<td>57.14k</td>
<td>-0.79</td>
<td>34</td>
<td>58.82k</td>
</tr>
<tr>
<td>115.2k</td>
<td>117.6k</td>
<td>2.12</td>
<td>16</td>
<td>111.1k</td>
</tr>
</tbody>
</table>
27.4.1 AUTO-BAUD DETECT

The EUSART module supports automatic detection and calibration of the baud rate.

In the Auto-Baud Detect (ABD) mode, the clock to the BRG is reversed. Rather than the BRG clocking the incoming RX signal, the RX signal is timing the BRG. The Baud Rate Generator is used to time the period of a received 55h (ASCII “U”) which is the Sync character for the LIN bus. The unique feature of this character is that it has five rising edges including the Stop bit edge.

Setting the ABDEN bit of the BAUDCON register starts the auto-baud calibration sequence (Figure 27-6). While the ABD sequence takes place, the EUSART state machine is held in idle. On the first rising edge of the receive line, after the Start bit, the SPBRG begins counting up using the BRG counter clock as shown in Table 27-6. The fifth rising edge will occur on the RX pin at the end of the eighth bit period. At that time, an accumulated value totaling the proper BRG period is left in the SPBRGH, SPBRGL register pair, the ABDEN bit is automatically cleared and the RCIF interrupt flag is set. The value in the RCREG needs to be read to clear the RCIF interrupt. RCREG content should be discarded. When calibrating for modes that do not use the SPBRGH register the user can verify that the SPBRGL register did not overflow by checking for 00h in the SPBRGL register.

The BRG auto-baud clock is determined by the BRG16 and BRGH bits as shown in Table 27-6. During ABD, both the SPBRGH and SPBRGL registers are used as a 16-bit counter, independent of the BRG16 bit setting. While calibrating the baud rate period, the SPBRGH and SPBRGL registers are clocked at 1/8th the BRG base clock rate. The resulting byte measurement is the average bit time when clocked at full speed.

Note 1: If the WUE bit is set with the ABDEN bit, auto-baud detection will occur on the byte following the Break character (see Section 27.4.3 “Auto-Wake-up on Break”).

2: It is up to the user to determine that the incoming character baud rate is within the range of the selected BRG clock source. Some combinations of oscillator frequency and EUSART baud rates are not possible.

3: During the auto-baud process, the auto-baud counter starts counting at 1. Upon completion of the auto-baud sequence, to achieve maximum accuracy, subtract 1 from the SPBRGH:SPBRGL register pair.

<table>
<thead>
<tr>
<th>BRG16</th>
<th>BRGH</th>
<th>BRG Base Clock</th>
<th>BRG ABD Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Fosc/64</td>
<td>Fosc/512</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Fosc/16</td>
<td>Fosc/128</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Fosc/16</td>
<td>Fosc/128</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Fosc/4</td>
<td>Fosc/32</td>
</tr>
</tbody>
</table>

Note: During the ABD sequence, SPBRGL and SPBRGH registers are both used as a 16-bit counter, independent of BRG16 setting.

FIGURE 27-6: AUTOMATIC BAUD RATE CALIBRATION

Note 1: The ABD sequence requires the EUSART module to be configured in Asynchronous mode.
27.4.2 AUTO-BAUD OVERFLOW

During the course of automatic baud detection, the ABDOVF bit of the BAUDCON register will be set if the baud rate counter overflows before the fifth rising edge is detected on the RX pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the SPBRGH:SPBRGL register pair. After the ABDOVF bit has been set, the counter continues to count until the fifth rising edge is detected on the RX pin. Upon detecting the fifth RX edge, the hardware will set the RCIF interrupt flag and clear the ABDEN bit of the BAUDCON register. The RCIF flag can be subsequently cleared by reading the RCREG register. The ABDOVF flag of the BAUDCON register can be cleared by software directly.

To terminate the auto-baud process before the RCIF flag is set, clear the ABDEN bit then clear the ABDOVF bit of the BAUDCON register. The ABDOVF bit will remain set if the ABDEN bit is not cleared first.

27.4.3 AUTO-WAKE-UP ON BREAK

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the Baud Rate Generator is inactive and a proper character reception cannot be performed. The Auto-Wake-up feature allows the controller to wake-up due to activity on the RX/DT line. This feature is available only in Asynchronous mode.

The Auto-Wake-up feature is enabled by setting the WUE bit of the BAUDCON register. Once set, the normal receive sequence on RX/DT is disabled, and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RX/DT line. (This coincides with the start of a Sync Break or a wake-up signal character for the LIN protocol.)

The EUSART module generates an RCIF interrupt coincident with the wake-up event. The interrupt is generated synchronously to the Q clocks in normal CPU operating modes (Figure 27-7), and asynchronously if the device is in Sleep mode (Figure 27-8). The interrupt condition is cleared by reading the RCREG register.

The WUE bit is automatically cleared by the low-to-high transition on the RX line at the end of the Break. This signals to the user that the Break event is over. At this point, the EUSART module is in Idle mode waiting to receive the next character.

27.4.3.1 Special Considerations

**Break Character**

To avoid character errors or character fragments during a wake-up event, the wake-up character must be all zeros.

When the wake-up is enabled the function works independent of the low time on the data stream. If the WUE bit is set and a valid non-zero character is received, the low time from the Start bit to the first rising edge will be interpreted as the wake-up event. The remaining bits in the character will be received as a fragmented character and subsequent characters can result in framing or overrun errors.

Therefore, the initial character in the transmission must be all ‘0’s. This must be ten or more bit times, 13-bit times recommended for LIN bus, or any number of bit times for standard RS-232 devices.

**Oscillator Start-up Time**

Oscillator start-up time must be considered, especially in applications using oscillators with longer start-up intervals (i.e., LP, XT or HS/PLL mode). The Sync Break (or wake-up signal) character must be of sufficient length, and be followed by a sufficient interval, to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

**WUE Bit**

The wake-up event causes a receive interrupt by setting the RCIF bit. The WUE bit is cleared in hardware by a rising edge on RX/DT. The interrupt condition is then cleared in software by reading the RCREG register and discarding its contents.

To ensure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process before setting the WUE bit. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.
FIGURE 27-7: AUTO-WAKE-UP BIT (WUE) TIMING DURING NORMAL OPERATION

Note 1: The EUSART remains in idle while the WUE bit is set.

FIGURE 27-8: AUTO-WAKE-UP BIT (WUE) TIMINGS DURING SLEEP

Note 1: If the wake-up event requires long oscillator warm-up time, the automatic clearing of the WUE bit can occur while the stposc signal is still active. This sequence should not depend on the presence of Q clocks.

2: The EUSART remains in idle while the WUE bit is set.
27.4.4 BREAK CHARACTER SEQUENCE

The EUSART module has the capability of sending the special Break character sequences that are required by the LIN bus standard. A Break character consists of a Start bit, followed by 12 ‘0’ bits and a Stop bit.

To send a Break character, set the SENDB and TXEN bits of the TXSTA register. The Break character transmission is then initiated by a write to the TXREG. The value of data written to TXREG will be ignored and all ‘0’s will be transmitted.

The SENDB bit is automatically reset by hardware after the corresponding Stop bit is sent. This allows the user to preload the transmit FIFO with the next transmit byte following the Break character (typically, the Sync character in the LIN specification).

The TRMT bit of the TXSTA register indicates when the transmit operation is active or idle, just as it does during normal transmission. See Figure 27-9 for the timing of the Break character sequence.

27.4.4.1 Break and Sync Transmit Sequence

The following sequence will start a message frame header made up of a Break, followed by an auto-baud Sync byte. This sequence is typical of a LIN bus master.

1. Configure the EUSART for the desired mode.
2. Set the TXEN and SENDB bits to enable the Break sequence.
3. Load the TXREG with a dummy character to initiate transmission (the value is ignored).
4. Write ‘55h’ to TXREG to load the Sync character into the transmit FIFO buffer.
5. After the Break has been sent, the SENDB bit is reset by hardware and the Sync character is then transmitted.

When the TXREG becomes empty, as indicated by the TXIF, the next data byte can be written to TXREG.

27.4.5 RECEIVING A BREAK CHARACTER

The Enhanced EUSART module can receive a Break character in two ways.

The first method to detect a Break character uses the FERR bit of the RCSTA register and the received data as indicated by RCREG. The Baud Rate Generator is assumed to have been initialized to the expected baud rate.

A Break character has been received when;
   • RCIF bit is set
   • FERR bit is set
   • RCREG = 00h

The second method uses the Auto-Wake-up feature described in Section 27.4.3 “Auto-Wake-up on Break”. By enabling this feature, the EUSART will sample the next two transitions on RX/DT, cause an RCIF interrupt, and receive the next data byte followed by another interrupt.

Note that following a Break character, the user will typically want to enable the Auto-Baud Detect feature. For both methods, the user can set the ABDEN bit of the BAUDCON register before placing the EUSART in Sleep mode.

FIGURE 27-9: SEND BREAK CHARACTER SEQUENCE
27.5  EUSART Synchronous Mode

Synchronous serial communications are typically used in systems with a single master and one or more slaves. The master device contains the necessary circuitry for baud rate generation and supplies the clock for all devices in the system. Slave devices can take advantage of the master clock by eliminating the internal clock generation circuitry.

There are two signal lines in Synchronous mode: a bidirectional data line and a clock line. Slaves use the external clock supplied by the master to shift the serial data into and out of their respective receive and transmit shift registers. Since the data line is bidirectional, synchronous operation is half-duplex only. Half-duplex refers to the fact that master and slave devices can receive and transmit data but not both simultaneously. The EUSART can operate as either a master or slave device.

Start and Stop bits are not used in synchronous transmissions.

27.5.1  SYNCHRONOUS MASTER MODE

The following bits are used to configure the EUSART for synchronous master operation:

- **SYNC = 1**
- **CSRC = 1**
- **SREN = 0** (for transmit); **SREN = 1** (for receive)
- **CREN = 0** (for transmit); **CREN = 1** (for receive)
- **SPEN = 1**

Setting the **SYNC** bit of the **TXSTA** register configures the device for synchronous operation. Setting the **CSRC** bit of the **TXSTA** register configures the device as a master. Clearing the **SREN** and **CREN** bits of the **RCSTA** register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the **SPEN** bit of the **RCSTA** register enables the EUSART.

27.5.1.1  Master Clock

Synchronous data transfers use a separate clock line, which is synchronous with the device. A device configured as a master transmits the clock on the TX/CK line. The TX/CK pin output driver is automatically enabled when the EUSART is configured for synchronous transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One clock cycle is generated for each data bit. Only as many clock cycles are generated as there are data bits.

27.5.1.2  Clock Polarity

A clock polarity option is provided for Microwire compatibility. Clock polarity is selected with the **SCKP** bit of the BAUDCON register. Setting the **SCKP** bit sets the clock Idle state as high. When the **SCKP** bit is set, the data changes on the falling edge of each clock.

Clearing the **SCKP** bit sets the Idle state as low. When the **SCKP** bit is cleared, the data changes on the rising edge of each clock.

27.5.1.3  Synchronous Master Transmission

Data is transferred out of the device on the RX/DT pin. The RX/DT and TX/CK pin output drivers are automatically enabled when the EUSART is configured for synchronous master transmit operation.

A transmission is initiated by writing a character to the TXREG register. If the **TSR** still contains all or part of a previous character the new character data is held in the TXREG until the last bit of the previous character has been transmitted. If this is the first character, or the previous character has been completely flushed from the **TSR**, the data in the **TXREG** is immediately transferred to the **TSR**. The transmission of the character commences immediately following the transfer of the data to the **TSR** from the **TXREG**.

Each data bit changes on the leading edge of the master clock and remains valid until the subsequent leading clock edge.

Note: The **TSR** register is not mapped in data memory, so it is not available to the user.

27.5.1.4  Synchronous Master Transmission

Set-up:

1. Initialize the **SPBRGH**, **SPBRGL** register pair and the **BRGH** and **BRG16** bits to achieve the desired baud rate (see Section 27.4 “EUSART Baud Rate Generator (BRG)”).
2. Enable the synchronous master serial port by setting bits **SYNC**, **SPEN** and **CSRC**.
3. Disable Receive mode by clearing bits **SREN** and **CREN**.
4. Enable Transmit mode by setting the **TXEN** bit.
5. If 9-bit transmission is desired, set the **TX9** bit.
6. If interrupts are desired, set the **TXIE** bit of the **PIE1** register and the **GIE** and **PEIE** bits of the **INTCON** register.
7. If 9-bit transmission is selected, the ninth bit should be loaded in the **TX9D** bit.
8. Start transmission by loading data to the **TXREG** register.
FIGURE 27-10: SYNCHRONOUS TRANSMISSION

FIGURE 27-11: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)

TABLE 27-7: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>APFCON1</td>
<td>C2OUTSEL</td>
<td>CC1PSEL</td>
<td>SDOSEL</td>
<td>SCKSEL</td>
<td>SSISEL</td>
<td>TXSEL</td>
<td>RXSEL</td>
<td>CCP2SEL</td>
<td>127</td>
</tr>
<tr>
<td>BAUDCON</td>
<td>ABDOLF</td>
<td>RCDI</td>
<td>—</td>
<td>SCKP</td>
<td>BRG16</td>
<td>—</td>
<td>WUE</td>
<td>ABDEN</td>
<td>347</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMROIE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMROIF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>93</td>
</tr>
<tr>
<td>PIE1</td>
<td>TMROGIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSP1IE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>94</td>
</tr>
<tr>
<td>PIR1</td>
<td>TMRO1IE</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1IF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>98</td>
</tr>
<tr>
<td>RCSTA</td>
<td>SPEN</td>
<td>RX9</td>
<td>SREN</td>
<td>CREN</td>
<td>ADDEN</td>
<td>FERR</td>
<td>OERR</td>
<td>RX9D</td>
<td>346</td>
</tr>
<tr>
<td>SPBRG</td>
<td>BRG&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>348</td>
</tr>
<tr>
<td>SPBRGH</td>
<td>BRG&lt;15:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>348</td>
</tr>
<tr>
<td>TRISC</td>
<td>TRISC7</td>
<td>TRISC6</td>
<td>TRISC5</td>
<td>TRISC4</td>
<td>TRISC3</td>
<td>TRISC2</td>
<td>TRISC1</td>
<td>TRISC0</td>
<td>142</td>
</tr>
<tr>
<td>TXREG</td>
<td>EUSART Transmit Data Register</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>337*</td>
</tr>
<tr>
<td>TXSTA</td>
<td>CSRC</td>
<td>TX9</td>
<td>TXEN</td>
<td>SYNC</td>
<td>SENDB</td>
<td>BRG9</td>
<td>TRMT</td>
<td>TX9D</td>
<td>345</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used for synchronous master transmission.

* Page provides register information.
27.5.1.5 Synchronous Master Reception

Data is received at the RX/DT pin. The RX/DT pin output driver is automatically disabled when the EUSART is configured for synchronous master receive operation.

In Synchronous mode, reception is enabled by setting either the Single Receive Enable bit (SREN of the RCSTA register) or the Continuous Receive Enable bit (CREN of the RCSTA register).

When SREN is set and CREN is clear, only as many clock cycles are generated as there are data bits in a single character. The SREN bit is automatically cleared at the completion of one character. When CREN is set, clocks are continuously generated until CREN is cleared. If CREN is cleared in the middle of a character, the CK clock stops immediately and the partial character is discarded. If SREN and CREN are both set, then SREN is cleared at the completion of the first character and CREN takes precedence.

To initiate reception, set either SREN or CREN. Data is sampled at the RX/DT pin on the trailing edge of the TX/CK clock pin and is shifted into the Receive Shift Register (RSR). When a complete character is received into the RSR, the RCIF bit is set and the character is automatically transferred to the two character receive FIFO. The Least Significant eight bits of the top character in the receive FIFO are available in RCREG. The RCIF bit remains set as long as there are unread characters in the receive FIFO.

Note: If the RX/DT function is on an analog pin, the corresponding ANSEL bit must be cleared for the receiver to function.

27.5.1.6 Slave Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a slave receives the clock on the TX/CK line. The TX/CK pin output driver is automatically disabled when the device is configured for synchronous slave transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One data bit is transferred for each clock cycle. Only as many clock cycles should be received as there are data bits.

Note: If the device is configured as a slave and the TX/CK function is on an analog pin, the corresponding ANSEL bit must be cleared.

27.5.1.7 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before RCREG is read to access the FIFO. When this happens the OERR bit of the RCSTA register is set. Previous data in the FIFO will not be overwritten. The two characters in the FIFO buffer can be read, however, no additional characters will be received until the error is cleared. The OERR bit can only be cleared by clearing the overrun condition. If the overrun error occurred when the SREN bit is set and CREN is clear then the error is cleared by reading RCREG. If the overrun occurred when the CREN bit is set then the error condition is cleared by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

27.5.1.8 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift 9-bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth, and Most Significant, data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

27.5.1.9 Synchronous Master Reception

Set-up:
1. Initialize the SPBRGH, SPBRGL register pair for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
4. Ensure bits CREN and SREN are clear.
5. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
6. If 9-bit reception is desired, set bit RX9.
7. Start reception by setting the SREN bit or for continuous reception, set the CREN bit.
8. Interrupt flag bit RCIF will be set when reception of a character is complete. An interrupt will be generated if the enable bit RCIE was set.
9. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
10. Read the 8-bit received data by reading the RCREG register.
11. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

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FIGURE 27-12: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)

TABLE 27-8: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>APFCON1</td>
<td>C2OUTSEL</td>
<td>CC1PSEL</td>
<td>SDOSEL</td>
<td>SCKSEL</td>
<td>SDISEL</td>
<td>TXSEL</td>
<td>RXSEL</td>
<td>CCP2SEL</td>
<td>127</td>
</tr>
<tr>
<td>BAUDCON</td>
<td>ABDOVF</td>
<td>RCIDL</td>
<td>—</td>
<td>SCKP</td>
<td>BRG16</td>
<td>—</td>
<td>WUE</td>
<td>ABDEN</td>
<td>347</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCF</td>
<td>93</td>
</tr>
<tr>
<td>PIE1</td>
<td>TMR1GIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSP1IE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>94</td>
</tr>
<tr>
<td>PIR1</td>
<td>TMR1GIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1IF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>98</td>
</tr>
<tr>
<td>RCREG</td>
<td>EUSART Receive Data Register</td>
<td>340*</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RCSTA</td>
<td>SPEN</td>
<td>RX9</td>
<td>SREN</td>
<td>CREN</td>
<td>ADDEN</td>
<td>FERR</td>
<td>OERR</td>
<td>RX9D</td>
<td>346</td>
</tr>
<tr>
<td>SPBRG</td>
<td>BRG&lt;7:0&gt;</td>
<td>348</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPBRGL</td>
<td>BRG&lt;15:8&gt;</td>
<td>348</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TRISC</td>
<td>TRISC7</td>
<td>TRISC6</td>
<td>TRISC5</td>
<td>TRISC4</td>
<td>TRISC3</td>
<td>TRISC2</td>
<td>TRISC1</td>
<td>TRISC0</td>
<td>142</td>
</tr>
<tr>
<td>TXSTA</td>
<td>CSRC</td>
<td>TX9</td>
<td>TXEN</td>
<td>SYNC</td>
<td>SENSE</td>
<td>BRGH</td>
<td>TRMT</td>
<td>TX9D</td>
<td>345</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for synchronous master reception.

* Page provides register information.
27.5.2 SYNCHRONOUS SLAVE MODE

The following bits are used to configure the EUSART for synchronous slave operation:

- **SYNC = 1**
- **CSRC = 0**
- **SREN = 0** (for transmit); **SREN = 1** (for receive)
- **CREN = 0** (for transmit); **CREN = 1** (for receive)
- **SPEN = 1**

Setting the **SYNC** bit of the **TXSTA** register configures the device for synchronous operation. Clearing the **CSRC** bit of the **TXSTA** register configures the device as a slave. Clearing the **SREN** and **CREN** bits of the **RCSTA** register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the **SPEN** bit of the **RCSTA** register enables the EUSART.

27.5.2.1 EUSART Synchronous Slave Transmit

The operation of the Synchronous Master and Slave modes are identical (see Section 27.5.1.3 “Synchronous Master Transmission”), except in the case of the Sleep mode.

If two words are written to the **TXREG** and then the **SLEEP** instruction is executed, the following will occur:

1. The first character will immediately transfer to the **TSR** register and transmit.
2. The second word will remain in **TXREG** register.
3. The **TXIF** bit will not be set.
4. After the first character has been shifted out of **TSR**, the **TXREG** register will transfer the second character to the **TSR** and the **TXIF** bit will now be set.
5. If the **PEIE** and **TXIE** bits are set, the interrupt will wake the device from Sleep and execute the next instruction. If the **GIE** bit is also set, the program will call the Interrupt Service Routine.

27.5.2.2 Synchronous Slave Transmission Set-up:

1. Set the **SYNC** and **SPEN** bits and clear the **CSRC** bit.
2. Clear the **ANSEL** bit for the **CK** pin (if applicable).
3. Clear the **CREN** and **SREN** bits.
4. If interrupts are desired, set the **TXIE** bit of the **PIE1** register and the **GIE** and **PEIE** bits of the **INTCON** register.
5. If 9-bit transmission is desired, set the **TX9** bit.
6. Enable transmission by setting the **TXEN** bit.
7. If 9-bit transmission is selected, insert the Most Significant bit into the **TX9D** bit.
8. Start transmission by writing the Least Significant eight bits to the **TXREG** register.

### TABLE 27-9: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>APFCON1</td>
<td>C2OUTSEL</td>
<td>CC1PSEL</td>
<td>SDSEL</td>
<td>SCKSEL</td>
<td>SDISEL</td>
<td>TXSEL</td>
<td>RXSEL</td>
<td>CCP2SEL</td>
<td>127</td>
</tr>
<tr>
<td>BAUDCON</td>
<td>ABDOVF</td>
<td>RCIDL</td>
<td>—</td>
<td>SCKP</td>
<td>BRG16</td>
<td>—</td>
<td>WUE</td>
<td>ABDEN</td>
<td>347</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>93</td>
</tr>
<tr>
<td>PIE1</td>
<td>TMR1GIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSP1IE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>94</td>
</tr>
<tr>
<td>PIR1</td>
<td>TMR1GIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1IF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>98</td>
</tr>
<tr>
<td>RCSTA</td>
<td>SPEN</td>
<td>RX9</td>
<td>SREN</td>
<td>CREN</td>
<td>ADDEN</td>
<td>FERR</td>
<td>OERR</td>
<td>RX9D</td>
<td>346</td>
</tr>
<tr>
<td>TRISC</td>
<td>TRISC7</td>
<td>TRISC6</td>
<td>TRISC5</td>
<td>TRISC4</td>
<td>TRISC3</td>
<td>TRISC2</td>
<td>TRISC1</td>
<td>TRISC0</td>
<td>142</td>
</tr>
<tr>
<td>TXREG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>EUSART Transmit Data Register</td>
<td>337*</td>
</tr>
<tr>
<td>TXSTA</td>
<td>CSRC</td>
<td>TX9</td>
<td>TXEN</td>
<td>SYNC</td>
<td>SENDB</td>
<td>BRGH</td>
<td>TRMT</td>
<td>TX9D</td>
<td>345</td>
</tr>
</tbody>
</table>

Legend:
- — = unimplemented location, read as ‘0’. Shaded cells are not used for synchronous slave transmission.
- * Page provides register information.
27.5.2.3 EUSART Synchronous Slave Reception

The operation of the Synchronous Master and Slave modes is identical (Section 27.5.1.5 “Synchronous Master Reception”), with the following exceptions:

- Sleep
- CREN bit is always set, therefore the receiver is never idle
- SREN bit, which is a “don’t care” in Slave mode

A character may be received while in Sleep mode by setting the CREN bit prior to entering Sleep. Once the word is received, the RSR register will transfer the data to the RCREG register. If the RCIE enable bit is set, the interrupt generated will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will branch to the interrupt vector.

27.5.2.4 Synchronous Slave Reception

Set-up:

1. Set the SYNC and SPEN bits and clear the CSRC bit.
2. Clear the ANSEL bit for both the CK and DT pins (if applicable).
3. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
4. If 9-bit reception is desired, set the RX9 bit.
5. Set the CREN bit to enable reception.
6. The RCIF bit will be set when reception is complete. An interrupt will be generated if the RCIE bit was set.
7. If 9-bit mode is enabled, retrieve the Most Significant bit from the RX9D bit of the RCSTA register.
8. Retrieve the eight Least Significant bits from the receive FIFO by reading the RCREG register.
9. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

### TABLE 27-10: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>APFCON1</td>
<td>C2OUTSEL</td>
<td>CC1PSEL</td>
<td>SDOSEL</td>
<td>SCKSEL</td>
<td>SCLSEL</td>
<td>TXSEL</td>
<td>RXSEL</td>
<td>CCP2SEL</td>
<td>127</td>
</tr>
<tr>
<td>BAUDCON</td>
<td>ABDVF</td>
<td>RCIDL</td>
<td>—</td>
<td>SCKP</td>
<td>BRG16</td>
<td>—</td>
<td>WUE</td>
<td>ABDEN</td>
<td>347</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TMR0IE</td>
<td>INTE</td>
<td>IOCIE</td>
<td>TMR0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>93</td>
</tr>
<tr>
<td>PIE1</td>
<td>TMR1GIE</td>
<td>ADIE</td>
<td>RCIE</td>
<td>TXIE</td>
<td>SSP1IE</td>
<td>CCP1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>94</td>
</tr>
<tr>
<td>PIR1</td>
<td>TMR1GIF</td>
<td>ADIF</td>
<td>RCIF</td>
<td>TXIF</td>
<td>SSP1IF</td>
<td>CCP1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>98</td>
</tr>
<tr>
<td>RCREG</td>
<td>EUSART Receive Data Register</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>340*</td>
</tr>
<tr>
<td>RXSTA</td>
<td>SPEN</td>
<td>RX9</td>
<td>SREN</td>
<td>CREN</td>
<td>ADDEN</td>
<td>FERR</td>
<td>OERR</td>
<td>RX9D</td>
<td>346</td>
</tr>
<tr>
<td>TRISC</td>
<td>TRISC7</td>
<td>TRISC6</td>
<td>TRISC5</td>
<td>TRISC4</td>
<td>TRISC3</td>
<td>TRISC2</td>
<td>TRISC1</td>
<td>TRISC0</td>
<td>142</td>
</tr>
<tr>
<td>TXSTA</td>
<td>CSRC</td>
<td>TX9</td>
<td>TXEN</td>
<td>SYNC</td>
<td>SEDB</td>
<td>BRGH</td>
<td>TRMT</td>
<td>TX9D</td>
<td>345</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented location, read as ‘0’. Shaded cells are not used for synchronous slave reception.

* Page provides register information.
27.6 EUSART Operation During Sleep

The EUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

27.6.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Reception (see Section 27.5.2.4 “Synchronous Slave Reception Set-up:”).
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- The RCIF interrupt flag must be cleared by reading RCREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT pin and transmit data on the TX/CK pin, respectively. When the data word has been completely clocked in by the external device, the RCIF interrupt flag bit of the PIR1 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit is also set then the Interrupt Service Routine at address 004h will be called.

27.6.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for synchronous slave transmission (see Section 27.5.2.2 “Synchronous Slave Transmission Set-up:”).
- The TXIF interrupt flag must be cleared by writing the output data to the TXREG, thereby filling the TSR and transmit buffer.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the PEIE bit of the INTCON register.
- Interrupt enable bits TXIE of the PIE1 register and PEIE of the INTCON register must set.

Upon entering Sleep mode, the device will be ready to accept clocks on TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXREG will transfer to the TSR and the TXIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXREG is available to accept another character for transmission, which will clear the TXIF flag.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit is also set then the Interrupt Service Routine at address 004h will be called.

27.6.3 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register, APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see Section 13.1 “Alternate Pin Function” for more information.
28.0 IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

ICSP™ programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process, allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP™ programming:
- ICSPCLK
- ICSPDAT
- MCLR/VPP
- VDD
- VSS

In Program/Verify mode the program memory, user IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input. For more information on ICSP™ refer to the “PIC16(L)F178X Memory Programming Specification” (DS41457).

28.1 High-Voltage Programming Entry Mode

The device is placed into High-Voltage Programming Entry mode by holding the ICSPCLK and ICSPDAT pins low then raising the voltage on MCLR/VPP to VIH.

28.2 Low-Voltage Programming Entry Mode

The Low-Voltage Programming Entry mode allows the PIC® Flash MCUs to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Words is set to ‘1’, the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to ‘0’.

Entry into the Low-Voltage Programming Entry mode requires the following steps:

1. MCLR is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

Once the key sequence is complete, MCLR must be held at VIL for as long as Program/Verify mode is to be maintained.

If low-voltage programming is enabled (LVP = 1), the MCLR Reset function is automatically enabled and cannot be disabled. See Section 5.5 “MCLR” for more information.

The LVP bit can only be reprogrammed to ‘0’ by using the High-Voltage Programming mode.

28.3 Common Programming Interfaces

Connection to a target device is typically done through an ICSP™ header. A commonly found connector on development tools is the RJ-11 in the 6P6C (6-pin, 6 connector) configuration. See Figure 28-1.

FIGURE 28-1: ICD RJ-11 STYLE CONNECTOR INTERFACE

Another connector often found in use with the PICKit™ programmers is a standard 6-pin header with 0.1 inch spacing. Refer to Figure 28-2.

For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices such as resistors, diodes, or even jumpers. See Figure 28-3 for more information.
FIGURE 28-2: PICkit™ PROGRAMMER STYLE CONNECTOR INTERFACE

Pin 1 Indicator

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VPP/MCLR</td>
</tr>
<tr>
<td>2</td>
<td>VDD Target</td>
</tr>
<tr>
<td>3</td>
<td>Vss (ground)</td>
</tr>
<tr>
<td>4</td>
<td>ICSPDAT</td>
</tr>
<tr>
<td>5</td>
<td>ICSPCLK</td>
</tr>
<tr>
<td>6</td>
<td>No Connect</td>
</tr>
</tbody>
</table>

* The 6-pin header (0.100" spacing) accepts 0.025" square pins.

FIGURE 28-3: TYPICAL CONNECTION FOR ICSP™ PROGRAMMING

External Programming Signals

- VDD
- VPP
- Vss
- Data
- Clock

Device to be Programmed

- VDD
- MCLR/VPP
- Vss
- ICSPDAT
- ICSPCLK

* Isolation devices (as required).
29.0 INSTRUCTION SET SUMMARY

Each instruction is a 14-bit word containing the operation code (opcode) and all required operands. The opcodes are broken into three broad categories.

- Byte Oriented
- Bit Oriented
- Literal and Control

The literal and control category contains the most varied instruction word format.

Table 29-3 lists the instructions recognized by the MPASM™ assembler.

All instructions are executed within a single instruction cycle, with the following exceptions, which may take two or three cycles:

- Subroutine takes two cycles (CALL, CALLW)
- Returns from interrupts or subroutines take two cycles (RETURN, RETLW, RETFIE)
- Program branching takes two cycles (GOTO, BRA, BRW, BTFSS, BTFSC, DECFSZ, INCSFZ)

- One additional instruction cycle will be used when any instruction references an indirect file register and the file select register is pointing to program memory.

One instruction cycle consists of 4 oscillator cycles; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution rate of 1 MHz.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

29.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator ‘d’. A read operation is performed on a register even if the instruction writes to that register.

### TABLE 29-1: OPCODE FIELD DESCRIPTIONS

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>f</td>
<td>Register file address (0x00 to 0x7F)</td>
</tr>
<tr>
<td>W</td>
<td>Working register (accumulator)</td>
</tr>
<tr>
<td>b</td>
<td>Bit address within an 8-bit file register</td>
</tr>
<tr>
<td>k</td>
<td>Literal field, constant data or label</td>
</tr>
<tr>
<td>x</td>
<td>Don’t care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.</td>
</tr>
<tr>
<td>d</td>
<td>Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.</td>
</tr>
<tr>
<td>n</td>
<td>FSR or INDF number. (0-1)</td>
</tr>
<tr>
<td>mm</td>
<td>Pre-post increment-decrement mode selection</td>
</tr>
</tbody>
</table>

### TABLE 29-2: ABBREVIATION DESCRIPTIONS

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC</td>
<td>Program Counter</td>
</tr>
<tr>
<td>TO</td>
<td>Time-Out bit</td>
</tr>
<tr>
<td>C</td>
<td>Carry bit</td>
</tr>
<tr>
<td>DC</td>
<td>Digit Carry bit</td>
</tr>
<tr>
<td>Z</td>
<td>Zero bit</td>
</tr>
<tr>
<td>PD</td>
<td>Power-Down bit</td>
</tr>
</tbody>
</table>
FIGURE 29-1: GENERAL FORMAT FOR INSTRUCTIONS

<table>
<thead>
<tr>
<th>Byte-oriented file register operations</th>
</tr>
</thead>
<tbody>
<tr>
<td>13 8 7 6 0</td>
</tr>
<tr>
<td>OPCODE d f (FILE #)</td>
</tr>
<tr>
<td>d = 0 for destination W</td>
</tr>
<tr>
<td>d = 1 for destination f</td>
</tr>
<tr>
<td>f = 7-bit file register address</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit-oriented file register operations</th>
</tr>
</thead>
<tbody>
<tr>
<td>13 10 9 7 6 0</td>
</tr>
<tr>
<td>OPCODE b f (FILE #)</td>
</tr>
<tr>
<td>b = 3-bit bit address</td>
</tr>
<tr>
<td>f = 7-bit file register address</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Literal and control operations</th>
</tr>
</thead>
<tbody>
<tr>
<td>General</td>
</tr>
<tr>
<td>13 8 7 0</td>
</tr>
<tr>
<td>OPCODE k (literal)</td>
</tr>
<tr>
<td>k = 8-bit immediate value</td>
</tr>
</tbody>
</table>

| CALL and GOTO instructions only       |
| 13 11 10 0                            |
| OPCODE k (literal)                    |
| k = 11-bit immediate value            |

| MOVLP instruction only                |
| 13 7 6 0                              |
| OPCODE k (literal)                    |
| k = 7-bit immediate value             |

| MOVLB instruction only                |
| 13 5 4 0                              |
| OPCODE k (literal)                    |
| k = 5-bit immediate value             |

| BRA instruction only                  |
| 13 9 8 0                              |
| OPCODE k (literal)                    |
| k = 9-bit immediate value             |

| FSR Offset instructions               |
| 13 7 6 5 0                            |
| OPCODE n k (literal)                  |
| n = appropriate FSR                   |
| k = 6-bit immediate value             |

| FSR Increment instructions            |
| 13 3 2 1 0                            |
| OPCODE n m (mode)                     |
| n = appropriate FSR                   |
| m = 2-bit mode value                  |

|_OPCODE only                           |
| 13 0                                  |
| OPCODE                                |
### TABLE 29-3: ENHANCED MID-RANGE INSTRUCTION SET

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycle s</th>
<th>14-Bit Opcode</th>
<th>Status Affected</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSb</td>
<td>LSb</td>
<td></td>
</tr>
<tr>
<td><strong>BYTE-ORIENTED FILE REGISTER OPERATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADDWF f, d</td>
<td>Add W and f</td>
<td>1</td>
<td>00</td>
<td>0111 dfff ffff</td>
<td>C, DC, Z</td>
</tr>
<tr>
<td>ADDWF f, d</td>
<td>Add with Carry W and f</td>
<td>1</td>
<td>11</td>
<td>1101 dfff ffff</td>
<td>C, DC, Z</td>
</tr>
<tr>
<td>C</td>
<td>AND W with f</td>
<td>1</td>
<td>00</td>
<td>0101 dfff ffff</td>
<td>Z</td>
</tr>
<tr>
<td>ANDWF f, d</td>
<td>Arithmetic Right Shift</td>
<td>1</td>
<td>11</td>
<td>1111 dfff ffff</td>
<td>C, Z</td>
</tr>
<tr>
<td>ASRF f, d</td>
<td>Logical Left Shift</td>
<td>1</td>
<td>11</td>
<td>1011 dfff ffff</td>
<td>C, Z</td>
</tr>
<tr>
<td>LSLF f, d</td>
<td>Logical Right Shift</td>
<td>1</td>
<td>11</td>
<td>0110 dfff ffff</td>
<td>C, Z</td>
</tr>
<tr>
<td>LSRF f</td>
<td>Clear f</td>
<td>1</td>
<td>00</td>
<td>0001 1fff ffff</td>
<td>Z</td>
</tr>
<tr>
<td>CLRF –</td>
<td>Clear W</td>
<td>1</td>
<td>00</td>
<td>1001 dfff ffff</td>
<td>Z</td>
</tr>
<tr>
<td>CLRWF f, d</td>
<td>Complement f</td>
<td>1</td>
<td>00</td>
<td>0011 dfff ffff</td>
<td>Z</td>
</tr>
<tr>
<td>COMF f, d</td>
<td>Decrement f</td>
<td>1</td>
<td>00</td>
<td>1010 dfff ffff</td>
<td>Z</td>
</tr>
<tr>
<td>DECF f, d</td>
<td>Increment f</td>
<td>1</td>
<td>00</td>
<td>0100 dfff ffff</td>
<td>Z</td>
</tr>
<tr>
<td>INCF f, d</td>
<td>Inclusive OR W with f</td>
<td>1</td>
<td>00</td>
<td>1000 dfff ffff</td>
<td>Z</td>
</tr>
<tr>
<td>IORWF f, d</td>
<td>Move f</td>
<td>1</td>
<td>00</td>
<td>0000 1fff ffff</td>
<td>Z</td>
</tr>
<tr>
<td>MOVF f</td>
<td>Move W to f</td>
<td>1</td>
<td>00</td>
<td>1101 dfff ffff</td>
<td>Z</td>
</tr>
<tr>
<td>MOVWF f, d</td>
<td>Rotate Left f through Carry</td>
<td>1</td>
<td>00</td>
<td>1100 dfff ffff</td>
<td>C</td>
</tr>
<tr>
<td>RLF f, d</td>
<td>Rotate Right f through Carry</td>
<td>1</td>
<td>00</td>
<td>0010 dfff ffff</td>
<td>C</td>
</tr>
<tr>
<td>RRF f, d</td>
<td>Subtract W from f</td>
<td>1</td>
<td>11</td>
<td>1011 dfff ffff</td>
<td>C, DC, Z</td>
</tr>
<tr>
<td>SUBWF f, d</td>
<td>Subtract with Borrow W from f</td>
<td>1</td>
<td>00</td>
<td>1110 dfff ffff</td>
<td>C, DC, Z</td>
</tr>
<tr>
<td>SUB-, d</td>
<td>Swap nibbles in f</td>
<td>1</td>
<td></td>
<td></td>
<td>Z</td>
</tr>
<tr>
<td>WFB f, d</td>
<td>Exclusive OR W with f</td>
<td>1</td>
<td></td>
<td></td>
<td>Z</td>
</tr>
<tr>
<td>SWAPF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XORWF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| **BYTE ORIENTED SKIP OPERATIONS** | | | | | |
| DECFSZ f, d         | Decrement f, Skip if 0 | 1(2) | 00  | 1011 dfff ffff | 1, 2     |
| INCFSZ f, d         | Increment f, Skip if 0 | 1(2) | 00  | 1111 dfff ffff | 1, 2     |

| **BIT-ORIENTED FILE REGISTER OPERATIONS** | | | | | |
| BCF f, b            | Bit Clear f | 1       | 01  | 00bb bfff ffff | 2         |
| BSF f, b            | Bit Set f  | 1       | 01  | 01bb bfff ffff | 2         |

| **BIT-ORIENTED SKIP OPERATIONS** | | | | | |
| BTFSC f, b          | Bit Test f, Skip if Clear | 1 (2) | 01  | 10bb bfff ffff | 1, 2     |
| BTFSS f, b          | Bit Test f, Skip if Set | 1 (2) | 01  | 11bb bfff ffff | 1, 2     |

| **LITERAL OPERATIONS** | | | | | |
| ADDLW k             | Add literal and W | 1       | 11  | 1110 kkkk kkkk | C, DC, Z  |
| ANDLW k             | AND literal with W | 1       | 11  | 1001 kkkk kkkk | Z         |
| IORLW k             | Inclusive OR literal with W | 1       | 11  | 1000 kkkk kkkk | Z         |
| MOVLB k             | Move literal to BSR | 1       | 00  | 0000 001k kkkk | Z         |
| MOVLP k             | Move literal to PCLATH | 1       | 11  | 0001 1kkk kkkk | Z         |
| MOVLW k             | Move literal to W | 1       | 11  | 0000 kkkk kkkk | Z         |
| SUBLW k             | Subtract W from literal | 1       | 11  | 1100 kkkk kkkk | C, DC, Z  |
| XORLW k             | Exclusive OR literal with W | 1       | 11  | 1010 kkkk kkkk | Z         |

**Note 1:** If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

**2:** If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.
### TABLE 29-4: ENHANCED MID-RANGE INSTRUCTION SET (CONTINUED)

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycle(s)</th>
<th>14-Bit Opcode</th>
<th>Status Affected</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CONTROL OPERATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BRA k</td>
<td>Relative Branch</td>
<td>2</td>
<td>11 001k kkkk kkkk</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BRW –</td>
<td>Relative Branch with W</td>
<td>2</td>
<td>00 0000 0000 1011</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CALL k</td>
<td>Call Subroutine</td>
<td>2</td>
<td>10 0kkk kkkk kkkk</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CALLW –</td>
<td>Call Subroutine with W</td>
<td>2</td>
<td>00 0000 0000 1010</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GOTO k</td>
<td>Go to address</td>
<td>2</td>
<td>10 1kkk kkkk kkkk</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RETFIE k</td>
<td>Return from interrupt</td>
<td>2</td>
<td>00 0000 0000 1001</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RETLW k</td>
<td>Return with literal in W</td>
<td>2</td>
<td>11 0100 kkkk kkkk</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RETUR –</td>
<td>Return from Subroutine</td>
<td>2</td>
<td>00 0000 0000 1000</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| **INHERENT OPERATIONS** | | | | | |
| CLR- – | Clear Watchdog Timer | 1 | 00 0000 0110 0100 | | |
| WDT – | No Operation | 1 | 00 0000 0000 0000 | | |
| NOP – | Load OPTION_REG register with W | 1 | 00 0000 0110 0010 | | |
| OPTION – | Software device Reset | 1 | 00 0000 0000 0001 | | |
| RESET – | Go into Standby mode | 1 | 00 0000 0110 0011 | | |
| SLEEP f | Load TRIS register with W | 1 | 00 0000 0110 00ff | | |

| **C-COMPILE OPTIMIZED** | | | | | |
| ADDFSR n, k | Add Literal k to FSRn | 1 | 11 0001 0nkk kkkk | Z | 2, 3 |
| MOVIW n mm | Move Indirect FSRn to W with pre/post inc/dec modifier, mm | 1 | 00 0000 0001 0nnm | Z | 2 |
| MOVWI k[n] | Move INDFn to W, Indexed Indirect. | 1 | 11 1111 0nkk kkkk | Z | 2, 3 |
| MOVWI k[n] | Move W to Indirect FSRn with pre/post inc/dec modifier, mm | 1 | 11 1111 1nkk kkkk | | |

**Note 1:** If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

**Note 2:** If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.

**Note 3:** See Table in the MOVIW and MOVWI instruction descriptions.

### 29.2 Instruction Descriptions

**ADDFS**

**Add Literal to FSRn**

**Syntax:**

```
[label] ADDFSR FSRn, k
```

**Operands:**

-32 ≤ k ≤ 31
n ∈ [0, 1]

**Operation:**

FSR(n) + k → FSR(n)

**Status Affected:** None

**Description:**

The signed 6-bit literal ‘k’ is added to the contents of the FSRnH:FSRnL register pair.

FSRn is limited to the range 0000h - FFFFh. Moving beyond these bounds will cause the FSR to wrap-around.
### ADDLW Add literal and W

**Syntax:** \[
\text{label} \] ADDLW \ k
\]

**Operands:** \(0 \leq k \leq 255\)

**Operation:** \((W) + k \rightarrow (W)\)

**Status Affected:** C, DC, Z

**Description:** The contents of the W register are added to the 8-bit literal 'k' and the result is placed in the W register.

### ANDLW AND literal with W

**Syntax:** \[
\text{label} \] ANDLW \ k
\]

**Operands:** \(0 \leq k \leq 255\)

**Operation:** \((W) .AND. (k) \rightarrow (W)\)

**Status Affected:** Z

**Description:** The contents of W register are AND'ed with the 8-bit literal 'k'. The result is placed in the W register.

### ADDWF Add W and f

**Syntax:** \[
\text{label} \] ADDWF \ f,d
\]

**Operands:** \(0 \leq f \leq 127\)
\(d \in [0,1]\)

**Operation:** \((W) + (f) \rightarrow (\text{destination})\)

**Status Affected:** C, DC, Z

**Description:** Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

### ANDWF AND W with f

**Syntax:** \[
\text{label} \] ANDWF \ f,d
\]

**Operands:** \(0 \leq f \leq 127\)
\(d \in [0,1]\)

**Operation:** \((W) .AND. (f) \rightarrow (\text{destination})\)

**Status Affected:** Z

**Description:** AND the W register with register 'f'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.

### ADDWFC ADD W and CARRY bit to f

**Syntax:** \[
\text{label} \] ADDWFC \ f {(,d)}
\]

**Operands:** \(0 \leq f \leq 127\)
\(d \in [0,1]\)

**Operation:** \((W) + (f) + (C) \rightarrow \text{dest}\)

**Status Affected:** C, DC, Z

**Description:** Add W, the Carry flag and data memory location 'f'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed in data memory location 'f'.

### ASRF Arithmetic Right Shift

**Syntax:** \[
\text{label} \] ASRF \ f {(,d)}
\]

**Operands:** \(0 \leq f \leq 127\)
\(d \in [0,1]\)

**Operation:** \((f<7>) \rightarrow \text{dest}<7>\)
\((f<7:1>) \rightarrow \text{dest}<6:0>\),
\((f<0>) \rightarrow C\)

**Status Affected:** C, Z

**Description:** The contents of register 'f' are shifted one bit to the right through the Carry flag. The MSb remains unchanged. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.
**BCF**

**Bit Clear f**

Syntax: \[ label \] BCF \ f, b

Operands: \(0 \leq f \leq 127\)  
\(0 \leq b \leq 7\)

Operation: \(0 \rightarrow (f \&<b>)\)

Status Affected: None

Description: Bit 'b' in register 'f' is cleared.

---

**BSF**

**Bit Set f**

Syntax: \[ label \] BSF \ f, b

Operands: \(0 \leq f \leq 127\)  
\(0 \leq b \leq 7\)

Operation: \(1 \rightarrow (f \&<b>)\)

Status Affected: None

Description: Bit 'b' in register 'f' is set.

---

**BRA**

**Relative Branch**

Syntax: \[ label \] BRA \ label  
\[ label \] BRA \ $+k$

Operands: \(-256 \leq \text{label} - \text{PC} + 1 \leq 255\)  
\(-256 \leq k \leq 255\)

Operation: \((\text{PC}) + 1 + k \rightarrow \text{PC}\)

Status Affected: None

Description: Add the signed 9-bit literal 'k' to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be \(\text{PC} + 1 + k\). This instruction is a 2-cycle instruction. This branch has a limited range.

---

**BRW**

**Relative Branch with W**

Syntax: \[ label \] BRW

Operands: None

Operation: \((\text{PC}) + (W) \rightarrow \text{PC}\)

Status Affected: None

Description: Add the contents of W (unsigned) to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be \(\text{PC} + 1 + (W)\). This instruction is a 2-cycle instruction.

---

**BTFSC**

**Bit Test f, Skip if Clear**

Syntax: \[ label \] BTFSC \ f, b

Operands: \(0 \leq f \leq 127\)  
\(0 \leq b \leq 7\)

Operation: skip if \((f \&<b>) = 0\)

Status Affected: None

Description: If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

---

**BTFSS**

**Bit Test f, Skip if Set**

Syntax: \[ label \] BTFSS \ f, b

Operands: None

Operation: skip if \((f \&<b>) = 1\)

Status Affected: None

Description: If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.
**CALL**  Call Subroutine

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ]  CALL  k</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>0 ≤ k ≤ 2047</td>
</tr>
<tr>
<td>Operation:</td>
<td>(PC)+1 → TOS, k → PC&lt;10:0&gt;, (PCLATH&lt;6:3&gt;) → PC&lt;14:11&gt;</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>None</td>
</tr>
<tr>
<td>Description:</td>
<td>Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The 11-bit immediate address is loaded into PC bits &lt;10:0&gt;. The upper bits of the PC are loaded from PCLATH. CALL is a 2-cycle instruction.</td>
</tr>
</tbody>
</table>

**CALLW**  Subroutine Call With W

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ]  CALLW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>None</td>
</tr>
<tr>
<td>Operation:</td>
<td>(PC) +1 → TOS, (W) → PC&lt;7:0&gt;, (PCLATH&lt;6:0&gt;) → PC&lt;14:8&gt;</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>None</td>
</tr>
<tr>
<td>Description:</td>
<td>Subroutine call with W. First, the return address (PC + 1) is pushed onto the return stack. Then, the contents of W is loaded into PC&lt;7:0&gt;, and the contents of PCLATH into PC&lt;14:8&gt;. CALLW is a 2-cycle instruction.</td>
</tr>
</tbody>
</table>

**CLRW**  Clear W

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ]  CLRW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>None</td>
</tr>
<tr>
<td>Operation:</td>
<td>00h → (W)</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>Z</td>
</tr>
<tr>
<td>Description:</td>
<td>W register is cleared. Zero bit (Z) is set.</td>
</tr>
</tbody>
</table>

**CLRWDT**  Clear Watchdog Timer

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ]  CLRWDT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>None</td>
</tr>
<tr>
<td>Operation:</td>
<td>00h → WDT, 1 → TO, 1 → PD</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>TO, PD</td>
</tr>
<tr>
<td>Description:</td>
<td>CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits TO and PD are set.</td>
</tr>
</tbody>
</table>

**COMF**  Complement f

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ]  COMF  f,d</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>0 ≤ f ≤ 127, d ∈ [0,1]</td>
</tr>
<tr>
<td>Operation:</td>
<td>(f) → (destination)</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>Z</td>
</tr>
<tr>
<td>Description:</td>
<td>The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.</td>
</tr>
</tbody>
</table>

**CLRF**  Clear f

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ]  CLRF  f</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>0 ≤ f ≤ 127</td>
</tr>
<tr>
<td>Operation:</td>
<td>00h → (f)</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>Z</td>
</tr>
<tr>
<td>Description:</td>
<td>The contents of register 'f' are cleared and the Z bit is set.</td>
</tr>
</tbody>
</table>

**DECF**  Decrement f

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ]  DECF  f,d</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>0 ≤ f ≤ 127, d ∈ [0,1]</td>
</tr>
<tr>
<td>Operation:</td>
<td>(f) - 1 → (destination)</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>Z</td>
</tr>
<tr>
<td>Description:</td>
<td>Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.</td>
</tr>
</tbody>
</table>
### DECFSZ

**Decrement f, Skip if 0**

**Syntax:**

\[
\text{[ label]} \ \text{DECFSZ} \ f,d
\]

**Operands:**

\[0 \leq f \leq 127\]
\[d \in [0,1]\]

**Operation:**

\[(f) - 1 \rightarrow \text{(destination)}; \text{skip if result} = 0\]

**Status Affected:** None

**Description:**

The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction.

### INCFSZ

**Increment f, Skip if 0**

**Syntax:**

\[
\text{[ label]} \ \text{INCFSZ} \ f,d
\]

**Operands:**

\[0 \leq f \leq 127\]
\[d \in [0,1]\]

**Operation:**

\[(f) + 1 \rightarrow \text{(destination)}; \text{skip if result} = 0\]

**Status Affected:** None

**Description:**

The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction.

### GOTO

**Unconditional Branch**

**Syntax:**

\[
\text{[ label]} \ \text{GOTO} \ k
\]

**Operands:**

\[0 \leq k \leq 2047\]

**Operation:**

\[k \rightarrow \text{PC}<10:0>\]
\[\text{PCLATH}<6:3> \rightarrow \text{PC}<14:11>\]

**Status Affected:** None

**Description:**

GOTO is an unconditional branch. The 11-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a 2-cycle instruction.

### INCF

**Increment f**

**Syntax:**

\[
\text{[ label]} \ \text{INCF} \ f,d
\]

**Operands:**

\[0 \leq f \leq 127\]
\[d \in [0,1]\]

**Operation:**

\[(f) + 1 \rightarrow \text{(destination)}\]

**Status Affected:** Z

**Description:**

The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

### IORLW

**Inclusive OR literal with W**

**Syntax:**

\[
\text{[ label]} \ \text{IORLW} \ k
\]

**Operands:**

\[0 \leq k \leq 255\]

**Operation:**

\[(\text{W}) .\text{OR.} k \rightarrow \text{(W)}\]

**Status Affected:** Z

**Description:**

The contents of the W register are OR'ed with the 8-bit literal 'k'. The result is placed in the W register.

### IORWF

**Inclusive OR W with f**

**Syntax:**

\[
\text{[ label]} \ \text{IORWF} \ f,d
\]

**Operands:**

\[0 \leq f \leq 127\]
\[d \in [0,1]\]

**Operation:**

\[(\text{W}) .\text{OR.} (f) \rightarrow \text{(destination)}\]

**Status Affected:** Z

**Description:**

Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.
### LSLF Logical Left Shift

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ] LSLF f {,d}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>$0 \leq f \leq 127$</td>
</tr>
<tr>
<td></td>
<td>$d \in {0,1}$</td>
</tr>
<tr>
<td>Operation:</td>
<td>$(f&lt;7&gt;) \rightarrow C$</td>
</tr>
<tr>
<td></td>
<td>$(f&lt;6:0&gt;) \rightarrow \text{dest}&lt;7:1&gt;$</td>
</tr>
<tr>
<td></td>
<td>$0 \rightarrow \text{dest}&lt;0&gt;$</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>C, Z</td>
</tr>
<tr>
<td>Description:</td>
<td>The contents of register 'f' are shifted one bit to the left through the Carry flag. A '0' is shifted into the LSb. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.</td>
</tr>
</tbody>
</table>

### LSRF Logical Right Shift

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ] LSRF f {,d}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>$0 \leq f \leq 127$</td>
</tr>
<tr>
<td></td>
<td>$d \in {0,1}$</td>
</tr>
<tr>
<td>Operation:</td>
<td>$0 \rightarrow \text{dest}&lt;7&gt;$</td>
</tr>
<tr>
<td></td>
<td>$(f&lt;7:1&gt;) \rightarrow \text{dest}&lt;6:0&gt;$,</td>
</tr>
<tr>
<td></td>
<td>$(f&lt;0&gt;) \rightarrow C$,</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>C, Z</td>
</tr>
<tr>
<td>Description:</td>
<td>The contents of register 'f' are shifted one bit to the right through the Carry flag. A '0' is shifted into the MSb. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.</td>
</tr>
</tbody>
</table>

### MOVF Move f

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ] MOVF f,d</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>$0 \leq f \leq 127$</td>
</tr>
<tr>
<td></td>
<td>$d \in {0,1}$</td>
</tr>
<tr>
<td>Operation:</td>
<td>$(f) \rightarrow (\text{dest})$</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>Z</td>
</tr>
<tr>
<td>Description:</td>
<td>The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.</td>
</tr>
<tr>
<td>Words:</td>
<td>1</td>
</tr>
<tr>
<td>Cycles:</td>
<td>1</td>
</tr>
<tr>
<td>Example:</td>
<td>MOVF FSR, 0</td>
</tr>
<tr>
<td>After Instruction</td>
<td>$W = \text{value in FSR register}$</td>
</tr>
<tr>
<td></td>
<td>$Z = 1$</td>
</tr>
</tbody>
</table>
### MOVWI
Move INDFn to W

**Syntax:**
- 
- 
- 
- 
- 
- 

**Operands:**
- \( n \in [0, 1] \)
- \( mm \in [00, 01, 10, 11] \)
- \(-32 \leq k \leq 31\)

**Operation:** \( \text{INDFn} \rightarrow W \)

Effective address is determined by:
- \( \text{FSR} + 1 \) (preincrement)
- \( \text{FSR} - 1 \) (predecrement)
- \( \text{FSR} + k \) (relative offset)

After the Move, the FSR value will be either:
- \( \text{FSR} + 1 \) (all increments)
- \( \text{FSR} - 1 \) (all decrements)
- Unchanged

**Status Affected:** \( Z \)

<table>
<thead>
<tr>
<th>Mode</th>
<th>Syntax</th>
<th>mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preincrement</td>
<td>++FSRn</td>
<td>00</td>
</tr>
<tr>
<td>Predecrement</td>
<td>--FSRn</td>
<td>01</td>
</tr>
<tr>
<td>Postincrement</td>
<td>FSRn++</td>
<td>10</td>
</tr>
<tr>
<td>Postdecrement</td>
<td>FSRn--</td>
<td>11</td>
</tr>
</tbody>
</table>

**Description:**
This instruction is used to move data between \( W \) and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

**Note:** The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h - FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap-around.

---

### MOVLB
Move literal to BSR

**Syntax:**
- \( [\text{label}] \) MOVLB \( k \)

**Operands:** \( 0 \leq k \leq 31 \)

**Operation:** \( \text{k} \rightarrow \text{BSR} \)

**Status Affected:** None

**Description:** The 5-bit literal \( 'k' \) is loaded into the Bank Select Register (BSR).

### MOVLW
Move literal to W

**Syntax:**
- \( [\text{label}] \) MOVLW \( k \)

**Operands:** \( 0 \leq k \leq 255 \)

**Operation:** \( k \rightarrow (W) \)

**Status Affected:** None

**Description:** The 8-bit literal \( 'k' \) is loaded into the \( W \) register. The “don’t cares” will assemble as ‘0’

**Example:**

\[
\text{MOVLW 0x5A} \\
\text{After Instruction} \\
W = 0x5A
\]

### MOVLP
Move literal to PCLATH

**Syntax:**
- \( [\text{label}] \) MOVLP \( k \)

**Operands:** \( 0 \leq k \leq 127 \)

**Operation:** \( k \rightarrow \text{PCLATH} \)

**Status Affected:** None

**Description:** The 7-bit literal \( 'k' \) is loaded into the PCLATH register.

### MOVWF
Move W to f

**Syntax:**
- \( [\text{label}] \) MOVWF \( f \)

**Operands:** \( 0 \leq f \leq 127 \)

**Operation:** \( (W) \rightarrow (f) \)

**Status Affected:** None

**Description:** Move data from \( W \) register to register ‘f’.

**Example:**

\[
\text{MOVWF OPTION_REG} \\
\text{Before Instruction} \\
\text{OPTION_REG} = 0xFF \\
W = 0x4F \\
\text{After Instruction} \\
\text{OPTION_REG} = 0x4F \\
W = 0x4F
\]
### MOVWI

**Move W to INDFn**

**Syntax:**

- \([\text{label}]\) MOVWI ++FSRn
- \([\text{label}]\) MOVWI --FSRn
- \([\text{label}]\) MOVWI FSRn++
- \([\text{label}]\) MOVWI FSRn--
- \([\text{label}]\) MOVWI k[FSRn]

**Operands:**

- \(n \in [0, 1]\)
- \(mm \in [00, 01, 10, 11]\)
- \(-32 \leq k \leq 31\)

**Operation:**

\(W \rightarrow \text{INDFn}\)

Effective address is determined by:

- \(\text{FSR} + 1\) (preincrement)
- \(\text{FSR} - 1\) (predecrement)
- \(\text{FSR} + k\) (relative offset)

After the Move, the FSR value will be either:

- \(\text{FSR} + 1\) (all increments)
- \(\text{FSR} - 1\) (all decrements)
- Unchanged

**Status Affected:** None

<table>
<thead>
<tr>
<th>Mode</th>
<th>Syntax</th>
<th>mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preincrement</td>
<td>++FSRn</td>
<td>00</td>
</tr>
<tr>
<td>Predecrement</td>
<td>--FSRn</td>
<td>01</td>
</tr>
<tr>
<td>Postincrement</td>
<td>FSRn++</td>
<td>10</td>
</tr>
<tr>
<td>Postdecrement</td>
<td>FSRn--</td>
<td>11</td>
</tr>
</tbody>
</table>

**Description:**

This instruction is used to move data between W and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

**Note:** The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h-FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap-around.

The increment/decrement operation on FSRn WILL NOT affect any Status bits.

### NOP

**No Operation**

**Syntax:**

\([\text{label}]\) NOP

**Operands:** None

**Operation:** No operation

**Status Affected:** None

**Description:** No operation.

**Words:** 1

**Cycles:** 1

**Example:**

NOP

### OPTION

**Load OPTION_REG Register with W**

**Syntax:**

\([\text{label}]\) OPTION

**Operands:** None

**Operation:** \((W) \rightarrow \text{OPTION_REG}\)

**Status Affected:** None

**Description:** Move data from W register to OPTION_REG register.

### RESET

**Software Reset**

**Syntax:**

\([\text{label}]\) RESET

**Operands:** None

**Operation:** Execute a device Reset. Resets the RI flag of the PCON register.

**Status Affected:** None

**Description:** This instruction provides a way to execute a hardware Reset by software.
<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RETFIE</strong></td>
<td>Return from Interrupt</td>
</tr>
<tr>
<td>Syntax:</td>
<td>[ label ] RETFIE</td>
</tr>
<tr>
<td>Operands:</td>
<td>None</td>
</tr>
<tr>
<td>Operation:</td>
<td>TOS → PC, 1 → GIE</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>None</td>
</tr>
<tr>
<td>Description:</td>
<td>Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON&lt;7&gt;). This is a 2-cycle instruction.</td>
</tr>
<tr>
<td>Words:</td>
<td>1</td>
</tr>
<tr>
<td>Cycles:</td>
<td>2</td>
</tr>
<tr>
<td>Example:</td>
<td>RETFIE</td>
</tr>
<tr>
<td>After Interrupt</td>
<td>PC = TOS, GIE = 1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RETLW</strong></td>
<td>Return with literal in W</td>
</tr>
<tr>
<td>Syntax:</td>
<td>[ label ] RETLW k</td>
</tr>
<tr>
<td>Operands:</td>
<td>0 ≤ k ≤ 255</td>
</tr>
<tr>
<td>Operation:</td>
<td>k → (W); TOS → PC</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>None</td>
</tr>
<tr>
<td>Description:</td>
<td>The W register is loaded with the 8-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.</td>
</tr>
<tr>
<td>Words:</td>
<td>1</td>
</tr>
<tr>
<td>Cycles:</td>
<td>2</td>
</tr>
<tr>
<td>Example:</td>
<td>CALL TABLE;W contains table</td>
</tr>
<tr>
<td></td>
<td>;offset value</td>
</tr>
<tr>
<td></td>
<td>• ;W now has table value</td>
</tr>
<tr>
<td></td>
<td>•</td>
</tr>
<tr>
<td></td>
<td>ADDWF PC ;W = offset</td>
</tr>
<tr>
<td></td>
<td>RETLW k1 ;Begin table</td>
</tr>
<tr>
<td></td>
<td>RETLW k2 ;</td>
</tr>
<tr>
<td></td>
<td>•</td>
</tr>
<tr>
<td></td>
<td>•</td>
</tr>
<tr>
<td></td>
<td>RETLW kn ; End of table</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RLF</strong></td>
<td>Rotate Left f through Carry</td>
</tr>
<tr>
<td>Syntax:</td>
<td>[ label ] RLF f,d</td>
</tr>
<tr>
<td>Operands:</td>
<td>0 ≤ f ≤ 127</td>
</tr>
<tr>
<td>d ∈ [0,1]</td>
<td></td>
</tr>
<tr>
<td>Operation:</td>
<td>See description below</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>C</td>
</tr>
<tr>
<td>Description:</td>
<td>The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.</td>
</tr>
<tr>
<td>Words:</td>
<td>1</td>
</tr>
<tr>
<td>Cycles:</td>
<td>1</td>
</tr>
<tr>
<td>Example:</td>
<td>RLF REG1,0</td>
</tr>
</tbody>
</table>

### Before Instruction

<table>
<thead>
<tr>
<th>REG1</th>
<th>1110</th>
</tr>
</thead>
<tbody>
<tr>
<td>0110</td>
<td>0</td>
</tr>
</tbody>
</table>

### After Instruction

<table>
<thead>
<tr>
<th>REG1</th>
<th>1110</th>
</tr>
</thead>
<tbody>
<tr>
<td>0110</td>
<td>W = 1100</td>
</tr>
<tr>
<td>1100</td>
<td>C = 1</td>
</tr>
</tbody>
</table>
**RRF**  
**Rotate Right f through Carry**

**Syntax:** \[ label \] RRF f,d  
**Operands:**  
\[ 0 \leq f \leq 127 \]  
\[ d \in [0,1] \]  
**Operation:** See description below  
**Status Affected:** C  
**Description:** The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

**SLEEP**  
**Enter Sleep mode**

**Syntax:** \[ label \] SLEEP  
**Operands:** None  
**Operation:**  
\[ 00h \rightarrow \text{WDT}, \]  
\[ 0 \rightarrow \text{WDT prescaler}, \]  
\[ 1 \rightarrow \text{TO}, \]  
\[ 0 \rightarrow \text{PD} \]  
**Status Affected:** TO, PD  
**Description:** The power-down Status bit, PD is cleared. Time-out Status bit, TO is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

**SUBWF**  
**Subtract W from f**

**Syntax:** \[ label \] SUBWF f,d  
**Operands:**  
\[ 0 \leq f \leq 127 \]  
\[ d \in [0,1] \]  
**Operation:** \( f \cdot (W) \rightarrow (destination) \)  
**Status Affected:** C, DC, Z  
**Description:** Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

| C = 0 | W > f |
| C = 1 | W ≤ f |
| DC = 0 | W<3:0> > f<3:0> |
| DC = 1 | W<3:0> ≤ f<3:0> |

**SUBWF B**  
**Subtract W from f with Borrow**

**Syntax:** SUBWFB f \{d\}  
**Operands:**  
\[ 0 \leq f \leq 127 \]  
\[ d \in [0,1] \]  
**Operation:** \( f \cdot (W) - (\overline{B}) \rightarrow \text{dest} \)  
**Status Affected:** C, DC, Z  
**Description:** Subtract W and the BORROW flag (CARRY) from register 'f' (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

**SWAPF**  
**Swap Nibbles in f**

**Syntax:** \[ label \] SWAPF f,d  
**Operands:**  
\[ 0 \leq f \leq 127 \]  
\[ d \in [0,1] \]  
**Operation:** \( (f<3:0>) \rightarrow (\text{destination}<7:4>), \)  
\( (f<7:4>) \rightarrow (\text{destination}<3:0>) \)  
**Status Affected:** None  
**Description:** The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

| C = 0 | W > k |
| C = 1 | W ≤ k |
| DC = 0 | W<3:0> > k<3:0> |
| DC = 1 | W<3:0> ≤ k<3:0> |
### TRIS

**Load TRIS Register with W**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ] TRIS f</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>$5 \leq f \leq 7$</td>
</tr>
<tr>
<td>Operation:</td>
<td>(W) $\rightarrow$ TRIS register ‘f’</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>None</td>
</tr>
<tr>
<td>Description:</td>
<td>Move data from W register to TRIS register. When ‘f’ = 5, TRISA is loaded. When ‘f’ = 6, TRISB is loaded. When ‘f’ = 7, TRISC is loaded.</td>
</tr>
</tbody>
</table>

### XORLW

**Exclusive OR literal with W**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ] XORLW k</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operands:</td>
<td>$0 \leq k \leq 255$</td>
</tr>
<tr>
<td>Operation:</td>
<td>(W) .XOR. k $\rightarrow$ (W)</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>Z</td>
</tr>
<tr>
<td>Description:</td>
<td>The contents of the W register are XOR’ed with the 8-bit literal ‘k’. The result is placed in the W register.</td>
</tr>
</tbody>
</table>

### XORWF

**Exclusive OR W with f**

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>[ label ] XORWF f,d</th>
</tr>
</thead>
</table>
| Operands: | $0 \leq f \leq 127$  
| | $d \in [0,1]$ |
| Operation: | (W) .XOR. (f) $\rightarrow$ (destination) |
| Status Affected: | Z |
| Description: | Exclusive OR the contents of the W register with register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’. |
30.0 ELECTRICAL SPECIFICATIONS

30.1 Absolute Maximum Ratings

Ambient temperature under bias ...................................................................................................... -40°C to +125°C
Storage temperature ........................................................................................................................ -65°C to +150°C

Voltage on pins with respect to Vss

- on VDD pin
  - PIC16F1784/6/7 ........................................................................................................ -0.3V to +6.5V
  - PIC16LF1784/6/7 ...................................................................................................... -0.3V to +4.0V
- on MCLR pin .......................................................................................................................... -0.3V to +9.0V
- on all other pins .................................................................................................................... -0.3V to (VDD + 0.3V)

Maximum current

- on Vss pin (1)
  - -40°C ≤ TA ≤ +85°C .................................................................................. 340 mA
  - -40°C ≤ TA ≤ +125°C .................................................................................. 140 mA
- on VDD pin (1)
  - -40°C ≤ TA ≤ +85°C (PIC16(L)F1786 only) .................................................. 170 mA
  - -40°C ≤ TA ≤ +125°C (PIC16(L)F1786 only) .................................................. 70 mA
  - -40°C ≤ TA ≤ +85°C .................................................................................. 340 mA
  - -40°C ≤ TA ≤ +125°C .................................................................................. 140 mA
- on any I/O pin .................................................................................................................... ±25 mA

Clamp current, IK (VPIN < 0 or VPIN > VDD) ........................................................................... ±20 mA

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Section 30.4 “Thermal Considerations” to calculate device specifications.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.
30.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:
Operating Voltage: \[ \text{VDDMIN} \leq \text{VDD} \leq \text{VDDMAX} \]
Operating Temperature: \[ \text{TA_MIN} \leq \text{TA} \leq \text{TA_MAX} \]

**VDD — Operating Supply Voltage**

PIC16LF1784/6/7

- \( \text{VDDMIN} (\text{Fosc} \leq 16 \text{ MHz}) \) ........................................................... +1.8V
- \( \text{VDDMIN} (16 \text{ MHz} < \text{Fosc} \leq 32 \text{ MHz}) \) ................................................ +2.5V
- \( \text{VDDMAX} \) ......................................................................................... +3.6V

PIC16F1784/6/7

- \( \text{VDDMIN} (\text{Fosc} \leq 16 \text{ MHz}) \) ........................................................... +2.3V
- \( \text{VDDMIN} (16 \text{ MHz} < \text{Fosc} \leq 32 \text{ MHz}) \) ................................................ +2.5V
- \( \text{VDDMAX} \) ......................................................................................... +5.5V

**TA — Operating Ambient Temperature Range**

Industrial Temperature

- \( \text{TA_MIN} \) ......................................................................................... -40°C
- \( \text{TA_MAX} \) ......................................................................................... +85°C

Extended Temperature

- \( \text{TA_MIN} \) ......................................................................................... -40°C
- \( \text{TA_MAX} \) ......................................................................................... +125°C

**Note 1:** See Parameter D001, DC Characteristics: Supply Voltage.
FIGURE 30-1: PIC16F1784/6/7 VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 30-6 for each Oscillator mode’s supported frequencies.

FIGURE 30-2: PIC16LF1784/6/7 VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 30-6 for each Oscillator mode’s supported frequencies.
30.3 DC Characteristics

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
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<tbody>
<tr>
<td>D001</td>
<td>VDD</td>
<td>Supply Voltage (VDDMIN, VDDMAX)</td>
<td>1.8</td>
<td>—</td>
<td>3.6</td>
<td>V</td>
<td>Fosc ≤ 16 MHz:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.5</td>
<td>—</td>
<td>3.6</td>
<td>V</td>
<td>Fosc ≤ 32 MHz (Note 2)</td>
</tr>
<tr>
<td>D001</td>
<td></td>
<td></td>
<td>2.3</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>Fosc ≤ 16 MHz:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.5</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>Fosc ≤ 32 MHz (Note 2)</td>
</tr>
<tr>
<td>D002*</td>
<td>VDR</td>
<td>RAM Data Retention Voltage(1)</td>
<td>1.5</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>Device in Sleep mode</td>
</tr>
<tr>
<td>D002*</td>
<td></td>
<td></td>
<td>1.7</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>Device in Sleep mode</td>
</tr>
<tr>
<td>VPOR*</td>
<td></td>
<td>Power-on Reset Release Voltage</td>
<td>—</td>
<td>1.6</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VPORR*</td>
<td></td>
<td>Power-on Reset Rearm Voltage</td>
<td>—</td>
<td>0.8</td>
<td>—</td>
<td>V</td>
<td>Device in Sleep mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>1.5</td>
<td>—</td>
<td>V</td>
<td>Device in Sleep mode</td>
</tr>
<tr>
<td>D003</td>
<td>VFVR</td>
<td>Fixed Voltage Reference Voltage(3)</td>
<td>-4</td>
<td>—</td>
<td>4</td>
<td>%</td>
<td>1.024V, VDD ≥ 2.5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-4</td>
<td>—</td>
<td>4</td>
<td>%</td>
<td>2.048V, VDD ≥ 2.5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-5</td>
<td>—</td>
<td>5</td>
<td>%</td>
<td>4.096V, VDD ≥ 4.75V</td>
</tr>
<tr>
<td>D004*</td>
<td>SVDD</td>
<td>VDD Rise Rate to ensure internal Power-on Reset signal</td>
<td>0.05</td>
<td>—</td>
<td>—</td>
<td>V/μs</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.
2: PLL required for 32 MHz operation.
3: Industrial temperature range only.
FIGURE 30-3: POR AND POR REARM WITH SLOW RISING VDD

Note 1: When NPOR is low, the device is held in Reset.
2: TPOR 1 μs typical.
3: TVLOW 2.7 μs typical.
### TABLE 30-2: SUPPLY VOLTAGE (IDD)\(^{(1,2)}\)

<table>
<thead>
<tr>
<th>PIC16LF1784/6/7</th>
<th>Standard Operating Conditions (unless otherwise stated)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC16F1784/6/7</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Device Characteristics</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D009</td>
<td>LDO Regulator</td>
<td>—</td>
<td>75</td>
<td>—</td>
<td>μA</td>
<td>— High Power mode, normal operation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>15</td>
<td>—</td>
<td>μA</td>
<td>— Sleep VREGCON&lt;1&gt; = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.3</td>
<td>—</td>
<td>μA</td>
<td>— Sleep VREGCON&lt;1&gt; = 1</td>
</tr>
<tr>
<td>D010</td>
<td></td>
<td>—</td>
<td>8</td>
<td>20</td>
<td>μA</td>
<td>1.8 FOSC = 32 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>12</td>
<td>24</td>
<td>μA</td>
<td>3.0 LP Oscillator mode (Note 4), -40°C ≤ TA ≤ +85°C</td>
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<tr>
<td>D010</td>
<td></td>
<td>—</td>
<td>18</td>
<td>63</td>
<td>μA</td>
<td>2.3 FOSC = 32 kHz</td>
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<tr>
<td></td>
<td></td>
<td>—</td>
<td>20</td>
<td>74</td>
<td>μA</td>
<td>3.0 LP Oscillator mode (Note 4, 5), -40°C ≤ TA ≤ +85°C</td>
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<tr>
<td></td>
<td></td>
<td>—</td>
<td>22</td>
<td>79</td>
<td>μA</td>
<td>5.0</td>
</tr>
<tr>
<td>D012</td>
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<td>—</td>
<td>160</td>
<td>650</td>
<td>μA</td>
<td>1.8 FOSC = 4 MHz</td>
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<tr>
<td></td>
<td></td>
<td>—</td>
<td>320</td>
<td>1000</td>
<td>μA</td>
<td>3.0 XT Oscillator mode (Note 5)</td>
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<tr>
<td>D012</td>
<td></td>
<td>—</td>
<td>260</td>
<td>700</td>
<td>μA</td>
<td>2.3 FOSC = 4 MHz</td>
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<tr>
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<td>—</td>
<td>330</td>
<td>1100</td>
<td>μA</td>
<td>3.0 XT Oscillator mode (Note 5)</td>
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<td>—</td>
<td>380</td>
<td>1300</td>
<td>μA</td>
<td>5.0</td>
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</table>

**Note**  
1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.  
2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.  
3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.  
4: FVR and BOR are disabled.  
5: 0.1 μF capacitor on VCAP.  
6: 8 MHz crystal oscillator with 4x PLL enabled.
### TABLE 30-2: SUPPLY VOLTAGE (I\text{DD})^{(1,2)} (CONTINUED)

<table>
<thead>
<tr>
<th>PIC16F1784/6/7</th>
<th>Standard Operating Conditions (unless otherwise stated)</th>
</tr>
</thead>
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<td><strong>PIC16F1784/6/7</strong></td>
<td><strong>Param No.</strong></td>
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</tr>
<tr>
<td></td>
<td>—</td>
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<tr>
<td><strong>D014</strong></td>
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<td>—</td>
</tr>
<tr>
<td><strong>D015</strong></td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td><strong>D015</strong></td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td><strong>D017</strong></td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td><strong>D017</strong></td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td><strong>D019</strong></td>
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</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td><strong>D019</strong></td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td><strong>D020</strong></td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td><strong>D020</strong></td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td><strong>D022</strong></td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>—</td>
</tr>
<tr>
<td><strong>D022</strong></td>
<td>—</td>
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</table>

**Note 1:** The test conditions for all I\text{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V\text{DD}; MCLR = V\text{DD}; WDT disabled.

**Note 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

**Note 3:** For RC oscillator configurations, current through R\text{EXT} is not included. The current through the resistor can be extended by the formula \(I_R = V\text{DD}/2R\text{EXT}\) (mA) with R\text{EXT} in kΩ.

**Note 4:** FVR and BOR are disabled.

**Note 5:** 0.1 μF capacitor on V\text{CAP}.

**Note 6:** 8 MHz crystal oscillator with 4x PLL enabled.
**TABLE 30-3: POWER-DOWN CURRENTS \(I_{PD}\)\(^{(1,2,4)}\)**

<table>
<thead>
<tr>
<th>PIC16F1784/6/7</th>
<th>Operating Conditions: (unless otherwise stated) Low-Power Sleep Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC16F1784/6/7</td>
<td>Low-Power Sleep Mode, VREGPM = 1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Device Characteristics</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max. +85°C</th>
<th>Max. +125°C</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D023</td>
<td>Power-down Base Current (I_{PD})(^{(2)})</td>
<td>—</td>
<td>0.05</td>
<td>1.0</td>
<td>8.0</td>
<td>µA</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.08</td>
<td>2.0</td>
<td>9.0</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td>D023</td>
<td>Base (I_{PD})</td>
<td>—</td>
<td>0.3</td>
<td>3</td>
<td>11</td>
<td>µA</td>
<td>2.3</td>
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<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.4</td>
<td>4</td>
<td>12</td>
<td>µA</td>
<td>3.0</td>
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<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.5</td>
<td>6</td>
<td>15</td>
<td>µA</td>
<td>5.0</td>
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<tr>
<td>D023A</td>
<td>Base (I_{PD})</td>
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<td>10</td>
<td>16</td>
<td>18</td>
<td>µA</td>
<td>2.3</td>
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<td></td>
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<td></td>
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<td>6</td>
<td>15</td>
<td>µA</td>
<td>2.3</td>
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<tr>
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<td>7</td>
<td>20</td>
<td>µA</td>
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<td>1.0</td>
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<td>µA</td>
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<td>12</td>
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<td>µA</td>
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<td>µA</td>
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<td>µA</td>
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<td>µA</td>
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<td>8.5</td>
<td>20</td>
<td>µA</td>
<td>3.0</td>
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<td>—</td>
<td>1.4</td>
<td>10</td>
<td>25</td>
<td>µA</td>
<td>5.0</td>
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</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The peripheral current is the sum of the base \(I_{PD}\) and the additional current consumed when this peripheral is enabled. The peripheral \(\Delta\) current can be determined by subtracting the base \(I_{O}\) or \(I_{PD}\) current from this limit. Max values should be used when calculating total current consumption.

**2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to Vss.

**3:** ADC oscillator source is FRC.

**4:** 0.1 µF capacitor on VCAP.

**5:** VREGPM = 0.
### TABLE 30-3: POWER-DOWN CURRENTS (IPD) (1,2,4) (CONTINUED)

<table>
<thead>
<tr>
<th>PIC16LF1784/6/7</th>
<th>Operating Conditions: (unless otherwise stated) Low-Power Sleep Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-Power Sleep Mode, VREGPM = 1</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Device Characteristics</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max. +85°C</th>
<th>Max. +125°C</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D029</td>
<td>Power-down Base Current (IPD) (2)</td>
<td>—</td>
<td>0.05</td>
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<td>9</td>
<td>µA</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
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<td>0.08</td>
<td>3</td>
<td>10</td>
<td>µA</td>
<td>3.0</td>
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<td>D029</td>
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<td>—</td>
<td>350</td>
<td>—</td>
<td>—</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td>D031</td>
<td></td>
<td>—</td>
<td>250</td>
<td>650</td>
<td>—</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>350</td>
<td>850</td>
<td>—</td>
<td>µA</td>
<td>5.0</td>
</tr>
<tr>
<td>D032</td>
<td></td>
<td>—</td>
<td>250</td>
<td>650</td>
<td>—</td>
<td>µA</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>300</td>
<td>700</td>
<td>—</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td>D032</td>
<td></td>
<td>—</td>
<td>280</td>
<td>650</td>
<td>—</td>
<td>µA</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>300</td>
<td>700</td>
<td>—</td>
<td>µA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>310</td>
<td>700</td>
<td>—</td>
<td>µA</td>
<td>5.0</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The peripheral current is the sum of the base IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

**Note 2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VSS.

**Note 3:** ADC oscillator source is FRC.

**Note 4:** 0.1 µF capacitor on VCAP.

**Note 5:** VREGPM = 0.
### TABLE 30-4: I/O PORTS

**Standard Operating Conditions (unless otherwise stated)**

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D034</td>
<td></td>
<td>Input Low Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D034A</td>
<td></td>
<td>I/O PORT:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>with TTL buffer</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>4.5V ≤ VDD ≤ 5.5V</td>
</tr>
<tr>
<td>D035</td>
<td></td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D036</td>
<td></td>
<td>with Schmitt Trigger buffer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D036A</td>
<td></td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>with I²C™ levels</td>
<td>—</td>
<td>—</td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>MCLR, OSC1 (RC mode)(1)</td>
<td>—</td>
<td>—</td>
<td>0.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>OSC1 (HS mode)</td>
<td>—</td>
<td>—</td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D040</td>
<td></td>
<td>Input High Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D040A</td>
<td></td>
<td>I/O ports:</td>
<td>—</td>
<td>—</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>with TTL buffer</td>
<td>2.0</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>4.5V ≤ VDD ≤ 5.5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.25 VDD + 0.8</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>1.8V ≤ VDD ≤ 4.5V</td>
</tr>
<tr>
<td>D041</td>
<td></td>
<td>with Schmitt Trigger buffer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D041A</td>
<td></td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>with I²C™ levels</td>
<td>0.8</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>2.0V ≤ VDD ≤ 5.5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.7 VDD</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>MCLR</td>
<td>2.1</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>2.7V ≤ VDD ≤ 5.5V</td>
</tr>
<tr>
<td>D042</td>
<td></td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D043A</td>
<td></td>
<td>OSC1 (HS mode)</td>
<td>0.8</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D043B</td>
<td></td>
<td>OSC1 (RC mode)</td>
<td>0.9</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D060</td>
<td></td>
<td>Input Leakage Current(2)</td>
<td>—</td>
<td>± 5</td>
<td>± 125</td>
<td>nA</td>
<td>VSS ≤ VPIN ≤ VDD, Pin at high-impedance @ 85°C</td>
</tr>
<tr>
<td>D061</td>
<td></td>
<td>MCLR(3)</td>
<td>—</td>
<td>± 5</td>
<td>± 1000</td>
<td>nA</td>
<td>125°C</td>
</tr>
<tr>
<td>D070*</td>
<td></td>
<td>Weak Pull-up Current</td>
<td>25</td>
<td>100</td>
<td>300</td>
<td>µA</td>
<td>VDD = 3.3V, VPIN = VSS</td>
</tr>
<tr>
<td>D070</td>
<td></td>
<td></td>
<td>25</td>
<td>140</td>
<td>300</td>
<td>µA</td>
<td>VDD = 5.0V, VPIN = VSS</td>
</tr>
<tr>
<td>D080</td>
<td></td>
<td>Output Low Voltage(4)</td>
<td>—</td>
<td>—</td>
<td>0.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D090</td>
<td></td>
<td>Output High Voltage(4)</td>
<td>—</td>
<td>—</td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

**Note 2:** Negative current is defined as current sourced by the pin.

**Note 3:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**Note 4:** Including OSC2 in CLKOUT mode.
### Capacitive Loading Specs on Output Pins

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D101*</td>
<td>COSC2</td>
<td>OSC2 pin</td>
<td>—</td>
<td>—</td>
<td>15</td>
<td>pF</td>
<td>In XT, HS and LP modes when external clock is used to drive OSC1</td>
</tr>
<tr>
<td>D101A*</td>
<td>Cio</td>
<td>All I/O pins</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

### VCap Capacitor Charging

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D102</td>
<td></td>
<td>Charging current</td>
<td>—</td>
<td>200</td>
<td>—</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>D102A</td>
<td></td>
<td>Source/sink capability when charging complete</td>
<td>—</td>
<td>0.0</td>
<td>—</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

**Note 2:** Negative current is defined as current sourced by the pin.

**Note 3:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**Note 4:** Including OSC2 in CLKOUT mode.
### TABLE 30-5: MEMORY PROGRAMMING REQUIREMENTS

#### Standard Operating Conditions (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D110</td>
<td>VIHH</td>
<td>Program Memory Programming Specifications</td>
<td>8.0</td>
<td>—</td>
<td>9.0</td>
<td>V</td>
<td>(Note 3)</td>
</tr>
<tr>
<td>D111</td>
<td>IDDIP</td>
<td>Voltage on MCLR/VPP/RE3 pin Supply Current during Programming</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>D112</td>
<td>VDD</td>
<td>Supply Current during Programming VDD for Bulk Erase</td>
<td>2.7</td>
<td>—</td>
<td>VDDMAX</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D113</td>
<td>VPEW</td>
<td>VDD for Write or Row Erase</td>
<td>VDDMIN</td>
<td>—</td>
<td>VDDMAX</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D114</td>
<td>IPPGM</td>
<td>Current on MCLR/VPP during Erase/Write</td>
<td>—</td>
<td>—</td>
<td>1.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>D115</td>
<td>IDDPGM</td>
<td>Current on VDD during Erase/Write</td>
<td>—</td>
<td>—</td>
<td>5.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>D116</td>
<td>ED</td>
<td>Byte Endurance</td>
<td>100K</td>
<td>—</td>
<td>—</td>
<td>E/W</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>D117</td>
<td>VDRW</td>
<td>VDD for Read/Write</td>
<td>VDDMIN</td>
<td>—</td>
<td>VDDMAX</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D118</td>
<td>TDEW</td>
<td>Erase/Write Cycle Time</td>
<td>—</td>
<td>4.0</td>
<td>5.0</td>
<td>ms</td>
<td>Provided no other specifications are violated</td>
</tr>
<tr>
<td>D119</td>
<td>TRET</td>
<td>Characteristic Retention</td>
<td>—</td>
<td>40</td>
<td>—</td>
<td>Year</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>D120</td>
<td>TREF</td>
<td>Number of Total Erase/Write Cycles before Refresh(2)</td>
<td>100k</td>
<td>—</td>
<td>—</td>
<td>E/W</td>
<td></td>
</tr>
<tr>
<td>D121</td>
<td>EP</td>
<td>Cell Endurance</td>
<td>10K</td>
<td>—</td>
<td>—</td>
<td>E/W</td>
<td>-40°C to +85°C (Note 1)</td>
</tr>
<tr>
<td>D122</td>
<td>VPR</td>
<td>VDD for Read</td>
<td>VDDMIN</td>
<td>—</td>
<td>VDDMAX</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D123</td>
<td>TiW</td>
<td>Self-timed Write Cycle Time</td>
<td>—</td>
<td>2</td>
<td>2.5</td>
<td>ms</td>
<td>Provided no other specifications are violated</td>
</tr>
<tr>
<td>D124</td>
<td>TRET</td>
<td>Characteristic Retention</td>
<td>—</td>
<td>40</td>
<td>—</td>
<td>Year</td>
<td></td>
</tr>
</tbody>
</table>

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Self-write and Block Erase.

2: Refer to Section 12.2 “Using the Data EEPROM” for a more detailed discussion on data EEPROM endurance.

3: Required only if single-supply programming is disabled.
### 30.4 Thermal Considerations

#### Standard Operating Conditions (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Typ.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>TH01</td>
<td>θJA</td>
<td>Thermal Resistance Junction to Ambient</td>
<td>60</td>
<td>°C/W</td>
<td>28-pin SPDIP package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>80</td>
<td>°C/W</td>
<td>28-pin SOIC package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>90</td>
<td>°C/W</td>
<td>28-pin SSOP package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>27.5</td>
<td>°C/W</td>
<td>28-pin QFN 6x6mm package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>47.2</td>
<td>°C/W</td>
<td>40-pin DIP package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>41</td>
<td>°C/W</td>
<td>40-pin UQFN 5x5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>46</td>
<td>°C/W</td>
<td>44-pin TQFP package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>24.4</td>
<td>°C/W</td>
<td>44-pin QFN 8x8mm package</td>
</tr>
<tr>
<td>TH02</td>
<td>θJC</td>
<td>Thermal Resistance Junction to Case</td>
<td>31.4</td>
<td>°C/W</td>
<td>28-pin SPDIP package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>24</td>
<td>°C/W</td>
<td>28-pin SOIC package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>24</td>
<td>°C/W</td>
<td>28-pin SSOP package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>24</td>
<td>°C/W</td>
<td>28-pin QFN 6x6mm package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>24.7</td>
<td>°C/W</td>
<td>40-pin DIP package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5.5</td>
<td>°C/W</td>
<td>40-pin UQFN 5x5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>14.5</td>
<td>°C/W</td>
<td>44-pin TQFP package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20</td>
<td>°C/W</td>
<td>44-pin QFN 8x8mm package</td>
</tr>
<tr>
<td>TH03</td>
<td>TJMAX</td>
<td>Maximum Junction Temperature</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>TH04</td>
<td>PD</td>
<td>Power Dissipation</td>
<td>—</td>
<td>W</td>
<td>PD = PINTERNAL + PI/O</td>
</tr>
<tr>
<td>TH05</td>
<td>PINTERNAL</td>
<td>Internal Power Dissipation</td>
<td>—</td>
<td>W</td>
<td>PINTERNAL = IDD x VDD(1)</td>
</tr>
<tr>
<td>TH06</td>
<td>PI/O</td>
<td>I/O Power Dissipation</td>
<td>—</td>
<td>W</td>
<td>PI/O = Σ (IOL x VOL) + Σ (IOH x (VDD - VOH))</td>
</tr>
<tr>
<td>TH07</td>
<td>PDER</td>
<td>Derated Power</td>
<td>—</td>
<td>W</td>
<td>PDER = PDMAX (TJ - TA)/θJA(2)</td>
</tr>
</tbody>
</table>

**Note 1:** IDD is current to run the chip alone without driving any load on the output pins.

2. **TA** = Ambient Temperature

3. **TJ** = Junction Temperature
30.5 AC Characteristics

Timing Parameter Symbology has been created with one of the following formats:

1. TppS2ppS
2. TppS

<table>
<thead>
<tr>
<th>T</th>
<th>F</th>
<th>Frequency</th>
<th>T</th>
<th>Time</th>
</tr>
</thead>
</table>

Lowercase letters (pp) and their meanings:

- **cc**: CCP1
- **ck**: CLKOUT
- **cs**: CS
- **di**: SDI
- **do**: SDO
- **dt**: Data In
- **io**: I/O PORT
- **mc**: MCLR

<table>
<thead>
<tr>
<th>Uppercase letters and their meanings:</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>S</strong></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

**FIGURE 30-4: LOAD CONDITIONS**

Load Condition

Legend: CL=50 pF for all pins
### FIGURE 30-5: CLOCK TIMING

![Clock Timing Diagram](image)

### TABLE 30-6: CLOCK OSCILLATOR TIMING REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS01</td>
<td>Fosc</td>
<td>External CLKIN Frequency(^{(1)})</td>
<td>DC</td>
<td>—</td>
<td>0.5</td>
<td>MHz</td>
<td>EC Oscillator mode (low)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DC</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
<td>EC Oscillator mode (medium)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DC</td>
<td>—</td>
<td>20</td>
<td>MHz</td>
<td>EC Oscillator mode (high)</td>
</tr>
<tr>
<td></td>
<td>Oscillator Frequency(^{(1)})</td>
<td>—</td>
<td>32.768</td>
<td>—</td>
<td>kHz</td>
<td>LP Oscillator mode</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.1</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
<td>XT Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
<td>HS Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>—</td>
<td>20</td>
<td>MHz</td>
<td>HS Oscillator mode, VDD &gt; 2.7V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DC</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
<td>RC Oscillator mode, VDD &gt; 2.0V</td>
</tr>
<tr>
<td>OS02</td>
<td>Tosc</td>
<td>External CLKIN Period(^{(1)})</td>
<td>27</td>
<td>—</td>
<td>—</td>
<td>μs</td>
<td>LP Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>250</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>XT Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>HS Oscillator mode</td>
</tr>
<tr>
<td></td>
<td>Oscillator Period(^{(1)})</td>
<td>30.5</td>
<td>—</td>
<td>—</td>
<td>μs</td>
<td>LP Oscillator mode</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>250</td>
<td>—</td>
<td>10,000</td>
<td>ns</td>
<td>XT Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>—</td>
<td>1,000</td>
<td>ns</td>
<td>HS Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>250</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>RC Oscillator mode</td>
</tr>
<tr>
<td>OS03</td>
<td>Tcy</td>
<td>Instruction Cycle Time(^{(1)})</td>
<td>200</td>
<td>Tcy</td>
<td>DC</td>
<td>ns</td>
<td>Tcy = 4/Fosc</td>
</tr>
<tr>
<td>OS04(^*)</td>
<td>TosH,</td>
<td>External CLKIN High,</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>μs</td>
<td>LP oscillator</td>
</tr>
<tr>
<td></td>
<td>TosL</td>
<td>External CLKIN Low</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>XT oscillator</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>HS oscillator</td>
</tr>
<tr>
<td>OS05(^*)</td>
<td>TosR,</td>
<td>External CLKIN Rise,</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>LP oscillator</td>
</tr>
<tr>
<td></td>
<td>TosF</td>
<td>External CLKIN Fall</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>XT oscillator</td>
</tr>
</tbody>
</table>

\(^*\) These parameters are characterized but not tested.

\(^†\) Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock applied to OSC1 pin. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.
## TABLE 30-7: OSCILLATOR PARAMETERS

### Standard Operating Conditions (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Freq. Tolerance</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS08</td>
<td>HFosc</td>
<td>Internal Calibrated HFINTOSC Frequency(^{(2)})</td>
<td>±2%</td>
<td>—</td>
<td>16.0</td>
<td>MHz</td>
<td>0°C ≤ TA ≤ 60°C, VDD ≥ 2.5V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>±3%</td>
<td>—</td>
<td>16.0</td>
<td>MHz</td>
<td>60°C ≤ TA ≤ 85°C, VDD ≥ 2.5V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>±5%</td>
<td>—</td>
<td>16.0</td>
<td>MHz</td>
<td>-40°C ≤ TA ≤ +125°C</td>
<td></td>
</tr>
<tr>
<td>OS08A</td>
<td>MFosc</td>
<td>Internal Calibrated MFINTOSC Frequency(^{(2)})</td>
<td>±2%</td>
<td>—</td>
<td>500</td>
<td>kHz</td>
<td>0°C ≤ TA ≤ 60°C, VDD ≥ 2.5V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>±3%</td>
<td>—</td>
<td>500</td>
<td>kHz</td>
<td>60°C ≤ TA ≤ 85°C, VDD ≥ 2.5V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>±5%</td>
<td>—</td>
<td>500</td>
<td>kHz</td>
<td>-40°C ≤ TA ≤ +125°C</td>
<td></td>
</tr>
<tr>
<td>OS09</td>
<td>LFosc</td>
<td>Internal LFINTOSC Frequency</td>
<td>—</td>
<td>—</td>
<td>31</td>
<td>kHz</td>
<td>-40°C ≤ TA ≤ +125°C</td>
<td></td>
</tr>
<tr>
<td>OS10*</td>
<td>Tiosc</td>
<td>Start-up Time</td>
<td>—</td>
<td>—</td>
<td>3.2</td>
<td>8 µs</td>
<td>VREGPM = 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Wake-up from Sleep Start-up Time</td>
<td>—</td>
<td>—</td>
<td>24</td>
<td>35 µs</td>
<td>VREGPM = 0</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

### Note 1:
Instruction cycle period (TCy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

### Note 2:
To ensure these oscillator frequency tolerances, VCC and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

### Note 3:
By design.

## FIGURE 30-6: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE

![HFINTOSC Frequency Accuracy Over Device VDD and Temperature](image-url)
TABLE 30-8: PLL CLOCK TIMING SPECIFICATIONS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>F10</td>
<td>FOSC</td>
<td>Oscillator Frequency Range</td>
<td>4</td>
<td>—</td>
<td>8</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>F11</td>
<td>FSYS</td>
<td>On-Chip VCO System Frequency</td>
<td>16</td>
<td>—</td>
<td>32</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>F12</td>
<td>TRC</td>
<td>PLL Start-up Time (Lock Time)</td>
<td>—</td>
<td>—</td>
<td>2</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>F13*</td>
<td>△CLK</td>
<td>CLKOUT Stability (Jitter)</td>
<td>-0.25%</td>
<td>—</td>
<td>+0.25%</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 30-7: CLKOUT AND I/O TIMING
### TABLE 30-9: CLKOUT AND I/O TIMING PARAMETERS

**Standard Operating Conditions (unless otherwise stated)**

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS11</td>
<td>Tosh2ckL</td>
<td>Fosc↑ to CLKOUT↓&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>—</td>
<td>—</td>
<td>70</td>
<td>ns</td>
<td>VDD = 3.3-5.0V</td>
</tr>
<tr>
<td>OS12</td>
<td>Tosh2ckH</td>
<td>Fosc↑ to CLKOUT↑&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>—</td>
<td>—</td>
<td>72</td>
<td>ns</td>
<td>VDD = 3.3-5.0V</td>
</tr>
<tr>
<td>OS13</td>
<td>Tckl2ioV</td>
<td>CLKOUT↓ to Port out valid&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OS14</td>
<td>TioV2ckH</td>
<td>Port input valid before CLKOUT↑&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>Tosc + 200 ns</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OS15</td>
<td>Tosh2ioV</td>
<td>Fosc↑ (Q1 cycle) to Port out valid</td>
<td>—</td>
<td>50</td>
<td>70*</td>
<td>ns</td>
<td>VDD = 3.3-5.0V</td>
</tr>
<tr>
<td>OS16</td>
<td>Tosh2iol</td>
<td>Fosc↑ (Q2 cycle) to Port input invalid</td>
<td>50</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>VDD = 3.3-5.0V</td>
</tr>
<tr>
<td>OS17</td>
<td>TioV2osH</td>
<td>Port input valid to Fosc↑ (Q2 cycle)</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OS18*</td>
<td>TioR</td>
<td>Port output rise time</td>
<td>—</td>
<td>40</td>
<td>72</td>
<td>32</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>15</td>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OS19*</td>
<td>TioF</td>
<td>Port output fall time</td>
<td>—</td>
<td>28</td>
<td>55</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>15</td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OS20*</td>
<td>Tinp</td>
<td>INT pin input high or low time</td>
<td>25</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OS21*</td>
<td>Tioc</td>
<td>Interrupt-on-change new input level time</td>
<td>25</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated.

**Note 1:** Measurements are taken in RC mode where CLKOUT output is 4 x Tosc.
FIGURE 30-8:  RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

VDD
MCLR
Internal POR
PWRT Time-out
OSC Start-up Time
Internal Reset(1)
Watchdog Timer Reset(1)
I/O pins

Note 1:  Asserted low.

FIGURE 30-9:  BROWN-OUT RESET TIMING AND CHARACTERISTICS

VDD VBOR VBOR and VHYST
( Device in Brown-out Reset)

Reset (due to BOR)

Note 1:  The delay, (TPWRT) releasing Reset, only occurs when the Power-up Timer is enabled, (PWRTE = 0).
**TABLE 30-10:  RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS**

**Standard Operating Conditions** (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>TMCL</td>
<td>MCLR Pulse Width (low)</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td>VDD = 3.3-5V, -40°C to +85°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td>VDD = 3.3-5V</td>
</tr>
<tr>
<td>31</td>
<td>TWDTLP</td>
<td>Low-Power Watchdog Timer</td>
<td>10</td>
<td>16</td>
<td>27</td>
<td>ms</td>
<td>VDD = 3.3V-5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Time-out Period</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1:16 Prescaler used</td>
</tr>
<tr>
<td>32</td>
<td>TOST</td>
<td>Oscillator Start-up Timer Period</td>
<td>—</td>
<td>1024</td>
<td>—</td>
<td>Tosc</td>
<td>(Note 3)</td>
</tr>
<tr>
<td>33*</td>
<td>TPWRT</td>
<td>Power-up Timer Period, PWRTE = 0</td>
<td>40</td>
<td>65</td>
<td>140</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>34*</td>
<td>TOIZ</td>
<td>I/O high-impedance from MCLR Low or Watchdog Timer Reset</td>
<td>—</td>
<td>—</td>
<td>2.0</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>VBOR</td>
<td>Brown-out Reset Voltage</td>
<td>2.55</td>
<td>2.70</td>
<td>2.85</td>
<td>V</td>
<td>BORV = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.30</td>
<td>2.45</td>
<td>2.6</td>
<td>V</td>
<td>BORV=1 (F device)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.80</td>
<td>1.90</td>
<td>2.10</td>
<td>V</td>
<td>BORV=1 (LF device)</td>
</tr>
<tr>
<td>35A</td>
<td>VLPBOR</td>
<td>Low-Power Brown-out</td>
<td>1.8</td>
<td>2.1</td>
<td>2.5</td>
<td>V</td>
<td>LPBOR = 1</td>
</tr>
<tr>
<td>36*</td>
<td>VHYST</td>
<td>Brown-out Reset Hysteresis</td>
<td>0</td>
<td>25</td>
<td>75</td>
<td>mV</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>37*</td>
<td>TBORDC</td>
<td>Brown-out Reset DC Response Time</td>
<td>1</td>
<td>3</td>
<td>35</td>
<td>µs</td>
<td>VDD ≤ VBOR</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

2: By design.
3: Period of the slower clock.
4: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.
TABLE 30-11: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>40*</td>
<td>T0H</td>
<td>T0CKI High Pulse Width</td>
<td>0.5 Tcy + 20</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>No Prescaler</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>41*</td>
<td>T0L</td>
<td>T0CKI Low Pulse Width</td>
<td>0.5 Tcy + 20</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>No Prescaler</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>42*</td>
<td>T0P</td>
<td>T0CKI Period</td>
<td>Greater of:</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>20 or Tcy + 40 N</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td>N = prescale value (2, 4, ..., 256)</td>
</tr>
<tr>
<td>45*</td>
<td>T1H</td>
<td>T1CKI High Time</td>
<td>0.5 Tcy + 20</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Synchronous, No Prescaler</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Synchronous, with Prescaler</td>
<td>15</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Asynchronous</td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>46*</td>
<td>T1L</td>
<td>T1CKI Low Time</td>
<td>0.5 Tcy + 20</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Synchronous, No Prescaler</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Synchronous, with Prescaler</td>
<td>15</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Asynchronous</td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>47*</td>
<td>T1P</td>
<td>T1CKI Input Period</td>
<td>Greater of:</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>30 or Tcy + 40 N</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td>N = prescale value (1, 2, 4, 8)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Synchronous</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Asynchronous</td>
<td>60</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>48</td>
<td>F1</td>
<td>Timer1 Oscillator Input Frequency Range</td>
<td>32.4</td>
<td>32.768</td>
<td>33.1</td>
<td>kHz</td>
<td>(oscillator enabled by setting bit T1OSCEN)</td>
</tr>
<tr>
<td>49*</td>
<td>TCEZE0</td>
<td>Delay from External Clock Edge to Timer Increment</td>
<td>2 Tosc</td>
<td></td>
<td>7 Tosc</td>
<td></td>
<td>Timers in Sync mode</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
FIGURE 30-11: CAPTURE/COMPARE/PWM TIMINGS (CCP)

![Diagram showing capture/compare/pwm timings](image)

Note: Refer to Figure 30-5 for load conditions.

TABLE 30-12: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC01*</td>
<td>TccL</td>
<td>CCPx Input Low Time</td>
<td>No Prescaler</td>
<td>0.5Tcy + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>CC02*</td>
<td>TccH</td>
<td>CCPx Input High Time</td>
<td>No Prescaler</td>
<td>0.5Tcy + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>CC03*</td>
<td>TccP</td>
<td>CCPx Input Period</td>
<td>3Tcy + 40N</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>N = prescale value (1, 4 or 16)</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
### TABLE 30-13: ADC CONVERTER (ADC) 12-BIT DIFFERENTIAL CHARACTERISTICS:

**Operating Conditions**  
VDD = 3V, Temp. = 25°C, Single-ended 2 µs TAD, VREF+ = 3V, VREF- = VSS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Symp</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD01</td>
<td>NR</td>
<td>Resolution</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>bit</td>
<td></td>
</tr>
<tr>
<td>AD02</td>
<td>EIL</td>
<td>Integral Error</td>
<td>±1</td>
<td>±1.6</td>
<td>1.6</td>
<td>LSb</td>
<td></td>
</tr>
<tr>
<td>AD03</td>
<td>EDL</td>
<td>Differential Error</td>
<td>±1</td>
<td>±1.4</td>
<td>1.4</td>
<td>LSb</td>
<td>No missing codes</td>
</tr>
<tr>
<td>AD04</td>
<td>EOFF</td>
<td>Offset Error</td>
<td>±1</td>
<td>±3.5</td>
<td>3.5</td>
<td>LSb</td>
<td></td>
</tr>
<tr>
<td>AD05</td>
<td>EGN</td>
<td>Gain Error</td>
<td>±1</td>
<td>±2</td>
<td>2</td>
<td>LSb</td>
<td></td>
</tr>
<tr>
<td>AD06</td>
<td>VREF</td>
<td>Reference Voltage(3)</td>
<td>1.8</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>AD07</td>
<td>VAIN</td>
<td>Full-Scale Range</td>
<td>—</td>
<td>VREF</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AD08</td>
<td>ZAIN</td>
<td>Recommended Impedance of Analog Voltage Source</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>kΩ</td>
<td>Can go higher if external 0.01µF capacitor is present on input pin.</td>
</tr>
<tr>
<td>AD09</td>
<td>NR</td>
<td>Resolution</td>
<td>—</td>
<td>—</td>
<td>12</td>
<td>bit</td>
<td></td>
</tr>
<tr>
<td>AD10</td>
<td>EIL</td>
<td>Integral Error</td>
<td>±2</td>
<td>—</td>
<td>—</td>
<td>LSb</td>
<td></td>
</tr>
<tr>
<td>AD11</td>
<td>EDL</td>
<td>Differential Error</td>
<td>±2</td>
<td>—</td>
<td>—</td>
<td>LSb</td>
<td></td>
</tr>
<tr>
<td>AD12</td>
<td>EOFF</td>
<td>Offset Error</td>
<td>±1</td>
<td>—</td>
<td>—</td>
<td>LSb</td>
<td></td>
</tr>
<tr>
<td>AD13</td>
<td>EGN</td>
<td>Gain Error</td>
<td>±1</td>
<td>—</td>
<td>—</td>
<td>LSb</td>
<td></td>
</tr>
<tr>
<td>AD14</td>
<td>VREF</td>
<td>Reference Voltage(3)</td>
<td>1.8</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>AD15</td>
<td>VAIN</td>
<td>Full-Scale Range</td>
<td>—</td>
<td>VREF</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AD16</td>
<td>ZAIN</td>
<td>Recommended Impedance of Analog Voltage Source</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>kΩ</td>
<td>Can go higher if external 0.01µF capacitor is present on input pin.</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.  
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.  

**Note 1:** Total Absolute Error includes integral, differential, offset and gain errors.  
2: The ADC conversion result never decreases with an increase in the input voltage and has no missing codes.  
3: ADC VREF is from external VREF, VDD pin or FVR, whichever is selected as reference input.  
4: When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.

### TABLE 30-14: ADC CONVERSION REQUIREMENTS

**Standard Operating Conditions** (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Symp</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD130</td>
<td>TAD</td>
<td>ADC Clock Period</td>
<td>1.0</td>
<td>—</td>
<td>9.0</td>
<td>µs</td>
<td>Tosc-based</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ADC Internal RC Oscillator Period</td>
<td>1.0</td>
<td>2.5</td>
<td>6.0</td>
<td>µs</td>
<td>ADCS&lt;1:0&gt; = 11 (ADRC mode)</td>
</tr>
<tr>
<td>AD131</td>
<td>TCNV</td>
<td>Conversion Time (not including Acquisition Time)(1)</td>
<td>—</td>
<td>15 (12-bit)</td>
<td>13 (10-bit)</td>
<td>—</td>
<td>TAD</td>
</tr>
<tr>
<td>AD132</td>
<td>TACQ</td>
<td>Acquisition Time</td>
<td>—</td>
<td>5.0</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.  
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.  

**Note 1:** The ADRES register may be read on the following TCY cycle.
FIGURE 30-12: ADC CONVERSION TIMING (NORMAL MODE)

Note 1: If the ADC clock source is selected as RC, a time of TCY is added before the ADC clock starts. This allows the SLEEP instruction to be executed.

FIGURE 30-13: ADC CONVERSION TIMING (SLEEP MODE)

Note 1: If the ADC clock source is selected as RC, a time of TCY is added before the ADC clock starts. This allows the SLEEP instruction to be executed.
### TABLE 30-15: OPERATIONAL AMPLIFIER (OPA)

**DC CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Symbol</th>
<th>Parameters</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA01*</td>
<td>GBWP</td>
<td>Gain Bandwidth Product</td>
<td>—</td>
<td>3.5</td>
<td>—</td>
<td>MHz</td>
<td>High-Power mode</td>
</tr>
<tr>
<td>OPA02*</td>
<td>TON</td>
<td>Turn on Time</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>OPA03*</td>
<td>PM</td>
<td>Phase Margin</td>
<td>—</td>
<td>60</td>
<td>—</td>
<td>degrees</td>
<td></td>
</tr>
<tr>
<td>OPA04*</td>
<td>SR</td>
<td>Slew Rate</td>
<td>—</td>
<td>3</td>
<td>—</td>
<td>V/μs</td>
<td></td>
</tr>
<tr>
<td>OPA05</td>
<td>OFF</td>
<td>Offset</td>
<td>—</td>
<td>±3</td>
<td>±9</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>OPA06</td>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>55</td>
<td>70</td>
<td>—</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>OPA07*</td>
<td>AOL</td>
<td>Open Loop Gain</td>
<td>—</td>
<td>90</td>
<td>—</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>OPA08</td>
<td>VCM</td>
<td>Input Common Mode Voltage</td>
<td>0</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
<td>VDD &gt; 2.5</td>
</tr>
<tr>
<td>OPA09*</td>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>—</td>
<td>80</td>
<td>—</td>
<td>dB</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.

**Operating Conditions:**

**VDD = 3.0V, Temperature = 25°C (unless otherwise stated).**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CM01</td>
<td>VIOFF</td>
<td>Input Offset Voltage</td>
<td>—</td>
<td>±2.5</td>
<td>±9</td>
<td>mV</td>
<td>Normal-Power mode VCM = VDD/2</td>
</tr>
<tr>
<td>CM02</td>
<td>VCM</td>
<td>Input Common Mode Voltage</td>
<td>0</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CM03</td>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>40</td>
<td>50</td>
<td>—</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>CM04A</td>
<td>TRESP</td>
<td>Response Time Rising Edge</td>
<td>—</td>
<td>60</td>
<td>125</td>
<td>ns</td>
<td>Normal-Power mode measured at VDD/2 (Note 1)</td>
</tr>
<tr>
<td>CM04B</td>
<td></td>
<td>Response Time Falling Edge</td>
<td>—</td>
<td>60</td>
<td>110</td>
<td>ns</td>
<td>Normal-Power mode measured at VDD/2 (Note 1)</td>
</tr>
<tr>
<td>CM04C</td>
<td></td>
<td>Response Time Rising Edge</td>
<td>—</td>
<td>85</td>
<td>—</td>
<td>ns</td>
<td>Low-Power mode measured at VDD/2 (Note 1)</td>
</tr>
<tr>
<td>CM04D</td>
<td></td>
<td>Response Time Falling Edge</td>
<td>—</td>
<td>85</td>
<td>—</td>
<td>ns</td>
<td>Low-Power mode measured at VDD/2 (Note 1)</td>
</tr>
<tr>
<td>CM05</td>
<td>Tmc2ov</td>
<td>Comparator Mode Change to Output Valid*</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>μs</td>
<td>Comparator Hysteresis is available when the CxHYS bit of the CMxCON0 register is enabled.</td>
</tr>
<tr>
<td>CM06</td>
<td>CHYSTER</td>
<td>Comparator Hysteresis</td>
<td>20</td>
<td>45</td>
<td>75</td>
<td>mV</td>
<td>Hysteresis ON, High Power measured at VDD/2 (Note 2)</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.

**Note 1:** Response time measured with one comparator input at VDD/2, while the other input transitions from VSS to VDD.

**Note 2:** Comparator Hysteresis is available when the CxHYS bit of the CMxCON0 register is enabled.
TABLE 30-17: DIGITAL-TO-ANALOG CONV ERTER (DAC) SPECIFICATIONS

Operating Conditions: VDD = 3V, Temperature = 25°C (unless otherwise stated).

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC01*</td>
<td>CLSB</td>
<td>Step Size</td>
<td>—</td>
<td>—</td>
<td>VDD/256</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>DAC02*</td>
<td>CACC</td>
<td>Absolute Accuracy</td>
<td>—</td>
<td>—</td>
<td>±1.5 LSb</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DAC03*</td>
<td>CR</td>
<td>Unit Resistor Value (R)</td>
<td>—</td>
<td>600</td>
<td>—</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>DAC04*</td>
<td>CST</td>
<td>Settling Time(^{(1)})</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>μs</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.

Note 1: Settling time measured while DACR<7:0> transitions from "0x00" to "0xFF".

FIGURE 30-14: EUSART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

Note: Refer to Figure 30-4 for load conditions.

TABLE 30-18: EUSART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>US120</td>
<td>TCKH2DTV</td>
<td>SYNC XMIT (Master and Slave)</td>
<td>3.0-5.5V</td>
<td>—</td>
<td>80</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Clock high to data-out valid</td>
<td>1.8-5.5V</td>
<td>—</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>US121</td>
<td>TCKRF</td>
<td>Clock out rise time and fall time</td>
<td>3.0-5.5V</td>
<td>—</td>
<td>45</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(Master mode)</td>
<td>1.8-5.5V</td>
<td>—</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>US122</td>
<td>TDTRF</td>
<td>Data-out rise time and fall time</td>
<td>3.0-5.5V</td>
<td>—</td>
<td>45</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.8-5.5V</td>
<td>—</td>
<td>50</td>
<td>ns</td>
</tr>
</tbody>
</table>

FIGURE 30-15: EUSART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

Note: Refer to Figure 30-4 for load conditions.


### TABLE 30-19: EUSART SYNCHRONOUS RECEIVE REQUIREMENTS

**Standard Operating Conditions** (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>US125</td>
<td>TDV2CKL</td>
<td>SYNC RCV (Master and Slave)</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Data-hold before CK ↓ (DT hold time)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>US126</td>
<td>TCKL2DTL</td>
<td>Data-hold after CK ↓ (DT hold time)</td>
<td>15</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
FIGURE 30-16: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

Note: Refer to Figure 30-4 for load conditions.

FIGURE 30-17: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)

Note: Refer to Figure 30-4 for load conditions.
FIGURE 30-18: SPI SLAVE MODE TIMING (CKE = 0)

Note: Refer to Figure 30-4 for load conditions.

FIGURE 30-19: SPI SLAVE MODE TIMING (CKE = 1)

Note: Refer to Figure 30-4 for load conditions.
### TABLE 30-20: SPI MODE REQUIREMENTS

**Standard Operating Conditions** (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>SP70*</td>
<td>TssL2sch, TssL2scl</td>
<td>$SS \downarrow$ to SCK$\downarrow$ or SCK$\uparrow$ input</td>
<td>2.25*Tcy</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP71*</td>
<td>Tsch</td>
<td>SCK input high time (Slave mode)</td>
<td>Tcy + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP72*</td>
<td>TscL</td>
<td>SCK input low time (Slave mode)</td>
<td>Tcy + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP73*</td>
<td>TdvV2sch, TdvV2scl</td>
<td>Setup time of SDI data input to SCK edge</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP74*</td>
<td>Tsch2diL, Tsch2diL</td>
<td>Hold time of SDI data input to SCK edge</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP75*</td>
<td>TooR</td>
<td>SDO data output rise time</td>
<td>3.0-5.5V</td>
<td>—</td>
<td>10</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.8-5.5V</td>
<td>—</td>
<td>25</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>SP76*</td>
<td>TooF</td>
<td>SDO data output fall time</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>SP77*</td>
<td>TssH2doZ</td>
<td>$SS \uparrow$ to SDO output high-impedance</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>SP78*</td>
<td>Tscr</td>
<td>SCK output rise time (Master mode)</td>
<td>3.0-5.5V</td>
<td>—</td>
<td>10</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.8-5.5V</td>
<td>—</td>
<td>25</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>SP79*</td>
<td>TscF</td>
<td>SCK output fall time (Master mode)</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>SP80*</td>
<td>Tsch2doV, TscL2doV</td>
<td>SDO data output valid after SCK edge</td>
<td>3.0-5.5V</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.8-5.5V</td>
<td>—</td>
<td>—</td>
<td>145</td>
<td>ns</td>
</tr>
<tr>
<td>SP81*</td>
<td>TooV2sch, TooV2scl</td>
<td>SDO data output setup to SCK edge</td>
<td>Tcy</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SP82*</td>
<td>TssL2doV</td>
<td>SDO data output valid after $SS \downarrow$ edge</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>SP83*</td>
<td>Tsch2ssh, Tsch2ssh</td>
<td>$SS \uparrow$ after SCK edge</td>
<td>1.5Tcy + 40</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

### FIGURE 30-20: I²C™ BUS START/STOP BITS TIMING

![Figure 30-20: I²C™ BUS START/STOP BITS TIMING](image)

**Note:** Refer to Figure 30-4 for load conditions.
TABLE 30-21: \( \text{i}^2\text{C} \)™ BUS START/STOP BITS REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>SP90*</td>
<td>TSU:STA</td>
<td>Start condition</td>
<td>100 kHz mode</td>
<td>4700</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Setup time</td>
<td>400 kHz mode</td>
<td>600</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>SP91*</td>
<td>THD:STA</td>
<td>Start condition</td>
<td>100 kHz mode</td>
<td>4000</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hold time</td>
<td>400 kHz mode</td>
<td>600</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>SP92*</td>
<td>TSU:STO</td>
<td>Stop condition</td>
<td>100 kHz mode</td>
<td>4700</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Setup time</td>
<td>400 kHz mode</td>
<td>600</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>SP93</td>
<td>THD:STO</td>
<td>Stop condition</td>
<td>100 kHz mode</td>
<td>4000</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hold time</td>
<td>400 kHz mode</td>
<td>600</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.

FIGURE 30-21: \( \text{i}^2\text{C} \)™ BUS DATA TIMING

Note: Refer to Figure 30-4 for load conditions.
### TABLE 30-22: \( \text{i}^2\text{C} \)™ BUS DATA REQUIREMENTS

#### Standard Operating Conditions (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SP100</strong></td>
<td>THIGH</td>
<td>Clock high time</td>
<td>100 kHz mode</td>
<td>4.0</td>
<td>—</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>0.6</td>
<td>—</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SSP module</td>
<td>1.5Tcy</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td><strong>SP101</strong></td>
<td>TLOW</td>
<td>Clock low time</td>
<td>100 kHz mode</td>
<td>4.7</td>
<td>—</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>1.3</td>
<td>—</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SSP module</td>
<td>1.5Tcy</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td><strong>SP102</strong></td>
<td>TR</td>
<td>SDA and SCL rise time</td>
<td>100 kHz mode</td>
<td>—</td>
<td>1000</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>20 + 0.1C_{B}</td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td><strong>SP103</strong></td>
<td>TF</td>
<td>SDA and SCL fall time</td>
<td>100 kHz mode</td>
<td>—</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>20 + 0.1C_{B}</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td><strong>SP106</strong></td>
<td>THD:DAT</td>
<td>Data input hold time</td>
<td>100 kHz mode</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>0</td>
<td>0.9</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td><strong>SP107</strong></td>
<td>TSU:DAT</td>
<td>Data input setup time</td>
<td>100 kHz mode</td>
<td>250</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>100</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td><strong>SP109</strong></td>
<td>TAA</td>
<td>Output valid from clock</td>
<td>100 kHz mode</td>
<td>—</td>
<td>3500</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td><strong>SP110</strong></td>
<td>TBUF</td>
<td>Bus free time</td>
<td>100 kHz mode</td>
<td>4.7</td>
<td>—</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400 kHz mode</td>
<td>1.3</td>
<td>—</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td><strong>SP111</strong></td>
<td>C_{B}</td>
<td>Bus capacitive loading</td>
<td>—</td>
<td>400</td>
<td>pF</td>
<td>—</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.

**Note 1:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**Note 2:** A Fast mode (400 kHz) \( \text{i}^2\text{C} \)™ bus device can be used in a Standard mode (100 kHz) \( \text{i}^2\text{C} \) bus system, but the requirement \( \text{TSU:DAT} \geq 250 \text{ ns} \) must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line \( \text{TR max.} + \text{TSU:DAT} = 1000 + 250 = 1250 \text{ ns} \) (according to the Standard mode \( \text{i}^2\text{C} \) bus specification), before the SCL line is released.
31.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for design guidance and are not tested.

In some graphs or tables, the data presented are outside specified operating range (i.e., outside specified VDD range). This is for information only and devices are ensured to operate properly only within the specified range.

Unless otherwise noted, all graphs apply to both the F and LF devices.

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

“Typical” represents the mean of the distribution at 25°C. “Maximum”, “Max.”, “Minimum” or “Min.” represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.
Note: Unless otherwise noted, $V_{IN} = 5\, V$, $F_{OSC} = 300\, kHz$, $C_{IN} = 0.1\, \mu F$, $T_{A} = 25^\circ C$.

**FIGURE 31-1:** $I_{DD}$, LP Oscillator Mode, $F_{OSC} = 32\, kHz$, PIC16LF1784/6/7 Only.

**FIGURE 31-2:** $I_{DD}$, LP Oscillator Mode, $F_{OSC} = 32\, kHz$, PIC16F1784/6/7 Only.

**FIGURE 31-3:** $I_{DD}$ Typical, XT and EXTRC Oscillator, PIC16LF1784/6/7 Only.

**FIGURE 31-4:** $I_{DD}$ Maximum, XT and EXTRC Oscillator, PIC16LF1784/6/7 Only.

**FIGURE 31-5:** $I_{DD}$ Typical, XT and EXTRC Oscillator, PIC16F1784/6/7 Only.

**FIGURE 31-6:** $I_{DD}$ Maximum, XT and EXTRC Oscillator, PIC16F1784/6/7 Only.
Note: Unless otherwise noted, $V_{IN} = 5\, \text{V}$, $F_{OSC} = 300\, \text{kHz}$, $C_{IN} = 0.1\, \mu\text{F}$, $T_A = 25^\circ\text{C}$.

**FIGURE 31-7:** $I_D\text{D}$, EC Oscillator LP Mode, $F_{OSC} = 32\, \text{kHz}$, PIC16LF1784/6/7 Only.

**FIGURE 31-8:** $I_D\text{D}$, EC Oscillator LP Mode, $F_{OSC} = 32\, \text{kHz}$, PIC16F1784/6/7 Only.

**FIGURE 31-9:** $I_D\text{D}$, EC Oscillator LP Mode, $F_{OSC} = 500\, \text{kHz}$, PIC16LF1784/6/7 Only.

**FIGURE 31-10:** $I_D\text{D}$, EC Oscillator LP Mode, $F_{OSC} = 500\, \text{kHz}$, PIC16F1784/6/7 Only.

**FIGURE 31-11:** $I_D\text{D}$ Typical, EC Oscillator MP Mode, PIC16LF1784/6/7 Only.

**FIGURE 31-12:** $I_D\text{D}$ Maximum, EC Oscillator MP Mode, PIC16LF1784/6/7 Only.
Note: Unless otherwise noted, VIN = 5V, Fosc = 300 kHz, Cin = 0.1 µF, TA = 25°C.

**FIGURE 31-13:** IDD Typical, EC Oscillator
MP Mode, PIC16F1784/6/7 Only.

**FIGURE 31-14:** IDD Maximum, EC Oscillator
MP Mode, PIC16F1784/6/7 Only.

**FIGURE 31-15:** IDD Typical, EC Oscillator
HP Mode, PIC16LF1784/6/7 Only.

**FIGURE 31-16:** IDD Maximum, EC Oscillator
HP Mode, PIC16LF1784/6/7 Only.

**FIGURE 31-17:** IDD Typical, EC Oscillator
HP Mode, PIC16F1784/6/7 Only.

**FIGURE 31-18:** IDD Maximum, EC Oscillator
HP Mode, PIC16F1784/6/7 Only.
Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.
**Note:** Unless otherwise noted, $V_{IN} = 5\, V$, $F_{OSC} = 300\, kHz$, $C_{IN} = 0.1\, \mu F$, $T_A = 25\, ^\circ C$.

**FIGURE 31-25:** $I_{DD}$ Typical, HFINTOSC Mode, PIC16F1784/6/7 Only.

**FIGURE 31-26:** $I_{DD}$ Maximum, HFINTOSC Mode, PIC16F1784/6/7 Only.

**FIGURE 31-27:** $I_{DD}$ Typical, HS Oscillator, 25°C, PIC16LF1784/6/7 Only.

**FIGURE 31-28:** $I_{DD}$ Maximum, HS Oscillator, PIC16LF1784/6/7 Only.

**FIGURE 31-29:** $I_{DD}$ Typical, HS Oscillator, 25°C, PIC16F1784/6/7 Only.

**FIGURE 31-30:** $I_{DD}$ Maximum, HS Oscillator, PIC16F1784/6/7 Only.
Note: Unless otherwise noted, $V_{IN} = 5V$, $F_{OSC} = 300$ kHz, $C_{IN} = 0.1 \mu F$, $T_a = 25^\circ C$.

**FIGURE 31-31:** $I_{DD}$, HS Oscillator, 32 MHz (8 MHz + 4x PLL), PIC16LF1784/6/7 Only.

**FIGURE 31-32:** $I_{DD}$, HS Oscillator, 32 MHz (8 MHz + 4x PLL), PIC16F1784/6/7 Only.

**FIGURE 31-33:** $I_{PD}$, Base, LP Sleep Mode, PIC16LF1784/6/7 Only.

**FIGURE 31-34:** $I_{PD}$, Base, LP Sleep Mode ($V_{REGPM} = 1$), PIC16F1784/6/7 Only.

**FIGURE 31-35:** $I_{PD}$, Watchdog Timer (WDT), PIC16LF1784/6/7 Only.

**FIGURE 31-36:** $I_{PD}$, Watchdog Timer (WDT), PIC16F1784/6/7 Only.
**Note:** Unless otherwise noted, $V_{IN} = 5\, \text{V}$, $F_{OSC} = 300\, \text{kHz}$, $C_{IN} = 0.1\, \mu\text{F}$, $T_A = 25\, \degree\text{C}$.

**FIGURE 31-37:** $I_{PD}$, Fixed Voltage Reference (FVR), PIC16LF1784/6/7 Only.

**FIGURE 31-38:** $I_{PD}$, Fixed Voltage Reference (FVR), PIC16F1784/6/7 Only.

**FIGURE 31-39:** $I_{PD}$, Brown-Out Reset (BOR), $B_{ORV} = 1$, PIC16LF1784/6/7 Only.

**FIGURE 31-40:** $I_{PD}$, Brown-Out Reset (BOR), $B_{ORV} = 1$, PIC16F1784/6/7 Only.

**FIGURE 31-41:** $I_{PD}$, Low-Power Brown-Out Reset ($LP_{BOR} = 0$), PIC16LF1784/6/7 Only.

**FIGURE 31-42:** $I_{PD}$, Low-Power Brown-Out Reset ($LP_{BOR} = 0$), PIC16F1784/6/7 Only.
Note: Unless otherwise noted, \( V_{\text{IN}} = 5\, \text{V}, \quad F_{\text{OSC}} = 300\, \text{kHz}, \quad C_{\text{IN}} = 0.1\, \mu\text{F}, \quad T_A = 25^\circ\text{C} \).

**FIGURE 31-43:** IPD, Timer1 Oscillator, \( F_{\text{OSC}} = 32\, \text{kHz}, \) PIC16LF1784/6/7 Only.

**FIGURE 31-44:** IPD, Timer1 Oscillator, \( F_{\text{OSC}} = 32\, \text{kHz}, \) PIC16F1784/6/7 Only.

**FIGURE 31-45:** IPD, Op Amp, High GBWP Mode (OPA\text{xSP} = 1), PIC16LF1784/6/7 Only.

**FIGURE 31-46:** IPD, Op Amp, High GBWP Mode (OPA\text{xSP} = 1), PIC16F1784/6/7 Only.

**FIGURE 31-47:** IPD, ADC Non-Converting, PIC16LF1784/6/7 Only.

**FIGURE 31-48:** IPD, ADC Non-Converting, PIC16F1784/6/7 Only.
Note: Unless otherwise noted, \( \text{VIN} = 5\, \text{V}, \text{FOSC} = 300\, \text{kHz}, \text{CIN} = 0.1\, \mu\text{F}, \text{TA} = 25^\circ\text{C} \).

**FIGURE 31-49:** \( \text{IPD}, \text{Comparator, NP Mode (C}_{\text{SP}} = 1) \), PIC16LF1784/6/7 Only.

**FIGURE 31-50:** \( \text{IPD}, \text{Comparator, NP Mode (C}_{\text{SP}} = 1) \), PIC16F1784/6/7 Only.

**FIGURE 31-51:** \( \text{VOH vs. IOH Over Temperature, VDD = 5.0V, PIC16F1784/6/7 Only} \).

**FIGURE 31-52:** \( \text{VOL vs. IOL Over Temperature, VDD = 5.0V, PIC16F1784/6/7 Only} \).

**FIGURE 31-53:** \( \text{VOH vs. IOH Over Temperature, VDD = 3.0V} \).

**FIGURE 31-54:** \( \text{VOL vs. IOL Over Temperature, VDD = 3.0V} \).
**Note:** Unless otherwise noted, \( V_{\text{IN}} = 5 \text{ V}, F_{\text{OSC}} = 300 \text{ kHz}, C_{\text{IN}} = 0.1 \mu\text{F}, T_{\text{A}} = 25^\circ \text{C} \).
**Note:** Unless otherwise noted, $V_{IN} = 5\, \text{V}$, $F_{OSC} = 300\, \text{kHz}$, $C_{IN} = 0.1\, \mu\text{F}$, $T_A = 25^\circ\text{C}$.

**FIGURE 31-61:** Brown-Out Reset Voltage, Low Trip Point ($B_{ORV} = 1$), PIC16LF1784/6/7 Only.

**FIGURE 31-62:** Brown-Out Reset Hysteresis, Low Trip Point ($B_{ORV} = 1$), PIC16LF1784/6/7 Only.

**FIGURE 31-63:** Brown-Out Reset Voltage, Low Trip Point ($B_{ORV} = 1$), PIC16F1784/6/7 Only.

**FIGURE 31-64:** Brown-Out Reset Hysteresis, Low Trip Point ($B_{ORV} = 1$), PIC16F1784/6/7 Only.

**FIGURE 31-65:** Brown-Out Reset Voltage, High Trip Point ($B_{ORV} = 0$).

**FIGURE 31-66:** Brown-Out Reset Hysteresis, High Trip Point ($B_{ORV} = 0$).
Note: Unless otherwise noted, VIN = 5 V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

**FIGURE 31-67:** LPBOR Reset Voltage.

**FIGURE 31-68:** LPBOR Reset Hysteresis.

**FIGURE 31-69:** PWRT Period, PIC16F1784/6/7 Only.

**FIGURE 31-70:** PWRT Period, PIC16LF1784/6/7 Only.

**FIGURE 31-71:** POR Release Voltage.

**FIGURE 31-72:** POR Rearm Voltage, NP Mode (VREGPM = 0), PIC16F1784/6/7 Only.
Note: Unless otherwise noted, \( \text{VIN} = 5 \, \text{V} \), \( \text{FOSC} = 300 \, \text{kHz} \), \( C_{\text{IN}} = 0.1 \, \mu\text{F} \), \( T_A = 25^\circ \text{C} \).

**FIGURE 31-73:** POR Rearm Voltage, NP Mode, PIC16LF1784/6/7 Only.

**FIGURE 31-74:** Wake From Sleep, \( V_{\text{REGPM}} = 0 \).

**FIGURE 31-75:** Wake From Sleep, \( V_{\text{REGPM}} = 1 \).

**FIGURE 31-76:** FVR Stabilization Period.

**FIGURE 31-77:** ADC 10-bit Mode, Single-Ended DNL, \( V_{\text{DD}} = 3.0 \, \text{V} \), \( T_{\text{AD}} = 1 \, \mu\text{s} \), \( 25^\circ \text{C} \).

**FIGURE 31-78:** ADC 10-bit Mode, Single-Ended DNL, \( V_{\text{DD}} = 3.0 \, \text{V} \), \( T_{\text{AD}} = 4 \, \mu\text{s} \), \( 25^\circ \text{C} \).
Note: Unless otherwise noted, \( V_{IN} = 5\, \text{V} \), \( F_{OSC} = 300\, \text{kHz} \), \( C_{IN} = 0.1\, \mu\text{F} \), \( T_{A} = 25\, ^\circ\text{C} \).

**FIGURE 31-79:** ADC 10-bit Mode, Single-Ended INL, \( V_{DD} = 3.0\, \text{V} \), \( T_{AD} = 1\, \mu\text{s} \), 25°C.

**FIGURE 31-80:** ADC 10-bit Mode, Single-Ended INL, \( V_{DD} = 3.0\, \text{V} \), \( T_{AD} = 4\, \mu\text{s} \), 25°C.

**FIGURE 31-81:** ADC 10-bit Mode, Single-Ended DNL, \( V_{DD} = 3.0\, \text{V} \).

**FIGURE 31-82:** ADC 10-bit Mode, Single-Ended INL, \( V_{DD} = 3.0\, \text{V} \), \( V_{REF} = 3.0\, \text{V} \).

**FIGURE 31-83:** ADC 10-bit Mode, Single-Ended DNL, \( V_{DD} = 3.0\, \text{V} \), \( T_{AD} = 1\, \mu\text{s} \).

**FIGURE 31-84:** ADC 10-bit Mode, Single-Ended INL, \( V_{DD} = 3.0\, \text{V} \), \( T_{AD} = 1\, \mu\text{s} \).
Note: Unless otherwise noted, $V_{IN} = 5V$, $F_{OSC} = 300 kHz$, $C_{IN} = 0.1 \mu F$, $T_A = 25^\circ C$.

**FIGURE 31-85:** ADC 12-bit Mode, Single-Ended DNL, $V_{DD} = 3.0V$, $T_{AD} = 1 \mu S$, $25^\circ C$.

**FIGURE 31-86:** ADC 12-bit Mode, Single-Ended DNL, $V_{DD} = 3.0V$, $T_{AD} = 4 \mu S$, $25^\circ C$.

**FIGURE 31-87:** ADC 12-bit Mode, Single-Ended INL, $V_{DD} = 3.0V$, $T_{AD} = 1 \mu S$, $25^\circ C$.

**FIGURE 31-88:** ADC 12-bit Mode, Single-Ended INL, $V_{DD} = 3.0V$, $T_{AD} = 4 \mu S$, $25^\circ C$.

**FIGURE 31-89:** ADC 12-bit Mode, Single-Ended DNL, $V_{DD} = 3.0V$, $V_{REF} = 3.0V$.

**FIGURE 31-90:** ADC 12-bit Mode, Single-Ended INL, $V_{DD} = 3.0V$, $V_{REF} = 3.0V$. 

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Note: Unless otherwise noted, $V_{IN} = 5\, \text{V}$, $F_{OSC} = 300\, \text{kHz}$, $C_{IN} = 0.1\, \mu\text{F}$, $T_{A} = 25\, ^\circ\text{C}$.

**FIGURE 31-91:** ADC 12-bit Mode, Single-Ended DNL, $V_{DD} = 3.0\, \text{V}$, $T_{AD} = 1\, \mu\text{S}$.

**FIGURE 31-92:** ADC 12-bit Mode, Single-Ended INL, $V_{DD} = 3.0\, \text{V}$, $T_{AD} = 1\, \mu\text{S}$.

**FIGURE 31-93:** ADC 12-bit Mode, Single-Ended DNL, $V_{DD} = 5.5\, \text{V}$, $T_{AD} = 1\, \mu\text{S}$, $25\, ^\circ\text{C}$.

**FIGURE 31-94:** ADC 12-bit Mode, Single-Ended DNL, $V_{DD} = 5.5\, \text{V}$, $T_{AD} = 4\, \mu\text{S}$, $25\, ^\circ\text{C}$.

**FIGURE 31-95:** ADC 12-bit Mode, Single-Ended INL, $V_{DD} = 5.5\, \text{V}$, $T_{AD} = 1\, \mu\text{S}$, $25\, ^\circ\text{C}$.

**FIGURE 31-96:** ADC 12-bit Mode, Single-Ended INL, $V_{DD} = 5.5\, \text{V}$, $T_{AD} = 4\, \mu\text{S}$, $25\, ^\circ\text{C}$.
Note: Unless otherwise noted, \( V_{\text{IN}} = 5 \text{V}, \ F_{\text{OSC}} = 300 \text{ kHz}, \ C_{\text{IN}} = 0.1 \mu\text{F}, \ TA = 25^\circ \text{C}. \)

**FIGURE 31-97:** ADC 12-bit Mode, Single-Ended DNL, \( V_{\text{DD}} = 5.5 \text{V}, \ V_{\text{REF}} = 5.5 \text{V}. \)

**FIGURE 31-98:** ADC 12-bit Mode, Single-Ended INL, \( V_{\text{DD}} = 5.5 \text{V}, \ V_{\text{REF}} = 5.5 \text{V}. \)

**FIGURE 31-99:** Temp. Indicator Initial Offset, High Range, Temp. = 20°C, PIC16F1784/6/7 Only.

**FIGURE 31-100:** Temp. Indicator Initial Offset, Low Range, Temp. = 20°C, PIC16F1784/6/7 Only.

**FIGURE 31-101:** Temp. Indicator Initial Offset, Low Range, Temp. = 20°C, PIC16LF1784/6/7 Only.

**FIGURE 31-102:** Temp. Indicator Slope Normalized to 20°C, High Range, \( V_{\text{DD}} = 5.5 \text{V}, \) PIC16F1784/6/7 Only.
Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

**FIGURE 31-103:** Temp. Indicator Slope Normalized to 20°C, High Range, VDD = 3.6V, PIC16F1784/6/7 Only.

**FIGURE 31-104:** Temp. Indicator Slope Normalized to 20°C, Low Range, VDD = 3.0V, PIC16F1784/6/7 Only.

**FIGURE 31-105:** Temp. Indicator Slope Normalized to 20°C, Low Range, VDD = 1.8V, PIC16LF1784/6/7 Only.

**FIGURE 31-106:** Temp. Indicator Slope Normalized to 20°C, Low Range, VDD = 3.0V, PIC16LF1784/6/7 Only.

**FIGURE 31-107:** Temp. Indicator Slope Normalized to 20°C, High Range, VDD = 3.6V, PIC16LF1784/6/7 Only.

**FIGURE 31-108:** Op Amp, Common Mode Rejection Ratio (CMRR), VDD = 3.0V.
Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

**FIGURE 31-109:** Op Amp, Output Voltage Histogram, VDD = 3.0V, VCM = VDD/2.

**FIGURE 31-110:** Op Amp, Offset Over Common Mode Voltage, VDD = 3.0V, Temp. = 25°C.

**FIGURE 31-111:** Op Amp, Offset Over Common Mode Voltage, VDD = 5.0V, Temp. = 25°C, PIC16F1784/6/7 Only.

**FIGURE 31-112:** Op Amp, Output Slew Rate, Rising Edge, PIC16LF1784/6/7 Only.

**FIGURE 31-113:** Op Amp, Output Slew Rate, Falling Edge, PIC16LF1784/6/7 Only.

**FIGURE 31-114:** Op Amp, Output Slew Rate, Rising Edge, PIC16F1784/6/7 Only.
Note: Unless otherwise noted, $V_{IN} = 5\, \text{V}$, $F_{OSC} = 300 \, \text{kHz}$, $C_{IN} = 0.1 \, \mu\text{F}$, $T_A = 25^\circ\text{C}$.

**FIGURE 31-115:** Op Amp, Output Slew Rate, Falling Edge, PIC16F1784/6/7 Only.

**FIGURE 31-116:** Comparator Hysteresis, NP Mode ($C_{XSP} = 1$), $V_{DD} = 3.0\, \text{V}$, Typical Measured Values.

**FIGURE 31-117:** Comparator Offset, NP Mode ($C_{XSP} = 1$), $V_{DD} = 3.0\, \text{V}$, Typical Measured Values at $25^\circ\text{C}$.

**FIGURE 31-118:** Comparator Offset, NP Mode ($C_{XSP} = 1$), $V_{DD} = 3.0\, \text{V}$, Typical Measured Values From $-40^\circ\text{C}$ to $125^\circ\text{C}$.

**FIGURE 31-119:** Comparator Hysteresis, NP Mode ($C_{XSP} = 1$), $V_{DD} = 5.5\, \text{V}$, Typical Measured Values, PIC16F1784/6/7 Only.
Note: Unless otherwise noted, \( V_{\text{IN}} = 5 \text{V}, F_{\text{OSC}} = 300 \text{kHz}, C_{\text{IN}} = 0.1 \mu \text{F}, T_A = 25^\circ \text{C} \).

**FIGURE 31-120:** Comparator Offset, NP Mode (\( C_{\text{SP}} = 1 \)), \( V_{\text{DD}} = 5.0 \text{V} \), Typical Measured Values at 25°C, PIC16F1784/6/7 Only.

**FIGURE 31-121:** Comparator Offset, NP Mode (\( C_{\text{SP}} = 1 \)), \( V_{\text{DD}} = 5.0 \text{V} \), Typical Measured Values From -40°C to 125°C, PIC16F1784/6/7 Only.

**FIGURE 31-122:** Comparator Response Time Over Voltage, NP Mode (\( C_{\text{SP}} = 1 \)), Typical Measured Values, PIC16LF1784/6/7 Only.

**FIGURE 31-123:** Comparator Response Time Over Voltage, NP Mode (\( C_{\text{SP}} = 1 \)), Typical Measured Values, PIC16F1784/6/7 Only.

**FIGURE 31-124:** Comparator Output Filter Delay Time Over Temp., NP Mode (\( C_{\text{SP}} = 1 \)), Typical Measured Values, PIC16LF1784/6/7 Only.

**FIGURE 31-125:** Comparator Output Filter Delay Time Over Temp., NP Mode (\( C_{\text{SP}} = 1 \)), Typical Measured Values, PIC16F1784/6/7 Only.
Note: Unless otherwise noted, V\text{IN} = 5\, \text{V}, \text{FOSC} = 300\, \text{kHz}, \text{CIN} = 0.1\, \mu\text{F}, \text{T_A} = 25^\circ\text{C}.

**FIGURE 31-126:** Typical DAC DNL Error, \( V_{\text{DD}} = 3.0\, \text{V}, \text{VREF} = \text{External} \, 3\, \text{V}. 

**FIGURE 31-127:** Typical DAC INL Error, \( V_{\text{DD}} = 3.0\, \text{V}, \text{VREF} = \text{External} \, 3\, \text{V}. 

**FIGURE 31-128:** Typical DAC INL Error, \( V_{\text{DD}} = 5.0\, \text{V}, \text{VREF} = \text{External} \, 5\, \text{V}, \) PIC16F1784/6/7 Only.

**FIGURE 31-129:** Typical DAC INL Error, \( V_{\text{DD}} = 5.0\, \text{V}, \text{VREF} = \text{External} \, 5\, \text{V}, \) PIC16F1784/6/7 Only.

**FIGURE 31-130:** Absolute Value of DAC DNL Error, \( V_{\text{DD}} = 3.0\, \text{V}, \text{VREF} = \text{VDD}. 

**FIGURE 31-131:** Absolute Value of DAC INL Error, \( V_{\text{DD}} = 3.0\, \text{V}. \)
**Note:** Unless otherwise noted, $V_{IN} = 5\, V$, $F_{OSC} = 300\, kHz$, $C_{IN} = 0.1\, \mu F$, $T_A = 25^\circ C$.

**FIGURE 31-132:** Absolute Value of DAC DNL Error, $V_{DD} = 5.0\, V$, PIC16F1784/6/7 Only.

**FIGURE 31-133:** Absolute Value of DAC INL Error, $V_{DD} = 5.0\, V$, PIC16F1784/6/7 Only.
32.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/
    MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

32.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:
- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:
- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:
- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:
- Local file history feature
- Built-in support for Bugzilla issue tracker
32.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip’s 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

32.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

32.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

32.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility
32.6 **MPLAB X SIM Software Simulator**
The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.
The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

32.7 **MPLAB REAL ICE In-Circuit Emulator System**
The MPLAB REAL ICE In-Circuit Emulator System is Microchip’s next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.
The emulator is connected to the design engineer’s PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

32.8 **MPLAB ICD 3 In-Circuit Debugger System**
The MPLAB ICD 3 In-Circuit Debugger System is Microchip’s most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.
The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer’s PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

32.9 **PICkit 3 In-Circuit Debugger/Programmer**
The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer’s PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

32.10 **MPLAB PM3 Device Programmer**
The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at $V_{DDMIN}$ and $V_{DDMAX}$ for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.
32.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

32.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®
33.0 PACKAGING INFORMATION

33.1 Package Marking Information

Legend:

- XX...X Customer-specific information
- Y Year code (last digit of calendar year)
- YY Year code (last 2 digits of calendar year)
- WW Week code (week of January 1 is week ‘01’)
- NNN Alphanumeric traceability code
- e3 Pb-free JEDEC® designator for Matte Tin (Sn)
- * This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
Package Marking Information (Continued)

28-Lead QFN (6x6 mm) Example

40-Lead PDIP (600 mil) Example

40-Lead UQFN (5x5x0.5 mm) Example

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Package Marking Information (Continued)

44-Lead QFN (8x8x0.9 mm)

Example

PIN 1

44-Lead TQFP (10x10x1 mm)

Example

PIN 1
33.2 Package Details
The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

### Notes:
For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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**Diagram**

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**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. $\$ Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2
28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

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</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
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<td>Contact Pad Width (X28)</td>
<td>X</td>
</tr>
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<tr>
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<td>Gx</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
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Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A
28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
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<tr>
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<tbody>
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<tr>
<td>Pitch</td>
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</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
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<td>Foot Length</td>
<td>L</td>
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<td>φ</td>
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<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B
28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

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<table>
<thead>
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<tbody>
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<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
</tr>
<tr>
<td>Contact Pad Width (X28)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X28)</td>
<td>Y1</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
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</table>

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M
   *BSC: Basic Dimension, Theoretically exact value shown without tolerances.*

Microchip Technology Drawing No. C04-2073A
28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
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<td>0.90</td>
<td>1.00</td>
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<tr>
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<tr>
<td>Overall Width</td>
<td>E</td>
<td>6.00 BSC</td>
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<td></td>
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</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E2</td>
<td>3.65</td>
<td>3.70</td>
<td>4.20</td>
<td></td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
<td>6.00 BSC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D2</td>
<td>3.65</td>
<td>3.70</td>
<td>4.20</td>
<td></td>
</tr>
<tr>
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<td>b</td>
<td>0.23</td>
<td>0.30</td>
<td>0.35</td>
<td></td>
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<td>0.70</td>
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<tr>
<td>Contact-to-Exposed Pad</td>
<td>K</td>
<td>0.20</td>
<td>–</td>
<td>–</td>
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**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B
28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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<td>0.65 BSC</td>
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<tr>
<td>Optional Center Pad Width W2</td>
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</tr>
<tr>
<td>Optional Center Pad Length T2</td>
<td>4.25</td>
</tr>
<tr>
<td>Contact Pad Spacing C1</td>
<td>5.70</td>
</tr>
<tr>
<td>Contact Pad Spacing C2</td>
<td>5.70</td>
</tr>
<tr>
<td>Contact Pad Width (X28) X1</td>
<td>0.37</td>
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<tr>
<td>Contact Pad Length (X28) Y1</td>
<td>1.00</td>
</tr>
<tr>
<td>Distance Between Pads G</td>
<td>0.20</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A
40-Lead Plastic Dual In-Line (P) – 600 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
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<tr>
<td>Pitch e</td>
<td>0.40 BSC</td>
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<tr>
<td>Contact Thickness A3</td>
<td>0.127 REF</td>
</tr>
<tr>
<td>Overall Width E</td>
<td>5.00 BSC</td>
</tr>
<tr>
<td>Exposed Pad Width E2</td>
<td>3.60</td>
</tr>
<tr>
<td>Overall Length D</td>
<td>5.00 BSC</td>
</tr>
<tr>
<td>Exposed Pad Length D2</td>
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</tr>
<tr>
<td>Contact Width b</td>
<td>0.15</td>
</tr>
<tr>
<td>Contact Length L</td>
<td>0.30</td>
</tr>
<tr>
<td>Contact-to-Exposed Pad K</td>
<td>0.20</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
40-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) - 5x5 mm Body [UQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

**Table:**

<table>
<thead>
<tr>
<th>Unit</th>
<th>Dimension Limits</th>
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<th>NOM</th>
<th>MAX</th>
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<tbody>
<tr>
<td>Contact Pitch</td>
<td>E</td>
<td>0.40</td>
<td>BSC</td>
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<tr>
<td>Optional Center Pad Width</td>
<td>W2</td>
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<td>3.80</td>
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<td>Optional Center Pad Length</td>
<td>T2</td>
<td></td>
<td>3.80</td>
<td></td>
</tr>
<tr>
<td>Contact Pad Spacing C1</td>
<td></td>
<td>5.00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact Pad Spacing C2</td>
<td></td>
<td>5.00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact Pad Width X40</td>
<td>X1</td>
<td></td>
<td>0.20</td>
<td></td>
</tr>
<tr>
<td>Contact Pad Length X40</td>
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</tr>
<tr>
<td>Distance Between Pads G</td>
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</table>

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

<table>
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</tr>
<tr>
<td>Pitch</td>
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</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Terminal Thickness</td>
<td>A3</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E2</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D2</td>
</tr>
<tr>
<td>Terminal Width</td>
<td>b</td>
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<td>Terminal Length</td>
<td>L</td>
</tr>
<tr>
<td>Terminal-to-Exposed-Pad</td>
<td>K</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.
44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

![Recommended Land Pattern Diagram]

<table>
<thead>
<tr>
<th>Units</th>
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<tbody>
<tr>
<td><strong>Dimension Limits</strong></td>
<td><strong>MIN</strong></td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Optional Center Pad Width</td>
<td>W2</td>
</tr>
<tr>
<td>Optional Center Pad Length</td>
<td>T2</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C1</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C2</td>
</tr>
<tr>
<td>Contact Pad Width (X44)</td>
<td>X1</td>
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<tr>
<td>Contact Pad Length (X44)</td>
<td>Y1</td>
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<tr>
<td>Distance Between Pads</td>
<td>G</td>
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</tbody>
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**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M
2. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B
44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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<tr>
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<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
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<td>Overall Width</td>
<td>E</td>
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<tr>
<td>Molded Package Length</td>
<td>D1</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
<tr>
<td>Mold Draft Angle Top</td>
<td>α</td>
</tr>
<tr>
<td>Mold Draft Angle Bottom</td>
<td>β</td>
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</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

**BSC:** Basic Dimension. Theoretically exact value shown without tolerances.
**REF:** Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B
PIC16(L)F1784/6/7

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

**Recommended Land Pattern**

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<table>
<thead>
<tr>
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<td>Contact Pad Spacing C2</td>
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**Notes:**
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B
APPENDIX A: DATA SHEET

REVISION HISTORY

Revision A (06/2012)
Initial release.

Revision B (11/2012)
Minor updates.

Revision C (08/2014)
Change from Preliminary to Final data sheet.
Corrected the following Tables: Family Types Table on page 3, Table 3-3, Table 3-8, Table 20-3, Table 22-2, Table 22-3, Table 23-1, Table 25-3, Table 30-1, Table 30-2, Table 30-3, Table 30-6, Table 30-7, Table 30-13, Table 30-14, Table 30-15, Table 30-16, Table 30-20.
Corrected the following Sections: Section 3.2, Section 9.2, Section 13.3, Section 17.1.6, Section 15.1, Section 15.3, Section 17.2.5, Section 18.2, Section 18.3, Section 19.0, Section 22.6.5, Section 22.9, Section 23.0, Section 23.1, Section 24.2.4, Section 24.2.5, Section 24.2.7, Section 24.8, Section 25.0, Section 26.6.7.4, Section 30.3.
Corrected the following Registers: Register 4-2, Register 8-2, Register 8-5, Register 17-3, Register 18-1, Register 24-3, Register 24-4.
Corrected Equation 17-1.
Corrected Figure 30-9. Removed Figure 24-21.
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- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- Field Application Engineer (FAE)
- Technical Support

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Technical support is available through the web site at: http://microchip.com/support
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
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<th>PART NO.</th>
<th>Device</th>
<th>Tape and Reel Option</th>
<th>Temperature Range</th>
<th>Package</th>
<th>Pattern</th>
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<td></td>
<td></td>
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<td>MV = UQFN</td>
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<td>P = PDIP</td>
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<td>SS = SSOP</td>
<td></td>
</tr>
</tbody>
</table>

Examples:

a) PIC16LF1784/7- I/P Industrial temperature PDIP package
b) PIC16F1786- E/SS Extended temperature, SSOP package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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