Section 21. 8-bit A/D Converter

HIGHLIGHTS

This section of the manual contains the following major topics:

21.1 Introduction ............................................................................................................... 21-2
21.2 Control Registers ..................................................................................................... 21-3
21.3 Operation ................................................................................................................ 21-5
21.4 A/D Acquisition Requirements .................................................................................. 21-6
21.5 Selecting the A/D Conversion Clock ....................................................................... 21-8
21.6 Configuring Analog Port Pins .................................................................................. 21-9
21.7 A/D Conversions ...................................................................................................... 21-10
21.8 A/D Operation During Sleep ................................................................................... 21-12
21.9 A/D Accuracy/Error .............................................................................................. 21-13
21.10 Effects of a RESET ............................................................................................... 21-13
21.11 Use of the CCP Trigger ......................................................................................... 21-14
21.12 Connection Considerations ................................................................................... 21-14
21.13 Transfer Function ................................................................................................. 21-14
21.14 Initialization .......................................................................................................... 21-15
21.15 Design Tips ........................................................................................................... 21-16
21.16 Related Application Notes .................................................................................... 21-17
21.17 Revision History ................................................................................................. 21-18

Note: Please refer to Appendix C.3 or device Data Sheet to determine which devices use this module.
21.1 Introduction

The analog-to-digital (A/D) converter module has up to eight analog inputs. The A/D allows conversion of an analog input signal to a corresponding 8-bit digital number. The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltage is software selectable to either the device's positive supply voltage (VDD) or the voltage level on the VREF pin. The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode.

The A/D module has three registers. These registers are:

- A/D Result Register (ADRES)
- A/D Control Register0 (ADCON0)
- A/D Control Register1 (ADCON1)

The ADCON0 register, shown in Figure 21-1, controls the operation of the A/D module. The ADCON1 register, shown in Figure 21-2, configures the functions of the port pins. The I/O pins can be configured as analog inputs (one I/O can also be a voltage reference) or as digital I/O.

The block diagram of the A/D module is shown in Figure 21-1.

**Figure 21-1: 8-bit A/D Block Diagram**

Note: On some devices this is a separate pin called AVDD. This allows the A/D VDD to be connected to a precise voltage source.
## Section 21. 8-bit A/D Converter

### 21.2 Control Registers

**Register 21-1: ADCON0 Register**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td><strong>ADCS1:</strong> A/D Conversion Clock Select bits</td>
<td>00, 01, 10, 11</td>
<td>00 = Fosc/2, 01 = Fosc/8, 10 = Fosc/32, 11 = FRC (clock derived from the internal A/D RC oscillator)</td>
</tr>
<tr>
<td>6</td>
<td><strong>ADCS0:</strong> A/D Conversion Clock Select bits</td>
<td>00, 01, 10, 11</td>
<td>00 = Fosc/2, 01 = Fosc/8, 10 = Fosc/32, 11 = FRC (clock derived from the internal A/D RC oscillator)</td>
</tr>
<tr>
<td>5</td>
<td><strong>CHS2:</strong> Analog Channel Select bits</td>
<td>000, 001, 010, 011, 100, 101, 110, 111</td>
<td>000 = channel 0, (AN0), 001 = channel 1, (AN1), 010 = channel 2, (AN2), 011 = channel 3, (AN3), 100 = channel 4, (AN4), 101 = channel 5, (AN5), 110 = channel 6, (AN6), 111 = channel 7, (AN7)</td>
</tr>
<tr>
<td>4</td>
<td><strong>CHS1:</strong> Analog Channel Select bits</td>
<td>000, 001, 010, 011, 100, 101, 110, 111</td>
<td>000 = channel 0, (AN0), 001 = channel 1, (AN1), 010 = channel 2, (AN2), 011 = channel 3, (AN3), 100 = channel 4, (AN4), 101 = channel 5, (AN5), 110 = channel 6, (AN6), 111 = channel 7, (AN7)</td>
</tr>
<tr>
<td>3</td>
<td><strong>CHS0:</strong> Analog Channel Select bits</td>
<td>000, 001, 010, 011, 100, 101, 110, 111</td>
<td>000 = channel 0, (AN0), 001 = channel 1, (AN1), 010 = channel 2, (AN2), 011 = channel 3, (AN3), 100 = channel 4, (AN4), 101 = channel 5, (AN5), 110 = channel 6, (AN6), 111 = channel 7, (AN7)</td>
</tr>
<tr>
<td>2</td>
<td><strong>GO/DONE:</strong> A/D Conversion Status bit</td>
<td>0, 1</td>
<td>0 = A/D conversion not in progress, 1 = A/D conversion in progress (Setting this bit starts the A/D conversion. This bit is automatically cleared by hardware when the A/D conversion is complete)</td>
</tr>
<tr>
<td>1</td>
<td><strong>Reserved:</strong> Always maintain this bit cleared.</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td><strong>ADON:</strong> A/D On bit</td>
<td>0, 1</td>
<td>0 = A/D converter module is shutoff and consumes no operating current, 1 = A/D converter module is operating</td>
</tr>
</tbody>
</table>

**Legend**

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- n = Value at POR reset

For devices that do not implement the full 8 A/D channels, the unimplemented selections are reserved. Do not select any unimplemented channels.
Register 21-2: ADCON1 Register

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7:3  **Unimplemented:** Read as '0'
bit 2:0  **PCFG2:PCFG0:** A/D Port Configuration Control bits

<table>
<thead>
<tr>
<th>PCFG2:PCFG0</th>
<th>AN7</th>
<th>AN6</th>
<th>AN5</th>
<th>AN4</th>
<th>AN3</th>
<th>AN2</th>
<th>AN1</th>
<th>AN0</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
</tr>
<tr>
<td>001</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>VREF</td>
<td>A</td>
<td>A</td>
<td>A</td>
</tr>
<tr>
<td>010</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
</tr>
<tr>
<td>011</td>
<td>D</td>
<td>D</td>
<td>A</td>
<td>A</td>
<td>VREF</td>
<td>A</td>
<td>A</td>
<td>A</td>
</tr>
<tr>
<td>100</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>A</td>
<td>D</td>
<td>A</td>
<td>A</td>
<td>A</td>
</tr>
<tr>
<td>101</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>VREF</td>
<td>D</td>
<td>A</td>
<td>A</td>
<td>A</td>
</tr>
<tr>
<td>11x</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
</tr>
</tbody>
</table>

A = Analog input  D = Digital I/O

**Note:** When AN3 is selected as VREF, the A/D reference is the voltage on the AN3 pin. When AN3 is selected as an analog input (A), then the voltage reference for the A/D is the device VDD.

---

**Legend**

<table>
<thead>
<tr>
<th>R</th>
<th>W</th>
<th>U</th>
<th>n</th>
</tr>
</thead>
<tbody>
<tr>
<td>Readable bit</td>
<td>Writable bit</td>
<td>Unimplemented bit, read as '0'</td>
<td>Value at POR reset</td>
</tr>
</tbody>
</table>

**Note 1:** On any device reset, the Port pins multiplexed with analog functions (ANx) are forced to be an analog input.
21.3 Operation

When the A/D conversion is complete, the result is loaded into the ADRES register, the GO/DONE bit (ADCON0<2>) is cleared, and A/D interrupt flag bit, ADIF, is set.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see Subsection 21.4 “A/D Acquisition Requirements.” After this acquisition time has elapsed the A/D conversion can be started. The following steps should be followed for doing an A/D conversion:

1. Configure the A/D module:
   - Configure analog pins / voltage reference / and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D conversion clock (ADCON0)
   - Turn on A/D module (ADCON0)

2. Configure A/D interrupt (if desired):
   - Clear the ADIF bit
   - Set the ADIE bit
   - Set the GIE bit

3. Wait the required acquisition time.

4. Start conversion:
   - Set the GO/DONE bit (ADCON0)

5. Wait for A/D conversion to complete, by either:
   - Polling for the GO/DONE bit to be cleared
   - Waiting for the A/D interrupt

6. Read A/D Result register (ADRES), clear the ADIF bit, if required.

7. For next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as $T_{AD}$. A minimum wait of $2T_{AD}$ is required before next acquisition starts.

Figure 21-2 shows the conversion sequence, and the terms that are used. Acquisition time is the time that the A/D module’s holding capacitor is connected to the external voltage level. Then there is the conversion time of $10T_{AD}$, which is started when the GO bit is set. The sum of these two times is the sampling time. There is a minimum acquisition time to ensure that the holding capacitor is charged to a level that will give the desired accuracy for the A/D conversion.

Figure 21-2: A/D Conversion Sequence

- Acquisition Time: When A/D holding capacitor start to charge.
- Conversion Time: After A/D conversion, or new A/D channel is selected.
- A/D conversion complete, result is loaded in ADRES register. Holding capacitor begins acquiring voltage level on selected channel. ADIF bit is set.
- A/D conversion is started (setting the GO bit). Holding capacitor is disconnected from the analog input before the conversion is started.
21.4 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 21-3. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD) (Figure 21-3). The maximum recommended impedance for analog sources is 10 kΩ. After the analog input channel is selected (changed) the acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 21-1 may be used. This equation assumes that 1/2 LSb error is used (512 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

**Equation 21-1: Acquisition Time**

\[
T_{ACQ} = \text{Amplifier Settling Time} + \\
\quad \text{Holding Capacitor Charging Time} + \\
\quad \text{Temperature Coefficient}
\]

\[
T_{ACQ} = T_{AMP} + T_{C} + T_{COFF}
\]

**Equation 21-2: A/D Minimum Charging Time**

\[
\begin{align*}
V_{HOLD} &= (V_{REF} - (V_{REF}/512)) \cdot (1 - e^{-T_{C}/C_{HOLD}(R_{IC} + R_{SS} + R_{S})}) \\
T_{C} &= -(51.2 \text{ pF}(1 \text{ kΩ} + R_{SS} + R_{S}) \text{ ln}(1/511))
\end{align*}
\]

**Example 21-1** shows the calculation of the minimum required acquisition time TACQ. This calculation is based on the following system assumptions.

- Rs = 10 kΩ
- Conversion Error ≤ 1/2 LSb
- VDD = 5V → RSS = 7 kΩ (see graph in Figure 21-3)
- Temperature = 50°C (system max.)
- V_{HOLD} = 0V @ time = 0

**Example 21-1: Calculating the Minimum Required Acquisition Time**

\[
\begin{align*}
T_{ACQ} &= T_{AMP} + T_{C} + T_{COFF} \\
T_{ACQ} &= 5 \mu s + T_{C} + ((Temp - 25°C)(0.05 \mu s/°C)) \\
T_{C} &= -C_{HOLD}(R_{IC} + R_{SS} + R_{S}) \text{ ln}(1/512) \\
&= -(51.2 \text{ pF}(1 \text{ kΩ} + 7 \text{ kΩ} + 10 \text{ kΩ}) \text{ ln}(0.0020)) \\
&= -(51.2 \text{ pF}(18 \text{ kΩ}) \text{ ln}(0.0020)) \\
&= -0.921 \mu s (-6.2146) \\
&= 5.724 \mu s
\end{align*}
\]

\[
T_{ACQ} = 5 \mu s + 5.724 \mu s + ((50°C - 25°C)(0.05 \mu s/°C)) \\
&= 10.724 \mu s + 1.25 \mu s \\
&= 11.974 \mu s
\]
Section 21. 8-bit A/D Converter

**Note 1:** The reference voltage (V_{REF}) has no effect on the equation, since it cancels itself out.

**Note 2:** The charge holding capacitor (CHOLD) is not discharged after each conversion.

**Note 3:** The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

**Note 4:** After a conversion has completed, a 2.0 TAD delay must complete before acquisition can begin again. During this time the holding capacitor is not connected to the selected A/D input channel.

---

**Figure 21-3: Analog Input Model**

Legend:
- CPIN = input capacitance
- VT = threshold voltage
- I Leakage = leakage current at the pin due to various junctions
- RIC = interconnect resistance
- SS = sampling switch
- CHOLD = sample/hold capacitance (from DAC)
- VAIN = Analog input voltage

![Analog Input Model Diagram](image-url)
21.5 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as $T_{AD}$. The A/D conversion requires $9.5 \cdot T_{AD}$ per 8-bit conversion. The source of the A/D conversion clock is software selected. The four possible options for $T_{AD}$ are:

- $2 \cdot T_{Osc}
- 8 \cdot T_{Osc}
- 32 \cdot T_{Osc}
- Internal RC oscillator

For correct A/D conversions, the A/D conversion clock ($T_{AD}$) must be selected to ensure a minimum $T_{AD}$ time of 1.6 $\mu$s for all devices, as shown in parameter 130 of the devices electrical specifications.

Table 21-1 and Table 21-2 show the resultant $T_{AD}$ times derived from the device operating frequencies and the A/D clock source selected.

### Table 21-1: $T_{AD}$ vs. Device Operating Frequencies (for Standard, C, Devices)

<table>
<thead>
<tr>
<th>AD Clock Source (TAD)</th>
<th>Device Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation ADCS1:ADCS0</td>
<td>20 MHz</td>
</tr>
<tr>
<td>2Tosc 00</td>
<td>400 ns(2)</td>
</tr>
<tr>
<td>8Tosc 01</td>
<td>400 ns(2)</td>
</tr>
<tr>
<td>32Tosc 10</td>
<td>1.6 $\mu$s</td>
</tr>
<tr>
<td>RC 11</td>
<td>2 - 6 $\mu$s(1,4)</td>
</tr>
</tbody>
</table>

Legend: Shaded cells are outside of recommended range.

Note 1: The RC source has a typical $T_{AD}$ time of 4 $\mu$s.

2: These values violate the minimum required $T_{AD}$ time.

3: For faster conversion times, the selection of another clock source is recommended.

4: For device frequencies above 1 MHz, the device must be in SLEEP for the entire conversion, or the A/D accuracy may be out of specification.

### Table 21-2: $T_{AD}$ vs. Device Operating Frequencies (for Extended, LC, Devices)

<table>
<thead>
<tr>
<th>AD Clock Source (TAD)</th>
<th>Device Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation ADCS1:ADCS0</td>
<td>4 MHz</td>
</tr>
<tr>
<td>2Tosc 00</td>
<td>500 ns(2)</td>
</tr>
<tr>
<td>8Tosc 01</td>
<td>4.0 $\mu$s</td>
</tr>
<tr>
<td>32Tosc 10</td>
<td>8.0 $\mu$s</td>
</tr>
<tr>
<td>RC 11</td>
<td>3 - 9 $\mu$s(1,4)</td>
</tr>
</tbody>
</table>

Legend: Shaded cells are outside of recommended range.

Note 1: The RC source has a typical $T_{AD}$ time of 6 $\mu$s.

2: These values violate the minimum required $T_{AD}$ time.

3: For faster conversion times, the selection of another clock source is recommended.

4: For device frequencies above 1 MHz, the device must be in SLEEP for the entire conversion, or the A/D accuracy may be out of specification.
Section 21. 8-bit A/D Converter

21.6 Configuring Analog Port Pins

ADCON1 and the corresponding TRIS registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS2:CHS0 bits and the TRIS bits.

| Note 1: | When reading the port register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs, will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy. |
| Note 2: | Analog levels on any pin that is defined as a digital input (including the AN7:AN0 pins), may cause the input buffer to consume current that is out of the devices specification. |
21.7 A/D Conversions

Example 21-2 show how to perform an A/D conversion. The I/O pins are configured as analog inputs. The analog reference (VREF) is the device VDD. The A/D interrupt is enabled, and the A/D conversion clock is FRC. The conversion is performed on the AN0 channel.

**Note:** The GO/DONE bit should **NOT** be set in the same instruction that turns on the A/D, due to the required acquisition time requirement.

Clearing the GO/DONE bit during a conversion will abort the current conversion. The ADRES register will NOT be updated with the partially completed A/D conversion sample. That is, the ADRES register will continue to contain the value of the last completed conversion (or the last value written to the ADRES register). After the A/D conversion is aborted, a 2TAD wait is required before the next acquisition is started. After this 2TAD wait, an acquisition is automatically started on the selected channel.

Example 21-2: Doing an A/D Conversion

```
BSF STATUS, RP0       ; Select Bank1
CLRF ADCON1           ; Configure A/D inputs
BSF PIR1, ADIE        ; Enable A/D interrupts
BCF STATUS, RP0       ; Select Bank0
MOVLW 0xC1            ; RC Clock, A/D is on, Channel 0 is selected
MOVWF ADCON0          ;
BCF PIR1, ADIF        ; Clear A/D interrupt flag bit
BSF INTCON, PEIE      ; Enable peripheral interrupts
BSF INTCON, GIE       ; Enable all interrupts
;
; Ensure that the required sampling time for the selected input
; channel has elapsed. Then the conversion may be started.
;
BSF ADCON0, GO        ; Start A/D Conversion
; The ADIF bit will be set and the GO/DONE
; bit is cleared upon completion of the
; A/D Conversion.
```

Figure 21-4: A/D Conversion TAD Cycles

- **Set GO bit:** Holding capacitor is disconnected from analog input
- **Next Q4:** ADRES is loaded
- **GO bit is cleared:** ADIF bit is set
- **Holding capacitor is connected to analog input**
Figure 21-5: Flowchart of A/D Operation

- Acquire
- ADON = 0?
  - Yes
  - ADON = 0
  - No
  - Acquire Selected Channel

- GO = 0?
  - Yes
  - GO = 0
  - No
  - Wait 2TAD

- A/D Clock = RC?
  - Yes
  - Start of A/D Conversion Delayed 1 Instruction Cycle
  - SLEEP
  - Instruction?
  - No
  - Finish Conversion
    - GO = 0
    - ADIF = 1
    - Wait 2TAD
  - From Sleep?
    - Yes
    - Wake-up
    - No
    - Stay in Sleep
    - Power-down A/D

- Device in SLEEP?
  - Yes
  - Abort Conversion
    - GO = 0
    - ADIF = 0
  - SLEEP
  - No
  - Finish Conversion
    - GO = 0
    - ADIF = 1
  - Wait 2TAD
21.7.1 Faster Conversion - Lower Resolution Trade-off

Not all applications require a result with 8-bits of resolution, but may instead require a faster conversion time. The A/D module allows users to make the trade-off of conversion speed to resolution. Regardless of the resolution required, the acquisition time is the same. To speed up the conversion, the clock source of the A/D module may be switched so that the $T_{AD}$ time violates the minimum specified time (see the applicable electrical specification). Once the $T_{AD}$ time violates the minimum specified time, all the following A/D result bits are not valid (see A/D Conversion Timing in the Electrical Specifications section). The clock sources may only be switched between the three oscillator versions (cannot be switched from/to RC). The equation to determine the time before the oscillator can be switched is as follows:

$$\text{Conversion time} = T_{AD} + N \cdot T_{AD} + (10 - N)(2T_{OSC})$$

Where: $N = \text{number of bits of resolution required}.$

Since the $T_{AD}$ is based from the device oscillator, the user must use some method (a timer, software loop, etc.) to determine when the A/D oscillator may be changed. Example 21-3 shows a comparison of time required for a conversion with 4-bits of resolution, versus the 8-bit resolution conversion. The example is for devices operating at 20 MHz (The A/D clock is programmed for 32T_{OSC}), and assumes that immediately after 5T_{AD}, the A/D clock is programmed for 2T_{OSC}.

The 2T_{OSC} violates the minimum $T_{AD}$ time since the last 4-bits will not be converted to correct values.

Example 21-3: 4-bit vs. 8-bit Conversion Times

<table>
<thead>
<tr>
<th></th>
<th>Freq. (MHz$^{(1)}$)</th>
<th>Resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>4-bit</td>
</tr>
<tr>
<td>$T_{AD}$</td>
<td>20</td>
<td>1.6 $\mu$s</td>
</tr>
<tr>
<td>$T_{OSC}$</td>
<td>20</td>
<td>50 ns</td>
</tr>
<tr>
<td>$T_{AD} + N \cdot T_{AD} + (10 - N)(2T_{OSC})$</td>
<td>20</td>
<td>8.6 $\mu$s</td>
</tr>
</tbody>
</table>

Note 1: A minimum $T_{AD}$ time of 1.6 $\mu$s is required.
Note 2: If the full 8-bit conversion is required, the A/D clock source should not be changed.

21.8 A/D Operation During Sleep

The A/D module can operate during SLEEP mode. This requires that the A/D clock source be set to RC (ADCS1:ADCS0 = 11). When the RC clock source is selected, the A/D module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed, which eliminates all internal digital switching noise from the conversion. When the conversion is completed the GO/DONE bit will be cleared, and the result loaded into the ADRES register. If the A/D interrupt is enabled, the device will wake-up from SLEEP. If the A/D interrupt is not enabled, the A/D module will then be turned off (to conserve power), although the ADON bit will remain set.

When the A/D clock source is another clock option (not RC), a SLEEP instruction will cause the present conversion to be aborted and the A/D module to be turned off, though the ADON bit will remain set.

Turning off the A/D places the A/D module in its lowest current consumption state.

Note: For the A/D module to operate in SLEEP, the A/D clock source must be set to RC (ADCS1:ADCS0 = 11). To perform an A/D conversion in SLEEP, the GO/DONE bit must be set, followed by the SLEEP instruction.
21.9  A/D Accuracy/Error

In systems where the device frequency is low, use of the A/D RC clock is preferred. At moderate to high frequencies, \( T_{AD} \) should be derived from the device oscillator.

The absolute accuracy specified for the A/D converter includes the sum of all contributions for quantization error, integral error, differential error, full scale error, offset error, and monotonicity. It is defined as the maximum deviation from an actual transition versus an ideal transition for any code. The absolute error of the A/D converter is specified at \(< \pm 1 \text{ LSB} \) for \( V_{DD} = V_{REF} \) (over the device’s specified operating range). However, the accuracy of the A/D converter will degrade as \( V_{DD} \) diverges from \( V_{REF} \).

For a given range of analog inputs, the output digital code will be the same. This is due to the quantization of the analog input to a digital code. Quantization error is typically \( \pm 1/2 \text{ LSB} \) and is inherent in the analog to digital conversion process. The only way to reduce quantization error is to increase the resolution of the A/D converter.

Offset error measures the first actual transition of a code versus the first ideal transition of a code. Offset error shifts the entire transfer function. Offset error can be calibrated out of a system or introduced into a system through the interaction of the total leakage current and source impedance at the analog input.

Gain error measures the maximum deviation of the last actual transition and the last ideal transition adjusted for offset error. This error appears as a change in slope of the transfer function. The difference in gain error to full scale error is that full scale does not take offset error into account. Gain error can be calibrated out in software.

Linearity error refers to the uniformity of the code changes. Linearity errors cannot be calibrated out of the system. Integral non-linearity error measures the actual code transition versus the ideal code transition adjusted by the gain error for each code.

Differential non-linearity measures the maximum actual code width versus the ideal code width. This measure is unadjusted.

The maximum pin leakage current is specified in the Device Data Sheet electrical specification parameter D060.

In systems where the device frequency is low, use of the A/D RC clock is preferred. At moderate to high frequencies, \( T_{AD} \) should be derived from the device oscillator. \( T_{AD} \) must not violate the minimum and should be minimized to reduce inaccuracies due to noise and sampling capacitor bleed off.

In systems where the device will enter SLEEP mode after the start of the A/D conversion, the RC clock source selection is required. In this mode, the digital noise from the modules in SLEEP are stopped. This method gives high accuracy.

21.10  Effects of a RESET

A device reset forces all registers to their reset state. This forces the A/D module to be turned off, and any conversion is aborted. The value that is in the ADRES register is not modified for a Power-on Reset. The ADRES register will contain unknown data after a Power-on Reset.
21.11 Use of the CCP Trigger

An A/D conversion may be started by the “special event trigger” of a CCP module. This requires
that the CCPxM3:CCPxM0 bits (CCPxCON<3:0>) be programmed as 1011 and that the A/D
module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, start-
ing the A/D conversion, and the Timer1 counter will be reset to zero. Timer1 is reset to automatic-
ically repeat the A/D acquisition period with minimal software overhead (moving the ADRES to
the desired location). The appropriate analog input channel must be selected and the minimum
acquisition done before the “special event trigger” sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), then the “special event trigger” will be
ignored by the A/D module, but will still reset the Timer1 counter.

21.12 Connection Considerations

If the input voltage exceeds the rail values (VSS or VDD) by greater than 0.3V, then the accuracy
of the conversion is out of specification.

An external RC filter can sometimes be added for anti-aliasing of the input signal. The R compo-
nent should be selected to ensure that the total source impedance is kept under the 10 kΩ rec-
ommended specification. Any external components connected (via hi-impedance) to an analog
input pin (capacitor, zener diode, etc.) should have very little leakage current at the pin.

21.13 Transfer Function

The ideal transfer function of the A/D converter is as follows: the first transition occurs when the
analog input voltage (VAIN) is 1 LSb (or Analog VREF / 256) (Figure 21-6).

Figure 21-6: A/D Transfer Function
Section 21. 8-bit A/D Converter

21.14 Initialization

Example 21-4 shows the initialization of the A/D module for the PIC16C74A

Example 21-4: A/D Initialization (for PIC16C74A)

BSF STATUS, RP0 ; Select Bank1
CLRF ADCON1 ; Configure A/D inputs
BSF PIE1, ADIE ; Enable A/D interrupts
BCF STATUS, RP0 ; Select Bank0
MOVLW 0xC1 ; RC Clock, A/D is on, Channel 0 is selected
MOVWF ADCON0 ;
BCF PIR1, ADIF ; Clear A/D interrupt flag bit
BSF INTCON, PEIE ; Enable peripheral interrupts
BSF INTCON, GIE ; Enable all interrupts
;
; Ensure that the required sampling time for the selected input
; channel has elapsed. Then the conversion may be started.
;
BSF ADCON0, GO ; Start A/D Conversion
; The ADIF bit will be set and the GO/DONE
; bit is cleared upon completion of the
; A/D Conversion.
Question 1: I am using one of your PIC16C7X devices, and I find that the Analog to Digital Converter result is not always accurate. What can I do to improve accuracy?

Answer 1:

1. Make sure you are meeting all of the timing specifications. If you are turning the A/D module off and on, there is a minimum delay you must wait before taking a sample, if you are changing input channels, there is a minimum delay you must wait for this as well, and finally there is Tad, which is the time selected for each bit conversion. This is selected in ADCON0 and should be between 2 and 6\( \mu \)s. If TAD is too short, the result may not be fully converted before the conversion is terminated, and if TAD is made too long the voltage on the sampling capacitor can droop before the conversion is complete. These timing specifications are provided in the data book in a table or by way of a formula, and should be looked up for your specific part and circumstances.

2. Often the source impedance of the analog signal is high (greater than 1k ohms) so the current drawn from the source to charge the sample capacitor can affect accuracy. If the input signal does not change too quickly, try putting a 0.1 \( \mu \)F capacitor on the analog input. This capacitor will charge to the analog voltage being sampled, and supply the instantaneous current needed to charge the 51.2 pf internal holding capacitor.

3. Finally, straight from the data book: “In systems where the device frequency is low, use of the A/D clock derived from the device oscillator is preferred...this reduces, to a large extent, the effects of digital switching noise.” and “In systems where the device will enter SLEEP mode after start of A/D conversion, the RC clock source selection is required. This method gives the highest accuracy.”

Question 2: After starting an A/D conversion may I change the input channel (for my next conversion)?

Answer 2:

After the holding capacitor is disconnected from the input channel, one TAD after the GO bit is set, the input channel may be changed.

Question 3: Do you know of a good reference on A/D’s?

Answer 3:

Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the Mid-Range MCU family (that is they may be written for the Base-Line, or High-End families), but the concepts are pertinent, and could be used (with modification and possible limitations). The current application notes related to the 8-bit A/D are:

<table>
<thead>
<tr>
<th>Title</th>
<th>Application Note #</th>
</tr>
</thead>
<tbody>
<tr>
<td>Using the Analog to Digital Converter</td>
<td>AN546</td>
</tr>
<tr>
<td>Four Channel Digital Voltmeter with Display and Keyboard</td>
<td>AN557</td>
</tr>
</tbody>
</table>
21.17 Revision History

Revision A

This is the initial released revision of the 8-bit A/D module description.