Section 13. Timer2

HIGHLIGHTS

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13.1 Introduction

Timer2 is an 8-bit timer with a prescaler, a postscaler, and a period register. Using the prescaler and postscaler at their maximum settings, the overflow time is the same as a 16-bit timer. Timer2 is the PWM time-base when the CCP module(s) is used in the PWM mode.

Figure 13-1 shows a block diagram of Timer2. The postscaler counts the number of times that the TMR2 register matched the PR2 register. This can be useful in reducing the overhead of the interrupt service routine on the CPU performance.

**Figure 13-1: Timer2 Block Diagram**

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**Note:** TMR2 register output can be software selected by the SSP Module as a baud clock.
13.2 Control Register

Register 13-1 shows the Timer2 control register.

Register 13-1: T2CON: Timer2 Control Register

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6:3</th>
<th>Bit 2</th>
<th>Bit 1:0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOUTPS3</td>
<td>TOUTPS2</td>
<td>TOUTPS1</td>
<td>TOUTPS0</td>
</tr>
<tr>
<td>TMR2ON</td>
<td>T2CKPS1</td>
<td>T2CKPS0</td>
<td></td>
</tr>
<tr>
<td>Unimplemented: Read as ‘0’</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- n = Value at POR reset
13.3 Timer Clock Source
The Timer2 module has one source of input clock, the device clock (Fosc/4). A prescale option of 1:1, 1:4 or 1:16 is software selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

13.4 Timer (TMR2) and Period (PR2) Registers
The TMR2 register is readable and writable, and is cleared on all device resets. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register.

TMR2 is cleared when a WDT, POR, MCLR, or a BOR reset occurs, while the PR2 register is set.

Timer2 can be shut off (disabled from incrementing) by clearing the TMR2ON control bit (T2CON<2>). This minimizes the power consumption of the module.

13.5 TMR2 Match Output
The match output of TMR2 goes to two sources:
1. Timer2 Postscaler
2. SSP Clock Input

There are four bits which select the postscaler. This allows the postscaler a 1:1 to 1:16 scaling (inclusive). After the postscaler overflows, the TMR2 Interrupt flag bit (TMR2IF) is set to indicate the Timer2 overflow. This is useful in reducing the software overhead of the Timer2 interrupt service routine, since it will only execute once every postscaler # of matches.

The match output of TMR2 is also routed to the Synchronous Serial Port module, which may software select this as the clock source for the shift clock.

13.6 Clearing the Timer2 Prescaler and Postscaler
The prescaler and postscaler counters are cleared when any of the following occurs:
• a write to the TMR2 register
• a write to the T2CON register

Note: When T2CON is written TMR2 does not clear.
• any device reset (Power-on Reset, MCLR reset, Watchdog Timer Reset, Brown-out Reset, or Parity Error Reset)

13.7 Sleep Operation
During sleep, TMR2 will not increment. The prescaler will retain the last prescale count, ready for operation to resume after the device wakes from sleep.

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on: POR, BOR, PER</th>
<th>Value on all other resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 000x</td>
<td>0000 000u</td>
</tr>
<tr>
<td>PIR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>PIE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>TMR2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>T2CON</td>
<td>-</td>
<td>TOUTPS3</td>
<td>TOUTPS2</td>
<td>TOUTPS1</td>
<td>TOUTPS0</td>
<td>TMR2ON</td>
<td>T2CKPS1</td>
<td>T2CKPS0</td>
<td>-000 0000</td>
<td>-000 0000</td>
</tr>
<tr>
<td>PR2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1111 1111</td>
<td>1111 1111</td>
</tr>
</tbody>
</table>

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.
Shaded cells are not used by the Timer2 module.

Note 1: The position of this bit is device dependent.
13.8 Initialization

Example 13-1 shows how to initialize the Timer2 module, including specifying the Timer2 prescaler and postscaler.

**Example 13-1: Timer2 Initialization**

```
CLRF T2CON ; Stop Timer2, Prescaler = 1:1, Postscaler = 1:1
CLRF TMR2 ; Clear Timer2 register
CLRF INTCON ; Disable interrupts
BSF STATUS, RP0 ; Bank1
CLRF PIE1 ; Disable peripheral interrupts
BCF STATUS, RP0 ; Bank0
CLAF PIR1 ; Clear peripheral interrupts Flags
MOVWF T2CON ; Timer2 is off
BSF T2CON, TMR2ON ; Timer2 starts to increment

; The Timer2 interrupt is disabled, do polling on the overflow bit

T2_OVFL_WAIT
BTFSS PIR1, TMR2IF ; Has TMR2 interrupt occurred?
GOTO T2_OVFL_WAIT ; NO, continue loop

; Timer has overflowed

BCF PIR1, TMR2IF ; YES, clear flag and continue.
```
13.9 Design Tips

No related Design Tips at this time.
13.10 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the Mid-Range MCU family (that is they may be written for the Base-Line, or High-End families), but the concepts are pertinent, and could be used (with modification and possible limitations). The current application notes related to the Timer2 Module are:

<table>
<thead>
<tr>
<th>Title</th>
<th>Application Note #</th>
</tr>
</thead>
<tbody>
<tr>
<td>Using the CCP Module</td>
<td>AN594</td>
</tr>
<tr>
<td>Air Flow Control using Fuzzy Logic</td>
<td>AN600</td>
</tr>
<tr>
<td>Adaptive Differential Pulse Code Modulation using PICmicros</td>
<td>AN643</td>
</tr>
</tbody>
</table>
13.11 Revision History

Revision A

This is the initial released revision of the Timer2 module description.