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2.0 LCD Registers ............................................................................................................. 3
3.0 LCD Segment Pins Configuration ............................................................................... 6
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1.0 INTRODUCTION

The Liquid Crystal Display (LCD) driver module generates the timing control to drive a Static or Multiplexed LCD panel. In the 100-pin devices (PIC24FJXXXGA3XX), the module drives panels of up to eight commons and up to 60 segments when 5 to 8 commons are used, and up to 64 segments when 1 to 4 commons are used. It also provides control of the LCD pixel data.

The LCD driver module supports:

- Direct driving of LCD panel
- Three LCD clock sources with selectable prescaler
- Up to eight commons:
  - Static (one common)
  - 1/2 Multiplex (two commons)
  - 1/3 Multiplex (three commons)
  - 1/8 Multiplex (eight commons)
- Up to 60 segments (in 100-pin devices when 1/5-1/8 Multiplex is selected), 64 (in 100-pin devices when up to 1/4 Multiplex is selected), 46 (in 80-pin devices when 1/5-1/8 Multiplex is selected), 50 (in 80-pin devices when up to 1/4 Multiplex is selected), 30 (in 64-pin devices when up to 1/4 Multiplex is selected)
- Static, 1/2 or 1/3 LCD Bias
- On-chip Bias generator with dedicated charge pump to support a range of fixed and variable Bias options
- Internal resistors for Bias voltage generation
- Software contrast control for LCD using the internal biasing

A simplified block diagram of the module is shown in Figure 1-1.
Liquid Crystal Display (LCD)

2.0 LCD REGISTERS

The LCD driver module has 40 registers:

- LCD Control Register (LCDCON)
- LCD Phase Register (LCDPS)
- LCD Voltage Regulator Control Register (LCDREG)
- LCD Reference Ladder Control Register (LCDREF)
- Four LCD Segment Enable Registers (LCDSE3:LCDSE0)
- 32 LCD Data Registers (LCDDATA31:LCDDATA0)

The LCDCON register, shown in Register 2-1, controls the overall operation of the module. Once the module is configured, the LCDEN (LCDCON<15>) bit is used to enable or disable the LCD module. The LCD panel can also operate during Sleep by clearing the SLPEN (LCDCON<6>) bit.

The LCDPS register, shown in Register 2-2, configures the LCD clock source prescaler and the type of waveform: Type-A or Type-B. For details on these features, see Section 4.0 “LCD Clock Source Selection”, Table 14-1 and Section 10.0 “LCD Waveform Generation”.

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Register 2-1:  **LCDCON: LCD Control Register**

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCDEN</td>
<td>—</td>
<td>LCDSIDL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 15</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/W-0</th>
<th>R/C-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>SLPEN</td>
<td>WERR</td>
<td>CS1</td>
<td>CS0</td>
<td>LMUX2</td>
<td>LMUX1</td>
<td>LMUX0</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- C = Clearable bit
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**bit 15**  
**LCDEN:** LCD Driver Enable bit  
1 = LCD driver module is enabled  
0 = LCD driver module is disabled

**bit 14**  
Unimplemented: Read as ‘0’

**bit 13**  
**LCDSIDL:** LCD Stop in CPU Idle Mode Control bit  
1 = LCD driver halts in CPU Idle mode  
0 = LCD driver continues to operate in CPU Idle mode

**bit 12-7**  
Unimplemented: Read as ‘0’

**bit 6**  
**SLPEN:** LCD Driver Enable in Sleep Mode bit  
1 = LCD driver module is disabled in Sleep mode  
0 = LCD driver module is enabled in Sleep mode

**bit 5**  
**WERR:** LCD Write Failed Error bit  
1 = LCDDATAx register is written while WA (LCDPS<4>) = 0 (must be cleared in software)  
0 = No LCD write error

**bit 4-3**  
**CS<1:0>:** Clock Source Select bits  
00 = FRC  
01 = LPRC  
1x = SOSC

**bit 2-0**  
**LMUX<2:0>:** LCD Commons Select bits

<table>
<thead>
<tr>
<th>LMUX&lt;2:0&gt;</th>
<th>Multiplex</th>
<th>Bias</th>
</tr>
</thead>
<tbody>
<tr>
<td>111</td>
<td>1/8 MUX (COM&lt;7:0&gt;)</td>
<td>1/3</td>
</tr>
<tr>
<td>110</td>
<td>1/7 MUX (COM&lt;6:0&gt;)</td>
<td>1/3</td>
</tr>
<tr>
<td>101</td>
<td>1/6 MUX (COM&lt;5:0&gt;)</td>
<td>1/3</td>
</tr>
<tr>
<td>100</td>
<td>1/5 MUX (COM&lt;4:0&gt;)</td>
<td>1/3</td>
</tr>
<tr>
<td>011</td>
<td>1/4 MUX (COM&lt;3:0&gt;)</td>
<td>1/3</td>
</tr>
<tr>
<td>010</td>
<td>1/3 MUX (COM&lt;2:0&gt;)</td>
<td>1/2 or 1/3</td>
</tr>
<tr>
<td>001</td>
<td>1/2 MUX (COM&lt;1:0&gt;)</td>
<td>1/2 or 1/3</td>
</tr>
<tr>
<td>000</td>
<td>Static (COM0)</td>
<td>Static</td>
</tr>
</tbody>
</table>
Liquid Crystal Display (LCD)

Register 2-2: LCDPS: LCD Phase Register

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 15-8 Unimplemented: Read as ‘0’

bit 7 WFT: Waveform Type Select bit
1 = Type-B waveform (phase changes on each frame boundary)
0 = Type-A waveform (phase changes within each common type)

bit 6 BIASMD: Bias Mode Select bit
When LMUX<2:0> = 000 or 011-111:
0 = Static Bias mode/1/3 Bias mode (do not set this bit to ‘1’)
When LMUX<2:0> = 001 or 010:
1 = 1/2 Bias mode
0 = 1/3 Bias mode

bit 5 LCDA: LCD Active Status bit
1 = LCD driver module is active
0 = LCD driver module is inactive

bit 4 WA: LCD Write Allow Status bit
1 = Write into the LCDDATAx registers is allowed
0 = Write into the LCDDATAx registers is not allowed

bit 3-0 LP<3:0>: LCD Prescaler Select bits

Legend:
- r = Reserved bit
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

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3.0 LCD SEGMENT PINS CONFIGURATION

The LCDSEx registers configure the functions of the port pins. Setting the segment enable bit for a particular segment configures that pin as an LCD driver. There are four LCD Segment Enable registers, as shown in Table 3-1. The prototype LCDSEx register is shown in Register 3-1.

### Table 3-1: LCDSEx Registers and Associated Segments

<table>
<thead>
<tr>
<th>Register</th>
<th>Segments</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCDSE0</td>
<td>Seg 15:Seg 0</td>
</tr>
<tr>
<td>LCDSE1</td>
<td>Seg 31:Seg 16</td>
</tr>
<tr>
<td>LCDSE2</td>
<td>Seg 47:Seg 32</td>
</tr>
<tr>
<td>LCDSE3</td>
<td>Seg 63:Seg 48</td>
</tr>
</tbody>
</table>

Once the module is initialized for the LCD panel, the individual bits of the LCDDATAx registers are cleared, or set, to represent a clear or dark pixel, respectively.

Specific sets of LCDDATAx registers are used with specific segments and common signals. Each bit represents a unique combination of a specific segment connected to a specific common.

Individual LCDDATAx bits are named by the convention, “SxxCy”, with “xx” as the segment number and “y” as the common number. The relationship is summarized in Register 2-2. The prototype LCDDATAx register is shown in Register 3-2.

**Note:** Not all LCDSEx and LCDDATAx registers are implemented in all devices. Refer to the specific device data sheet for more details.

### Register 3-1: LCDSEx: LCD Segment x Enable Register

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SE(n+15)</td>
<td>SE(n+14)</td>
<td>SE(n+13)</td>
<td>SE(n+12)</td>
<td>SE(n+11)</td>
<td>SE(n+10)</td>
<td>SE(n+9)</td>
<td>SE(n+8)</td>
</tr>
<tr>
<td>bit 15</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>SE(n+7)</td>
<td>SE(n+6)</td>
<td>SE(n+5)</td>
<td>SE(n+4)</td>
<td>SE(n+3)</td>
<td>SE(n+2)</td>
<td>SE(n+1)</td>
<td>SE(n)</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**bit 7-0 SE(n + 15):SE(n): Segment Enable bits**
- For LCDSE0: n = 0
- For LCDSE1: n = 16
- For LCDSE2: n = 32
- For LCDSE3: n = 48
- 1 = Segment function of the pin is enabled; digital I/O is disabled
- 0 = Segment function of the pin is disabled
## Liquid Crystal Display (LCD)

### Register 3-2: LCDDATAx: LCD Data x Register

<table>
<thead>
<tr>
<th>Bit 15</th>
<th>Bit 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>S(n+15)Cy</td>
<td>S(n+14)Cy</td>
</tr>
<tr>
<td>S(n+13)Cy</td>
<td>S(n+12)Cy</td>
</tr>
<tr>
<td>S(n+11)Cy</td>
<td>S(n+10)Cy</td>
</tr>
<tr>
<td>S(n+9)Cy</td>
<td>S(n+8)Cy</td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **-n** = Value at POR
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **x** = Bit is unknown

### Pixel On bits

- **S(n + 15)Cy**: Pixel On bits
- For registers, LCDDATA0 through LCDDATA3: n = (16x), y = 0
- For registers, LCDDATA4 through LCDDATA7: n = (16(x – 4)), y = 1
- For registers, LCDDATA8 through LCDDATA11: n = (16(x – 8)), y = 2
- For registers, LCDDATA12 through LCDDATA15: n = (16(x – 12)), y = 3
- For registers, LCDDATA16 through LCDDATA19: n = (16(x – 16)), y = 4
- For registers, LCDDATA20 through LCDDATA23: n = (16(x – 20)), y = 5
- For registers, LCDDATA24 through LCDDATA27: n = (16(x – 24)), y = 6
- For registers, LCDDATA28 through LCDDATA31: n = (16(x – 28)), y = 7

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>S(n+7)Cy</td>
<td>S(n+6)Cy</td>
</tr>
<tr>
<td>S(n+5)Cy</td>
<td>S(n+4)Cy</td>
</tr>
<tr>
<td>S(n+3)Cy</td>
<td>S(n+2)Cy</td>
</tr>
<tr>
<td>S(n+1)Cy</td>
<td>S(n)Cy</td>
</tr>
</tbody>
</table>

### Table 3-2: LCDDATAx Registers and Bits for Segment and COM Combinations

<table>
<thead>
<tr>
<th>COM Lines</th>
<th>Segments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to 15</td>
<td>16 to 31</td>
</tr>
<tr>
<td>0</td>
<td>LCDDATA0 S00C0:S15C0</td>
</tr>
<tr>
<td>1</td>
<td>LCDDATA4 S00C1:S15C1</td>
</tr>
<tr>
<td>3</td>
<td>LCDDATA12 S00C3:S15C3</td>
</tr>
<tr>
<td>4</td>
<td>LCDDATA16 S00C4:S15C4</td>
</tr>
<tr>
<td>5</td>
<td>LCDDATA20 S00C5:S15C5</td>
</tr>
<tr>
<td>7</td>
<td>LCDDATA28 S00C7:S15C7</td>
</tr>
</tbody>
</table>
4.0 LCD CLOCK SOURCE SELECTION

The LCD driver module has three possible clock sources:

- FRC/8192
- SOSC Clock/32
- LPRC/32

The first clock source is the 8 MHz Fast Internal RC (FRC) oscillator, divided by 8,192. This divider ratio is chosen to provide about 1 kHz output. The divider is not programmable. Instead, the LCD Prescaler bits, LCDPS<3:0>, are used to set the LCD frame clock rate.

The second clock source is the SOSC oscillator/32. This also outputs about 1 kHz when a 32.768 kHz crystal is used with the SOSC oscillator. To use the SOSC oscillator as a clock source, set the SOSCEN (OSCCON<1>) bit.

The third clock source is a 31.25 kHz internal LPRC oscillator/32 that provides approximately 1 kHz output.

The second and third clock sources may be used to continue running the LCD while the processor is in Sleep.

These clock sources are selected through the bits, CS<1:0> (LCDCON<4:3>).

4.1 LCD Prescaler

A 16-bit counter is available as a prescaler for the LCD clock. The prescaler is not directly readable or writable. Its value is set by the LP<2:0> bits (LCDPS<2:0>) that determine the prescaler assignment and prescale ratio.

Selectable prescale values are from 1:1 through 1:16, in increments of one.

Figure 4-1: LCD Clock Generation
5.0 LCD BIAS TYPES

The LCD module can be configured in one of three Bias types:

• Static Bias (Two Voltage Levels: VSS and VDD)
• 1/2 Bias (Three Voltage Levels: VSS, 1/2 VDD and VDD)
• 1/3 Bias (Four Voltage Levels: VSS, 1/3 VDD, 2/3 VDD and VDD)

LCD Bias voltages can be generated with an internal resistor ladder, internal Bias generator or external resistor ladder.

5.1 Internal Resistor Biasing

This mode does not use external resistors, but rather internal resistor ladders that are configured to generate the Bias voltage.

The internal reference ladder actually consists of three separate ladders. Disabling the internal reference ladder disconnects all of the ladders, allowing external voltages to be supplied.

Depending on the total resistance of the resistor ladders, the biasing can be classified as low, medium or high power.

Table 5-1 shows the total resistance of each of the ladders. Figure 5-1 shows the internal resistor ladder connections. When the internal resistor ladder is selected, the Bias voltage will be internal; it can also provide software contrast control (using LCDCST<2:0>).

<table>
<thead>
<tr>
<th>Power Mode</th>
<th>Nominal Resistance of Entire Ladder</th>
<th>IDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>3 MΩ</td>
<td>1 µA</td>
</tr>
<tr>
<td>Medium</td>
<td>300 kΩ</td>
<td>10 µA</td>
</tr>
<tr>
<td>High</td>
<td>30 kΩ</td>
<td>100 µA</td>
</tr>
</tbody>
</table>
There are two power modes, designated as “Mode A” and “Mode B”. Mode A is set by the bits, LRLAP<1:0>, and Mode B by the LRLBP<1:0> bits. The resistor ladder to use for Modes A and B are selected by the bits, LRLAP<1:0> and LRLBP<1:0>, respectively.

Each ladder has a matching contrast control ladder, tuned to the nominal resistance of the reference ladder. This contrast control resistor can be controlled by the LCDCST<2:0> bits (LCDREF<13:11>). Disabling the internal reference ladder results in all of the ladders being disconnected, allowing external voltages to be supplied.

To get additional current in High-Power mode, when LRLAP<1:0> (LCDREF<7:6>) = 11, both the medium and high-power resistor ladders are activated.

Whenever the LCD module is inactive (LCDA (LCDPS<5>) = 0), the reference ladder will be turned off.
5.1.1 AUTOMATIC POWER MODE SWITCHING

As an LCD segment is electrically only a capacitor, current is drawn only during the interval when the voltage is switching. To minimize total device current, the LCD reference ladder can be operated in a different power mode for the transition portion of the duration. This is controlled by the LCDREF register.

Mode A Power mode is active for a programmable time, beginning at the time when the LCD segment waveform is transitioning. The LRLAT<2:0> (LCDREF<2:0>) bits select how long the transition or if the Mode A is active. Mode B Power mode is active for the remaining time before the segments or commons change again.

As shown in Figure 5-2, there are 32 counts in a single segment time. Type-A can be chosen during the time when the waveform is in transition. Type-B can be used when the clock is stable or not in transition.

By using this feature of automatic power switching using Type-A/Type-B, the power consumption can be optimized for a given contrast.

Figure 5-2: LCD Reference Ladder Power Mode Switching Diagram
5.1.2 CONTRAST CONTROL
The LCD contrast control circuit consists of a 7-tap resistor ladder, controlled by the LCDCST<2:0> bits (see Figure 5-3).

Figure 5-3: Internal Reference and Contrast Control Block Diagram

5.1.3 INTERNAL REFERENCE
Under firmware control, an internal reference for the LCD Bias voltages can be enabled. When enabled, the source of this voltage can be VDD.

When no internal reference is selected, the LCD contrast control circuit is disabled and the LCD Bias must be provided externally. Whenever the LCD module is inactive (LCDA = 0), the internal reference will be turned off.

5.1.4 VLCDxPE PINS
The VLCD3PE, VLCD2PE and VLCD1PE pins provide the ability for an external LCD Bias network to be used instead of the internal ladder. Use of the VLCDxPE pins does not prevent use of the internal ladder.

Each VLCDxPE pin has an independent control in the LCDREF register, allowing access to any or all of the LCD Bias signals.

This architecture allows for maximum flexibility in different applications. The VLCDxPE pins could be used to add capacitors to the internal reference ladder for increasing the drive capacity. For applications where the internal contrast control is insufficient, the firmware can choose to enable only the VLCD3PE pin, allowing an external contrast control circuit to use the internal reference divider.
## Liquid Crystal Display (LCD)

### Register 5-1: LCDREF: LCD Reference Ladder Control Register

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCDIRE</td>
<td>—</td>
<td>LCDCST2</td>
<td>LCDCST1</td>
<td>LCDCST0</td>
<td>VLCD3PE</td>
<td>VLCD2PE</td>
<td>VLCD1PE</td>
</tr>
</tbody>
</table>

**bit 15**  
LCDIRE: LCD Internal Reference Enable bit  
1 = Internal LCD reference is enabled and connected to the internal contrast control circuit  
0 = Internal LCD reference is disabled

**bit 14**  
Unimplemented: Read as ‘0’

**bit 13-11**  
LCDCST<2:0>: LCD Contrast Control bits  
Selects the Resistance of the LCD Contrast Control Resistor Ladder:  
111 = Resistor ladder is at maximum resistance (minimum contrast)  
110 = Resistor ladder is at 6/7th of maximum resistance  
101 = Resistor ladder is at 5/7th of maximum resistance  
100 = Resistor ladder is at 4/7th of maximum resistance  
011 = Resistor ladder is at 3/7th of maximum resistance  
010 = Resistor ladder is at 2/7th of maximum resistance  
001 = Resistor ladder is at 1/7th of maximum resistance  
000 = Minimum resistance (maximum contrast); resistor ladder is shorted

**bit 10**  
VLCD3PE: LCD Bias 3 Pin Enable bit  
1 = Bias 3 level is connected to the external pin, LCDBIAS3  
0 = Bias 3 level is internal (internal resistor ladder)

**bit 9**  
VLCD2PE: LCD Bias 2 Pin Enable bit  
1 = Bias 2 level is connected to the external pin, LCDBIAS2  
0 = Bias 2 level is internal (internal resistor ladder)

**bit 8**  
VLCD1PE: LCD Bias 1 Pin Enable bit  
1 = Bias 1 level is connected to the external pin, LCDBIAS1  
0 = Bias 1 level is internal (internal resistor ladder)

**bit 7-6**  
LRLAP<1:0>: LCD Reference Ladder A Time Power Control bits  
During Time Interval A:  
11 = Internal LCD reference ladder is powered in High-Power mode  
10 = Internal LCD reference ladder is powered in Medium Power mode  
01 = Internal LCD reference ladder is powered in Low-Power mode  
00 = Internal LCD reference ladder is powered down and unconnected

**bit 5-4**  
LRLBP<1:0>: LCD Reference Ladder B Time Power Control bits  
During Time Interval B:  
11 = Internal LCD reference ladder is powered in High-Power mode  
10 = Internal LCD reference ladder is powered in Medium Power mode  
01 = Internal LCD reference ladder is powered in Low-Power mode  
00 = Internal LCD reference ladder is powered down and unconnected

**bit 3**  
Unimplemented: Read as ‘0’

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5.2 LCD Bias Generation

The LCD driver module is capable of generating the required Bias voltages for LCD operation with a minimum of external components. This includes the ability to generate the different voltage levels required by the different Bias types that are required by the LCD. The driver module can also provide Bias voltages, both above and below the microcontroller VDD, through the use of an on-chip LCD voltage regulator.

5.2.1 LCD BIAS TYPES

There is support for three Bias types based on the waveforms generated to control segments and commons:

- Static (two discrete levels)
- 1/2 Bias (three discrete levels)
- 1/3 Bias (four discrete levels)

The use of different waveforms in driving the LCD is discussed in more detail in Section 10.0 “LCD Waveform Generation”.

5.2.2 LCD VOLTAGE REGULATOR

The purpose of the LCD regulator is to provide proper Bias voltage and good contrast for the LCD, regardless of VDD levels. This module contains a charge pump and internal voltage reference. The regulator can be configured by using external components to boost Bias voltage above VDD. It can also operate a display at a constant voltage below VDD. The regulator can also be selectively disabled to allow Bias voltages to be generated by an external resistor network.

The LCD regulator is controlled through the LCDREG register (Register 5-2). It is enabled or disabled using the CKSEL<1:0> bits, while the charge pump can be selectively enabled using the CPEN bit. When the regulator is enabled, the MODE13 bit is used to select the Bias type. The peak LCD Bias voltage, measured as a difference between the potentials of LCDBIAS3 and LCDBIAS0, is configured with the BIAS<2:0> bits.
Liquid Crystal Display (LCD)

Register 5-2: LCDREG: LCD Voltage Regulator Control Register

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 15: CPEN: LCD Charge Pump Enable bit
- 1 = Charge pump enabled; highest LCD Bias voltage is 3.6V
- 0 = Charge pump disabled; highest LCD Bias voltage is \( \text{AVDD} \)

bit 14-6: Unimplemented: Read as ‘0’

bit 5-3: BIAS<2:0>: Regulator Voltage Output Control bits

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>111</td>
<td>3.60V peak (offset on LCDBIAS0 of 0V)</td>
</tr>
<tr>
<td>110</td>
<td>3.47V peak (offset on LCDBIAS0 of 0.13V)</td>
</tr>
<tr>
<td>101</td>
<td>3.34V peak (offset on LCDBIAS0 of 0.26V)</td>
</tr>
<tr>
<td>100</td>
<td>3.21V peak (offset on LCDBIAS0 of 0.39V)</td>
</tr>
<tr>
<td>011</td>
<td>3.08V peak (offset on LCDBIAS0 of 0.52V)</td>
</tr>
<tr>
<td>010</td>
<td>2.95V peak (offset on LCDBIAS0 of 0.65V)</td>
</tr>
<tr>
<td>001</td>
<td>2.82V peak (offset on LCDBIAS0 of 0.78V)</td>
</tr>
<tr>
<td>000</td>
<td>2.69V peak (offset on LCDBIAS0 of 0.91V)</td>
</tr>
</tbody>
</table>

bit 2: MODE13: 1/3 LCD Bias Enable bit
- 1 = Regulator output supports 1/3 LCD Bias mode
- 0 = Regulator output supports Static LCD Bias mode

bit 1-0: CKSEL<1:0>: Regulator Clock Source Select bits

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>31 kHz LPRC</td>
</tr>
<tr>
<td>10</td>
<td>8 MHz FRC</td>
</tr>
<tr>
<td>01</td>
<td>SOSC</td>
</tr>
<tr>
<td>00</td>
<td>LCD regulator is disabled</td>
</tr>
</tbody>
</table>
5.3 Bias Configurations

dsPIC33/PIC24 family devices have four distinct circuit configurations for LCD Bias generation:

- M0: Regulator with Boost
- M1: Regulator without Boost
- M2: Resistor Ladder with Software Contrast
- M3: Resistor Ladder with Hardware Contrast

5.3.1 M0 (REGULATOR WITH BOOST)

In M0 operation, the LCD charge pump feature is enabled. This allows the regulator to generate voltages up to +3.6V to the LCD (as measured at LCDBIAS3).

M0 uses a Flyback Capacitor connected between VLCAP1 and VLCAP2, as well as filter capacitors on LCDBIAS0 through LCDBIAS3, to obtain the required voltage boost (Figure 5-4). The output voltage (VBIAS) is the difference of the potential between LCDBIAS3 and LCDBIAS0. It is set by the BIAS<2:0> bits, which adjust the offset between LCDBIAS0 and VSS. The Flyback Capacitor (CFLY) acts as a charge storage element for large LCD loads. This mode is useful in those cases where the voltage requirements of the LCD are higher than the microcontroller’s VDD. It also permits software control of the display’s contrast, by adjustment of the Bias voltage, by changing the value of the BIASx bits.

M0 supports Static and 1/3 Bias types. Generation of the voltage levels for 1/3 Bias is handled automatically, but must be configured in software.

M0 is enabled by selecting a valid regulator clock source (CKSEL<1:0> set to any value except ‘00’) and setting the CPEN bit. If a Static Bias type is required, the MODE13 bit must be cleared.

5.3.2 M1 (REGULATOR WITHOUT BOOST)

M1 operation is similar to M0, but does not use the LCD charge pump. It can provide VBIAS up to the voltage level supplied directly to LCDBIAS3. It can be used in cases where VDD for the application is expected to never drop below a level that can provide adequate contrast for the LCD. The connection of external components is very similar to M0, except that LCDBIAS3 must be tied directly to VDD (Figure 5-4).

Note: When the device is put to Sleep while operating in M0 or M1 mode, make sure that the Bias capacitors are fully discharged to get the lowest Sleep current.

- The BIAS<2:0> bits can still be used to adjust contrast in software by changing VBIAS. As with M0, changing these bits changes the offset between LCDBIAS0 and VSS. In M1, this is reflected in the change between the LCDBIAS0 and the voltage tied to LCDBIAS3. Thus, if VDD should change, VBIAS will also change; where in M0, the level of VBIAS is constant.

- Like M0, M1 supports Static and 1/3 Bias types. Generation of the voltage levels for 1/3 Bias is handled automatically, but must be configured in software. M1 is enabled by selecting a valid regulator clock source (CKSEL<1:0> set to any value except ‘00’) and clearing the CPEN bit. If 1/3 Bias type is required, the MODE13 bit should also be set.
Figure 5-4: LCD Regulator Connections for M0 and M1 Configurations

Note 1: These values are provided for design guidance only. They should be optimized for the application by the designer based on the actual LCD specifications.
5.3.3 M2 (RESISTOR LADDER WITH SOFTWARE CONTRAST)

M2 operation also uses the LCD regulator but disables the charge pump. The regulator’s internal voltage reference remains active as a way to regulate contrast. It is used in cases where the current requirements of the LCD exceed the capacity of the regulator’s charge pump.

In this configuration, the LCD Bias voltage levels are created by an external resistor voltage divider, connected across LCDBIAS0 through LCDBIAS3, with the top of the divider tied to VDD (Figure 5-5). The potential at the bottom of the ladder is determined by the LCD regulator’s voltage reference, tied internally to LCDBIAS0. The Bias type is determined by the voltages on the LCDBIAS pins, which are controlled by the configuration of the resistor ladder. Most applications using M2 will use a 1/3 or 1/2 Bias type. While Static Bias can also be used, it offers extremely limited contrast range and additional current consumption over other Bias Generation modes.

Like M1, the LCDBIAS bits can be used to control contrast, limited by the level of VDD supplied to the device. Also, since there is no capacitor required across VLCA1 and VLCAP2, these pins are available as digital I/O ports: RG2 and RG3. M2 is selected by clearing the CKSEL<1:0> bits and setting the CPEN bit.

Figure 5-5: Resistor Ladder Connections for M2 Configuration

<table>
<thead>
<tr>
<th>Bias Level at Pin</th>
<th>Bias Type</th>
<th>1/2 Bias</th>
<th>1/3 Bias</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCDBIAS0</td>
<td>(Internal Low Reference Voltage)</td>
<td>(Internal Low Reference Voltage)</td>
<td></td>
</tr>
<tr>
<td>LCDBIAS1</td>
<td>1/2 VBIAS</td>
<td>1/3 VBIAS</td>
<td></td>
</tr>
<tr>
<td>LCDBIAS2</td>
<td>1/2 VBIAS</td>
<td>2/3 VBIAS</td>
<td></td>
</tr>
<tr>
<td>LCDBIAS3</td>
<td>VBIAS (up to AVDD)</td>
<td>VBIAS (up to AVDD)</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: These values are provided for design guidance only. They should be optimized for the application by the designer based on the actual LCD specifications.
5.3.4 M3 (RESISTOR LADDER WITH HARDWARE CONTRAST)
In M3, the LCD regulator is completely disabled. Like M2, LCD Bias levels are tied to AVDD and are generated using an external divider. The difference is that the internal voltage reference is also disabled and the bottom of the ladder is tied to ground (VSS) (see Figure 5-6). The value of the resistors, and the difference between VSS and AVDD, determine the contrast range; no software adjustment is possible. This configuration is also used where the LCD module’s current requirements exceed the capacity of the charge pump and software contrast control is not needed.

Depending on the Bias type required, resistors are connected between some or all of the pins. A potentiometer can also be connected between LCDBIAS3 and VDD to allow for hardware controlled contrast adjustment.

M3 is selected by clearing the CKSEL<1:0> and CPEN bits.

Figure 5-6: Resistor Ladder Connections for M3 Configuration

<table>
<thead>
<tr>
<th>Bias Level at Pin</th>
<th>Bias Type</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Static</td>
</tr>
<tr>
<td>LCDBIAS0</td>
<td>AVSS</td>
</tr>
<tr>
<td>LCDBIAS1</td>
<td>AVSS</td>
</tr>
<tr>
<td>LCDBIAS2</td>
<td>AVDD</td>
</tr>
<tr>
<td>LCDBIAS3</td>
<td>AVDD</td>
</tr>
</tbody>
</table>

Note 1: These values are provided for design guidance only. They should be optimized for the application by the designer based on the actual LCD specifications.

2: A potentiometer for manual contrast adjustment is optional; it may be omitted entirely.
5.4 Design Considerations for the LCD Charge Pump

When designing applications that use the LCD regulator with the charge pump enabled, users must always consider both the dynamic current and RMS (Static) current requirements of the display, and what the charge pump can deliver. Both dynamic and Static current can be determined by Equation 5-1:

**Equation 5-1:**

\[ I = C \times \frac{\Delta V}{\Delta T} \]

For dynamic current, \( C \) is the value of the capacitors attached to LCDBIAS3 and LCDBIAS2. The variable, \( \Delta V \), is the voltage drop allowed on C2 and C3 during a voltage switch on the LCD display, and \( \Delta T \) is the duration of the transient current after a clock pulse occurs.

For practical design purposes, these will be assumed to be 0.047 ìF for \( C \), 0.1V for \( \Delta V \) and 1 is for \( \Delta T \). This yields a dynamic current of 4.7 mA for 1 is.

RMS (Root Mean Square) current is determined by the value of CFLY for \( C \), the voltage across VLCAP1 and VLCAP2 for \( \Delta V \), and the regulator clock period (TPER) for \( \Delta T \). Assuming a CFLY value of 0.047 ìF, a value of 1.02V across CFLY and a TPER of 30, the maximum theoretical Static current will be 1.8 mA. Since the charge pump must charge five capacitors, the maximum current becomes 360 ìA.

For a real world assumption of 50% efficiency, this yields a practical current of 180 ìA. Users should compare the calculated current capacity against the requirements of the LCD. While \( \Delta V \) and \( \Delta T \) are relatively fixed by device design, the values of CFLY and the capacitors on the LCDBIAS pins can be changed to increase or decrease current. As always, any changes should be evaluated in the actual circuit for their impact on the application.
6.0 LCD MULTIPLEX TYPES

The LCD driver module can be configured into four Multiplex types:

- Static (only COM0 used)
- 1/2 Multiplex (COM0 and COM1 are used)
- 1/3 Multiplex (COM0, COM1 and COM2 are used)
- 1/4 Multiplex (COM0, COM1, COM2 and COM3 are used)
- 1/5 Multiplex (COM0, COM1, COM2, COM3 and COM4 are used)
- 1/6 Multiplex (COM0, COM1, COM2, COM3, COM4 and COM5 are used)
- 1/7 Multiplex (COM0, COM1, COM2, COM3, COM4, COM5 and COM6 are used)
- 1/8 Multiplex (COM0, COM1, COM2, COM3, COM4, COM5, COM6 and COM7 are used)

The LMUX<2:0> bits setting (LCDCON<2:0>) decides the function of the COM pins. (For details, see Table 6-1.)

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. If the pin is a COM drive, the TRIS setting of that pin is overridden.

**Note:**
On a Power-on Reset, the LMUX<2:0> bits are '000'.

<table>
<thead>
<tr>
<th>LMUX&lt;2:0&gt;</th>
<th>COM7 Pin</th>
<th>COM6 Pin</th>
<th>COM5 Pin</th>
<th>COM4 Pin</th>
<th>COM3 Pin</th>
<th>COM2 Pin</th>
<th>COM1 Pin</th>
<th>COM0 Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>111</td>
<td>COM7</td>
<td>COM6</td>
<td>COM5</td>
<td>COM4</td>
<td>COM3</td>
<td>COM2</td>
<td>COM1</td>
<td>COM0</td>
</tr>
<tr>
<td>110</td>
<td>I/O Pin</td>
<td>COM6</td>
<td>COM5</td>
<td>COM4</td>
<td>COM3</td>
<td>COM2</td>
<td>COM1</td>
<td>COM0</td>
</tr>
<tr>
<td>101</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>COM5</td>
<td>COM4</td>
<td>COM3</td>
<td>COM2</td>
<td>COM1</td>
<td>COM0</td>
</tr>
<tr>
<td>100</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>COM4</td>
<td>COM3</td>
<td>COM2</td>
<td>COM1</td>
<td>COM0</td>
</tr>
<tr>
<td>011</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>COM3</td>
<td>COM2</td>
<td>COM1</td>
<td>COM0</td>
</tr>
<tr>
<td>010</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>COM2</td>
<td>COM1</td>
<td>COM0</td>
</tr>
<tr>
<td>001</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>COM1</td>
<td>COM0</td>
</tr>
<tr>
<td>000</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>I/O Pin</td>
<td>COM0</td>
</tr>
</tbody>
</table>

**Note:** Pins, COM<7:4>, can also be used as SEG pins when 1/4 Multiplex to Static Multiplex are used. These pins can be used as I/O pins only if the respective bits in the LCDSEEx registers are set to '0'.
7.0 SEGMENT ENABLES

The LCDSEx registers are used to select the pin function for each segment pin. The selection allows each pin to operate as either an LCD segment driver or a digital only pin. To configure the pin as a segment driver, the corresponding bits in the LCDSEx registers must be set to '1'. If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. Any bit set in the LCDSEx registers overrides any bit settings in the corresponding TRIS register.

8.0 PIXEL CONTROL

The LCDDATAx registers contain bits that define the state of each pixel. Each bit defines one unique pixel. Table 3-2 shows the correlation of each bit in the LCDDATAx registers to the respective common and segment signals. Any LCD pixel location not being used for display can be used as general purpose RAM.

9.0 LCD FRAME FREQUENCY

The rate at which the COM and SEG outputs change is called the LCD frame frequency.

Table 9-1: Frame Frequency Formulas

<table>
<thead>
<tr>
<th>Multiplex</th>
<th>Frame Frequency =</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static (000)</td>
<td>Clock Source/(4 x 1 x (LP&lt;3:0&gt; + 1))</td>
</tr>
<tr>
<td>1/2 (001)</td>
<td>Clock Source/(2 x 2 x (LP&lt;3:0&gt; + 1))</td>
</tr>
<tr>
<td>1/3 (010)</td>
<td>Clock Source/(1 x 3 x (LP&lt;3:0&gt; + 1))</td>
</tr>
<tr>
<td>1/4 (011)</td>
<td>Clock Source/(1 x 4 x (LP&lt;3:0&gt; + 1))</td>
</tr>
<tr>
<td>1/5 (100)</td>
<td>Clock Source/(1 x 5 x (LP&lt;3:0&gt; + 1))</td>
</tr>
<tr>
<td>1/6 (101)</td>
<td>Clock Source/(1 x 6 x (LP&lt;3:0&gt; + 1))</td>
</tr>
<tr>
<td>1/7 (110)</td>
<td>Clock Source/(1 x 7 x (LP&lt;3:0&gt; + 1))</td>
</tr>
<tr>
<td>1/8 (111)</td>
<td>Clock Source/(1 x 8 x (LP&lt;3:0&gt; + 1))</td>
</tr>
</tbody>
</table>

Note: The clock source is FRC/8192, SOSC/32 or LPRC/32.

10.0 LCD WAVEFORM GENERATION

LCD waveform generation is based on the philosophy that the net AC voltage across the dark pixel should be maximized and the net AC voltage across the clear pixel should be minimized. The net DC voltage across any pixel should be zero.

The COM signal represents the time slice for each common, while the SEG contains the pixel data.

The pixel signal (COM-SEG) will have no DC component and can take only one of the two RMS values. The higher RMS value will create a dark pixel and a lower RMS value will create a clear pixel.

As the number of commons increases, the delta between the two RMS values decreases. The delta represents the maximum contrast that the display can have.

The LCDs can be driven by two types of waveforms: Type-A and Type-B. In a Type-A waveform, the phase changes within each common type, whereas a Type-B waveform's phase changes on each frame boundary. Thus, Type-A waveforms maintain 0 Vdc over a single frame, whereas Type-B waveforms take two frames.

Note: If Sleep has to be executed with LCD Sleep enabled (SLPEN (LCDCON<6>) = 1), care must be taken to execute Sleep only when the Vdc on all the pixels is '0'.
Figure 10-1 through Figure 10-13 provide waveforms for Static, Half-Multiplex, One-Third Multiplex and Quarter Multiplex drives for Type-A and Type-B waveforms.

Figure 10-1: Type-A/Type-B Waveforms in Static Drive
Figure 10-2: Type-A Waveforms in 1/2 MUX, 1/2 Bias Drive

- COM0
- COM1
- SEG0
- SEG1
- SEG2
- SEG3

V2
V1
V0
V2
V1
V0
V2
V1
V0
V2
V1
V0
V2
V1
V0
V2
V1
V0

COM0-SEG0
COM0-SEG1

1 Frame
Figure 10-3: Type-B Waveforms in 1/2 MUX, 1/2 Bias Drive
Figure 10-4: Type-A Waveforms in 1/2 MUX, 1/3 Bias Drive
Figure 10-5: Type-B Waveforms in 1/2 MUX, 1/3 Bias Drive

- V3
- V2
- V1
- V0
- V3
- V2
- V1
- V0
- V3
- V2
- V1
- V0
- V3
- V2
- V1
- V0

COM0-SEG0

COM0-SEG1

2 Frames
Figure 10-6: Type-A Waveforms in 1/3 MUX, 1/2 Bias Drive
Figure 10-7: Type-B Waveforms in 1/3 MUX, 1/2 Bias Drive
Figure 10-8: Type-A Waveforms in 1/3 MUX, 1/3 Bias Drive
Figure 10-9: Type-B Waveforms in 1/3 MUX, 1/3 Bias Drive
Figure 10-10: Type-A Waveforms in 1/4 MUX, 1/3 Bias Drive
Figure 10-11: Type-B Waveforms in 1/4 MUX, 1/3 Bias Drive

<table>
<thead>
<tr>
<th>COM3</th>
<th>COM2</th>
<th>COM1</th>
<th>COM0</th>
<th>SEG0</th>
<th>SEG1</th>
</tr>
</thead>
<tbody>
<tr>
<td>V3</td>
<td>V2</td>
<td>V1</td>
<td>V0</td>
<td>V3</td>
<td>V2</td>
</tr>
<tr>
<td>V3</td>
<td>V2</td>
<td>V1</td>
<td>V0</td>
<td>V3</td>
<td>V2</td>
</tr>
<tr>
<td>V3</td>
<td>V2</td>
<td>V1</td>
<td>V0</td>
<td>V3</td>
<td>V2</td>
</tr>
<tr>
<td>V3</td>
<td>V2</td>
<td>V1</td>
<td>V0</td>
<td>V3</td>
<td>V2</td>
</tr>
<tr>
<td>V3</td>
<td>V2</td>
<td>V1</td>
<td>V0</td>
<td>V3</td>
<td>V2</td>
</tr>
<tr>
<td>V3</td>
<td>V2</td>
<td>V1</td>
<td>V0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- 2 Frames
Figure 10-12: Type-A Waveforms in 1/8 MUX, 1/3 Bias Drive
Figure 10-13: Type-B Waveforms in 1/8 MUX, 1/3 Bias Drive
11.0 LCD INTERRUPTS

The LCD timing generation provides an interrupt that defines the LCD frame timing. This interrupt can be used to coordinate the writing of the pixel data with the start of a new frame, which produces a visually crisp transition of the image.

This interrupt can also be used to synchronize external events to the LCD. For example, the interface to an external segment driver can be synchronized for segment data updates to the LCD frame.

A new frame is defined as beginning at the leading edge of the COM0 common signal. The interrupt will be set immediately after the LCD controller completes accessing all pixel data required for a frame. This will occur at a fixed interval before the frame boundary (TFINT), as shown in Figure 11-1.

The LCD controller will begin to access data for the next frame, within the interval from the interrupt to when the controller begins accessing data after the interrupt (TFWR). New data must be written within TFWR, as this is when the LCD controller will begin to access the data for the next frame.

When the LCD driver is running with Type-B waveforms and the LMUX<2:0> bits are not equal to '00', there are some additional issues.

Since the DC voltage on the pixel takes two frames to maintain 0V, the pixel data must not change between subsequent frames. If the pixel data was allowed to change, the waveform for the odd frames would not necessarily be the complement of the waveform generated in the even frames, and a DC component would be introduced into the panel. Because of this, using Type-B waveforms requires synchronizing the LCD pixel updates to occur within a subframe after the frame interrupt.

To correctly sequence writing in Type-B, the interrupt only occurs on complete phase intervals. If the user attempts to write when the write is disabled, the WERR bit (LCDCON<5>) is set.

Note: The interrupt is not generated when the Type-A waveform is selected and when the Type-B with no Multiplex (Static) is selected.
Liquid Crystal Display (LCD)

Figure 11-1: Example Waveforms and Interrupt Timing in Quarter Duty Cycle Drive

TFWR = TFRAME/2 * (LMUX<2:0> + 1) + TCY/2

TFINT = (TFWR/2 – (2 TCY + 40 ns)) → Minimum = 1.5(TFRAME/4) – (2 TCY + 40 ns)

(TFWR/2 – (1 TCY + 40 ns)) → Maximum = 1.5(TFRAME/4) – (1 TCY + 40 ns)
12.0 CONFIGURING THE LCD MODULE

To configure the LCD module:

1. Select the frame clock prescale using bits, LP<2:0> (LCDPS<2:0>).
2. Configure the appropriate pins to function as segment drivers using the LCDSEx registers.
3. If using the internal reference resistors for biasing, enable the internal reference ladder and:
   • Define the Mode A and Mode B interval by using the LRLAT<2:0> bits (LCDREF<2:0>)
   • Define the low, medium or high ladder for Mode A and Mode B by using the
     LRLAP<1:0> bits (LCDREF<7:6>) and the LRLBP<1:0> bits (LCDREF<5:4>), respectively
   • Set the VLCDxPE bits (LCDREF<10:8>) and enable the LCDIRE bit (LCDREF<15>)
4. Configure the following LCD module functions using the LCDCON register:
   • Multiplex and Bias mode – LMUX<2:0> bits
   • Timing Source – CS<1:0> bits
   • Sleep mode – SLPEN bit
5. Write the initial values to the LCD Pixel Data registers: LCDDATA0 through LCDDATA31.
6. Clear the LCD Interrupt Flag, LCDIF, and if desired, enable the interrupt by setting bit, LCDIE.
7. Enable the LCD module by setting bit, LCDEN (LCDCON<15>).
13.0 OPERATION DURING SLEEP

The LCD module can operate during Sleep. The selection is controlled by the SLPEN bit (LCDCON<6>). Setting the SLPEN bit allows the LCD module to go to Sleep. Clearing the SLPEN bit allows the module to continue to operate during Sleep.

If a SLEEP instruction is executed and SLPEN = 1, the LCD module will cease all functions and go into a very Low-Current Consumption mode. The module will stop operation immediately and drive the minimum LCD voltage on both segment and common lines. Figure 13-1 shows this operation.

The LCD module current consumption will not decrease in this mode, but the overall consumption of the device will be lower due to the shutdown of the core and other peripheral functions.

To ensure that no DC component is introduced on the panel, the SLEEP instruction should be executed immediately after a LCD frame boundary. The LCD interrupt can be used to determine the frame boundary. See Section 11.0 “LCD Interrupts” for the formulas to calculate the delay.

If a SLEEP instruction is executed and SLPEN = 0, the module will continue to display the current contents of the LCDDATAx registers. The LCD data cannot be changed.

Figure 13-1: Sleep Entry/Exit when SLPEN = 1 or CS<1:0> = 00
### 14.0 REGISTERS

#### Table 14-1: Special Function Registers Associated with LCD Driver Module

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<th>Bit 14</th>
<th>Bit 13</th>
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<td>Legend:</td>
<td>— Unimplemented bit; r = Reserved bit</td>
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15.0 REVISION HISTORY

Revision A (December 2010)
This is the initial released revision of this document.

Revision B (October 2013)
Corrected CS<1:0> bit information in Register 2-1.
Removed MUX from Figure 5-3.
Minor typographical edits throughout document.
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