The SST39VF1681 / SST39VF1682 are 2M x8 CMOS Multi-Purpose Flash Plus (MPF+) manufactured with SST proprietary, high performance CMOS Super-Flash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39VF1681 / SST39VF1682 write (Program or Erase) with a 2.7-3.6V power supply. These devices conforms to JEDEC standard pinouts for x8 memories.

Features

- Organized as 2M x8
- Single Voltage Read and Write Operations
  - 2.7-3.6V
- Superior Reliability
  - Endurance: 100,000 Cycles (Typical)
  - Greater than 100 years Data Retention
- Low Power Consumption (typical values at 5 MHz)
  - Active Current: 9 mA (typical)
  - Standby Current: 3 µA (typical)
  - Auto Low Power Mode: 3 µA (typical)
- Hardware Block-Protection/ WP# Input Pin
  - Top Block-Protection (top 64 KByte) for SST39VF1682
  - Bottom Block-Protection (bottom 64 KByte) for SST39VF1681
- Sector-Erase Capability
  - Uniform 4 KByte sectors
- Block-Erase Capability
  - Uniform 64 KByte blocks
- Chip-Erase Capability
- Erase-Suspend/Erase-Resume Capabilities
- Hardware Reset Pin (RST#)
- Security-ID Feature
  - SST: 128 bits; User: 128 bits
- Fast Read Access Time:
  - 70 ns
- Latched Address and Data
- Fast Erase and Byte-Program:
  - Sector-Erase Time: 18 ms (typical)
  - Block-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 40 ms (typical)
  - Byte-Program Time: 7 µs (typical)
- Automatic Write Timing
  - Internal VPP Generation
- End-of-Write Detection
  - Toggle Bits
  - Data# Polling
- CMOS I/O Compatibility
- JEDEC Standard
  - Flash EEPROM Pinouts and Command sets
- Packages Available
  - 48-ball TFBGA (6mm x 8mm)
  - 48-lead TSOP (12mm x 20mm)
- All devices are RoHS compliant
Product Description

The SST39VF168x devices are 2M x8 CMOS Multi-Purpose Flash Plus (MPF+) manufactured with SST’s proprietary, high performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39VF168x write (Program or Erase) with a 2.7-3.6V power supply. These devices conform to JEDEC standard pinouts for x8 memories.

Featuring high performance Byte-Program, the SST39VF168x devices provide a typical Byte-Program time of 7 µsec. These devices use Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent write, they have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed typical endurance of 100,000 cycles. Data retention is rated at greater than 100 years.

The SST39VF168x devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, they significantly improve performance and reliability, while lowering power consumption. They inherently use less energy during Erase and Program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. These devices also improve flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet high density, surface mount requirements, the SST39VF168x are offered in both 48-ball TFBGA and 48-lead TSOP packages. See Figures 2 and 3 for pin assignments.
Block Diagram

Figure 1: SST39VF1681 / SST39VF1682 Block Diagram

Pin Description

Figure 2: Pin Assignments for 48-lead TFBGA
Figure 3: Pin Assignments for 48-lead TSOP

Table 1: Pin Description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin Name</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{MS}$</td>
<td>Address Inputs</td>
<td>To provide memory addresses. During Sector-Erase $A_{MS}$-$A_{12}$ address lines will select the sector. During Block-Erase $A_{MS}$-$A_{16}$ address lines will select the block.</td>
</tr>
<tr>
<td>DQ7-DQ0</td>
<td>Data Input/output</td>
<td>To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.</td>
</tr>
<tr>
<td>WP#</td>
<td>Write Protect</td>
<td>To protect the top/bottom boot block from Erase/Program operation when grounded.</td>
</tr>
<tr>
<td>RST#</td>
<td>Reset</td>
<td>To reset and return the device to Read mode.</td>
</tr>
<tr>
<td>CE#</td>
<td>Chip Enable</td>
<td>To activate the device when CE# is low.</td>
</tr>
<tr>
<td>OE#</td>
<td>Output Enable</td>
<td>To gate the data output buffers.</td>
</tr>
<tr>
<td>WE#</td>
<td>Write Enable</td>
<td>To control the Write operations.</td>
</tr>
<tr>
<td>VDD</td>
<td>Power Supply</td>
<td>To provide power supply voltage: 2.7-3.6V</td>
</tr>
<tr>
<td>VSS</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>NC</td>
<td>No Connection</td>
<td>Unconnected pins.</td>
</tr>
</tbody>
</table>

1. $A_{MS} =$ Most significant address
   $A_{MS} = A_{20}$ for SST39VF1681/1682
Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

The SST39VF168x also have the Auto Low Power mode which puts the device in a near standby mode after data has been accessed with a valid Read operation. This reduces the $I_{DD}$ active read current from typically 9 mA to typically 3 $\mu$A. The Auto Low Power mode reduces the typical $I_{DD}$ active read current to the range of 2 mA/MHz of Read cycle time. The device exits the Auto Low Power mode with any address transition or control signal transition used to initiate another Read cycle, with no access time penalty. Note that the device does not enter Auto-Low Power mode after power-up with CE# held steadily low, until the first address transition or CE# is driven high.

Read

The Read operation of the SST39VF168x is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 4).

Byte-Program Operation

The SST39VF168x are programmed on a byte-by-byte basis. Before programming, the sector where the byte exists must be fully erased. The Program operation is accomplished in three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed within 10 $\mu$s. See Figures 5 and 6 for WE# and CE# controlled Program operation timing diagrams and Figure 20 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during the internal Program operation are ignored. During the command sequence, WP# should be statically held high or low.

Sector/Block-Erase Operation

The Sector- (or Block-) Erase operation allows the system to erase the device on a sector-by-sector (or block-by-block) basis. The SST39VF168x offer both Sector-Erase and Block-Erase mode. The sector architecture is based on uniform sector size of 4 KByte. The Block-Erase mode is based on uniform block size of 64 KByte. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (50H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (30H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit methods. See Figures 10 and 11 for...
timing waveforms and Figure 24 for the flowchart. Any commands issued during the Sector- or Block-
Erase operation are ignored. When WP# is low, any attempt to Sector- (Block-) Erase the protected
block will be ignored. During the command sequence, WP# should be statically held high or low.

Erase-Suspend/Erase-Resume Commands

The Erase-Suspend operation temporarily suspends a Sector- or Block-Erase operation thus allowing
data to be read from any memory location, or program data into any sector/block that is not suspended
for an Erase operation. The operation is executed by issuing one byte command sequence with Erase-
Suspend command (B0H). The device automatically enters read mode typically within 20 µs after the
Erase-Suspend command had been issued. Valid data can be read from any sector or block that is not
suspended from an Erase operation. Reading at address location within erase-suspended sectors/
blocks will output DQ2 toggling and DQ6 at “1”. While in Erase-Suspend mode, a Byte-Program opera-
tion is allowed except for the sector or block selected for Erase-Suspend.

To resume Sector-Erase or Block-Erase operation which has been suspended the system must issue Erase
Resume command. The operation is executed by issuing one byte command sequence with Erase Resume com-
mand (30H) at any address in the last Byte sequence.

Chip-Erase Operation

The SST39VF168x provide a Chip-Erase operation, which allows the user to erase the entire memory array to
the “1” state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command
(10H) at address AAAH in the last byte sequence. The Erase operation begins with the rising edge of the sixth
WE# or CE#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bit or Data# Poll-
ing. See Table 6 for the command sequence, Figure 10 for timing diagram, and Figure 24 for the flowchart.
Any commands issued during the Chip-Erase operation are ignored. When WP# is low, any attempt to Chip-
Erase will be ignored. During the command sequence, WP# should be statically held high or low.

Write Operation Status Detection

The SST39VF168x provide two software means to detect the completion of a Write (Program or
Erase) cycle, in order to optimize the system write cycle time. The software detection includes two sta-
tus bits: Data# Polling (DQ7) and Toggle Bit (DQ6). The End-of-Write detection mode is enabled after
the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the sys-
tem may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ7 or DQ6. In
order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop
to read the accessed location an additional two (2) times. If both reads are valid, then the device has com-
pleted the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ7)

When the SST39VF168x are in the internal Program operation, any attempt to read DQ7 will produce the
complement of the true data. Once the Program operation is completed, DQ7 will produce true data. Note that
even though DQ7 may have valid data immediately following the completion of an internal Write operation, the
remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent succes-
sive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read DQ7 will pro-
duce a ‘0’. Once the internal Erase operation is completed, DQ7 will produce a ‘1’. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7 for Data# Polling timing diagram and Figure 21 for a flowchart.

**Toggle Bits (DQ6 and DQ2)**

During the internal Program or Erase operation, any consecutive attempts to read DQ6 will produce alternating “1”s and “0”s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ6 bit will stop toggling. The device is then ready for the next operation. For Sector-, Block-, or Chip-Erase, the toggle bit (DQ6) is valid after the rising edge of sixth WE# (or CE#) pulse. DQ6 will be set to “1” if a Read operation is attempted on an Erase-Suspended Sector/Block. If Program operation is initiated in a sector/block not selected in Erase-Suspend mode, DQ6 will toggle.

An additional Toggle Bit is available on DQ2, which can be used in conjunction with DQ6 to check whether a particular sector is being actively erased or erase-suspended. Table 2 shows detailed status bits information. The Toggle Bit (DQ2) is valid after the rising edge of the last WE# (or CE#) pulse of Write operation. See Figure 8 for Toggle Bit timing diagram and Figure 21 for a flowchart.

<table>
<thead>
<tr>
<th>Status</th>
<th>DQ7</th>
<th>DQ6</th>
<th>DQ2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Operation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standard Program</td>
<td>DQ7#</td>
<td>Toggle</td>
<td>No Toggle</td>
</tr>
<tr>
<td>Standard Erase</td>
<td>0</td>
<td>Toggle</td>
<td></td>
</tr>
<tr>
<td>Erase-Suspend Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read from Erase Suspended Sector/Block</td>
<td>1</td>
<td>1</td>
<td>Toggle</td>
</tr>
<tr>
<td>Read from Non- Erase Suspended Sector/Block</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>Program</td>
<td>DQ7#</td>
<td>Toggle</td>
<td>N/A</td>
</tr>
</tbody>
</table>

**Table 2: Write Operation Status**

Note: DQ7 and DQ2 require a valid address when reading status information.

**Data Protection**

The SST39VF168x provide both hardware and software features to protect nonvolatile data from inadvertent writes.

**Hardware Data Protection**

*Noise/Glitch Protection:* A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

*VDD Power Up/Down Detection:* The Write operation is inhibited when VDD is less than 1.5V.

*Write Inhibit Mode:* Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.
Hardware Block Protection

The SST39VF1682 supports top hardware block protection, which protects the top 64 KByte block of the device. The SST39VF1681 supports bottom hardware block protection, which protects the bottom 64 KByte block of the device. The Boot Block address ranges are described in Table 3. Program and Erase operations are prevented on the 64 KByte when WP# is low. If WP# is left floating, it is internally held high via a pull-up resistor, and the Boot Block is unprotected, enabling Program and Erase operations on that block.

Table 3: Boot Block Address Ranges

<table>
<thead>
<tr>
<th>Product</th>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bottom Boot Block</td>
<td></td>
</tr>
<tr>
<td>SST39VF1681</td>
<td>000000H-00FFFFH</td>
</tr>
<tr>
<td>Top Boot Block</td>
<td></td>
</tr>
<tr>
<td>SST39VF1682</td>
<td>1F0000H-1FFFFFFH</td>
</tr>
</tbody>
</table>

Hardware Reset (RST#)

The RST# pin provides a hardware method of resetting the device to read array data. When the RST# pin is held low for at least TRP, any in-progress operation will terminate and return to Read mode. When no internal Program/Erase operation is in progress, a minimum period of TRHR is required after RST# is driven high before a valid Read can take place (see Figure 16).

The Erase or Program operation that has been interrupted needs to be re-initiated after the device resumes normal operation mode to ensure data integrity.

Software Data Protection (SDP)

The SST39VF168x provide the JEDEC approved Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte sequence. These devices are shipped with the Software Data Protection permanently enabled. See Table 6 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within TRC.

Common Flash Memory Interface (CFI)

The SST39VF168x also contain the CFI information to describe the characteristics of the device. In order to enter the CFI Query mode, the system must write three-byte sequence, same as product ID entry command with 98H (CFI Query command) to address AAAH in the last byte sequence. Once the device enters the CFI Query mode, the system can read CFI data at the addresses given in Tables 7 through 9. The system must write the CFI Exit command to return to Read mode from the CFI Query mode.
Product Identification

The Product Identification mode identifies the devices as the SST39VF1681 and SST39VF1682, and manufacturer as SST. Users may use the software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Table 6 for software operation, Figure 12 for the software ID Entry and Read timing diagram, and Figure 22 for the software ID Entry command sequence flowchart.

Table 4: Product Identification

<table>
<thead>
<tr>
<th>Address</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000H</td>
<td>BFH</td>
</tr>
<tr>
<td>0001H</td>
<td>C8H</td>
</tr>
<tr>
<td>0001H</td>
<td>C9H</td>
</tr>
</tbody>
</table>

Product Identification Mode Exit/CFI Mode Exit

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the software ID Exit command sequence, which returns the device to the Read mode. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. Please note that the software ID Exit/CFI Exit command is ignored during an internal Program or Erase operation. See Table 6 for software command codes, Figure 14 for timing waveform, and Figures 22 and 23 for flowcharts.

Security ID

The SST39VF168x devices offer a 256-bit Security ID space which is divided into two 128-bit segments. The first segment is programmed and locked at SST with a random 128-bit number. The user segment is left un-programmed for the customer to program as desired.

To program the user segment of the Security ID, the user must use the Security ID Byte-Program command. To detect end-of-write for the SEC ID, read the toggle bits. Do not use Data# Polling. Once this is complete, the Sec ID should be locked using the User Sec ID Program Lock-Out. This disables any future corruption of this space. Note that regardless of whether or not the Sec ID is locked, neither Sec ID segment can be erased.

The Security ID space can be queried by executing a three-byte command sequence with Enter-SecID command (88H) at address AAAH in the last byte sequence. Execute the Exit-Sec-ID command to exit this mode. Refer to Table 6 for more details.
## Operations

### Table 5: Operation Modes Selection

<table>
<thead>
<tr>
<th>Mode</th>
<th>CE#</th>
<th>OE#</th>
<th>WE#</th>
<th>DQ</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>VIL</td>
<td>VIL</td>
<td>VIH</td>
<td>DOUT</td>
<td>AIN</td>
</tr>
<tr>
<td>Program</td>
<td>VIL</td>
<td>VIL</td>
<td>VIH</td>
<td>D\text{IN}</td>
<td>AIN</td>
</tr>
<tr>
<td>Erase</td>
<td>VIL</td>
<td>VIL</td>
<td>VIH</td>
<td>X\text{1}</td>
<td>Sector or block address, XXH for Chip-Erase</td>
</tr>
<tr>
<td>Standby</td>
<td>VIL</td>
<td>X</td>
<td>X</td>
<td>High Z</td>
<td>X</td>
</tr>
<tr>
<td>Write Inhibit</td>
<td>X</td>
<td>VIL</td>
<td>X</td>
<td>High Z/ DOUT</td>
<td>X</td>
</tr>
<tr>
<td>Product Identification</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Software Mode</td>
<td>VIL</td>
<td>VIL</td>
<td>VIL</td>
<td>See Table 6</td>
<td></td>
</tr>
</tbody>
</table>

1. X can be V\text{IL} or V\text{IH}, but no other value.

### Table 6: Software Command Sequence

<table>
<thead>
<tr>
<th>Command Sequence</th>
<th>1st Bus Write Cycle</th>
<th>2nd Bus Write Cycle</th>
<th>3rd Bus Write Cycle</th>
<th>4th Bus Write Cycle</th>
<th>5th Bus Write Cycle</th>
<th>6th Bus Write Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Addr\text{1}</td>
<td>Data</td>
<td>Addr\text{1}</td>
<td>Data</td>
<td>Addr\text{1}</td>
<td>Data</td>
</tr>
<tr>
<td>Byte-Program</td>
<td>AAAH</td>
<td>AAH</td>
<td>555H</td>
<td>55H</td>
<td>AAAH</td>
<td>A0H</td>
</tr>
<tr>
<td>Sector-Erase</td>
<td>AAAH</td>
<td>AAH</td>
<td>555H</td>
<td>55H</td>
<td>AAAH</td>
<td>80H</td>
</tr>
<tr>
<td>Block-Erase</td>
<td>AAAH</td>
<td>AAH</td>
<td>555H</td>
<td>55H</td>
<td>AAAH</td>
<td>80H</td>
</tr>
<tr>
<td>Chip-Erase</td>
<td>AAAH</td>
<td>AAH</td>
<td>555H</td>
<td>55H</td>
<td>AAAH</td>
<td>80H</td>
</tr>
<tr>
<td>Erase-Suspend</td>
<td>XXXXH</td>
<td>B0H</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Erase-Resume</td>
<td>XXXXH</td>
<td>30H</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Query Sec ID\text{3}</td>
<td>AAAH</td>
<td>AAH</td>
<td>555H</td>
<td>55H</td>
<td>AAAH</td>
<td>88H</td>
</tr>
<tr>
<td>User Security ID</td>
<td>AAAH</td>
<td>AAH</td>
<td>555H</td>
<td>55H</td>
<td>AAAH</td>
<td>A5H</td>
</tr>
<tr>
<td>Byte-Program Lock-Out</td>
<td>AAAH</td>
<td>AAH</td>
<td>555H</td>
<td>55H</td>
<td>AAAH</td>
<td>85H</td>
</tr>
<tr>
<td>Software ID Entry\text{6,7}</td>
<td>AAAH</td>
<td>AAH</td>
<td>555H</td>
<td>55H</td>
<td>AAAH</td>
<td>90H</td>
</tr>
<tr>
<td>CFI Query Entry</td>
<td>AAAH</td>
<td>AAH</td>
<td>555H</td>
<td>55H</td>
<td>AAAH</td>
<td>98H</td>
</tr>
<tr>
<td>Software ID Exit\text{8,9} /CFI Exit/Sec ID Exit</td>
<td>AAAH</td>
<td>AAH</td>
<td>555H</td>
<td>55H</td>
<td>AAAH</td>
<td>F0H</td>
</tr>
<tr>
<td>Software ID Exit\text{8,9} /CFI Exit/Sec ID Exit</td>
<td>XXH</td>
<td>F0H</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. Address format A\text{11}-A0 (Hex).
2. Addresses A\text{20}-A12 can be V\text{IL} or V\text{IH}, but no other value, for Command sequence for SST39VF1681/1682.
3. BA = Program Byte Address
4. SA\text{X} for Sector-Erase; uses A\text{MS}-A12 address lines
5. BA\text{X} for Block-Erase; uses A\text{MS}-A16 address lines
6. A\text{MS} = Most significant address
7. A\text{MS} = A20 for SST39VF1681/1682
4. With $A_{MS}$-$A_5 = 0$: Sec ID is read with $A_4$-$A_0$.
   SST ID is read with $A_4 = 0$ (Address range = 00000H to 0000FH).
   User ID is read with $A_4 = 1$ (Address range = 00010H to 0001FH).
   Lock Status is read with $A_7$-$A_0 = 0000FFH$. Unlocked: DQ3 = 1 / Locked: DQ3 = 0.
5. Valid Byte Addresses for Sec ID are from 000000H-00000FH and 000020H-00002FH.
6. The device does not remain in Software Product ID Mode if powered down.
7. With $A_{MS}$-$A_1 = 0$: SST Manufacturer ID = 00BFH, is read with $A_0 = 0$,
   SST39VF1681 Device ID = C8H, is read with $A_0 = 1$,
   SST39VF1682 Device ID = C9H, is read with $A_0 = 1$,
   $A_{MS}$ = Most significant address
   $A_{MS} = A_{20}$ for SST39VF1681/1682
8. Both Software ID Exit operations are equivalent
9. If users never lock after programming, Sec ID can be programmed over the previously unprogrammed bits (data=1)
   using the Sec ID mode again (the programmed “0” bits cannot be reversed to “1”).

Table 7: CFI Query Identification String

<table>
<thead>
<tr>
<th>Address</th>
<th>Data</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>10H</td>
<td>51H</td>
<td>Query Unique ASCII string “QRY”</td>
</tr>
<tr>
<td>11H</td>
<td>52H</td>
<td></td>
</tr>
<tr>
<td>12H</td>
<td>59H</td>
<td></td>
</tr>
<tr>
<td>13H</td>
<td>01H</td>
<td>Primary OEM command set</td>
</tr>
<tr>
<td>14H</td>
<td>07H</td>
<td></td>
</tr>
<tr>
<td>15H</td>
<td>00H</td>
<td>Address for Primary Extended Table</td>
</tr>
<tr>
<td>16H</td>
<td>00H</td>
<td></td>
</tr>
<tr>
<td>17H</td>
<td>00H</td>
<td>Alternate OEM command set (00H = none exists)</td>
</tr>
<tr>
<td>18H</td>
<td>00H</td>
<td></td>
</tr>
<tr>
<td>19H</td>
<td>00H</td>
<td>Address for Alternate OEM extended Table (00H = none exits)</td>
</tr>
<tr>
<td>1AH</td>
<td>00H</td>
<td></td>
</tr>
</tbody>
</table>

1. Refer to CFI publication 100 for more details.

Table 8: System Interface Information

<table>
<thead>
<tr>
<th>Address</th>
<th>Data</th>
<th>Data</th>
</tr>
</thead>
</table>
| 18H     | 27H  | $V_{DD}$ Min (Program/Erase) $V_{DD}$-
   $DQ_7$-$DQ_4$: Volts, $DQ_3$-$DQ_0$: 100 millivolts |
| 1CH     | 36H  | $V_{DD}$ Max (Program/Erase) $V_{DD}$-
   $DQ_7$-$DQ_4$: Volts, $DQ_3$-$DQ_0$: 100 millivolts |
| 1DH     | 00H  | $V_{PP}$ min. (00H = no $V_{PP}$ pin)    |
| 1EH     | 00H  | $V_{PP}$ max. (00H = no $V_{PP}$ pin)    |
| 1FH     | 03H  | Typical time out for Byte-Program $2^N$ µs ($2^3 = 8$ µs) |
| 20H     | 00H  | Typical time out for min. size buffer program $2^N$ µs (00H = not supported) |
| 21H     | 04H  | Typical time out for individual Sector/Block-Erase $2^N$ ms ($2^4 = 16$ ms) |
| 22H     | 05H  | Typical time out for Chip-Erase $2^N$ ms ($2^5 = 32$ ms) |
| 23H     | 01H  | Maximum time out for Byte-Program $2^N$ times typical ($2^1 \times 2^3 = 16$ µs) |
| 24H     | 00H  | Maximum time out for buffer program $2^N$ times typical |
| 25H     | 01H  | Maximum time out for individual Sector/Block-Erase $2^N$ times typical ($2^1 \times 2^4 = 32$ ms) |
| 26H     | 01H  | Maximum time out for Chip-Erase $2^N$ times typical ($2^1 \times 2^5 = 64$ ms) |
### Table 9: Device Geometry Information

<table>
<thead>
<tr>
<th>Address</th>
<th>Data</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>27H</td>
<td>15H</td>
<td>Device size = $2^N$ Bytes ($15H = 21; 2^{21} = 2$ MByte)</td>
</tr>
<tr>
<td>28H</td>
<td>00H</td>
<td>Flash Device Interface description; 00H = x8-only asynchronous interface</td>
</tr>
<tr>
<td>29H</td>
<td>00H</td>
<td></td>
</tr>
<tr>
<td>2AH</td>
<td>00H</td>
<td>Maximum number of byte in multi-byte write $= 2^N$ (00H = not supported)</td>
</tr>
<tr>
<td>2BH</td>
<td>00H</td>
<td></td>
</tr>
<tr>
<td>2CH</td>
<td>02H</td>
<td>Number of Erase Sector/Block sizes supported by device</td>
</tr>
<tr>
<td>2DH</td>
<td>FFH</td>
<td>Sector Information ($y + 1$ = Number of sectors; $z \times 256B =$ sector size)</td>
</tr>
<tr>
<td>2EH</td>
<td>01H</td>
<td>$y = 511 + 1 = 512$ sectors ($01FF = 511$)</td>
</tr>
<tr>
<td>2FH</td>
<td>10H</td>
<td></td>
</tr>
<tr>
<td>30H</td>
<td>00H</td>
<td>$z = 16 \times 256$ Bytes = 4 KByte/sector ($0010H = 16$)</td>
</tr>
<tr>
<td>31H</td>
<td>1FH</td>
<td>Block Information ($y + 1$ = Number of blocks; $z \times 256B =$ block size)</td>
</tr>
<tr>
<td>32H</td>
<td>00H</td>
<td>$y = 31 + 1 = 32$ blocks ($1F = 31$)</td>
</tr>
<tr>
<td>33H</td>
<td>00H</td>
<td></td>
</tr>
<tr>
<td>34H</td>
<td>01H</td>
<td>$z = 256 \times 256$ Bytes = 64 KByte/block ($0100H = 256$)</td>
</tr>
</tbody>
</table>
Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ............................................. -55°C to +125°C
Storage Temperature ................................................ -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ...................... -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential .......... -2.0V to V_{DD}+2.0V
Voltage on A_9 Pin to Ground Potential ................................ -0.5V to 13.2V
Package Power Dissipation Capability (Ta = 25°C) ..................... 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) ............. 240°C
Output Short Circuit Current¹ ........................................ 50 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

Table 10: Operating Range

<table>
<thead>
<tr>
<th>Range</th>
<th>Ambient Temp</th>
<th>V_{DD}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>0°C to +70°C</td>
<td>2.7-3.6V</td>
</tr>
<tr>
<td>Industrial</td>
<td>-40°C to +85°C</td>
<td>2.7-3.6V</td>
</tr>
</tbody>
</table>

Table 11: AC Conditions of Test¹

<table>
<thead>
<tr>
<th>Input Rise/Fall Time</th>
<th>Output Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>5ns</td>
<td>C_L = 30 pF</td>
</tr>
</tbody>
</table>

1. See Figures 18 and 19
### Table 12: DC Operating Characteristics $V_{DD} = 2.7$-3.6V

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{DD}$</td>
<td>Power Supply Current</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read$^3$</td>
<td>18 mA</td>
<td>Address input=$V_{IL}/V_{IH}$, at $f=5$ MHz, $V_{DD}=V_{DD}$ Max $CE#=V_{IL}$, $OE#=WE#=V_{IH}$, all I/Os open</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Program and Erase</td>
<td>35 mA</td>
<td>$CE#=WE#=V_{IL}$, $OE#=V_{IH}$</td>
</tr>
<tr>
<td>$I_{SB}$</td>
<td>Standby $V_{DD}$ Current</td>
<td>20 µA</td>
<td>$CE#=V_{IHC}$, $V_{DD}=V_{DD}$ Max</td>
</tr>
<tr>
<td>$I_{ALP}$</td>
<td>Auto Low Power</td>
<td>20 µA</td>
<td>$CE#=V_{ILC}$, $V_{DD}=V_{DD}$ Max $All$ inputs=$V_{SS}$ or $V_{DD}$, $WE#=V_{IHC}$</td>
</tr>
<tr>
<td>$I_{LI}$</td>
<td>Input Leakage Current</td>
<td>1 µA</td>
<td>$V_{IN}=GND$ to $V_{DD}$, $V_{DD}=V_{DD}$ Max</td>
</tr>
<tr>
<td>$I_{LIW}$</td>
<td>Input Leakage Current on WP# pin and RST#</td>
<td>10 µA</td>
<td>$WP#=GND$ to $V_{DD}$ or RST#=GND to $V_{DD}$</td>
</tr>
<tr>
<td>$I_{LO}$</td>
<td>Output Leakage Current</td>
<td>10 µA</td>
<td>$V_{OUT}=GND$ to $V_{DD}$, $V_{DD}=V_{DD}$ Max</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>0.8 V</td>
<td>$V_{DD}=V_{DD}$ Min</td>
</tr>
<tr>
<td>$V_{ILC}$</td>
<td>Input Low Voltage (CMOS)</td>
<td>0.3 V</td>
<td>$V_{DD}=V_{DD}$ Max</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>0.7$V_{DD}$</td>
<td>$V_{DD}=V_{DD}$ Max</td>
</tr>
<tr>
<td>$V_{IHC}$</td>
<td>Input High Voltage (CMOS)</td>
<td>$V_{DD}$-0.3</td>
<td>$V_{DD}=V_{DD}$ Max</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>0.2 V</td>
<td>$I_{OL}=100$ µA, $V_{DD}=V_{DD}$ Min</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td>$V_{DD}$-0.2</td>
<td>$I_{OH}=100$ µA, $V_{DD}=V_{DD}$ Min</td>
</tr>
</tbody>
</table>

1. Typical conditions for the Active Current shown on the front page of the data sheet are average values at 25°C (room temperature), and $V_{DD}=3V$. Not 100% tested.
2. See Figure 18
3. The $I_{DD}$ current listed is typically less than 2mA/MHz, with OE# at $V_{IH}$. Typical $V_{DD}$ is 3V.

### Table 13: Recommended System Power-up Timings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{PU-READ}^1$</td>
<td>Power-up to Read Operation</td>
<td>100</td>
<td>µs</td>
</tr>
<tr>
<td>$T_{PU-WRITE}^1$</td>
<td>Power-up to Program/Erase Operation</td>
<td>100</td>
<td>µs</td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

### Table 14: Capacitance ($T_a = 25°C$, $f=1$ MHz, other pins open)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Condition</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{IO}^1$</td>
<td>I/O Pin Capacitance</td>
<td>$V_{I/O}=0V$</td>
<td>12 pF</td>
</tr>
<tr>
<td>$C_{IN}^1$</td>
<td>Input Capacitance</td>
<td>$V_{IN}=0V$</td>
<td>6 pF</td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
Table 15: Reliability Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum Specification</th>
<th>Units</th>
<th>Test Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>NEND(^{1,2})</td>
<td>Endurance</td>
<td>10,000</td>
<td>Cycles</td>
<td>JEDEC Standard A117</td>
</tr>
<tr>
<td>TDR(^1)</td>
<td>Data Retention</td>
<td>100</td>
<td>Years</td>
<td>JEDEC Standard A103</td>
</tr>
<tr>
<td>ILTH(^1)</td>
<td>Latch Up</td>
<td>100 + I(_DD)</td>
<td>mA</td>
<td>JEDEC Standard 78</td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. \(N_{END}\) endurance rating is qualified as a 10,000 cycle minimum for the whole device. A sector- or block-level rating would result in a higher minimum specification.

Table 16: Read Cycle Timing Parameters \(V_{DD} = 2.7-3.6\)V

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>(SST39VF168x-70)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRC</td>
<td>Read Cycle Time</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>TCE</td>
<td>Chip Enable Access Time</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TAA</td>
<td>Address Access Time</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TOE</td>
<td>Output Enable Access Time</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TCLZ(^1)</td>
<td>CE# Low to Active Output</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>TOLZ(^1)</td>
<td>OE# Low to Active Output</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>TCHZ(^1)</td>
<td>CE# High to High-Z Output</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>TOHZ(^1)</td>
<td>OE# High to High-Z Output</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>TOH(^1)</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>TRP(^1)</td>
<td>RST# Pulse Width</td>
<td>500</td>
<td></td>
</tr>
<tr>
<td>TRHR(^1)</td>
<td>RST# High before Read</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>TRY(^{1,2})</td>
<td>RST# Pin Low to Read Mode</td>
<td>20</td>
<td></td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase, Block-Erase, and Program operations.
   This parameter does not apply to Chip-Erase operations.
### Table 17: Program/Erase Cycle Timing Parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TBP</td>
<td>Byte-Program Time</td>
<td></td>
<td>10</td>
<td>µs</td>
</tr>
<tr>
<td>TAS</td>
<td>Address Setup Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TAH</td>
<td>Address Hold Time</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCS</td>
<td>WE# and CE# Setup Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCH</td>
<td>WE# and CE# Hold Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TOES</td>
<td>OE# High Setup Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TOEH</td>
<td>OE# High Hold Time</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCP</td>
<td>CE# Pulse Width</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TWP</td>
<td>WE# Pulse Width</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TWP(^1)</td>
<td>WE# Pulse Width High</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCH(^1)</td>
<td>CE# Pulse Width High</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TDS</td>
<td>Data Setup Time</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TDH(^1)</td>
<td>Data Hold Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TIDA(^1)</td>
<td>Software ID Access and Exit Time</td>
<td>150</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TSE</td>
<td>Sector-Erase</td>
<td></td>
<td>25</td>
<td>ms</td>
</tr>
<tr>
<td>TBE</td>
<td>Block-Erase</td>
<td></td>
<td>25</td>
<td>ms</td>
</tr>
<tr>
<td>TSC</td>
<td>Chip-Erase</td>
<td></td>
<td>50</td>
<td>ms</td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
**Figure 4:** Read Cycle Timing Diagram

<table>
<thead>
<tr>
<th>ADDRESS AMS-0</th>
<th>CE#</th>
<th>OE#</th>
<th>WE#</th>
<th>DQ15-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TCE</td>
<td>TOE</td>
<td>TOLZ</td>
<td>HIGH-Z</td>
</tr>
<tr>
<td></td>
<td>TRC</td>
<td>TAA</td>
<td></td>
<td>DATA VALID</td>
</tr>
</tbody>
</table>

**Note:** AMS = Most Significant Address  
AMS = A20 for SST39VF168x

**Figure 5:** WE# Controlled Program Cycle Timing Diagram

<table>
<thead>
<tr>
<th>ADDRESS AMS-0</th>
<th>AAA 555 AAA ADDR</th>
<th>WE#</th>
<th>TAH TWP TWSH</th>
<th>OE#</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TBP</td>
<td>CE#</td>
<td>TCH</td>
<td>TCS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DQ7-0</td>
<td>AA 55 A0 DATA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SW0 SW1 SW2</td>
<td>BYTE (ADDR/DATA)</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** AMS = Most Significant Address  
AMS = A20 for SST39VF168x  
WP# must be held in proper logic state (VIL or VIH) 1 µs prior to and 1 µs after the command sequence.  
X can be VIL or VIH, but no other value.
Figure 6: CE# Controlled Program Cycle Timing Diagram

Note: $A_{MS} = \text{Most Significant Address}$

$A_{MS} = A_{20}$ for SST39VF168x

WP# must be held in proper logic state ($V_{IL}$ or $V_{IH}$) 1 µs prior to and 1 µs after the command sequence.

X can be $V_{IL}$ or $V_{IH}$, but no other value.

Figure 7: Data# Polling Timing Diagram

Note: $A_{MS} = \text{Most Significant Address}$

$A_{MS} = A_{20}$ for SST39VF168x
**Figure 8:** Toggle Bits Timing Diagram

**Note:** $A_{MS} = \text{Most Significant Address}$

$A_{MS} = A_{20}$ for SST39VF168x

**Figure 9:** WE# Controlled Chip-Erase Timing Diagram

**Note:** This device also supports CE# controlled Chip-Erase operation.

The WE# and CE# signals are interchangeable as long as minimum timings are meet. (See Table 17.)

$A_{MS} = \text{Most Significant Address}$

$A_{MS} = A_{20}$ for SST39VF168x

WP# must be held in proper logic state ($V_{IL}$ or $V_{IH}$) 1 µs prior to and 1 µs after the command sequence.

X can be $V_{IL}$ or $V_{IH}$, but no other value.
Figure 10: WE# Controlled Block-Erase Timing Diagram

Note: This device also supports CE# controlled Chip-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 17.)

BAx = Block Address
AMS = Most Significant Address
AMS = A20 for SST39VF168x
WP# must be held in proper logic state (VIL or VIH) 1 µs prior to and 1 µs after the command sequence. X can be VIL or VIH, but no other value.
Figure 11: WE# Controlled Sector-Erase Timing Diagram

Note: This device also supports CE# controlled Chip-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 17.)

SAx = Sector Address
AMS = Most Significant Address
AMS = A20 for SST39VF168x
WP# must be held in proper logic state (VIL or VIH) 1 µs prior to and 1 µs after the command sequence.
X can be VIL or VIH, but no other value.
Figure 12: Software ID Entry and Read

ADDRESS A<sub>MS-0</sub>

AAA 555 AAA 0000 0001

Note: Device ID - See Table 4 on page 9
AMS = Most Significant Address
AMS = A<sub>20</sub> for SST39VF168x
WP# must be held in proper logic state (V<sub>IL</sub> or V<sub>IH</sub>) 1 µs prior to and 1 µs after the command sequence.
X can be V<sub>IL</sub> or V<sub>IH</sub> but no other value.

Figure 13: CFI Query Entry and Read

ADDRESS A<sub>MS-0</sub>

AAA 555 AAA

Note: AMS = Most Significant Address
AMS = A<sub>20</sub> for SST39VF168x
WP# must be held in proper logic state (V<sub>IL</sub> or V<sub>IH</sub>) 1 µs prior to and 1 µs after the command sequence.
X can be V<sub>IL</sub> or V<sub>IH</sub> but no other value.
**Figure 14:** Software ID Exit/CFI Exit

Note: $A_{MS} =$ Most Significant Address

$A_{MS} = A_{00}$ for SST39VF168x

WP# must be held in proper logic state ($V_{IL}$ or $V_{IH}$) 1 µs prior to and 1 µs after the command sequence.

X can be $V_{IL}$ or $V_{IH}$ but no other value.

**Figure 15:** Sec ID Entry

Note: $A_{MS} =$ Most Significant Address

$A_{MS} = A_{00}$ for SST39VF168x

WP# must be held in proper logic state ($V_{IL}$ or $V_{IH}$) 1 µs prior to and 1 µs after the command sequence.

X can be $V_{IL}$ or $V_{IH}$ but no other value.
**Figure 16:** RST# Timing Diagram (When no internal operation is in progress)

**Figure 17:** RST# Timing Diagram (During Program or Erase operation)
AC test inputs are driven at $V_{IHT}$ (0.9 $V_{DD}$) for a logic “1” and $V_{ILT}$ (0.1 $V_{DD}$) for a logic “0”. Measurement reference points for inputs and outputs are $V_{IT}$ (0.5 $V_{DD}$) and $V_{OT}$ (0.5 $V_{DD}$). Input rise and fall times (10% ↔ 90%) are <5 ns.

**Note:**
- $V_{IT}$ - $V_{INPUT}$ Test
- $V_{OT}$ - $V_{OUTPUT}$ Test
- $V_{IHT}$ - $V_{INPUT}$ HIGH Test
- $V_{ILT}$ - $V_{INPUT}$ LOW Test

**Figure 18:** AC Input/Output Reference Waveforms

**Figure 19:** A Test Load Example
Figure 20: Byte-Program Algorithm

Start

Load data: AAH
Address: AAAH

Load data: 55H
Address: 555H

Load data: A0H
Address: AAAH

Load Word
Address/Word
Data

Wait for end of
Program (TBP,
Data# Polling
bit, or Toggle bit
operation)

Program
Completed

X can be \( V_{IL} \) or \( V_{IH} \), but no other value
**Figure 21: Wait Options**

- **Internal Timer**
  - Program/Erase Initiated
  - Wait TBP, TSCE, TSE or TBE
  - Program/Erase Completed

- **Toggle Bit**
  - Program/Erase Initiated
  - Read word
  - Read same word
  - Does DQ6 match?
    - No
      - Program/Erase Completed
    - Yes
      - Program/Erase Completed

- **Data# Polling**
  - Program/Erase Initiated
  - Read DQ7
  - Is DQ7 = true data?
    - No
      - Program/Erase Completed
    - Yes
      - Program/Erase Completed
Figure 22: Software ID/CFI Entry Command Flowcharts

CFI Query Entry Command Sequence

1. Load data: AAH
   Address: AAAH
2. Load data: 55H
   Address: 555H
3. Load data: 98H
   Address: AAAH
4. Wait TIDA
5. Read CFI data

Sec ID Query Entry Command Sequence

1. Load data: AAH
   Address: AAAH
2. Load data: 55H
   Address: 555H
3. Load data: 88H
   Address: AAAH
4. Wait TIDA
5. Read Sec ID

Software Product ID Entry Command Sequence

1. Load data: AAH
   Address: AAAH
2. Load data: 55H
   Address: 555H
3. Load data: 90H
   Address: 5555H
4. Wait TIDA
5. Read Software ID

X can be VIL or VIH, but no other value
**Software ID Exit/CFI Exit/Sec ID Exit Command Sequence**

- **Load data: AAH**  
  **Address: AAAH**

- **Load data: 55H**  
  **Address: 555H**

- **Load data: F0H**  
  **Address: AAAH**

- **Wait T\text{IDA}**

- **Return to normal operation**

- **Load data: F0H**  
  **Address: XXH**

- **Wait T\text{IDA}**

- **Return to normal operation**

X can be $V_{IL}$ or $V_{IH}$, but no other value

---

**Figure 23:** Software ID/CFI Exit Command Flowcharts
Figure 24: Erase Command Sequence

**Chip-Erase Command Sequence**
- Load data: AAH
  Address: AAAH
- Load data: 55H
  Address: 555H
- Load data: 80H
  Address: AAAH
- Load data: AAH
  Address: AAAH
- Load data: 55H
  Address: 555H
- Load data: 10H
  Address: AAAH
- Wait TSCE
- Chip erased to FFFFH

**Sector-Erase Command Sequence**
- Load data: AAH
  Address: AAAH
- Load data: 55H
  Address: 555H
- Load data: 80H
  Address: AAAH
- Load data: AAH
  Address: AAAH
- Load data: 55H
  Address: 555H
- Load data: 50H
  Address: SAX
- Wait TSE
- Sector erased to FFFFH

**Block-Erase Command Sequence**
- Load data: AAH
  Address: AAAH
- Load data: 55H
  Address: 555H
- Load data: 80H
  Address: AAAH
- Load data: AAH
  Address: AAAH
- Load data: 55H
  Address: 555H
- Load data: 30H
  Address: BAX
- Wait TBE
- Block erased to FFFFH

X can be $V_{IL}$ or $V_{IH}$, but no other value
Product Ordering Information

<table>
<thead>
<tr>
<th>SST</th>
<th>39</th>
<th>VF</th>
<th>1681</th>
<th>-</th>
<th>70</th>
<th>-</th>
<th>4C</th>
<th>-</th>
<th>B3KE</th>
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</thead>
</table>

- **Environmental Attribute**
  - E¹ = non-Pb
- **Package Modifier**
  - K = 48 leads
- **Package Type**
  - B3 = TFBGA (6mm x 8mm, 0.8mm pitch)
  - E = TSOP (type1, die up, 12mm x 20mm)
- **Temperature Range**
  - C = Commercial = 0°C to +70°C
  - I = Industrial = -40°C to +85°C
- **Minimum Endurance**
  - 4 = 10,000 cycles
- **Read Access Speed**
  - 70 = 70 ns
- **Hardware Block Protection**
  - 1 = Bottom Boot-Block
  - 2 = Top Boot-Block
- **Device Density**
  - 168 = 16 Mbit
- **Voltage**
  - V = 2.7-3.6V
- **Product Series**
  - 39 = Multi-Purpose Flash

¹. Environmental suffix “E” denotes non-Pb solder. SST non-Pb solder devices are “RoHS Compliant”.

### Valid Combinations for SST39VF1681
- SST39VF1681-70-4C-EKE
- SST39VF1681-70-4C-B3KE
- SST39VF1681-70-4I-EKE
- SST39VF1681-70-4I-B3KE

### Valid Combinations for SST39VF1682
- SST39VF1682-70-4C-EKE
- SST39VF1682-70-4C-B3KE
- SST39VF1682-70-4I-EKE
- SST39VF1682-70-4I-B3KE

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.
Packaging Diagrams

Figure 25: 48-lead Thin Small Outline Package (TSOP) 12mm x 20mm
SST Package Code: EK

Note: 1. Complies with JEDEC publication 95 MO-142 DD dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.
Figure 26: 48-ball Thin-profile, Fine-pitch Ball Grid Array (TFBGA) 6mm x 8mm
SST Package Code: B3K

Note: 1. Complies with JEDEC Publication 95, MO-210, variant AB-1, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. Ball opening size is 0.38 mm (0.05 mm)
### Table 18: Revision History

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<th>Number</th>
<th>Description</th>
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<td>00</td>
<td>Initial release</td>
<td>May 2003</td>
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<tr>
<td>01</td>
<td>Change product number from 166x to 168x</td>
<td>Sep 2003</td>
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<tr>
<td>02</td>
<td>Added B3K package and associated MPNs (See page 31)</td>
<td>Oct 2003</td>
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<tr>
<td></td>
<td>Removed 90 ns Commercial temperature for the EK and EKE packages</td>
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<td>03</td>
<td>2004 Data Book</td>
<td>Nov 2003</td>
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<tr>
<td></td>
<td>Updated B3K package diagram</td>
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<tr>
<td>A</td>
<td>Updated document status to “Data Sheet.”</td>
<td>May 2011</td>
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<td>Removed all 90ns information. Edited “Features” on page 1, “Product Ordering Information” on page 31, and Table 16 on page 15.</td>
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<tr>
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<td>Updated T_MINA information in Table 17 on page 16</td>
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<tr>
<td></td>
<td>Applied new document format</td>
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</tr>
<tr>
<td></td>
<td>Released document under the letter revision system</td>
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