MCP65R41/6
3 µA Comparator with Integrated Reference Voltage

Features:
- Factory Set Reference Voltage
  - Available Voltage: 1.21V and 2.4V
  - Tolerance: ±1% (typical)
- Low Quiescent Current: 2.5 µA (typical)
- Propagation Delay: 4 µs with 100 mV Overdrive
- Input Offset Voltage: ±3mV (typical)
- Rail-to-Rail Input: VSS - 0.3V to VDD + 0.3V
- Output Options:
  - MCP65R41 → Push-Pull
  - MCP65R46 → Open-Drain
- Wide Supply Voltage Range: 1.8V to 5.5V
- Packages: SOT23-6

Typical Applications:
- Laptop Computers
- Mobile Phones
- Hand-held Metering Systems
- Hand-held Electronics
- RC Timers
- Alarm and Monitoring Circuits
- Window Comparators

Design Aids:
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards

Description:
The Microchip Technology Inc. MCP65R41/6 family of push-pull and open-drain output comparators are offered with integrated reference voltages of 1.21V and 2.4V. This family provides ±1% (typical) tolerance while consuming 2.5 µA (typical) current. These comparators operate with a single-supply voltage as low as 1.8V to 5.5V, which makes them ideal for low cost and/or battery powered applications.

These comparators are optimized for low-power, single-supply applications with greater than rail-to-rail input operation. The output limits supply current surges and dynamic power consumption while switching. The internal input hysteresis eliminates output switching due to internal noise voltage, reducing current draw. The MCP65R41 output interfaces to CMOS/TTL logic. The open-drain output device MCP65R46 can be used as a level-shifter from 1.6V to 10V using a pull-up resistor. It can also be used as a wired-OR logic.

This family of devices is available in the 6-lead SOT-23 package.

Package Types

Typical Application

Over-Temperature Alert

Thermistor

* Pull-up resistor required for the MCP65R46 only.
## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Absolute Maximum Ratings†

- \( V_{DD} - V_{SS} \) ........................................... 7.0V
- All other inputs and outputs........... \( V_{SS} - 0.3V \) to \( V_{DD} + 0.3V \)
- Difference Input voltage ........................... \( |V_{DD} - V_{SS}| \)
- Output Short Circuit Current ........................ ±25 mA
- Current at Input Pins .................................. ±2 mA
- Current at Output and Supply Pins ............... ±50 mA
- Storage temperature .............................. -65°C to +150°C
- Ambient temperature with power applied..... -40°C to +125°C
- Junction temperature ................................ +150°C
- ESD protection on all pins (HBM/MM)......... ≥ 4 kV/200V
- ESD protection on MCP65R46 OUT pin (HBM/MM)........ ≥ 4 kV/175V

†Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### DC CHARACTERISTICS

*Unless otherwise indicated, all limits are specified for: \( V_{DD} = +1.8V \) to +5.5V, \( V_{SS} = GND \), \( T_A = +25°C \), \( V_{IN+} = V_{DD}/2 \), \( V_{IN-} = V_{SS} \), \( R_L = 100 \, k\Omega \) to \( V_{DD}/2 \) (MCP65R41 only), and \( R_{Pull-Up} = 2.74 \, k\Omega \) to \( V_{DD} \) (MCP65R46 only).*

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>( V_{DD} )</td>
<td>1.8</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>I_{OUT} = 0</td>
</tr>
<tr>
<td>Quiescent Current per Comparator</td>
<td>( I_Q )</td>
<td>—</td>
<td>2.5</td>
<td>4</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio</td>
<td>( V_{DD} = 5V )</td>
<td>CMRR</td>
<td>55</td>
<td>70</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>PSRR</td>
<td>63</td>
<td>80</td>
<td>—</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>( V_{OS} )</td>
<td>-10</td>
<td>±3</td>
<td>+10</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Drift with Temperature</td>
<td>( \Delta V_{OS}/\Delta T )</td>
<td>—</td>
<td>±10</td>
<td>—</td>
<td>µV/°C</td>
<td></td>
</tr>
<tr>
<td>Input Hysteresis Voltage</td>
<td>( V_{HYST} )</td>
<td>1</td>
<td>3.3</td>
<td>5</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Drift with Temperature</td>
<td>( \Delta V_{HYST}/\Delta T )</td>
<td>—</td>
<td>6</td>
<td>—</td>
<td>µV/°C</td>
<td></td>
</tr>
<tr>
<td>Drift with Temperature</td>
<td>( \Delta V_{HYST}/\Delta T^2 )</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>µV/°C²</td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>( I_B )</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>Drift with Temperature</td>
<td>( T_A = +85°C )</td>
<td>( I_B )</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td>pA</td>
</tr>
<tr>
<td>Drift with Temperature</td>
<td>( T_A = +125°C )</td>
<td>( I_B )</td>
<td>—</td>
<td>5000</td>
<td>—</td>
<td>pA</td>
</tr>
<tr>
<td>Common Mode/ Differential Input Impedance</td>
<td>( Z_{CM/Z_{DIFF}} )</td>
<td>—</td>
<td>( 10^{15} )</td>
<td>—</td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** The input offset voltage is the center (average) of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

2: Limit the output current to Absolute Maximum Rating of 30 mA.

3: Do not short the output of the MCP65R46 comparators above \( V_{SS} + 10V \).

4: The low-power reference voltage pin is designed to drive small capacitive loads. See Section 4.5.2.
# MCP65R41/6

## DC CHARACTERISTICS (CONTINUED)

Unless otherwise indicated, all limits are specified for: \( V_{DD} = +1.8\text{V} \) to \(+5.5\text{V}\), \( V_{SS} = \text{GND} \), \( T_A = +25^\circ\text{C} \), \( V_{IN+} = V_{DD}/2 \), \( V_{IN-} = V_{SS} \), \( R_L = 100\text{k}\Omega \) to \( V_{DD}/2 \) (**MCP65R41** only), and \( R_{Pull-Up} = 2.74\text{k}\Omega \) to \( V_{DD} \) (**MCP65R46** only).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Push Pull Output</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High Level Output Voltage</td>
<td>( V_{OH} )</td>
<td>( V_{DD}-0.2 )</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>( I_{OUT} = -2\text{mA} ), ( V_{DD} = 5\text{V} )</td>
</tr>
<tr>
<td>Low Level Output Voltage</td>
<td>( V_{OL} )</td>
<td>—</td>
<td>—</td>
<td>( V_{SS}+0.2 )</td>
<td>V</td>
<td>( I_{OUT} = 2\text{mA} ), ( V_{DD} = 5\text{V} )</td>
</tr>
<tr>
<td>Short Circuit Current</td>
<td>( I_{SC} )</td>
<td>—</td>
<td>±50</td>
<td>—</td>
<td>mA</td>
<td>(Note 2) <strong>MCP65R41</strong></td>
</tr>
<tr>
<td></td>
<td>( I_{SC} )</td>
<td>—</td>
<td>±1.5</td>
<td>—</td>
<td>mA</td>
<td>(Note 2) <strong>MCP65R46</strong></td>
</tr>
</tbody>
</table>

| **Open Drain Output (MCP65R46)** | | | | | | |
| Low Level Output Voltage | \( V_{OL} \) | — | — | \( V_{SS}+0.2 \) | V | \( I_{OUT} = 2\text{mA} \) |
| Short Circuit Current | \( I_{SC} \) | — | ±50 | — | mA | |
| High-Level Output Current | \( I_{OH} \) | -100 | — | — | nA | \( V_{PU}= 10\text{V} \) |
| Pull-up Voltage | \( V_{PU} \) | 1.6 | — | 10 | V | Note 3 |
| Output Pin Capacitance | \( C_{OUT} \) | — | 8 | — | pF | |

| **Reference Voltage Output** | | | | | | |
| Initial Reference Tolerance | \( V_{TOL} \) | -2 | ±1 | +2 | % | \( I_{REF} = 0\text{A} \), \( V_{REF} = 1.21\text{V and 2.4V} \) |
| | \( V_{REF} \) | 1.185 | 1.21 | 1.234 | V | \( I_{REF} = 0\text{A} \) |
| | | 2.352 | 2.4 | 2.448 | V | |
| Reference Output Current | \( I_{REF} \) | — | ±500 | — | µA | \( V_{TOL} = \pm2\% \) (maximum) |
| Drift with Temperature (characterized but not production tested) | \( \Delta V_{REF}/\Delta T \) | — | 27 | 100 | ppm | \( V_{REF} = 1.21\text{V, } V_{DD} = 1.8\text{V} \) |
| | — | 22 | 100 | ppm | \( V_{REF} = 1.21\text{V, } V_{DD} = 5.5\text{V} \) |
| | — | 23 | 100 | ppm | \( V_{REF} = 2.4\text{V, } V_{DD} = 5.5\text{V} \) |
| Capacitive Load | \( C_{L} \) | — | 200 | — | pF | Note 4 |

**Note 1:** The input offset voltage is the center (average) of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

**Note 2:** Limit the output current to Absolute Maximum Rating of 30 mA.

**Note 3:** Do not short the output of the **MCP65R46** comparators above \( V_{SS} + 10\text{V} \).

**Note 4:** The low-power reference voltage pin is designed to drive small capacitive loads. See Section 4.5.2.
AC CHARACTERISTICS

Unless otherwise indicated, all limits are specified for: \( V_{DD} = +1.8V \) to +5.5V, \( V_{SS} = \) GND, \( T_A = +25^\circ C \), \( V_{IN+} = V_{DD}/2 \), \( \text{Step} = 200 \text{ mV}, \text{Overdrive} = 100 \text{ mV}, R_L = 100 \text{ k}\Omega \) to \( V_{DD}/2 \) (MCP65R41 only), \( R_{\text{Pull-Up}} = 2.74 \text{ k}\Omega \) to \( V_{DD} \) (MCP65R46 only), and \( C_L = 50 \text{ pF} \).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rise Time</td>
<td>( t_R )</td>
<td>—</td>
<td>0.85</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>Fall Time</td>
<td>( t_F )</td>
<td>—</td>
<td>0.85</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>Propagation Delay (High-to-Low)</td>
<td>( t_{PHL} )</td>
<td>—</td>
<td>4</td>
<td>8.0</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>Propagation Delay (Low-to-High)</td>
<td>( t_{PLH} )</td>
<td>—</td>
<td>4</td>
<td>8.0</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>Propagation Delay Skew</td>
<td>( t_{PDS} )</td>
<td>—</td>
<td>±0.2</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>Maximum Toggle Frequency</td>
<td>( f_{MAX} )</td>
<td>—</td>
<td>160</td>
<td>—</td>
<td>kHz</td>
<td>( V_{DD} = 1.8V )</td>
</tr>
<tr>
<td></td>
<td>( f_{MAX} )</td>
<td>—</td>
<td>120</td>
<td>—</td>
<td>kHz</td>
<td>( V_{DD} = 5.5V )</td>
</tr>
</tbody>
</table>

**Note 1:** Propagation Delay Skew is defined as: \( t_{PDS} = t_{PLH} - t_{PHL} \).

TEMPERATURE SPECIFICATIONS

Unless otherwise indicated, all limits are specified for: \( V_{DD} = +1.8V \) to +5.5V and \( V_{SS} = \) GND.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Ranges</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Specified Temperature Range</td>
<td>( T_A )</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>( T_A )</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>( T_A )</td>
<td>-65</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Thermal Package Resistances</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, SOT23-6</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>190.5</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

**1.2 Test Circuit Configuration**

**FIGURE 1-1:** Test Circuit for the Push-Pull Output Comparators.

**FIGURE 1-2:** Test Circuit for the Open-Drain Comparators.
2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 100 \, \Omega$ to $V_{DD}/2$ (MCP65R41 only), $R_{Pull-Up} = 2.74 \, \Omega$ to $V_{DD}/2$ (MCP65R46 only) and $C_L = 50 \, pF$.

![Figure 2-1: Input Offset Voltage.](image1)

![Figure 2-2: Input Offset Voltage vs. Temperature.](image2)

![Figure 2-3: Input Offset Voltage vs. Common-Mode Input Voltage.](image3)

![Figure 2-4: Input Offset Voltage Drift.](image4)

![Figure 2-5: Input Offset Voltage vs. Supply Voltage vs. Temperature.](image5)

![Figure 2-6: Input Offset Voltage vs. Common-Mode Input Voltage.](image6)
Note: Unless otherwise indicated, $V_{DD} = +1.8\text{V to } +5.5\text{V}$, $V_{SS} = \text{GND}$, $T_A = +25\text{°C}$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = \text{GND}$, $R_L = 100\ \text{k}\Omega$ to $V_{DD}/2$ (MCP65R41 only), $R_{Pull-Up} = 2.74\ \text{k}\Omega$ to $V_{DD}/2$ (MCP65R46 only) and $C_L = 50\ \text{pF}$.

FIGURE 2-7: Input Hysteresis Voltage at -40°C.

FIGURE 2-8: Input Hysteresis Voltage at +25°C.

FIGURE 2-9: Input Hysteresis Voltage at +125°C.

FIGURE 2-10: Input Hysteresis Voltage Drift – Linear Temperature Compensation (TC1).

FIGURE 2-11: Input Hysteresis Voltage Drift – Quadratic Temperature Compensation (TC2).

FIGURE 2-12: Input Hysteresis Voltage vs. Temperature.
Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{IN+} = V_{DD}/2, V_{IN-} = GND, R_L = 100 kΩ to V_{DD}/2 (MCP65R41 only), R_{Pull-Up} = 2.74 kΩ to V_{DD}/2 (MCP65R46 only) and C_L = 50 pF.

**FIGURE 2-13:** Input Hysteresis Voltage vs. Common-Mode Input Voltage.

**FIGURE 2-14:** Input Hysteresis Voltage vs. Common-Mode Input Voltage.

**FIGURE 2-15:** Input Hysteresis Voltage vs. Supply Voltage vs. Temperature.

**FIGURE 2-16:** Quiescent Current.

**FIGURE 2-17:** Quiescent Current vs. Common-Mode Input Voltage.

**FIGURE 2-18:** Quiescent Current vs. Common-Mode Input Voltage.
Note: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN}^+ = V_{DD}/2$, $V_{IN}^- = GND$, $R_L = 100 \, k\Omega$ to $V_{DD}/2$ (MCP65R41 only), $R_{Pull-Up} = 2.74 \, k\Omega$ to $V_{DD}/2$ (MCP65R46 only) and $C_L = 50 \, pF$.

**FIGURE 2-19:** Quiescent Current vs. Supply Voltage vs. Temperature.

**FIGURE 2-20:** Quiescent Current vs. Toggle Frequency.

**FIGURE 2-21:** Short Circuit Current vs. Supply Voltage vs. Temperature.

**FIGURE 2-22:** Quiescent Current vs. Common-Mode Input Voltage.

**FIGURE 2-23:** Quiescent Current vs. Pull-Up Voltage.

**FIGURE 2-24:** No Phase Reversal.
Note: Unless otherwise indicated, \( V_{DD} = +1.8V \) to +5.5V, \( V_{SS} = GND \), \( T_A = +25^\circ C \), \( V_{IN}^+ = V_{DD}/2 \), \( V_{IN}^- = GND \), \( R_L = 100 \, k\Omega \) to \( V_{DD}/2 \) (MCP65R41 only), \( R_{Pull-Up} = 2.74 \, k\Omega \) to \( V_{DD}/2 \) (MCP65R46 only) and \( C_L = 50 \, \mu F \).

**FIGURE 2-25:** Output Headroom vs. Output Current.

**FIGURE 2-26:** Low-to-High and High-to-Low Propagation Delays.

**FIGURE 2-27:** Low-to-High and High-to-Low Propagation Delays.

**FIGURE 2-28:** Output Headroom vs. Output Current.

**FIGURE 2-29:** Low-to-High and High-to-Low Propagation Delays.

**FIGURE 2-30:** Low-to-High and High-to-Low Propagation Delays.
**Note:** Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 100 \, \Omega$ to $V_{DD}/2$ (**MCP65R41** only), $R_{Pull-Up} = 2.74 \, k\Omega$ to $V_{DD}/2$ (**MCP65R46** only) and $C_L = 50 \, pF$.  

**FIGURE 2-31:** Propagation Delay vs. Common-Mode Input Voltage.  

**FIGURE 2-32:** Propagation Delay vs. Common-Mode Input Voltage.  

**FIGURE 2-33:** Propagation Delay vs. Supply Voltage.  

**FIGURE 2-34:** Propagation Delay vs. Common-Mode Input Voltage.  

**FIGURE 2-35:** Propagation Delay vs. Common-Mode Input Voltage.  

**FIGURE 2-36:** Propagation Delay vs. Supply Voltage.
Note: Unless otherwise indicated, \( V_{DD} = +1.8 \text{V to } +5.5 \text{V}, V_{SS} = \text{GND}, T_A = +25^\circ \text{C}, V_{IN}^+ = V_{DD}/2, V_{IN}^- = \text{GND}, R_L = 100 \, \text{k}\Omega \) to \( V_{DD}/2 \) (MCP65R41 only), \( R_{\text{Pull-Up}} = 2.74 \, \text{k}\Omega \) to \( V_{DD}/2 \) (MCP65R46 only) and \( C_L = 50 \, \text{pF} \).

FIGURE 2-37: Propagation Delay vs. Temperature.

FIGURE 2-38: Propagation Delay vs. Capacitive Load.

FIGURE 2-39: Propagation Delay vs. Input Over-Drive.

FIGURE 2-40: Propagation Delay vs. Temperature.

FIGURE 2-41: Propagation Delay vs. Capacitive Load.

FIGURE 2-42: Propagation Delay vs. Input Over-Drive.
Note: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN^+} = V_{DD}/2$, $V_{IN^-} = GND$, $R_L = 100 \, k\Omega$ to $V_{DD}/2$ (MCP65R41 only), $R_{Pull-Up} = 2.74 \, k\Omega$ to $V_{DD}/2$ (MCP65R46 only) and $C_L = 50 \, pF$.

**FIGURE 2-43:** Propagation Delay Skew.

**FIGURE 2-44:** Common-Mode Rejection Ratio and Power Supply Rejection Ratio vs. Temperature.

**FIGURE 2-45:** Common-Mode Rejection Ratio.

**FIGURE 2-46:** Propagation Delay Skew.

**FIGURE 2-47:** Common-Mode Rejection Ratio and Power Supply Rejection Ratio vs. Temperature.

**FIGURE 2-48:** Common-Mode Rejection Ratio.
Note: Unless otherwise indicated, $V_{DD} = +1.8\text{V to } +5.5\text{V}$, $V_{SS} = \text{GND}$, $T_A = +25\text{°C}$, $V_{IN^+} = V_{DD}/2$, $V_{IN^-} = \text{GND}$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ (MCP65R41 only), $R_{\text{Pull-Up}} = 2.74$ $\text{k}\Omega$ to $V_{DD}/2$ (MCP65R46 only) and $C_L = 50\text{ pF}$.

**FIGURE 2-49:** Input Offset Current and Input Bias Current vs. Temperature.

**FIGURE 2-50:** Input Offset Current and Input Bias Current vs. Common-Mode Input Voltage vs. Temperature.

**FIGURE 2-51:** Input Bias Current vs. Input Voltage vs. Temperature.

**FIGURE 2-52:** Power Supply Rejection Ratio.

**FIGURE 2-53:** $V_{REF}$ vs. $V_{DD}$.

**FIGURE 2-54:** $V_{REF}$ vs. $V_{DD}$. 
Note: Unless otherwise indicated, V\textsubscript{DD} = +1.8V to +5.5V, V\textsubscript{SS} = GND, T\textsubscript{A} = +25°C, V\textsubscript{IN+} = V\textsubscript{DD}/2, V\textsubscript{IN–} = GND, R\textsubscript{L} = 100 k\textOmega to V\textsubscript{DD}/2 (MCP65R41 only), R\textsubscript{Pull-Up} = 2.74 k\textOmega to V\textsubscript{DD}/2 (MCP65R46 only) and C\textsubscript{L} = 50 pF.

FIGURE 2-55: $V_{\text{REF}}$ vs. $I_{\text{REF}}$ over Temperature.

FIGURE 2-56: $V_{\text{REF}}$ vs. $I_{\text{REF}}$ over Temperature.

FIGURE 2-57: $V_{\text{REF}}$ vs. $I_{\text{REF}}$ over Temperature.

FIGURE 2-58: $V_{\text{REF}}$ vs. Temperature.

FIGURE 2-59: $V_{\text{REF}}$ vs. Temperature.

FIGURE 2-60: Short Circuit Current vs. $V_{\text{DD}}$. 

V\textsubscript{REF} = 1.21V
Note: Unless otherwise indicated, $V_{DD} = +1.8\, \text{V}$ to $+5.5\, \text{V}$, $V_{SS} = \text{GND}$, $T_A = +25^\circ\text{C}$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = \text{GND}$,
$R_L = 100 \, \text{k}\Omega$ to $V_{DD}/2$ (MCP65R41 only), $R_{\text{Pull-Up}} = 2.74 \, \text{k}\Omega$ to $V_{DD}/2$ (MCP65R46 only) and $C_L = 50 \, \text{pF}$.

**FIGURE 2-61:** Reference Voltage Tolerance.

**FIGURE 2-62:** Reference Voltage Tolerance.
3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

### TABLE 3-1: PIN FUNCTION TABLE

<table>
<thead>
<tr>
<th>MCP65R41/6 Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OUT</td>
</tr>
<tr>
<td>2</td>
<td>$V_{SS}$ Ground</td>
</tr>
<tr>
<td>3</td>
<td>$V_{IN^+}$ Non-inverting Input</td>
</tr>
<tr>
<td>4</td>
<td>$V_{IN^-}$ Inverting Input</td>
</tr>
<tr>
<td>5</td>
<td>$V_{REF}$ Reference Voltage Output</td>
</tr>
<tr>
<td>6</td>
<td>$V_{DD}$ Positive Power Supply</td>
</tr>
</tbody>
</table>

3.1 Analog Inputs

The comparator non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.2 Digital Outputs

The comparator outputs are CMOS/TTL compatible push-pull and open-drain digital outputs. The push-pull is designed to directly interface to a CMOS/TTL compatible pin while the open-drain output is designed for level shifting and wired-OR interfaces.

3.3 Analog Outputs

The $V_{REF}$ Output pin outputs a reference voltage of 1.21V or 2.4V.

3.4 Power Supply ($V_{SS}$ and $V_{DD}$)

The positive power supply pin ($V_{DD}$) is 1.8V to 5.5V higher than the negative power supply pin ($V_{SS}$). For normal operation, the other pins are at voltages between $V_{SS}$ and $V_{DD}$.

Typically, these parts are used in a single (positive) supply configuration. In this case, $V_{SS}$ is connected to ground and $V_{DD}$ is connected to the supply. $V_{DD}$ will need a local bypass capacitor (typically 0.01 μF to 0.1 μF) within 2 mm of the $V_{DD}$ pin. These can share a bulk capacitor with the nearby analog parts (within 100 mm), but it is not required.
4.0 APPLICATIONS INFORMATION

The MCP65R41/6 family of push-pull and open-drain output comparators are fabricated on Microchip’s state-of-the-art CMOS process. They are suitable for a wide range of high-speed applications requiring low power consumption.

4.1 Comparator Inputs

4.1.1 NORMAL OPERATION

The input stage of this family of devices uses three differential input stages in parallel: one operates at low input voltages, one at high input voltages, and one at mid input voltages. With this topology, the input voltage range is 0.3V above VDD and 0.3V below VSS, while providing low offset voltage throughout the Common mode range. The input offset voltage is measured at both VSS - 0.3V and VDD + 0.3V to ensure proper operation.

The MCP65R41/6 family has internally-set hysteresis VHYST that is small enough to maintain input offset accuracy, and large enough to eliminate the output chattering caused by the comparator’s own input noise voltage ENI. Figure 4-1 depicts this behavior. Input offset voltage (VOS) is the center (average) of the (input-referred) low-high and high-low trip points. Input hysteresis voltage (VHYST) is the difference between the same trip points.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-2. This structure was chosen to protect the input transistors, and to minimize the input bias current (Ib). The input ESD diodes clamp the inputs when trying to go more than one diode drop below VSS. They also clamp any voltages that go too far above VDD; their breakdown voltage is high enough to allow a normal operation, and low enough to bypass the ESD events within the specified limits.

In order to prevent damage and/or improper operation of these comparators, the circuit they are connected to limit the currents (and voltages) at the VIN+ and VIN- pins (see Absolute Maximum Ratings†). Figure 4-3 shows the recommended approach to protect these inputs. The internal ESD diodes prevent the input pins (VIN+ and VIN- ) from going too far below ground, and the resistors R1 and R2 limit the possible current drawn out of the input pin. Diodes D1 and D2 prevent the input pin (VIN+ and VIN- ) from going too far above VDD. When implemented as shown, resistors R1 and R2 also limit the current through D1 and D2.
It is also possible to connect the diodes to the left of the resistors $R_1$ and $R_2$. In this case, the currents through the diodes $D_1$ and $D_2$ need to be limited by some other mechanism. The resistor then serves as an in-rush current limiter; the DC current into the input pins ($V_{IN+}$ and $V_{IN-}$) should be very small.

A significant amount of current can flow out of the inputs when the Common mode voltage ($V_{CM}$) is below ground ($V_{SS}$); see Figure 4-3. The applications that are high impedance may need to limit the usable voltage range.

4.1.3 PHASE REVERSAL

The MCP65R41/6 comparator family uses CMOS transistors at the input. They are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-3 shows an input voltage exceeding both supplies with no resulting phase inversion.

4.2 Push-Pull Output

The push-pull output is designed to be compatible with CMOS and TTL logic, while the output transistors are configured to give a rail-to-rail output performance. They are driven with circuitry that minimizes any switching current (shoot-through current from supply to supply) when the output is transitioned from high-to-low, or from low-to-high (see Figures 2-18 and 2-19 for more information).

4.3 Externally Set Hysteresis

A greater flexibility in selecting the hysteresis (or the input trip points) is achieved by using external resistors. Hysteresis reduces output chattering when one input is slowly moving past the other. It also helps in systems where it is preferable not to cycle between high and low states too frequently (e.g., air conditioner thermostatic controls). Output chatter also increases the dynamic supply current.
4.3.1 NON-INVERTING CIRCUIT

Figure 4-4 shows a non-inverting circuit for single-supply applications using just two resistors. The resulting hysteresis diagram is shown in Figure 4-5.

* Pull-up resistor required for the MCP65R46 only.

**FIGURE 4-4:** Non-Inverting Circuit with Hysteresis for Single-Supply.

The trip points for Figures 4-4 and 4-5 are:

EXAMPLE 4-1:

\[
V_{THL} = V_{REF} \left( l + \frac{R_I}{R_F} \right) - V_{OL} \left( \frac{R_I}{R_F} \right)
\]

\[
V_{TLH} = V_{REF} \left( l + \frac{R_I}{R_F} \right) - V_{OH} \left( \frac{R_I}{R_F} \right)
\]

Where:

- \( V_{TLH} \) = trip voltage from low to high
- \( V_{THL} \) = trip voltage from high to low

4.3.2 INVERTING CIRCUIT

Figure 4-6 shows an inverting circuit for single-supply using three resistors. The resulting hysteresis diagram is shown in Figure 4-7.

* Pull-up resistor required for the MCP65R46 only.

**FIGURE 4-6:** Inverting Circuit with Hysteresis.
To determine the trip voltages ($V_{TLH}$ and $V_{THL}$) for the circuit shown in Figure 4-6, $R_2$ and $R_3$ can be simplified to the Thevenin equivalent circuit with respect to $V_{REF}$, as shown in Figure 4-8:

![Thevenin Equivalent Circuit](image)

Where:

$$R_{23} = \frac{R_2 R_3}{R_2 + R_3}$$

$$V_{23} = \frac{R_3}{R_2 + R_3} V_{REF}$$

* Pull-up resistor required for the MCP65R46 only.

**FIGURE 4-8:** Thevenin Equivalent Circuit.

By using this simplified circuit, the trip voltage can be calculated using the following equation:

**EQUATION 4-1:**

$$V_{THL} = V_{OH} \left( \frac{R_{23}}{R_{23} + R_F} \right) + V_{23} \left( \frac{R_F}{R_{23} + R_F} \right)$$

$$V_{THL} = V_{OL} \left( \frac{R_{23}}{R_{23} + R_F} \right) + V_{23} \left( \frac{R_F}{R_{23} + R_F} \right)$$

Where:

- $V_{TLH} =$ trip voltage from low to high
- $V_{THL} =$ trip voltage from high to low

Figures 2-25 and 2-28 can be used to determine the typical values for $V_{OH}$ and $V_{OL}$.

### 4.4 Bypass Capacitors

With this family of comparators, the power supply pin ($V_{DD}$ for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good edge rate performance.

### 4.5 Capacitive Loads

#### 4.5.1 OUT PIN

Reasonable capacitive loads (i.e., logic gates) have little impact on the propagation delay (see Figure 2-34). The supply current increases with the increasing toggle frequency (Figure 2-22), especially with higher capacitive loads. The output slew rate and propagation delay performance will be reduced with higher capacitive loads.

#### 4.5.2 $V_{REF}$ PIN

The reference output is designed to interface to the comparator input pins, either directly or with some resistive network (e.g., a voltage divider network) with minimal capacitive load. The recommended capacitive load is 200 pF (typical). Capacitive loads greater than 2000 pF may cause the $V_{REF}$ output to oscillate at power up.
4.6 PCB Surface Leakage

In applications where the low input bias current is critical, the Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other type of contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow. This is greater than the MCP65R41/6 family's bias current at +25°C (1 pA, typical).

The easiest way to reduce the surface leakage is to use a guard ring around the sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-9.

![Guard Ring](GuardRing.png)

**FIGURE 4-9:** Example of a Guard Ring Layout for Inverting Circuit.

Use the following steps for an inverting configuration (Figures 4-6):

1. Connect the guard ring to the non-inverting input pin ($V_{IN^+}$). This biases the guard ring to the same reference voltage as the comparator (e.g., $V_{DD}/2$ or ground).
2. Connect the inverting pin ($V_{IN^-}$) to the input pad without touching the guard ring.

Use the following steps for a non-inverting configuration (Figure 4-4):

1. Connect the non-inverting pin ($V_{IN^+}$) to the input pad without touching the guard ring.
2. Connect the guard ring to the inverting input pin ($V_{IN^-}$).

4.7 Typical Applications

4.7.1 PRECISE COMPARATOR

Some applications require a higher DC precision. A simple way to address this need is using an amplifier (such as the MCP6041 – a 600 nA low power and 14 kHz bandwidth op amp) to gain-up the input signal before it reaches the comparator. Figure 4-10 shows an example of this approach, which also level shifts to $V_{PU}$ using the Open-Drain option, the MCP65R46.

![Precise Inverting Comparator](PreciseComparator.png)

**FIGURE 4-10:** Precise Inverting Comparator.

4.7.2 BISTABLE MULTI-VIBRATOR

A simple bistable multi-vibrator design is shown in Figure 4-11. $V_{REF}$ needs to be between ground and the maximum comparator internal $V_{REF}$ of 2.4V to achieve oscillation. The output duty cycle changes with $V_{REF}$.

![Bistable Multi-Vibrator](BistableMultiVibrator.png)

**FIGURE 4-11:** Bistable Multi-Vibrator.
4.7.3 OVER-TEMPERATURE PROTECTION CIRCUIT

The MCP65R41 device can be used as an over-temperature protection circuit using a thermistor. The 2.4V $V_{REF}$ can be used as stable reference to the thermistor, the alert threshold and hysteresis threshold. This is ideal for battery powered applications, where the change in temperature and output toggle thresholds would remain fixed as battery voltage decays over time.

* Pull-up resistor required for the MCP65R46 only.

FIGURE 4-12: Over-Temperature Alert Circuit.
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

Legend:
- XX...X Customer-specific information
- Y Year code (last digit of calendar year)
- YY Year code (last 2 digits of calendar year)
- WW Week code (week of January 1 is week ‘01’)
- NNN Alphanumeric traceability code
- e3 Pb-free JEDEC designator for Matte Tin (Sn)
- * This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Example:

<table>
<thead>
<tr>
<th>Part Number Code</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP65R41T-1202E/CHY</td>
<td>HVNN</td>
</tr>
<tr>
<td>MCP65R41T-2402E/CHY</td>
<td>HWNN</td>
</tr>
<tr>
<td>MCP65R46T-1202E/CHY</td>
<td>HXNN</td>
</tr>
<tr>
<td>MCP65R46T-2402E/CHY</td>
<td>HYNN</td>
</tr>
</tbody>
</table>

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
6-Lead Plastic Small Outline Transistor (CHY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Outside Lead Pitch</td>
<td>e1</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
6-Lead Plastic Small Outline Transistor (CHY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>Dimension Limits</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contact Pitch</td>
<td>E</td>
<td></td>
<td>0.95 BSC</td>
<td></td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
<td></td>
<td>2.80</td>
<td></td>
</tr>
<tr>
<td>Contact Pad Width (X6)</td>
<td>X</td>
<td></td>
<td>0.60</td>
<td></td>
</tr>
<tr>
<td>Contact Pad Length (X6)</td>
<td>Y</td>
<td></td>
<td>1.10</td>
<td></td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
<td></td>
<td>1.70</td>
<td></td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>GX</td>
<td></td>
<td>0.35</td>
<td></td>
</tr>
<tr>
<td>Overall Width</td>
<td>Z</td>
<td></td>
<td>3.90</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A
APPENDIX A: REVISION HISTORY

Revision B (September 2011)
The following modification was made to this document:
   Updated the DC Characteristics table.

Revision A (December 2010)
   Original Release of this Document.
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>Device</th>
<th>Tape and</th>
<th>Reference Voltage</th>
<th>Reference Tolerance</th>
<th>Temperature Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>MCP65R41T: Push-pull Output Comparator</td>
<td>CHY= Plastic Small Outline Transistor, 6-Lead</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-XX</td>
<td>MCP65R46T: Open-drain Output Comparator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Examples:**

a) MCP65R41T-1202E/CHY: Push-Pull Output, 1.2VREF, Tape and Reel, 6LD SOT-23 Pkg.
b) MCP65R41T-2402E/CHY: Push-Pull Output, 2.4VREF, Tape and Reel, 6LD SOT-23 Pkg.
c) MCP65R46T-1202E/CHY: Open-Drain Output, 1.2VREF, Tape and Reel, 6LD SOT-23 Pkg.
d) MCP65R46T-2402E/CHY: Open-Drain Output, 2.4VREF, Tape and Reel, 6LD SOT-23 Pkg.
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