MCP1703

250 mA, 16V, Low Quiescent Current LDO Regulator

Features:

• 2.0 µA Typical Quiescent Current
• Input Operating Voltage Range: 2.7V to 16.0V
• 250 mA Output Current for Output Voltages ≥ 2.5V
• 200 mA Output Current for Output Voltages < 2.5V
• Low Dropout Voltage, 625 mV typical @ 250 mA for \( V_R = 2.8V \)
• 0.4% Typical Output Voltage Tolerance
• Standard Output Voltage Options:
  - 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 3.0V, 3.3V, 4.0V, 5.0V
• Output Voltage Range: 1.2V to 5.5V in 0.1V Increments (50 mV increments available upon request)
• Stable with 1.0 µF to 22 µF Ceramic Output Capacitance
• Short-Circuit Protection
• Overtemperature Protection

Applications:

• Battery-Powered Devices
• Battery-Powered Alarm Circuits
• Smoke Detectors
• CO² Detectors
• Pagers and Cellular Phones
• Smart Battery Packs
• Low Quiescent Current Voltage Reference
• PDAs
• Digital Cameras
• Microcontroller Power
• Solar-Powered Instruments
• Consumer Products
• Battery-Powered Data Loggers

Related Literature:

• AN765, “Using Microchip’s Micropower LDOs”, DS00765, Microchip Technology Inc., 2002
• AN766, “Pin-Compatible CMOS Upgrades to Bipolar LDOs”, DS00766, Microchip Technology Inc., 2002

Description:

The MCP1703 is a family of CMOS low dropout (LDO) voltage regulators that can deliver up to 250 mA of current while consuming only 2.0 µA of quiescent current (typical). The input operating range is specified from 2.7V to 16.0V, making it an ideal choice for two to six primary cell battery-powered applications, 9V alkaline and one or two cell Li-Ion-powered applications.

The MCP1703 is capable of delivering 250 mA with only 625 mV (typical) of input to output voltage differential (\( V_{OUT} = 2.8V \)). The output voltage tolerance of the MCP1703 is typically ±0.4% at +25°C and ±3% maximum over the operating junction temperature range of -40°C to +125°C. Line regulation is ±0.1% typical at +25°C.

Output voltages available for the MCP1703 range from 1.2V to 5.5V. The LDO output is stable when using only 1 µF of output capacitance. Ceramic, tantalum, or aluminum electrolytic capacitors can all be used for input and output. Overcurrent limit and overtemperature shutdown provide a robust solution for any application.

Package options include the SOT-223-3, SOT-23A, 2x3 DFN-8, and SOT-89-3.

Package Types

* Includes Exposed Thermal Pad (EP); see Table 3-1.
1.0  ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

VDD..................................................................................+18V
All inputs and outputs w.r.t. ..............(VSS-0.3V) to (VIN+0.3V)
Peak Output Current ...................................................500 mA
Storage temperature .....................................-65°C to +150°C
Maximum Junction Temperature.................................+150°C
ESD protection on all pins (HBM,MM).............. ≥ 4 kV; ≥ 400V

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input / Output Characteristics</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Operating Voltage</td>
<td>VIN</td>
<td>2.7</td>
<td>—</td>
<td>16.0</td>
<td>V</td>
<td>Note 1</td>
</tr>
<tr>
<td>Input Quiescent Current</td>
<td>IQ</td>
<td>—</td>
<td>2.0</td>
<td>5</td>
<td>µA</td>
<td>IV = 0 mA</td>
</tr>
<tr>
<td>Maximum Output Current</td>
<td>IOUT</td>
<td>250</td>
<td>—</td>
<td>—</td>
<td>mA</td>
<td>For VR ≥ 2.5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>50</td>
<td>100</td>
<td>—</td>
<td>mA</td>
<td>For VR &lt; 2.5V, VIN ≥ 2.7V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>mA</td>
<td>For VR &lt; 2.5V, VIN ≥ 2.95V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>150</td>
<td>200</td>
<td>—</td>
<td>mA</td>
<td>For VR &lt; 2.5V, VIN ≥ 3.2V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>200</td>
<td>250</td>
<td>—</td>
<td>mA</td>
<td>For VR &lt; 2.5V, VIN ≥ 3.45V</td>
</tr>
<tr>
<td>Output Short Circuit Current</td>
<td>IOUT_S</td>
<td>—</td>
<td>400</td>
<td>—</td>
<td>mA</td>
<td>VIN = VIN(MIN) (Note 2), VOUT = GND, Current (average current) measured 10 ms after short is applied.</td>
</tr>
<tr>
<td>Output Voltage Regulation</td>
<td>VOUT</td>
<td>VR-3.0%</td>
<td>VR±0.4%</td>
<td>VR+3.0%</td>
<td>V</td>
<td>Note 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VR-2.0%</td>
<td>VR±0.4%</td>
<td>VR+2.0%</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>VR-1.0%</td>
<td>VR±0.4%</td>
<td>VR+1.0%</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1% Custom</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOUT Temperature Coefficient</td>
<td>TCVOUT</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td>ppm/°C</td>
<td>Note 3</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>ΔVOUT/VVIN</td>
<td>-0.3</td>
<td>±0.1</td>
<td>+0.3</td>
<td>%/V</td>
<td>(VOUT(MAX) + VDROP(MAX)) ≤ VIN ≤ 16V, Note 1</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>ΔVOUT/VOUT</td>
<td>-2.5</td>
<td>±1.0</td>
<td>+2.5</td>
<td>%</td>
<td>IL = 1.0 mA to 250 mA for VR ≥ 2.5V IL = 1.0 mA to 200 mA for VR &lt; 2.5V VOUT = 3.65V, Note 4</td>
</tr>
</tbody>
</table>

Note 1: The minimum VIn must meet two conditions: VIn ≥ 2.7V and VIn ≥ (VOUT(MAX) + VDROP(MAX)).

Note 2: VR is the nominal regulator output voltage. For example: VR = 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 3.0V, 3.3V, 4.0V, or 5.0V. The input voltage VVin = VOUT(MAX) + VDROP(MAX) or VIN = 2.7V (whichever is greater); IOUT = 100 µA.

Note 3: TCVOUT = (VOUT(HIGH) - VOUT(LOW)) *106 / (VR * ΔTemperature), VOUT(HIGH) = highest voltage measured over the temperature range. VOUT(LOW) = lowest voltage measured over the temperature range.

Note 4: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification TCVOUT.

Note 5: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its measured value with an applied input voltage of VOUT(MAX) + VDROP(MAX) or 2.7V, whichever is greater.

Note 6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., Tj, θJA). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

Note 7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.
DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits are established for \( V_{IN} = V_{OUT\,MAX} + V_{DROP\,OUT\,MAX}, \) \textbf{Note 1.}
\[ I_{LOAD} = 100 \mu A, \ C_{OUT} = 1 \mu F \ (X7R), \ C_{IN} = 1 \mu F \ (X7R), \ T_A = +25^\circ C. \]

\textbf{Boldface} type applies for junction temperatures, \( T_J \) (\textbf{Note 7}) of -40°C to +125°C.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dropout Voltage</td>
<td>( V_{DROP,OUT} ) \textbf{Note 1, Note 5}</td>
<td>—</td>
<td>330</td>
<td>650</td>
<td>mV</td>
<td>( I_L = 250 , mA, , V_R = 5.0V )</td>
</tr>
<tr>
<td>Output Delay Time</td>
<td>( T_{DELAY} )</td>
<td>—</td>
<td>1000</td>
<td>—</td>
<td>( \mu s )</td>
<td>( V_{IN} = 0V ) to 6V, ( V_{OUT} = 90% , V_R, , R_L = 50, \Omega )</td>
</tr>
<tr>
<td>Output Noise</td>
<td>( e_N )</td>
<td>—</td>
<td>8</td>
<td>—</td>
<td>( \mu V/(Hz)^{1/2} )</td>
<td>( I_L = 50 , mA, , f = 1 , kHz, , C_{OUT} = 1 , \mu F )</td>
</tr>
<tr>
<td>Power Supply Ripple Rejection Ratio</td>
<td>PSRR</td>
<td>—</td>
<td>44</td>
<td>—</td>
<td>dB</td>
<td>( f = 100 , Hz, , C_{OUT} = 1 , \mu F, , I_L = 100 , \mu A, , V_{IN,AC} = 100 , mV , pk-pk, , C_{IN} = 0 , \mu F, , V_R = 1.2V )</td>
</tr>
</tbody>
</table>
| Thermal Shutdown Protection | \( T_{SD} \) | — | 150 | — | °C | \textbf{Note 1:} The minimum \( V_{IN} \) must meet two conditions: \( V_{IN} \geq 2.7V \) and \( V_{IN} \geq \max(V_{OUT\,MAX} + V_{DROP\,OUT\,MAX}) \).
|  |  |  |  |  |  |  |

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
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<td>Temperature Ranges</td>
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<td>—</td>
<td>+125</td>
<td>°C</td>
<td>Steady State</td>
<td></td>
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<tr>
<td>Maximum Junction Temperature</td>
<td>( T_{J} )</td>
<td>—</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td>Transient</td>
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<tr>
<td>Storage Temperature Range</td>
<td>( T_A )</td>
<td>—</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
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</table>

<table>
<thead>
<tr>
<th>Thermal Package Resistance (\textbf{Note 2})</th>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, 3LD SOT-223</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>62</td>
<td>—</td>
<td>°C/W</td>
<td>EIA/JEDEC JESD51-7</td>
</tr>
<tr>
<td></td>
<td>( \theta_{JC} )</td>
<td>—</td>
<td>15</td>
<td>—</td>
<td>°C/W</td>
<td>FR-4 0.063 4-Layer Board</td>
</tr>
<tr>
<td>Thermal Resistance, 3LD SOT-23A</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>336</td>
<td>—</td>
<td>°C/W</td>
<td>EIA/JEDEC JESD51-7</td>
</tr>
<tr>
<td></td>
<td>( \theta_{JC} )</td>
<td>—</td>
<td>110</td>
<td>—</td>
<td>°C/W</td>
<td>FR-4 0.063 4-Layer Board</td>
</tr>
<tr>
<td>Thermal Resistance, 3LD SOT-89</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>153.3</td>
<td>—</td>
<td>°C/W</td>
<td>EIA/JEDEC JESD51-7</td>
</tr>
<tr>
<td></td>
<td>( \theta_{JC} )</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>°C/W</td>
<td>FR-4 0.063 4-Layer Board</td>
</tr>
<tr>
<td>Thermal Resistance, 8LD 2x3 DFN</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>93</td>
<td>—</td>
<td>°C/W</td>
<td>EIA/JEDEC JESD51-7</td>
</tr>
<tr>
<td></td>
<td>( \theta_{JC} )</td>
<td>—</td>
<td>26</td>
<td>—</td>
<td>°C/W</td>
<td>FR-4 0.063 4-Layer Board</td>
</tr>
</tbody>
</table>

\textbf{Note 1:} The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., \( T_A, T_J, \theta_{JA} \)). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

\textbf{Note 2:} Thermal Resistance values are subject to change. Please visit the Microchip web site for the latest packaging information.
2.0  TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated: \( V_R = 1.8 \text{V}, C_{OUT} = 1 \text{µF Ceramic (X7R)}, C_{IN} = 1 \text{µF Ceramic (X7R)}, I_L = 100 \text{µA}, T_A = +25^\circ \text{C}, V_{IN} = V_{OUT(\text{MAX})} + V_{\text{DROPOUT(\text{MAX})}} \) or 2.7V, whichever is greater.

Note: Junction Temperature \((T_J)\) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

![Figure 2-1: Quiescent Current vs. Input Voltage.](image1)

![Figure 2-2: Quiescent Current vs. Input Voltage.](image2)

![Figure 2-3: Quiescent Current vs. Input Voltage.](image3)

![Figure 2-4: Ground Current vs. Load Current.](image4)

![Figure 2-5: Ground Current vs. Load Current.](image5)

![Figure 2-6: Quiescent Current vs. Junction Temperature.](image6)
Note: Unless otherwise indicated: $V_R = 1.8V$, $C_{OUT} = 1 \mu F$ Ceramic (X7R), $C_{IN} = 1 \mu F$ Ceramic (X7R), $I_L = 100 \mu A$, $T_A = +25^\circ C$, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$ or $2.7V$, whichever is greater.

**FIGURE 2-7:** Output Voltage vs. Input Voltage.

**FIGURE 2-8:** Output Voltage vs. Input Voltage.

**FIGURE 2-9:** Output Voltage vs. Input Voltage.

**FIGURE 2-10:** Output Voltage vs. Load Current.

**FIGURE 2-11:** Output Voltage vs. Load Current.

**FIGURE 2-12:** Output Voltage vs. Load Current.
Note: Unless otherwise indicated: $V_R = 1.8V$, $C_{OUT} = 1 \mu F$ Ceramic (X7R), $C_{IN} = 1 \mu F$ Ceramic (X7R), $I_L = 100 \mu A$, $T_A = +25^\circ C$, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$ or 2.7V, whichever is greater.

**FIGURE 2-13:** Dropout Voltage vs. Load Current.

**FIGURE 2-14:** Dropout Voltage vs. Load Current.

**FIGURE 2-15:** Dynamic Line Response.

**FIGURE 2-16:** Dynamic Line Response.

**FIGURE 2-17:** Short Circuit Current vs. Input Voltage.

**FIGURE 2-18:** Load Regulation vs. Temperature.
Note: Unless otherwise indicated: \( V_R = 1.8\text{V}, C_{\text{OUT}} = 1 \mu\text{F Ceramic (X7R)}, C_{\text{IN}} = 1 \mu\text{F Ceramic (X7R)}, I_L = 100 \mu\text{A}, T_A = +25^\circ\text{C}, V_{\text{IN}} = V_{\text{OUT(MAX)}} + V_{\text{DROPOUT(MAX)}} \) or 2.7\text{V}, whichever is greater.

**FIGURE 2-19:** Load Regulation vs. Temperature.

**FIGURE 2-20:** Load Regulation vs. Temperature.

**FIGURE 2-21:** Line Regulation vs. Temperature.

**FIGURE 2-22:** Line Regulation vs. Temperature.

**FIGURE 2-23:** Line Regulation vs. Temperature.

**FIGURE 2-24:** PSRR vs. Frequency.
Note: Unless otherwise indicated: \( V_R = 1.8V, \) \( C_{OUT} = 1 \mu F \) Ceramic (X7R), \( C_{IN} = 1 \mu F \) Ceramic (X7R), \( I_L = 100 \mu A, \) \( T_A = +25^\circ C, \) \( V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)} \) or 2.7V, whichever is greater.

**FIGURE 2-25:** PSRR vs. Frequency.

**FIGURE 2-26:** Output Noise vs. Frequency.

**FIGURE 2-27:** Power Up Timing.

**FIGURE 2-28:** Dynamic Load Response.

**FIGURE 2-29:** Dynamic Load Response.

**FIGURE 2-30:** Output Voltage vs. Input Voltage.
FIGURE 2-31: Output Voltage vs. Input Voltage.
3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

<table>
<thead>
<tr>
<th>Pin No. 2x3 DFN-8</th>
<th>Pin No. SOT-223-3</th>
<th>Pin No. SOT-23A</th>
<th>Pin No. SOT-89-3</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>2, Tab</td>
<td>1</td>
<td>1</td>
<td>GND</td>
<td>Ground Terminal</td>
</tr>
<tr>
<td>1</td>
<td>3</td>
<td>2</td>
<td>3</td>
<td>VOUT</td>
<td>Regulated Voltage Output</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>3</td>
<td>2, Tab</td>
<td>V_IN</td>
<td>Unregulated Supply Voltage</td>
</tr>
<tr>
<td>2, 3, 5, 6, 7</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>NC</td>
<td>No Connection</td>
</tr>
<tr>
<td>9</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>EP</td>
<td>Exposed Thermal Pad (EP); must be connected to VSS</td>
</tr>
</tbody>
</table>

3.1 Ground Terminal (GND)

Regulator ground. Tie GND to the negative side of the output and the negative side of the input capacitor. Only the LDO bias current (2.0 µA typical) flows out of this pin; there is no high current. The LDO output regulation is referenced to this pin. Minimize voltage drops between this pin and the negative side of the load.

3.2 Regulated Output Voltage (VOUT)

Connect VOUT to the positive side of the load and the positive terminal of the output capacitor. The positive side of the output capacitor should be physically located as close to the LDO VOUT pin as is practical. The current flowing out of this pin is equal to the DC load current.

3.3 Unregulated Input Voltage (VIN)

Connect VIN to the input unregulated source voltage. Like all low dropout linear regulators, low source impedance is necessary for the stable operation of the LDO. The amount of capacitance required to ensure low source impedance will depend on the proximity of the input source capacitors or battery type. For most applications, 1 µF of capacitance will ensure stable operation of the LDO circuit. For applications that have load currents below 100 mA, the input capacitance requirement can be lowered. The type of capacitor used can be ceramic, tantalum, or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high-frequency.

3.4 Exposed Thermal Pad (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the VSS pin; they must be connected to the same potential on the Printed Circuit Board (PCB).
4.0 DETAILED DESCRIPTION

4.1 Output Regulation
A portion of the LDO output voltage is fed back to the internal error amplifier and compared with the precision internal band gap reference. The error amplifier output will adjust the amount of current that flows through the P-Channel pass transistor, thus regulating the output voltage to the desired value. Any changes in input voltage or output current will cause the error amplifier to respond and adjust the output voltage to the target voltage (refer to Figure 4-1).

4.2 Overcurrent
The MCP1703 internal circuitry monitors the amount of current flowing through the P-Channel pass transistor. In the event of a short-circuit or excessive output current, the MCP1703 will turn off the P-Channel device for a short period, after which the LDO will attempt to restart. If the excessive current remains, the cycle will repeat itself.

4.3 Overtemperature
The internal power dissipation within the LDO is a function of input-to-output voltage differential and load current. If the power dissipation within the LDO is excessive, the internal junction temperature will rise above the typical shutdown threshold of 150°C. At that point, the LDO will shut down and begin to cool to the typical turn-on junction temperature of 130°C. If the power dissipation is low enough, the device will continue to cool and operate normally. If the power dissipation remains high, the thermal shutdown protection circuitry will again turn off the LDO, protecting it from catastrophic failure.

FIGURE 4-1: Block Diagram.
5.0 FUNCTIONAL DESCRIPTION

The MCP1703 CMOS low dropout linear regulator is intended for applications that need the lowest current consumption while maintaining output voltage regulation. The operating continuous load range of the MCP1703 is from 0 mA to 250 mA (VR ≥ 2.5V). The input operating voltage range is from 2.7V to 16.0V, making it capable of operating from two or more alkaline cells or single and multiple Li-Ion cell batteries.

5.1 Input

The input of the MCP1703 is connected to the source of the P-Channel PMOS pass transistor. As with all LDO circuits, a relatively low source impedance (10Ω) is needed to prevent the input impedance from causing the LDO to become unstable. The size and type of the capacitor needed depends heavily on the input source type (battery, power supply) and the output current range of the application. For most applications (up to 100 mA), a 1 µF ceramic capacitor will be sufficient to ensure circuit stability. Larger values can be used to improve circuit AC performance.

5.2 Output

The maximum rated continuous output current for the MCP1703 is 250 mA (VR ≥ 2.5V). For applications where VR < 2.5V, the maximum output current is 200 mA.

A minimum output capacitance of 1.0 µF is required for small signal stability in applications that have up to 250 mA output current capability. The capacitor type can be ceramic, tantalum, or aluminum electrolytic. The Equivalent Series Resistance (ESR) range on the output capacitor can range from 0Ω to 2.0Ω.

The output capacitor range for ceramic capacitors is 1 µF to 22 µF. Higher output capacitance values may be used for tantalum and electrolytic capacitors. Higher output capacitor values pull the pole of the LDO transfer function inward that results in higher phase shifts which in turn cause a lower crossover frequency. The circuit designer should verify the stability by applying line step and load step testing to their system when using capacitance values greater than 22 µF.

5.3 Output Rise Time

When powering up the internal reference output, the typical output rise time of 1000 µs is controlled to prevent overshoot of the output voltage.
6.0 APPLICATION CIRCUITS & ISSUES

6.1 Typical Application

The MCP1703 is most commonly used as a voltage regulator. Its low quiescent current and low dropout voltage make it ideal for many battery-powered applications.

![Typical Application Circuit](image)

**FIGURE 6-1:** Typical Application Circuit.

6.1.1 APPLICATION INPUT CONDITIONS

- **Package Type:** SOT-23A
- **Input Voltage Range:** 2.7V to 4.8V
- **V\text{IN}** maximum: 4.8V
- **V\text{OUT}** typical: 1.8V
- **I\text{OUT}** maximum: 50 mA

6.2 Power Calculations

6.2.1 POWER DISSIPATION

The internal power dissipation of the MCP1703 is a function of input voltage, output voltage and output current. The power dissipation, as a result of the quiescent current draw, is so low, it is insignificant \((2.0 \mu A \times V\text{IN})\). The following equation can be used to calculate the internal power dissipation of the LDO.

**EQUATION 6-1:**

\[
P_{\text{LDO}} = (V_{\text{IN}(\text{MAX})} - V_{\text{OUT}(\text{MIN})}) \times I_{\text{OUT}(\text{MAX})}
\]

Where:

- \(P_{\text{LDO}}\) = LDO Pass device internal power dissipation
- \(V_{\text{IN}(\text{MAX})}\) = Maximum input voltage
- \(V_{\text{OUT}(\text{MIN})}\) = LDO minimum output voltage

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the package maximum internal power dissipation.

**EQUATION 6-2:**

\[
T_{J(\text{MAX})} = P_{\text{TOTA}} \times R_{\theta JA} + T_{A\text{MAX}}
\]

Where:

- \(T_{J(\text{MAX})}\) = Maximum continuous junction temperature
- \(P_{\text{TOTA}}\) = Total device power dissipation
- \(R_{\theta JA}\) = Thermal resistance from junction-to-ambient
- \(T_{A\text{MAX}}\) = Maximum ambient temperature

**EQUATION 6-3:**

\[
P_{\text{D(\text{MAX})}} = \frac{(T_{J(\text{MAX})} - T_{A(\text{MAX})})}{R_{\theta JA}}
\]

Where:

- \(P_{\text{D(\text{MAX})}}\) = Maximum device power dissipation
- \(T_{J(\text{MAX})}\) = Maximum continuous junction temperature
- \(T_{A(\text{MAX})}\) = Maximum ambient temperature
- \(R_{\theta JA}\) = Thermal resistance from junction-to-ambient

**EQUATION 6-4:**

\[
T_{J(\text{RISE})} = P_{\text{D(\text{MAX})}} \times R_{\theta JA}
\]

Where:

- \(T_{J(\text{RISE})}\) = Rise in device junction temperature over the ambient temperature
- \(P_{\text{D(\text{MAX})}}\) = Maximum device power dissipation
- \(R_{\theta JA}\) = Thermal resistance from junction to ambient

**EQUATION 6-5:**

\[
T_J = T_{J(\text{RISE})} + T_A
\]

Where:

- \(T_J\) = Junction temperature
- \(T_{J(\text{RISE})}\) = Rise in device junction temperature over the ambient temperature
- \(T_A\) = Ambient temperature
6.3 Voltage Regulator

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation, as a result of ground current, is small enough to be neglected.

6.3.1 POWER DISSIPATION EXAMPLE

Package
- Package Type: SOT-23A
- Input Voltage: \(V_{\text{IN}} = 2.7\text{V} \text{ to } 4.8\text{V}\)

LDO Output Voltages and Currents
- \(V_{\text{OUT}} = 1.8\text{V}\)
- \(I_{\text{OUT}} = 50\text{ mA}\)

Maximum Ambient Temperature
- \(T_{\text{A(MAX)}} = +40°C\)

Internal Power Dissipation
Internal Power dissipation is the product of the LDO output current times the voltage across the LDO (\(V_{\text{IN}}\) to \(V_{\text{OUT}}\)).

\[ P_{\text{LDO(MAX)}} = (V_{\text{IN(MAX)}} - V_{\text{OUT(MIN)}}) \times I_{\text{OUT(MAX)}} \]
\[ P_{\text{LDO}} = (4.8\text{V} \times 0.97 \times 1.8\text{V}) \times 50\text{ mA} \]
\[ P_{\text{LDO}} = 152.7\text{ milli-Watts} \]

Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient \((R_{\theta JA})\) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface mount packages. The EIA/JEDEC specification is JESD51-7, “High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages”. The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to AN792, “A Method to Determine How Much Power a SOT23 Can Dissipate in an Application”, (DS00792), for more information regarding this subject.

\[ T_{\text{J(\text{RISE})}} = P_{\text{TOT}} \times R_{\theta JA} \]
\[ T_{\text{JRISE}} = 152.7\text{ milli-Watts} \times 336.0°C/\text{Watt} \]
\[ T_{\text{JRISE}} = 51.3°C \]

Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below.

\[ T_{\text{J}} = T_{\text{JRISE}} + T_{\text{A(MAX)}} \]
\[ T_{\text{J}} = 91.3°C \]

Maximum Package Power Dissipation at +40°C Ambient Temperature Assuming Minimal Copper Usage.

- SOT-23A (336.0°C/Watt = \(R_{\theta JA}\))
  \[ P_{\text{D(MAX)}} = \frac{(+125°C - 40°C)}{336°C/\text{Watt}} \]
  \[ P_{\text{D(MAX)}} = 253\text{ milli-Watts} \]
- SOT-89 (153.3°C/Watt = \(R_{\theta JA}\))
  \[ P_{\text{D(MAX)}} = \frac{(+125°C - 40°C)}{153.3°C/\text{Watt}} \]
  \[ P_{\text{D(MAX)}} = 0.554\text{ Watts} \]
- SOT-223 (62.9°C/Watt = \(R_{\theta JA}\))
  \[ P_{\text{D(MAX)}} = \frac{(+125°C - 40°C)}{62.9°C/\text{Watt}} \]
  \[ P_{\text{D(MAX)}} = 1.35\text{ Watts} \]

6.4 Voltage Reference

The MCP1703 can be used not only as a regulator, but also as a low quiescent current voltage reference. In many microcontroller applications, the initial accuracy of the reference can be calibrated using production test equipment or by using a ratio measurement. When the initial accuracy is calibrated, the thermal stability and line regulation tolerance are the only errors introduced by the MCP1703 LDO. The low-cost, low quiescent current and small ceramic output capacitor are all advantages when using the MCP1703 as a voltage reference.

![FIGURE 6-2: Using the MCP1703 as a Voltage Reference.](image-url)
6.5 Pulsed Load Applications

For some applications, there are pulsed load current events that may exceed the specified 250 mA maximum specification of the MCP1703. The internal current limit of the MCP1703 will prevent high peak load demands from causing non-recoverable damage. The 250 mA rating is a maximum average continuous rating. As long as the average current does not exceed 250 mA, pulsed higher load currents can be applied to the MCP1703. The typical current limit for the MCP1703 is 500 mA (T_A +25°C).
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

### Standard Options for SOT-23A and SOT-89

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Voltage *</th>
<th>Symbol</th>
<th>Voltage *</th>
</tr>
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<tbody>
<tr>
<td>HM</td>
<td>1.2</td>
<td>HT</td>
<td>3.0</td>
</tr>
<tr>
<td>HP</td>
<td>1.5</td>
<td>HU</td>
<td>3.3</td>
</tr>
<tr>
<td>HQ</td>
<td>1.8</td>
<td>HV</td>
<td>4.0</td>
</tr>
<tr>
<td>HR</td>
<td>2.5</td>
<td>HW</td>
<td>5.0</td>
</tr>
<tr>
<td>HS</td>
<td>2.8</td>
<td>—</td>
<td>—</td>
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</table>

* Custom output voltages available upon request. Contact your local Microchip sales office for more information.

### Example:

**HWNN**

### Standard Options for SOT-223

<table>
<thead>
<tr>
<th>Symbol</th>
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<th>Symbol</th>
<th>Voltage *</th>
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</thead>
<tbody>
<tr>
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<td>30</td>
<td>3.0</td>
</tr>
<tr>
<td>15</td>
<td>1.5</td>
<td>33</td>
<td>3.3</td>
</tr>
<tr>
<td>18</td>
<td>1.8</td>
<td>40</td>
<td>4.0</td>
</tr>
<tr>
<td>25</td>
<td>2.5</td>
<td>50</td>
<td>5.0</td>
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<tr>
<td>28</td>
<td>2.8</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
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* Custom output voltages available upon request. Contact your local Microchip sales office for more information.

### Example:

**HM1014**

### Standard Options for 8-Lead DFN (2 x 3)

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<th>Voltage *</th>
</tr>
</thead>
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<td>1.2</td>
<td>AAY</td>
<td>3.3</td>
</tr>
<tr>
<td>AAHV</td>
<td>1.8</td>
<td>AFR</td>
<td>4.0</td>
</tr>
<tr>
<td>AAHW</td>
<td>2.5</td>
<td>AAZ</td>
<td>5.0</td>
</tr>
<tr>
<td>AAT</td>
<td>3.0</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

* Custom output voltages available upon request. Contact your local Microchip sales office for more information.

### Example:

**AAU 014 25**

---

**Legend:**
- **XX...X** Customer-specific information
- **Y** Year code (last digit of calendar year)
- **YY** Year code (last 2 digits of calendar year)
- **WW** Week code (week of January 1 is week '01')
- **NNN** Alphanumeric traceability code
- **(e3)** Pb-free JEDEC designator for Matte Tin (Sn)
- **(*)** This package is Pb-free. The Pb-free JEDEC designator (**e3**) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
3-Lead Plastic Small Outline Transistor (CB) [SOT-23A]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

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<td><strong>Dimension Limits</strong></td>
<td><strong>MIN</strong></td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Lead Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Outside Lead Pitch</td>
<td>e1</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

**Notes:**
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.
   
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-130B
3-Lead Plastic Small Outline Transistor (CB) [SOT-23A]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

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<tr>
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<td>MIN NOM MAX</td>
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<tr>
<td>Contact Pitch</td>
<td>E 0.95 BSC</td>
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<tr>
<td>Contact Pad Spacing</td>
<td>C 2.70</td>
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<tr>
<td>Contact Pad Width (X3)</td>
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<tr>
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<tr>
<td>Distance Between Pads</td>
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<tr>
<td>Overall Width</td>
<td>Z 3.70</td>
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Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2130A
3-Lead Plastic Small Outline Transistor Header (MB) [SOT-89]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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<td>Number of Leads</td>
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<td>MIN</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
<td>1.50 BSC</td>
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<tr>
<td>Outside Lead Pitch</td>
<td>e1</td>
<td>3.00 BSC</td>
</tr>
<tr>
<td>Overall Height</td>
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<tr>
<td>Overall Width</td>
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<td>Molded Package Width at Top</td>
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<tr>
<td>Tab Length</td>
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<tr>
<td>Lead 2 Width</td>
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<tr>
<td>Leads 1 &amp; 3 Width</td>
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Notes:
1. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-029B
### MCP1703

#### 3-Lead Plastic Small Outline Transistor Header (MB) [SOT-89]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

![Diagram of 3-Lead Plastic Small Outline Transistor Header](image)

**Recommended Land Pattern**

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<td>Contact 2 Pad Length</td>
<td>Y2</td>
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**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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Microchip Technology Drawing No. C04-2029A
MCP1703

3-Lead Plastic Small Outline Transistor (DB) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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<td>Lead Pitch</td>
<td>e</td>
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<tr>
<td>Outside Lead Pitch</td>
<td>e1</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
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<td>Overall Width</td>
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<td>Molded Package Width</td>
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<td>Lead Angle</td>
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Notes:
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.
  BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-032B
3-Lead Plastic Small Outline Transistor (DB) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

![Recommended Land Pattern Diagram]

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<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Overall Pitch</td>
<td>E1</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
</tr>
<tr>
<td>Contact Pad Width</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Width</td>
<td>X2</td>
</tr>
<tr>
<td>Contact Pad Length</td>
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Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2032A
8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

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<td></td>
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</tr>
<tr>
<td>Pitch</td>
<td>e</td>
<td></td>
<td>0.50 BSC</td>
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<td></td>
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<tr>
<td>Overall Height</td>
<td>A</td>
<td></td>
<td>0.80</td>
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<td></td>
<td>2.00 BSC</td>
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<td></td>
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<tr>
<td>Overall Width</td>
<td>E</td>
<td></td>
<td>3.00 BSC</td>
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<td></td>
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<tr>
<td>Exposed Pad Length</td>
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<td>1.30</td>
<td>–</td>
<td>1.55</td>
</tr>
<tr>
<td>Exposed Pad Width</td>
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<tr>
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<tr>
<td>Contact-to-Exposed Pad</td>
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<td></td>
<td>0.20</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C
8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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**RECOMMENDED LAND PATTERN**

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</thead>
<tbody>
<tr>
<td></td>
<td><strong>Min</strong></td>
</tr>
<tr>
<td>Contact Pitch (E)</td>
<td></td>
</tr>
<tr>
<td>Optional Center Pad Width (W2)</td>
<td></td>
</tr>
<tr>
<td>Optional Center Pad Length (T2)</td>
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</tr>
<tr>
<td>Contact Pad Spacing (C1)</td>
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</tr>
<tr>
<td>Contact Pad Width (X8) (X1)</td>
<td></td>
</tr>
<tr>
<td>Contact Pad Length (X8) (Y1)</td>
<td></td>
</tr>
<tr>
<td>Distance Between Pads (G)</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123A
APPENDIX A: REVISION HISTORY

Revision F (February 2011)
The following is the list of modifications:
1. Added a new line to Output Voltage Regulation in the DC Characteristics table.
2. Added Figure 2-30 and Figure 2-31.

Revision E (November 2010)
The following is the list of modifications:
1. Updated the Thermal Resistance Typical value for the SOT-89 package in the Junction Temperature Estimate section.

Revision D (September 2009)
The following is the list of modifications:
1. Added the 8-Lead 2x3 DFN package.
2. Updated the Temperature Specification table.
3. Updated Table 3-1.
4. Added Section 3.4 “Exposed Thermal Pad (EP)”.
5. Updated the Package Outline Drawings and the information for the 8-Lead 2x3 DFN package.
6. Added the information for the 8-Lead 2x3 DFN package in the Product Identification System section.

Revision C (June 2009)
The following is the list of modifications:
1. Absolute Maximum Ratings: Updated this section.
2. DC Characteristics table: Updated.

Revision B (February 2008)
The following is the list of modifications:
1. Updated Temperature Specifications table.
2. Updated Table 3-1.
3. Updated Section 5.2 “Output”.
**PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>X-</th>
<th>XX</th>
<th>X</th>
<th>X</th>
<th>X/</th>
<th>XX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device:</td>
<td>MCP1703: 250 mA, 16V Low Quiescent Current LDO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tape and Reel:</td>
<td>T = Tape and Reel</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage*:</td>
<td>12 = 1.2V “Standard”</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>15 = 1.5V “Standard”</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>18 = 1.8V “Standard”</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>25 = 2.5V “Standard”</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>28 = 2.8V “Standard”</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>30 = 3.0V “Standard”</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>33 = 3.3V “Standard”</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>40 = 4.0V “Standard”</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>50 = 5.0V “Standard”</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>*Contact factory for other output voltage options.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Extra Feature Code:</td>
<td>0 = Fixed</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tolerance:</td>
<td>1 = 1.0% (Custom)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2 = 2.0% (Standard)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature:</td>
<td>E = -40°C to +125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package Type:</td>
<td>CB = Plastic Small Outline Transistor (SOT-23A) 3-lead,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DB = Plastic Small Outline Transistor (SOT-223) 3-lead,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MB = Plastic Small Outline Transistor (SOT-89) 3-lead,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MC = Plastic Dual Flat, No Lead Package (DFN) 2x3, 8-lead.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Examples:**

- a) MCP1703T-1202E/XX: 1.2V Low Quiescent LDO, Tape and Reel
- b) MCP1703T-1502E/XX: 1.5V Low Quiescent LDO, Tape and Reel
- c) MCP1703T-1802E/XX: 1.8V Low Quiescent LDO, Tape and Reel
- d) MCP1703T-2502E/XX: 2.5V Low Quiescent LDO, Tape and Reel
- e) MCP1703T-2802E/XX: 2.8V Low Quiescent LDO, Tape and Reel
- f) MCP1703T-3002E/XX: 3.0V Low Quiescent LDO, Tape and Reel
- g) MCP1703T-3302E/XX: 3.3V Low Quiescent LDO, Tape and Reel
- h) MCP1703T-3602E/XX: 3.6V Low Quiescent LDO, Tape and Reel
- i) MCP1703T-4002E/XX: 4.0V Low Quiescent LDO, Tape and Reel
- j) MCP1703T-5002E/XX: 5.0V Low Quiescent LDO, Tape and Reel

XX = CB for 3LD SOT-23A package
= DB for 3LD SOT-223 package
= MB for 3LD SOT-89 package
= MC for 8LD DFN package.
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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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