The Microchip Technology Inc. MCP6291/1R/2/3/4/5 family of operational amplifiers (op amps) provide wide bandwidth for the current. This family has a 10 MHz Gain Bandwidth Product (GBWP) and a 65° phase margin. This family also operates from a single supply voltage as low as 2.4V, while drawing 1 mA (typical) quiescent current. In addition, the MCP6291/1R/2/3/4/5 supports rail-to-rail input and output swing, with a common mode input voltage range of \( V_{DD} + 300 \text{ mV} \) to \( V_{SS} - 300 \text{ mV} \). This family of operational amplifiers is designed with Microchip’s advanced CMOS process.

The MCP6295 has a Chip Select (CS) input for dual op amps in an 8-pin package. This device is manufactured by cascading the two op amps, with the output of op amp A being connected to the non-inverting input of op amp B. The CS input puts the device in a Low-power mode.

The MCP6291/1R/2/3/4/5 family operates over the Extended Temperature Range of \(-40°C \) to \(+125°C\). It also has a power supply range of 2.4V to 6.0V.

### Description

The Microchip Technology Inc. MCP6291/1R/2/3/4/5 family of operational amplifiers (op amps) provide wide bandwidth for the current. This family has a 10 MHz Gain Bandwidth Product (GBWP) and a 65° phase margin. This family also operates from a single supply voltage as low as 2.4V, while drawing 1 mA (typical) quiescent current. In addition, the MCP6291/1R/2/3/4/5 supports rail-to-rail input and output swing, with a common mode input voltage range of \( V_{DD} + 300 \text{ mV} \) to \( V_{SS} - 300 \text{ mV} \). This family of operational amplifiers is designed with Microchip’s advanced CMOS process.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

- $V_{DD} - V_{SS} \leq 7.0V$
- Current at Input Pins: $\pm 2\ mA$
- Analog Inputs ($V_{IN+}, V_{IN-}$) †† $V_{SS} - 1.0V$ to $V_{DD} + 1.0V$
- All Other Inputs and Outputs: $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
- Difference Input Voltage: $|V_{DD} - V_{SS}|$
- Output Short Circuit Current: Continuous
- Current at Output and Supply Pins: $\pm 30\ mA$
- Storage Temperature: $-65°C$ to $+150°C$
- Maximum Junction Temperature ($T_J$): $+150°C$
- ESD Protection On All Pins (HBM; MM): $\geq 4\ kV$; $400V$

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See Section 4.1.2 “Input Voltage and Current Limits”.

DC ELECTRICAL SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage</td>
<td>$V_{OS}$</td>
<td>-3.0</td>
<td>—</td>
<td>+3.0</td>
<td>mV</td>
<td>$V_{CM} = V_{SS}$ (Note 1)</td>
</tr>
<tr>
<td>Input Offset Voltage (Extended Temperature)</td>
<td>$V_{OS}$</td>
<td>-5.0</td>
<td>—</td>
<td>+5.0</td>
<td>mV</td>
<td>$T_A = -40°C$ to $+125°C$, $V_{CM} = V_{SS}$ (Note 1)</td>
</tr>
<tr>
<td>Input Offset Temperature Drift</td>
<td>$\Delta V_{OS}/\Delta T_A$</td>
<td>—</td>
<td>±1.7</td>
<td>—</td>
<td>$\mu V/^°C$</td>
<td>$T_A = -40°C$ to $+125°C$, $V_{CM} = V_{SS}$ (Note 1)</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>PSRR</td>
<td>70</td>
<td>90</td>
<td>—</td>
<td>dB</td>
<td>$V_{CM} = V_{SS}$ (Note 1)</td>
</tr>
<tr>
<td>Input Bias, Input Offset Current and Impedance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>$I_B$</td>
<td>—</td>
<td>±1.0</td>
<td>—</td>
<td>pA</td>
<td>Note 2</td>
</tr>
<tr>
<td>At Temperature</td>
<td>$I_B$</td>
<td>—</td>
<td>50</td>
<td>200</td>
<td>pA</td>
<td>$T_A = +85°C$ (Note 2)</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>$I_{OS}$</td>
<td>—</td>
<td>±1.0</td>
<td>—</td>
<td>pA</td>
<td>Note 3</td>
</tr>
<tr>
<td>Common Mode Input Impedance</td>
<td>$Z_{CM}$</td>
<td>$10^{13}</td>
<td>6$</td>
<td>—</td>
<td>$\Omega</td>
<td></td>
</tr>
<tr>
<td>Differential Input Impedance</td>
<td>$Z_{DIFF}$</td>
<td>$10^{13}</td>
<td>3$</td>
<td>—</td>
<td>$\Omega</td>
<td></td>
</tr>
<tr>
<td>Common Mode (Note 4)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common Mode Input Range</td>
<td>$V_{CMR}$</td>
<td>$V_{SS} - 0.3$</td>
<td>—</td>
<td>$V_{DD} + 0.3$</td>
<td>V</td>
<td>$V_{CM} = -0.3V$ to $2.5V$, $V_{DD} = 5V$</td>
</tr>
<tr>
<td>Common Mode Rejection Ratio</td>
<td>CMRR</td>
<td>70</td>
<td>85</td>
<td>—</td>
<td>dB</td>
<td>$V_{CM} = -0.3V$ to $5.3V$, $V_{DD} = 5V$</td>
</tr>
<tr>
<td>Open-Loop Gain</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC Open-Loop Gain (Large Signal)</td>
<td>$A_{OL}$</td>
<td>90</td>
<td>110</td>
<td>—</td>
<td>dB</td>
<td>$V_{OUT} = 0.2V$ to $V_{DD} - 0.2V$, $V_{CM} = V_{SS}$ (Note 1)</td>
</tr>
<tr>
<td>Output</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Output Voltage Swing</td>
<td>$V_{OL}: V_{OH}$</td>
<td>$V_{SS} + 15$</td>
<td>—</td>
<td>$V_{DD} - 15$</td>
<td>mV</td>
<td>0.5V Input Overdrive</td>
</tr>
<tr>
<td>Output Short Circuit Current</td>
<td>$I_{SC}$</td>
<td>—</td>
<td>±25</td>
<td>—</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Power Supply</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>$V_{DD}$</td>
<td>2.4</td>
<td>—</td>
<td>6.0</td>
<td>V</td>
<td>$T_A = -40°C$ to $+125°C$ (Note 5)</td>
</tr>
<tr>
<td>Quiescent Current per Amplifier</td>
<td>$I_Q$</td>
<td>0.7</td>
<td>1.0</td>
<td>1.3</td>
<td>mA</td>
<td>$I_Q = 0$</td>
</tr>
</tbody>
</table>

Note 1: The MCP6295’s $V_{CM}$ for op amp B (pins $V_{OUTA}/V_{INB}+$ and $V_{INB}-$) is $V_{SS} + 100\ mV$.

2: The current at the MCP6295’s $V_{INB}-$ pin is specified by $I_B$ only.

3: This specification does not apply to the MCP6295’s $V_{OUTA}/V_{INB}+$ pin.

4: The MCP6295’s $V_{INB}-$ pin (op amp B) has a common mode range ($V_{CMR}$) of $V_{SS} + 100\ mV$ to $V_{DD} - 100\ mV$. The MCP6295’s $V_{OUTA}/V_{INB}+$ pin (op amp B) has a voltage range specified by $V_{OH}$ and $V_{OL}$.

5: All parts with date codes November 2007 and later have been screened to ensure operation at $V_{DD} = 6.0V$. However, the other minimum and maximum specifications are measured at $2.4V$ and $5.5V$. 

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### AC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +2.4V$ to $+5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \, k\Omega$ to $V_L$, $C_L = 60 \, pF$, and CS is tied low (refer to Figure 1-2 and Figure 1-3).

#### Parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain Bandwidth Product</td>
<td>GBWP</td>
<td>10.0</td>
<td></td>
<td></td>
<td>Hz</td>
<td></td>
</tr>
<tr>
<td>Phase Margin at Unity-Gain</td>
<td>PM</td>
<td>65</td>
<td></td>
<td></td>
<td>°</td>
<td>$G = +1 , V/V$</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>SR</td>
<td>7</td>
<td></td>
<td></td>
<td>V/µs</td>
<td></td>
</tr>
</tbody>
</table>

**Noise**

- Input Noise Voltage: $E_{ni}$
- Input Noise Voltage Density: $e_{ni}$
- Input Noise Current Density: $i_{ni}$

#### Parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Noise Voltage</td>
<td>$E_{ni}$</td>
<td>4.2</td>
<td></td>
<td></td>
<td>µV $\sqrt{P}$</td>
<td>$f = 0.1 , Hz$ to $10 , Hz$</td>
</tr>
<tr>
<td>Input Noise Voltage Density</td>
<td>$e_{ni}$</td>
<td>8.7</td>
<td></td>
<td></td>
<td>nV/$\sqrt{Hz}$</td>
<td>$f = 10 , kHz$</td>
</tr>
<tr>
<td>Input Noise Current Density</td>
<td>$i_{ni}$</td>
<td>3</td>
<td></td>
<td></td>
<td>fA/$\sqrt{Hz}$</td>
<td>$f = 1 , kHz$</td>
</tr>
</tbody>
</table>

---

### MCP6293/MCP6295 CHIP SELECT (CS) SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +2.4V$ to $+5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \, k\Omega$ to $V_L$, $C_L = 60 \, pF$, and CS is tied low (refer to Figure 1-2 and Figure 1-3).

#### CS Low Specifications

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS Logic Threshold, Low</td>
<td>$V_{IL}$</td>
<td>$V_{SS}$</td>
<td>0.2 $V_{DD}$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CS Input Current, Low</td>
<td>$I_{CSL}$</td>
<td></td>
<td>0.01</td>
<td></td>
<td>µA</td>
<td>CS = $V_{SS}$</td>
</tr>
</tbody>
</table>

#### CS High Specifications

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS Logic Threshold, High</td>
<td>$V_{IH}$</td>
<td>0.8 $V_{DD}$</td>
<td></td>
<td>$V_{DD}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CS Input Current, High</td>
<td>$I_{CSH}$</td>
<td></td>
<td>0.7</td>
<td>2</td>
<td>µA</td>
<td>CS = $V_{DD}$</td>
</tr>
<tr>
<td>GND Current per Amplifier</td>
<td>$I_{SS}$</td>
<td></td>
<td>-0.7</td>
<td></td>
<td>µA</td>
<td>CS = $V_{DD}$</td>
</tr>
<tr>
<td>Amplifier Output Leakage</td>
<td></td>
<td></td>
<td>0.01</td>
<td></td>
<td>µA</td>
<td>CS = $V_{DD}$</td>
</tr>
</tbody>
</table>

#### Dynamic Specifications (Note 1)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS Low to Valid Amplifier Output, Turn-on Time</td>
<td>$I_{ON}$</td>
<td></td>
<td>4</td>
<td>10</td>
<td>µs</td>
<td>CS Low $\leq 0.2 , V_{DD}$, $G = +1 , V/V$, $V_{IN} = V_{DD}/2$, $V_{OUT} = 0.9 , V_{DD}/2$, $V_{DD} = 5.0V$</td>
</tr>
<tr>
<td>CS High to Amplifier Output High-Z</td>
<td>$I_{OFF}$</td>
<td></td>
<td>0.01</td>
<td></td>
<td>µs</td>
<td>CS High $\geq 0.8 , V_{DD}$, $G = +1 , V/V$, $V_{IN} = V_{DD}/2$, $V_{OUT} = 0.1 , V_{DD}/2$</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>$V_{HYST}$</td>
<td>0.6</td>
<td></td>
<td>V</td>
<td></td>
<td>$V_{DD} = 5V$</td>
</tr>
</tbody>
</table>

**Note:** The input condition ($V_{IN}$) specified applies to both op amp A and B of the MCP6295. The dynamic specification is tested at the output of op amp B ($V_{OUTB}$).
TEMPERATURE SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated, \( V_{DD} = +2.4\text{V} \) to +5.5V and \( V_{SS} \) = GND.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Temperature Range</td>
<td>( T_A )</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td>Note</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>( T_A )</td>
<td>-65</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td><strong>Thermal Package Resistances</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 5L-SOT-23</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>256</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 6L-SOT-23</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>230</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 8L-PDIP</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>85</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 8L-SOIC</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>163</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 8L-MSOP</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>206</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 14L-PDIP</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>70</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 14L-SOIC</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>120</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 14L-TSSOP</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** The Junction Temperature (\( T_J \)) must not exceed the Absolute Maximum specification of +150°C.

1.1 **Test Circuits**

The test circuits used for the DC and AC tests are shown in Figure 1-2 and Figure 1-2. The bypass capacitors are laid out according to the rules discussed in Section 4.6 “Supply Bypass”.

**FIGURE 1-1:** Timing Diagram for the Chip Select (\( CS \)) pin on the MCP6293 and MCP6295.

**FIGURE 1-2:** AC and DC Test Circuit for Most Non-Inverting Gain Conditions.

**FIGURE 1-3:** AC and DC Test Circuit for Most Inverting Gain Conditions.
2.0  TYPICAL PERFORMANCE CURVES

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, TA = +25°C, VDD = +2.4V to +5.5V, VSS = GND, VCM = VDD/2, VOUT = VDD/2, VL = VDD/2, RL = 10 kΩ to VL, CL = 60 pF, and CS is tied low.

FIGURE 2-1: Input Offset Voltage.

FIGURE 2-2: Input Bias Current at TA = +85°C.

FIGURE 2-3: Input Offset Voltage vs. Common Mode Input Voltage at VDD = 2.4V.

FIGURE 2-4: Input Offset Voltage Drift.

FIGURE 2-5: Input Bias Current at TA = +125°C.

FIGURE 2-6: Input Offset Voltage vs. Common Mode Input Voltage at VDD = 5.5V.
TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +2.4V$ to $+5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \, k\Omega$ to $V_L$, $C_L = 60 \, pF$, and $CS$ is tied low.

**FIGURE 2-7:** Input Offset Voltage vs. Output Voltage.

**FIGURE 2-8:** CMRR, PSRR vs. Frequency.

**FIGURE 2-9:** Input Bias, Offset Currents vs. Common Mode Input Voltage at $T_A = +85^\circ C$.

**FIGURE 2-10:** Input Bias, Input Offset Currents vs. Ambient Temperature.

**FIGURE 2-11:** CMRR, PSRR vs. Ambient Temperature.

**FIGURE 2-12:** Input Bias, Offset Currents vs. Common Mode Input Voltage at $T_A = +125^\circ C$. 
TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: Unless otherwise indicated, \( T_A = +25°C \), \( V_{DD} = +2.4\text{V to } +5.5\text{V} \), \( V_{SS} = \text{GND} \), \( V_{CM} = V_{DD}/2 \), \( V_{OUT} = V_{DD}/2 \), \( V_L = V_{DD}/2 \), \( R_L = 10\text{kΩ} \) to \( V_L \), \( C_L = 60\text{ pF} \), and \( CS \) is tied low.

**FIGURE 2-13:** Quiescent Current vs. Power Supply Voltage.

**FIGURE 2-14:** Open-Loop Gain, Phase vs. Frequency.

**FIGURE 2-15:** Maximum Output Voltage Swing vs. Frequency.

**FIGURE 2-16:** Output Voltage Headroom vs. Output Current Magnitude.

**FIGURE 2-17:** Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.

**FIGURE 2-18:** Slew Rate vs. Ambient Temperature.
TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +2.4V$ to +5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\, k\Omega$ to $V_L$, $C_L = 60\, pF$, and $CS$ is tied low.

**FIGURE 2-19:** Input Noise Voltage Density vs. Frequency.

**FIGURE 2-20:** Output Short Circuit Current vs. Power Supply Voltage.

**FIGURE 2-21:** Quiescent Current vs. Chip Select (CS) Voltage at $V_{DD} = 2.4V$ (MCP6293 and MCP6295 only).

**FIGURE 2-22:** Input Noise Voltage Density vs. Common Mode Input Voltage at 10 kHz.

**FIGURE 2-23:** Channel-to-Channel Separation vs. Frequency (MCP6292, MCP6294 and MCP6295 only).

**FIGURE 2-24:** Quiescent Current vs. Chip Select (CS) Voltage at $V_{DD} = 5.5V$ (MCP6293 and MCP6295 only).
TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +2.4V$ to $+5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10$ k$\Omega$ to $V_L$, $C_L = 60$ pF, and $CS$ is tied low.

**FIGURE 2-25:** Large-Signal Non-inverting Pulse Response.

**FIGURE 2-26:** Small-Signal Non-inverting Pulse Response.

**FIGURE 2-27:** Chip Select ($CS$) to Amplifier Output Response Time at $V_{DD} = 2.4V$ (MCP6293 and MCP6295 only).

**FIGURE 2-28:** Large-Signal Inverting Pulse Response.

**FIGURE 2-29:** Small-Signal Inverting Pulse Response.

**FIGURE 2-30:** Chip Select ($CS$) to Amplifier Output Response Time at $V_{DD} = 5.5V$ (MCP6293 and MCP6295 only).
TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = +2.4V$ to $+5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \, k\Omega$ to $V_L$, $C_L = 60 \, pF$, and $CS$ is tied low.

**FIGURE 2-31:** Measured Input Current vs. Input Voltage (below $V_{SS}$).

**FIGURE 2-32:** The MCP6291/1R/2/3/4/5 Show No Phase Reversal.
3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1 (single op amps) and Table 3-2 (dual and quad op amps).

### TABLE 3-1: PIN FUNCTION TABLE FOR SINGLE OP AMPS

<table>
<thead>
<tr>
<th>MCP6291</th>
<th>MCP6291R</th>
<th>MCP6293</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDIP, SOIC, MSOP</td>
<td>SOT-23-5</td>
<td>PDIP, SOIC, MSOP</td>
<td>SOT-23-6</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>6</td>
<td>1</td>
<td>( V_{OUT} )</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>2</td>
<td>4</td>
<td>( V_{IN}^- )</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>( V_{IN}^+ )</td>
</tr>
<tr>
<td>7</td>
<td>5</td>
<td>7</td>
<td>6</td>
<td>( V_{DD} )</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>4</td>
<td>2</td>
<td>( V_{SS} )</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>8</td>
<td>CS</td>
</tr>
<tr>
<td>1,5,8</td>
<td>—</td>
<td>—</td>
<td>1,5</td>
<td>—</td>
</tr>
</tbody>
</table>

### TABLE 3-2: PIN FUNCTION TABLE FOR DUAL AND QUAD OP AMPS

<table>
<thead>
<tr>
<th>MCP6292</th>
<th>MCP6294</th>
<th>MCP6295</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>—</td>
<td>( V_{OUTA} )</td>
<td>Analog Output (op amp A)</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>2</td>
<td>( V_{INA}^- )</td>
<td>Inverting Input (op amp A)</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>3</td>
<td>( V_{INA}^+ )</td>
<td>Non-inverting Input (op amp A)</td>
</tr>
<tr>
<td>8</td>
<td>4</td>
<td>8</td>
<td>( V_{DD} )</td>
<td>Positive Power Supply</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>—</td>
<td>( V_{INB}^+ )</td>
<td>Non-inverting Input (op amp B)</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>6</td>
<td>( V_{INB}^- )</td>
<td>Inverting Input (op amp B)</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td>7</td>
<td>( V_{OUTB} )</td>
<td>Analog Output (op amp B)</td>
</tr>
<tr>
<td>—</td>
<td>8</td>
<td>—</td>
<td>( V_{OUTC} )</td>
<td>Analog Output (op amp C)</td>
</tr>
<tr>
<td>—</td>
<td>9</td>
<td>—</td>
<td>( V_{INC}^- )</td>
<td>Inverting Input (op amp C)</td>
</tr>
<tr>
<td>—</td>
<td>10</td>
<td>—</td>
<td>( V_{INC}^+ )</td>
<td>Non-inverting Input (op amp C)</td>
</tr>
<tr>
<td>4</td>
<td>11</td>
<td>4</td>
<td>( V_{SS} )</td>
<td>Negative Power Supply</td>
</tr>
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<td>—</td>
<td>12</td>
<td>—</td>
<td>( V_{IND}^+ )</td>
<td>Non-inverting Input (op amp D)</td>
</tr>
<tr>
<td>—</td>
<td>13</td>
<td>—</td>
<td>( V_{IND}^- )</td>
<td>Inverting Input (op amp D)</td>
</tr>
<tr>
<td>—</td>
<td>14</td>
<td>—</td>
<td>( V_{OUTD} )</td>
<td>Analog Output (op amp D)</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>1</td>
<td>( V_{OUTA}/V_{INB}^+ )</td>
<td>Analog Output (op amp A)/Non-inverting Input (op amp B)</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>5</td>
<td>CS</td>
<td>Chip Select</td>
</tr>
</tbody>
</table>

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 MCP6295’s \( V_{OUTA}/V_{INB}^+ \) Pin

For the MCP6295 only, the output of op amp A is connected directly to the non-inverting input of op amp B; this is the \( V_{OUTA}/V_{INB}^+ \) pin. This connection makes it possible to provide a Chip Select pin for duals in 8-pin packages.

3.4 Chip Select Digital Input

This is a CMOS, Schmitt-triggered input that places the part into a low power mode of operation.

3.5 Power Supply Pins

The positive power supply (\( V_{DD} \)) is 2.4V to 6.0V higher than the negative power supply (\( V_{SS} \)). For normal operation, the other pins are between \( V_{SS} \) and \( V_{DD} \). Typically, these parts are used in a single (positive) supply configuration. In this case, \( V_{SS} \) is connected to ground and \( V_{DD} \) is connected to the supply. \( V_{DD} \) will need bypass capacitors.
4.0 APPLICATION INFORMATION

The MCP6291/1R/2/3/4/5 family of op amps is manufactured using Microchip’s state of the art CMOS process, specifically designed for low-cost, low-power and general purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6291/1R/2/3/4/5 ideal for battery-powered applications.

4.1 Rail-to-Rail Inputs

4.1.1 PHASE REVERSAL

The MCP6291/1R/2/3/4/5 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-32 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current (Ib). The input ESD diodes clamp the inputs when they try to go more than one diode drop below VSS. They also clamp any voltages that go too far above VDD; their breakdown voltage is high enough to allow normal operation, and low enough to bypass quick ESD events within the specified limits.

![FIGURE 4-1: Simplified Analog Input ESD Structures.](image)

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the currents and voltages at the VIN+ and VIN– pins (see Absolute Maximum Ratings † at the beginning of Section 1.0 “Electrical Characteristics”). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (VIN+ and VIN–) from going too far below ground, and the resistors R1 and R2 limit the possible current drawn out of the input pins. Diodes D1 and D2 prevent the input pins (VIN+ and VIN–) from going too far above VDD, and dump any currents onto VDD. When implemented as shown, resistors R1 and R2 also limit the current through D1 and D2.

![FIGURE 4-2: Protecting the Analog Inputs.](image)

A significant amount of current can flow out of the inputs when the common mode voltage (VCM) is below ground (VSS); see Figure 2-31. Applications that are high impedance may need to limit the usable voltage range.

4.1.3 NORMAL OPERATION

The input stage of the MCP6291/1R/2/3/4/5 op amps use two differential CMOS input stages in parallel. One operates at low common mode input voltage (VCM), while the other operates at high VCM. With this topology, the device operates with VCM up to 0.3V past either supply rail. The input offset voltage (VOS) is measured at VCM = VSS - 0.3V and VDD + 0.3V to ensure proper operation.

The transition between the two input stages occurs when VCM = VDD - 1.1V. For the best distortion and gain linearity, with non-inverting gains, avoid this region of operation.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6291/1R/2/3/4/5 op amp is VDD – 15 mV (min.) and VSS + 15 mV (maximum) when R_L = 10 kΩ is connected to VDD/2 and VDD = 5.5V. Refer to Figure 2-16 for more information.
4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop’s phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity-gain buffer (G = +1) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-3) improves the feedback loop’s phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

![Figure 4-3: Output Resistor, R_{ISO} stabilizes large capacitive loads.](image)

Figure 4-4 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_{L}/G_{N}), where G_{N} is the circuit’s noise gain. For non-inverting gains, G_{N} and the Signal Gain are equal. For inverting gains, G_{N} = |Signal Gain| (e.g., -1 V/V gives G_{N} = +2 V/V).

![Figure 4-4: Recommended R_{ISO} Values for Capacitive Loads.](image)

4.4 MCP629X Chip Select

The MCP6293 and MCP6295 are single and dual op amps with Chip Select (CS), respectively. When CS is pulled high, the supply current drops to 0.7 µA (typical) and flows through the CS pin to V_{SS}. When this happens, the amplifier output is put into a high-impedance state. By pulling CS low, the amplifier is enabled. The CS pin has an internal 5 MΩ (typical) pull-down resistor connected to V_{SS}, so it will go low if the CS pin is left floating. Figure 1-1 shows the output voltage and supply current response to a CS pulse.

4.5 Cascaded Dual Op Amps (MCP6295)

The MCP6295 is a dual op amp with Chip Select (CS). The Chip Select input is available on what would be the non-inverting input of a standard dual op amp (pin 5). This is available because the output of op amp A connects to the non-inverting input of op amp B, as shown in Figure 4-5. The Chip Select input, which can be connected to a microcontroller I/O line, puts the device in Low-power mode. Refer to Section 4.4 “MCP629X Chip Select”.

![Figure 4-5: Cascaded Gain Amplifier.](image)

The output of op amp A is loaded by the input impedance of op amp B, which is typically 10^{12} Ω/6 pF, as specified in the DC specification table (Refer to Section 4.3 “Capacitive Loads” for further details regarding capacitive loads).

The common mode input range of these op amps is specified in the data sheet as V_{SS} – 300 mV and V_{DD} – 300 mV. However, since the output of op amp A is limited to V_{OL} and V_{OH} (20 mV from the rails with a 10 kΩ load), the non-inverting input range of op amp B is limited to the common mode input range of V_{SS} + 20 mV and V_{DD} – 20 mV.
4.6 Supply Bypass

With this family of operational amplifiers, the power supply pin (VDD for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with nearby analog parts.

4.7 Unused Op Amps

An unused op amp in a quad package (MCP6294) should be configured as shown in Figure 4-6. These circuits prevent the output from toggling and causing crosstalk. Circuits A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.

4.8 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface-leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}$ Ω. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP6291/1R/2/3/4/5 family’s bias current at 25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-7.

1. For Inverting Gain and Transimpedance Amplifiers (convert current to voltage, such as photo detectors):
   a. Connect the guard ring to the non-inverting input pin (V_IN+). This biases the guard ring to the same reference voltage as the op amp (e.g., VDD/2 or ground).
   b. Connect the inverting pin (V_IN–) to the input with a wire that does not touch the PCB surface.

2. Non-inverting Gain and Unity-Gain Buffer:
   a. Connect the non-inverting pin (V_IN+) to the input with a wire that does not touch the PCB surface.
   b. Connect the guard ring to the inverting input pin (V_IN–). This biases the guard ring to the common mode input voltage.
4.9 Application Circuits

4.9.1 MULTIPLE FEEDBACK LOW-PASS FILTER

The MCP6291/1R/2/3/4/5 op amp can be used in active-filter applications. Figure 4-8 shows an inverting, third-order, multiple feedback low-pass filter that can be used as an anti-aliasing filter.

![Multiple Feedback Low-Pass Filter](image)

**FIGURE 4-8:** Multiple Feedback Low-Pass Filter.

This filter, and others, can be designed using Microchip’s Filter design software. Refer to Section 5.0 “Design Aids”

4.9.2 PHOTODIODE AMPLIFIER

Figure 4-9 shows a photodiode biased in the photovoltaic mode for high precision. The resistor R converts the diode current ID to the voltage $V_{OUT}$. The capacitor is used to limit the bandwidth or to stabilize the circuit against the diode’s capacitance (it is not always needed).

![Photodiode Amplifier](image)

**FIGURE 4-9:** Photodiode Amplifier.

4.9.3 CASCADED OP AMP APPLICATIONS

The MCP6295 provides the flexibility of Low-power mode for dual op amps in an 8-pin package. The MCP6295 eliminates the added cost and space in battery-powered applications by using two single op amps with Chip Select lines or a 10-pin device with one Chip Select line for both op amps. Since the two op amps are internally cascaded, this device cannot be used in circuits that require active or passive elements between the two op amps. However, there are several applications where this op amp configuration with Chip Select line becomes suitable. The circuits below show possible applications for this device.

4.9.3.1 Load Isolation

With the cascaded op amp configuration, op amp B can be used to isolate the load from op amp A. In applications where op amp A is driving capacitive or low resistance loads in the feedback loop (such as an integrator circuit or filter circuit), the op amp may not have sufficient source current to drive the load. In this case, op amp B can be used as a buffer.

![Isolating the Load with a Buffer](image)

**FIGURE 4-10:** Isolating the Load with a Buffer.
4.9.3.2 Cascaded Gain

Figure 4-11 shows a cascaded gain circuit configuration with Chip Select. Op amps A and B are configured in a non-inverting amplifier configuration. In this configuration, it is important to note that the input offset voltage of op amp A is amplified by the gain of op amp A and B, as shown below:

\[
V_{OUT} = V_{IN}G_AG_B + V_{OSA}G_AG_B + V_{OSB}G_B
\]

Where:
- \( G_A \) = op amp A gain
- \( G_B \) = op amp B gain
- \( V_{OSA} \) = op amp A input offset voltage
- \( V_{OSB} \) = op amp B input offset voltage

Therefore, it is recommended to set most of the gain with op amp A and use op amp B with relatively small gain (e.g., a unity-gain buffer).

![Cascaded Gain Circuit Configuration](image)

4.9.3.3 Difference Amplifier

Figure 4-12 shows op amp A as a difference amplifier with Chip Select. In this configuration, it is recommended to use well-matched resistors (e.g., 0.1%) to increase the Common Mode Rejection Ratio (CMRR). Op amp B can be used for additional gain or as a unity-gain buffer to isolate the load from the difference amplifier.

![Difference Amplifier Circuit](image)

4.9.3.4 Buffered Non-inverting Integrator

Figure 4-13 shows a lossy non-inverting integrator that is buffered and has a Chip Select input. Op amp A is configured as a non-inverting integrator. In this configuration, matching the impedance at each input is recommended. \( R_F \) is used to provide a feedback loop at frequencies \(< 1/(2\pi R_1C_1)\) and makes this a lossy integrator (it has a finite gain at DC). Op amp B is used to isolate the load from the integrator.

![Buffered Non-inverting Integrator with Chip Select](image)

4.9.3.5 Inverting Integrator with Active Compensation and Chip Select

Figure 4-14 uses an active compensator (op amp B) to compensate for the non-ideal op amp characteristics introduced at higher frequencies. This circuit uses op amp B as a unity-gain buffer to isolate the integration capacitor \( C_1 \) from op amp A and drives the capacitor with low-impedance source. Since both op amps are matched very well, they provide a high quality integrator.

![Integrator Circuit with Active Compensation](image)
4.9.3.6 Second-Order MFB Low-Pass Filter with an Extra Pole-Zero Pair

Figure 4-15 is a second-order multiple feedback low-pass filter with Chip Select. Use the FilterLab® software from Microchip to determine the R and C values for the op amp A’s second-order filter. Op amp B can be used to add a pole-zero pair using $C_3$, $R_6$ and $R_7$.

![Diagram of Second-Order Multiple Feedback Low-Pass Filter with an Extra Pole-Zero Pair](image)

**FIGURE 4-15:** Second-Order Multiple Feedback Low-Pass Filter with an Extra Pole-Zero Pair.

4.9.3.7 Second-Order Sallen-Key Low-Pass Filter with an Extra Pole-Zero Pair

Figure 4-16 is a second-order, Sallen-Key low-pass filter with Chip Select. Use the FilterLab® software from Microchip to determine the R and C values for the op amp A’s second-order filter. Op amp B can be used to add a pole-zero pair using $C_3$, $R_5$ and $R_6$.

![Diagram of Second-Order Sallen-Key Low-Pass Filter with an Extra Pole-Zero Pair](image)

**FIGURE 4-16:** Second-Order Sallen-Key Low-Pass Filter with an Extra Pole-Zero Pair and Chip Select.

4.9.3.8 Capacitorless Second-Order Low-Pass Filter with Chip Select

The low-pass filter shown in Figure 4-17 does not require external capacitors and uses only three external resistors; the op amp’s GBWP sets the corner frequency. $R_1$ and $R_2$ are used to set the circuit gain and $R_3$ is used to set the Q. To avoid gain peaking in the frequency response, Q needs to be low (lower values need to be selected for $R_3$). Note that the amplifier bandwidth varies greatly over temperature and process. However, this configuration provides a low cost solution for applications with high bandwidth requirements.

![Diagram of Capacitorless Second-Order Low-Pass Filter with Chip Select](image)

**FIGURE 4-17:** Capacitorless Second-Order Low-Pass Filter with Chip Select.
5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6291/1R/2/3/4/5 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6291/1R/2/3/4/5 op amps is available on the Microchip web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp’s linear region of operation over the temperature range. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip’s FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Mindi™ Simulator Tool

Microchip’s Mindi™ simulator tool aids in the design of various circuits useful for active filter, amplifier and power-management applications. It is a free online simulation tool available from the Microchip web site at www.microchip.com/mindi. This interactive simulator enables designers to quickly generate circuit diagrams, simulate circuits. Circuits developed using the Mindi simulation tool can be downloaded to a personal computer or workstation.

5.4 MAPS (Microchip Advanced Part Selector)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip’s product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase, and Sampling of Microchip parts.

5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user’s guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Two of our boards that are especially useful are:

- P/N SOIC8EV: 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board
- P/N SOIC14EV: 14-Pin SOIC/TSSOP/DIP Evaluation Board

5.6 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

ADN003: “Select the Right Operational Amplifier for your Filtering Circuits”, DS21821

AN722: “Operational Amplifier Topologies and DC Specifications”, DS00722

AN723: “Operational Amplifier AC Specifications and Applications”, DS00723

AN884: “Driving Capacitive Loads With Op Amps”, DS00884

AN990: “Analog Sensor Conditioning Circuits – An Overview”, DS00990

These application notes and others are listed in the design guide:

“Signal Chain Design Guide”, DS21825
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

5-Lead SOT-23 (MCP6291 and MCP6291R)

Example:

```
Device  Code
MCP6291  CJNN
MCP6291R EVNN
```

Note: Applies to 5-Lead SOT-23

6-Lead SOT-23 (MCP6283)

Example:

```
Device  Code
MCP6293  CMNN
```

Note: Applies to 6-Lead SOT-23

8-Lead MSOP

Example:

```
Device  Code
```

8-Lead PDIP (300 mil)

Example:

```
Device  Code
MCP6291E OR MCP6291 E/P256 0436
OR MCP6291E OR MCP6291 E/P@3256 0743
```

Note: Applies to 8-Lead PDIP (300 mil)

8-Lead SOIC (150 mil)

Example:

```
Device  Code
MCP6291E OR MCP6291E SN@0743 256
OR MCP6291E OR MCP6291E SN@0743 256
```

Note: Applies to 8-Lead SOIC (150 mil)

Legend:

- XX...X Customer-specific information
- Y Year code (last digit of calendar year)
- YY Year code (last 2 digits of calendar year)
- WWW Week code (week of January 1 is week ‘01’)
- NNN Alphanumeric traceability code
- 3e Pb-free JEDEC designator for Matte Tin (Sn)
- * This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
Package Marking Information (Continued)

14-Lead PDIP (300 mil) (MCP6294)

Example:

14-Lead SOIC (150 mil) (MCP6294)

Example:

OR

14-Lead TSSOP (MCP6294)

Example:
5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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</thead>
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<td></td>
<td>Dimension</td>
<td>Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
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<td>5</td>
<td></td>
</tr>
<tr>
<td>Lead Pitch</td>
<td>e</td>
<td>0.95 BSC</td>
<td></td>
</tr>
<tr>
<td>Outside Lead Pitch</td>
<td>e1</td>
<td>1.90 BSC</td>
<td></td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
<td>0.90</td>
<td>–</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
<td>0.89</td>
<td>–</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
<td>0.00</td>
<td>–</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
<td>2.20</td>
<td>–</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
<td>1.30</td>
<td>–</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
<td>2.70</td>
<td>–</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
<td>0.10</td>
<td>–</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
<td>0.35</td>
<td>–</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
<td>0°</td>
<td>–</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
<td>0.08</td>
<td>–</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
<td>0.20</td>
<td>–</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
## 6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

### Dimensions

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
<th>Dimension Limits</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Pins</td>
<td>N</td>
<td>6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
<td>0.95 BSC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Outside Lead Pitch</td>
<td>e1</td>
<td>1.90 BSC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overall Height</td>
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<td>0.90</td>
<td>–</td>
<td>1.45</td>
<td></td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
<td>0.89</td>
<td>–</td>
<td>1.30</td>
<td></td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
<td>0.00</td>
<td>–</td>
<td>0.15</td>
<td></td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
<td>2.20</td>
<td>–</td>
<td>3.20</td>
<td></td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
<td>1.30</td>
<td>–</td>
<td>1.80</td>
<td></td>
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<tr>
<td>Overall Length</td>
<td>D</td>
<td>2.70</td>
<td>–</td>
<td>3.10</td>
<td></td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
<td>0.10</td>
<td>–</td>
<td>0.60</td>
<td></td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
<td>0.35</td>
<td>–</td>
<td>0.80</td>
<td></td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
<td>0°</td>
<td>–</td>
<td>30°</td>
<td></td>
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<tr>
<td>Lead Thickness</td>
<td>c</td>
<td>0.08</td>
<td>–</td>
<td>0.26</td>
<td></td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
<td>0.20</td>
<td>–</td>
<td>0.51</td>
<td></td>
</tr>
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</table>

### Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

### Dimensions

<table>
<thead>
<tr>
<th>Units</th>
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<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>ϕ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.
8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

<table>
<thead>
<tr>
<th>Units</th>
<th>Dimension Limits</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
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</thead>
<tbody>
<tr>
<td>Number of Pins</td>
<td>N</td>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
<td>.100 BSC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Top to Seating Plane</td>
<td>A</td>
<td>–</td>
<td>–</td>
<td>.210</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
<td>.115</td>
<td>.130</td>
<td>.195</td>
</tr>
<tr>
<td>Base to Seating Plane</td>
<td>A1</td>
<td>.015</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Shoulder to Shoulder Width</td>
<td>E</td>
<td>.290</td>
<td>.310</td>
<td>.325</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
<td>.240</td>
<td>.250</td>
<td>.280</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
<td>.348</td>
<td>.365</td>
<td>.400</td>
</tr>
<tr>
<td>Tip to Seating Plane</td>
<td>L</td>
<td>.115</td>
<td>.130</td>
<td>.150</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
<td>.008</td>
<td>.010</td>
<td>.015</td>
</tr>
<tr>
<td>Upper Lead Width</td>
<td>b1</td>
<td>.040</td>
<td>.060</td>
<td>.070</td>
</tr>
<tr>
<td>Lower Lead Width</td>
<td>b</td>
<td>.014</td>
<td>.018</td>
<td>.022</td>
</tr>
<tr>
<td>Overall Row Spacing §</td>
<td>eB</td>
<td>–</td>
<td>–</td>
<td>.430</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

---

**Microchip Technology Drawing C04-057B**
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

![Schematic showing the dimensions and land pattern for an 8-lead plastic small outline package.]

---

**Recommended Land Pattern**

<table>
<thead>
<tr>
<th>Units</th>
<th>MILIMETERS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
<td></td>
<td></td>
<td>1.27 BSC</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
<td></td>
<td></td>
<td>5.40</td>
</tr>
<tr>
<td>Contact Pad Width (X8)</td>
<td>X1</td>
<td></td>
<td></td>
<td>0.60</td>
</tr>
<tr>
<td>Contact Pad Length (X8)</td>
<td>Y1</td>
<td></td>
<td></td>
<td>1.55</td>
</tr>
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</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A
14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

![package diagram]

<table>
<thead>
<tr>
<th>Units</th>
<th>INCHES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension</td>
<td>Limits</td>
</tr>
</tbody>
</table>
| Number of Pins | N      | 14
| Pitch       | e      | .100 BSC
| Top to Seating Plane | A    | – |
| Molded Package Thickness  | A2  | .115, .130, .195
| Base to Seating Plane | A1   | .015 – –
| Shoulder to Shoulder Width | E | .290, .310, .325
| Molded Package Width | E1 | .240, .250, .280
| Overall Length | D | .735, .750, .775
| Tip to Seating Plane | L | .115, .130, .150
| Lead Thickness | c | .008, .010, .015
| Upper Lead Width | b1 | .045, .060, .070
| Lower Lead Width | b | .014, .018, .022
| Overall Row Spacing § | eB | – – .430

**Notes:**
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff §</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Chamfer (optional)</td>
<td>h</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
<tr>
<td>Mold Draft Angle Top</td>
<td>α</td>
</tr>
<tr>
<td>Mold Draft Angle Bottom</td>
<td>β</td>
</tr>
</tbody>
</table>

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B
14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Molded Package Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.
APPENDIX A: REVISION HISTORY

Revision E (November 2007)
The following is the list of modifications:
1. Updated notes to Section 1.0 “Electrical Characteristics”. Increased absolute maximum voltage range of input pins. Increased maximum operating supply voltage (VDD).
2. Added Test Circuits.
3. Added Figure 2-31 and Figure 2-32.
4. Added Section 4.1.1 “Phase Reversal”, Section 4.1.2 “Input Voltage and Current Limits”, and Section 4.1.3 “Normal Operation”.
5. Added Section 4.7 “Unused Op Amps”.
6. Updated Section 5.0 “Design Aids”.
7. Corrected Package Markings.
8. Updated Package Outline Drawing.

Revision D (December 2004)
The following is the list of modifications:
1. Added SOT-23-5 packages for the MCP6291 and MCP6291R single op amps.
2. Added SOT-23-6 package for the MCP6293 single op amp.
3. Added Section 3.0 “Pin Descriptions”.
4. Corrected application circuits (Section 4.9 “Application Circuits”).
5. Added SOT-23-5 and SOT-23-6 packages and corrected package marking information (Section 6.0 “Packaging Information”).
6. Added Appendix A: Revision History.

Revision C (June 2004)
• Undocumented changes.

Revision B (October 2003)
• Undocumented changes.

Revision A (June 2003)
• Original data sheet release.
## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>Device</th>
<th>Temperature Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>X</td>
<td>/XX</td>
<td></td>
</tr>
</tbody>
</table>

### Device:
- **MCP6291**: Single Op Amp
- **MCP6291T**: Single Op Amp (Tape and Reel) (SOIC, MSOP, SOT-23-5)
- **MCP6291RT**: Single Op Amp (Tape and Reel) (SOT-23-5)
- **MCP6292**: Dual Op Amp (Tape and Reel) (SOIC, MSOP)
- **MCP6293**: Single Op Amp with Chip Select (Tape and Reel) (SOIC, MSOP, SOT-23-6)
- **MCP6294**: Quad Op Amp (Tape and Reel) (SOIC, TSSOP)
- **MCP6295**: Dual Op Amp with Chip Select (Tape and Reel) (SOIC, MSOP)
- **MCP6291-E/SN**: Extended Temperature, 8 lead SOIC package.
- **MCP6291-E/MS**: Extended Temperature, 8 lead MSOP package.
- **MCP6291-E/P**: Extended Temperature, 8 lead PDIP package.
- **MCP6291T-E/OT**: Tape and Reel, Extended Temperature, 5 lead SOT-23 package.
- **MCP6291RT-E/OT**: Tape and Reel, Extended Temperature, 5 lead SOT-23 package.
- **MCP6292-E/SN**: Extended Temperature, 8 lead SOIC package.
- **MCP6292-E/MS**: Extended Temperature, 8 lead MSOP package.
- **MCP6292-E/P**: Extended Temperature, 8 lead PDIP package.
- **MCP6292T-E/SN**: Tape and Reel, Extended Temperature, 8 lead SOIC package.
- **MCP6293-E/SN**: Extended Temperature, 8 lead SOIC package.
- **MCP6293-E/MS**: Extended Temperature, 8 lead MSOP package.
- **MCP6293-E/P**: Extended Temperature, 8 lead PDIP package.
- **MCP6293T-E/CH**: Tape and Reel, Extended Temperature, 6 lead SOT-23 package.
- **MCP6294-E/P**: Extended Temperature, 14 lead PDIP package.
- **MCP6294T-E/SL**: Tape and Reel, Extended Temperature, 14 lead SOIC package.
- **MCP6294-E/SL**: Extended Temperature, 14 lead SOIC package.
- **MCP6294-E/ST**: Extended Temperature, 14 lead TSSOP package.
- **MCP6295-E/SN**: Extended Temperature, 8 lead SOIC package.
- **MCP6295-E/MS**: Extended Temperature, 8 lead MSOP package.
- **MCP6295-E/P**: Extended Temperature, 8 lead PDIP package.
- **MCP6295T-E/SN**: Tape and Reel, Extended Temperature, 8 lead SOIC package.
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