Features

- Dual Output LDO with Microcontroller Reset Monitor Functionality:
  - $V_{OUT1} = 1.5V$ to $3.3V @ 300 mA$
  - $V_{OUT2} = 1.5V$ to $3.3V @ 150 mA$
  - $V_{RESET} = 2.20V$ to $3.20V$
- Output Voltage and RESET Threshold Voltage Options Available (See Table 8-1)
- Low Dropout Voltage:
  - $V_{OUT1} = 104 mV @ 300 mA$ (typical)
  - $V_{OUT2} = 150 mV @ 150 mA$, (typical)
- Low Supply Current: 116 µA (typical), TC1301A/B with both output voltages available
- Reference Bypass Input for Low-Noise Operation
- Both Output Voltages Stable with a Minimum of 1 µF Ceramic Output Capacitor
- Separate Input for RESET Detect Voltage (TC1301A)
- Separate $V_{OUT1}$ and $V_{OUT2}$ SHDN pins (TC1301B)
- RESET Output Duration: 300 ms (typical)
- Power-Saving Shutdown Mode of Operation
- Wake-up from SHDN: 5.3 µs (typical)
- Small 8-pin DFN and MSOP Package Options
- Operating Junction Temperature Range: -40°C to +125°C
- Overtemperature and Overcurrent Protection

Applications

- Cellular/GSM/PHS Phones
- Battery-Operated Systems
- Hand-Held Medical Instruments
- Portable Computers/PDAs
- Linear Post-Regulators for SMPS
- Pagers

Related Literature

- AN766, “Pin-Compatible CMOS Upgrades to Bipolar LDOs”, DS00766, Microchip Technology Inc., 2002

Description

The TC1301A/B combines two Low Dropout (LDO) regulators and a microcontroller RESET function into a single 8-pin MSOP or DFN package. Both regulator outputs feature low dropout voltage, 104 mV @ 300 mA for $V_{OUT1}$, 150 mV @ 150 mA for $V_{OUT2}$, low quiescent current consumption, 58 µA each and a typical regulation accuracy of 0.5%. Several fixed-output voltage and detector voltage combinations are available. A reference bypass pin is available to further reduce output noise and improve the power supply rejection ratio of both LDOs.

The TC1301A/B is stable over all line and load conditions with a minimum of 1 µF of ceramic output capacitance, and utilizes a unique compensation scheme to provide fast dynamic response to sudden line voltage and load current changes.

For the TC1301A, the microcontroller RESET function operates independently of both $V_{OUT1}$ and $V_{OUT2}$. The input to the RESET function is connected to the $V_{DET}$ pin. The SHDN2 pin is used to control the output of $V_{OUT2}$ only. $V_{OUT1}$ will power-up and down with $V_{IN}$.

In the case of the TC1301B, the detect voltage input of the RESET function is connected internally to $V_{OUT1}$. Both $V_{OUT1}$ and $V_{OUT2}$ have independent shutdown capability.

Additional features include an overcurrent limit and overtemperature protection that, when combined, provide a robust design for all load fault conditions.

Package Types
Functional Block Diagrams

**TC1301A**

- **V**\textsubscript{IN} → **LDO #1** (300 mA)
- **LDO #1** → **V**\textsubscript{OUT1}
- **V**\textsubscript{DET} → **Threshold Detector**
- **Threshold Detector** → **Time Delay** (300 ms, typ)
- **Time Delay** → **RESET**
- **V**\textsubscript{DET} → **Bandgap Reference 1.2V**
- **Bandgap Reference 1.2V** → **SHDN2**
- **SHDN2** → **GND**
- **GND** → **Bypass**
- **V**\textsubscript{OUT2} → **V**\textsubscript{DET}

**TC1301B**

- **V**\textsubscript{IN} → **LDO #1** (300 mA)
- **LDO #1** → **V**\textsubscript{OUT1}
- **V**\text{DET} → **Threshold Detector**
- **Threshold Detector** → **Time Delay** (300 ms, typ)
- **Time Delay** → **RESET**
- **V**\text{DET} → **Bandgap Reference 1.2V**
- **Bandgap Reference 1.2V** → **SHDN2**
- **SHDN2** → **GND**
- **GND** → **Bypass**
- **V**\textsubscript{OUT2} → **V**\text{DET}

Typical Application Circuits

**TC1301A**

- **System RESET**
- **2.8V @ 300 mA**
- **C\textsubscript{OUT1}** (1 µF Ceramic X5R)
- **C\textsubscript{BYPASS}** (10 nF Ceramic)

**TC1301B**

- **System RESET**
- **2.8V @ 300 mA**
- **C\textsubscript{OUT1}** (1 µF Ceramic X5R)

**Note:**
- **C\textsubscript{BYPASS}** is optional

© 2008 Microchip Technology Inc.
# 1.0 ELECTRICAL CHARACTERISTICS

**Absolute Maximum Ratings †**

- $V_{DD} \leq 6.5V$
- Maximum Voltage on Any Pin: $(V_{SS} – 0.3)$ to $(V_{IN} + 0.3)V$
- Power Dissipation: Internally Limited (Note 7)
- Storage temperature: $-65°C$ to $+150°C$
- Maximum Junction Temperature, $T_J$: $+150°C$
- Continuous Operating Temperature Range: $-40°C$ to $+125°C$
- ESD protection on all pins, HBM, MM: $4\, kV, 400V$

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## DC CHARACTERISTICS

**Electrical Specifications:** Unless otherwise noted, $V_{IN} = V_R + 1V$, $I_{OUT1} = I_{OUT2} = 100\, \mu A$, $C_{IN} = 4.7\, \mu F$, $C_{OUT1} = C_{OUT2} = 1\, \mu F$, $C_{BYPASS} = 10\, nF$, $SHDN > V_BH \cdot T_A = +25°C$.

**Boldface** type specifications apply for junction temperatures of $-40°C$ to $+125°C$.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Operating Voltage</td>
<td>$V_{IN}$</td>
<td>2.7</td>
<td>—</td>
<td>6.0</td>
<td>V</td>
<td>Note 1</td>
</tr>
<tr>
<td>Maximum Output Current</td>
<td>$I_{OUT1, \text{Max}}$</td>
<td>300</td>
<td>—</td>
<td>—</td>
<td>mA</td>
<td>$V_{IN} = 2.7V$ to $6.0V$ (Note 1)</td>
</tr>
<tr>
<td>Maximum Output Current</td>
<td>$I_{OUT2, \text{Max}}$</td>
<td>150</td>
<td>—</td>
<td>—</td>
<td>mA</td>
<td>$V_{IN} = 2.7V$ to $6.0V$ (Note 1)</td>
</tr>
<tr>
<td>Output Voltage Tolerance ($V_{OUT1}$ and $V_{OUT2}$)</td>
<td>$V_{OUT}$</td>
<td>$V_R - 2.5$</td>
<td>$V_R \pm 0.5$</td>
<td>$V_R + 2.5$</td>
<td>%</td>
<td>Note 2</td>
</tr>
<tr>
<td>Temperature Coefficient ($V_{OUT1}$ and $V_{OUT2}$)</td>
<td>$TC_{OUT}$</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>ppm/°C</td>
<td>Note 3</td>
</tr>
<tr>
<td>Line Regulation ($V_{OUT1}$ and $V_{OUT2}$)</td>
<td>$\Delta V_{OUT}/\Delta V_{IN}$</td>
<td>—</td>
<td>0.02</td>
<td>0.2</td>
<td>%/V</td>
<td>$(V_R + 1V) \leq V_{IN} \leq 6V$</td>
</tr>
<tr>
<td>Load Regulation, $V_{OUT} \geq 2.5V$ ($V_{OUT1}$ and $V_{OUT2}$)</td>
<td>$\Delta V_{OUT}/V_{OUT}$</td>
<td>-1</td>
<td>0.1</td>
<td>+1</td>
<td>%</td>
<td>$I_{OUTX} = 0.1, mA$ to $I_{OUT, \text{Max}}$ (Note 4)</td>
</tr>
<tr>
<td>Load Regulation, $V_{OUT} &lt; 2.5V$ ($V_{OUT1}$ and $V_{OUT2}$)</td>
<td>$\Delta V_{OUT}/V_{OUT}$</td>
<td>-1.5</td>
<td>0.1</td>
<td>+1.5</td>
<td>%</td>
<td>$I_{OUTX} = 0.1, mA$ to $I_{OUT, \text{Max}}$ (Note 4)</td>
</tr>
<tr>
<td>Thermal Regulation</td>
<td>$\Delta V_{OUT}/\Delta PD$</td>
<td>—</td>
<td>0.04</td>
<td>—</td>
<td>%/W</td>
<td>Note 5</td>
</tr>
<tr>
<td>Dropout Voltage (Note 6)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OUT1} \geq 2.7V$</td>
<td>$V_{IN} - V_{OUT}$</td>
<td>—</td>
<td>104</td>
<td>180</td>
<td>mV</td>
<td>$I_{OUT1} = 300, mA$</td>
</tr>
<tr>
<td>$V_{OUT2} \geq 2.6V$</td>
<td>$V_{IN} - V_{OUT}$</td>
<td>—</td>
<td>150</td>
<td>250</td>
<td>mV</td>
<td>$I_{OUT2} = 150, mA$</td>
</tr>
</tbody>
</table>

**Supply Current**

- TC1301A: $I_{IN(A)}$ | — | 103 | 180 | µA |
- TC1301B: $I_{IN(B)}$ | — | 114 | 180 | µA |

| Note 1: | The minimum $V_{IN}$ has to meet two conditions: $V_{IN} \geq 2.7V$ and $V_{IN} \geq V_R + V_{\text{DROPOUT}}$.
| Note 2: | $V_R$ is defined as the higher of the two regulator nominal output voltages ($V_{OUT1}$ or $V_{OUT2}$).
| Note 3: | $TC_{OUT} = ((V_{OUT\, \text{Max}} - V_{OUT\, \text{Min}}) \cdot 10^6)/(V_{OUT} \cdot \Delta T)$.
| Note 4: | Regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.
| Note 5: | Thermal regulation is defined as the change in output voltage at a time t after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to $I_{MAX}$ at $V_{IN} = 6V$ for $t = 10\, ms$.
| Note 6: | Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its value measured at a 1V differential.
| Note 7: | The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction-to-air (i.e., $T_A$, $T_J$, $\theta_{JA}$). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown.
## DC CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Unless otherwise noted, \( V_{IN} = V_R + 1V, I_{OUT1} = I_{OUT2} = 100 \mu A, C_{IN} = 4.7 \mu F, C_{OUT1} = C_{OUT2} = 1 \mu F, C_{BYPASS} = 10 nF, SHDN > V_{IH}, T_A = +25^\circ C. 

**Boldface** type specifications apply for junction temperatures of -40°C to +125°C.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shutdown Supply Current TC1301A</td>
<td>( I_{IN_SHDN})</td>
<td>—</td>
<td>58</td>
<td>90</td>
<td>( \mu A )</td>
<td>( SHDN2 = GND, V_{DET} = OPEN )</td>
</tr>
<tr>
<td>Shutdown Supply Current TC1301B</td>
<td>( I_{IN_SHDN})</td>
<td>—</td>
<td>0.1</td>
<td>1</td>
<td>( \mu A )</td>
<td>( SHDN1 = SHDN2 = GND )</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>PSRR</td>
<td>—</td>
<td>58</td>
<td>—</td>
<td>dB</td>
<td>( f \leq 100 \text{ Hz}, I_{OUT1} = I_{OUT2} = 50 \text{ mA}, C_{IN} = 0 \mu F )</td>
</tr>
<tr>
<td>Output Noise</td>
<td>( eN )</td>
<td>—</td>
<td>830</td>
<td>—</td>
<td>nV/(Hz)(^{1/2} )</td>
<td>( f \leq 1 \text{ kHz}, I_{OUT1} = I_{OUT2} = 50 \text{ mA}, C_{IN} = 0 \mu F )</td>
</tr>
<tr>
<td>Output Short-Circuit Current (Average)</td>
<td>( V_{OUT1} )</td>
<td>( I_{OUTsc} )</td>
<td>—</td>
<td>200</td>
<td>mA</td>
<td>( R_{LOAD1} \leq 1 \Omega )</td>
</tr>
<tr>
<td></td>
<td>( V_{OUT2} )</td>
<td>( I_{OUTsc} )</td>
<td>—</td>
<td>140</td>
<td>mA</td>
<td>( R_{LOAD2} \leq 1 \Omega )</td>
</tr>
<tr>
<td>SHDN Input High Threshold</td>
<td>( V_{IH} )</td>
<td>45</td>
<td>—</td>
<td>—</td>
<td>%V_{IN}</td>
<td>( V_{IN} = 2.7V ) to 6.0V</td>
</tr>
<tr>
<td>SHDN Input Low Threshold</td>
<td>( V_{IL} )</td>
<td>—</td>
<td>—</td>
<td>15</td>
<td>%V_{IN}</td>
<td>( V_{IN} = 2.7V ) to 6.0V</td>
</tr>
</tbody>
</table>
| Wake-Up Time (From SHDN mode) (\( V_{OUT2} \)) | \( t_{WK} \) | — | 5.3 | 20 | \( \mu s \) | \( V_{IN} = 5V, I_{OUT1} = I_{OUT2} = 30 \text{ mA}, \) \*See Figure 5-1*
| Settling Time (From SHDN mode) (\( V_{OUT2} \)) | \( t_{S} \) | — | 50 | — | \( \mu s \) | \( V_{IN} = 5V, I_{OUT1} = I_{OUT2} = 50 \text{ mA}, \) \*See Figure 5-2*
| Thermal Shutdown Die Temperature | \( T_{SD} \) | — | 150 | — | °C | \( V_{IN} = 5V, I_{OUT1} = I_{OUT2} = 100 \text{ mA} \) |
| Thermal Shutdown Hysteresis | \( T_{HYS} \) | — | 10 | — | °C | \( V_{IN} = 5V \) |
| Voltage Range | \( V_{DET} \) | 1.0 | 1.2 | 6.0 | V | \( T_A = 0^\circ C \) to +70°C |
| | | | | | | \( T_A = -40^\circ C \) to +125°C |
| RESET Threshold | \( V_{TH} \) | -1.4 | — | +1.4 | % | \( T_A = 0^\circ C \) to +70°C |
| | | | | | | \( T_A = -40^\circ C \) to +125°C |
| RESET Threshold Tempco | \( \Delta V_{TH}/\Delta T \) | — | 30 | — | ppm/°C |
| RESET Delay | \( t_{RPD} \) | — | 180 | — | \( \mu s \) | \( V_{DET} = V_{TH} \) to \( (V_{TH} - 100 \text{ mV}) \), \*See Figure 5-3*
| RESET Active Time-out Period | \( t_{RPU} \) | 140 | 300 | 560 | ms | \( V_{DET} = V_{TH} - 100 \text{ mV} \) to \( V_{TH} + 100 \text{ mV}, I_{SINK} = 1.2 \text{ mA}, \) \*See Figure 5-3.*
| RESET Output Voltage Low | \( V_{OL} \) | — | — | 0.2 | V | \( V_{DET} = V_{TH\_min}, I_{SINK} = 1.2 \text{ mA}, I_{SINK} = 100 \mu A \) for \( V_{DET} < 1.8V, \) \*See Figure 5-3.*
| RESET Output Voltage High | \( V_{OH} \) | 0.9 | \( V_{DET} \) | — | — | V | \( V_{DET} > V_{TH\_max}, I_{SOURCE} = 500 \mu A, \) \*See Figure 5-3.*

**Note 1:** The minimum \( V_{IN} \) has to meet two conditions: \( V_{IN} \geq 2.7V \) and \( V_{IN} \geq V_R + V_{DROPOUT}. \)

**Note 2:** \( V_R \) is defined as the higher of the two regulator nominal output voltages (\( V_{OUT1} \) or \( V_{OUT2} \)).

**Note 3:** \( TCVOUT = ((V_{OUT\_max} - V_{OUT\_min}) * 10^6)/(V_{OUT} * \Delta T). \)

**Note 4:** Regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

**Note 5:** Thermal regulation is defined as the change in output voltage at a time \( t \) after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to \( I_{MAX} \) at \( V_{IN} = 6V \) for \( t = 10 \text{ ms}. \)

**Note 6:** Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its value measured at a 1V differential.

**Note 7:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction-to-air (i.e., \( T_A, T_J, \theta JA \)). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown.
TEMPERATURE SPECIFICATIONS

**Electrical Specifications:** Unless otherwise indicated, all limits are specified for: $V_{IN} = +2.7V$ to $+6.0V$.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Temperature Ranges</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Junction Temperature Range</td>
<td>$T_A$</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td>Steady State</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_A$</td>
<td>-65</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>$T_J$</td>
<td>—</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td>Transient</td>
</tr>
<tr>
<td><strong>Thermal Package Resistances</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 8LD MSOP</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>208</td>
<td>—</td>
<td>°C/W</td>
<td>Typical 4-Layer Board</td>
</tr>
<tr>
<td>Thermal Resistance, 8LD DFN</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>41</td>
<td>—</td>
<td>°C/W</td>
<td>Typical 4-Layer Board with Vias</td>
</tr>
</tbody>
</table>
2.0  TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, VIN = VR +1V, IOUT1 = IOUT2 = 100 µA, CIN = 4.7 µF, COUT1 = COUT2 = 1 µF (X5R or X7R), CBYPASS = 0 pF, SHDN1 = SHDN2 > VIH. For the TC1301A, VDET = VOUT1, RESET = OPEN, TA = +25°C.

FIGURE 2-1: Quiescent Current vs. Input Voltage.

FIGURE 2-2: SHDN Voltage Threshold vs. Input Voltage.

FIGURE 2-3: Quiescent Current vs. Junction Temperature.

FIGURE 2-4: Output Voltage vs. Input Voltage.

FIGURE 2-5: Output Voltage vs. Input Voltage.

FIGURE 2-6: Dropout Voltage vs. Output Current (VOUT1).
**Note:** Unless otherwise indicated, $V_{\text{IN}} = V_{R} + 1V$, $I_{\text{OUT1}} = I_{\text{OUT2}} = 100 \, \mu A$, $C_{\text{IN}} = 4.7 \, \mu F$, $C_{\text{OUT1}} = C_{\text{OUT2}} = 1 \, \mu F$ (X5R or X7R), $C_{\text{BYPASS}} = 0 \, \text{pF}$, $\text{SHDN1} = \text{SHDN2} > V_{\text{IH}}$. For the TC1301A, $V_{\text{DET}} = V_{\text{OUT1}}$, $\text{RESET} = \text{OPEN}$, $T_{A} = +25^\circ C$.  

**FIGURE 2-7:** Dropout Voltage vs. Junction Temperature ($V_{\text{OUT1}}$).  

**FIGURE 2-8:** Dropout Voltage vs. Output Current ($V_{\text{OUT2}}$).  

**FIGURE 2-9:** Dropout Voltage vs. Junction Temperature ($V_{\text{OUT2}}$).  

**FIGURE 2-10:** $V_{\text{OUT1}}$ and $V_{\text{OUT2}}$ Load Regulation vs. Junction Temperature.  

**FIGURE 2-11:** $V_{\text{OUT1}}$ and $V_{\text{OUT2}}$ Line Regulation vs. Junction Temperature.  

**FIGURE 2-12:** $V_{\text{OUT1}}$ vs. Junction Temperature.
Note: Unless otherwise indicated, $V_{IN} = V_R + 1V$, $I_{OUT1} = I_{OUT2} = 100 \mu A$, $C_{IN} = 4.7 \mu F$, $C_{OUT1} = C_{OUT2} = 1 \mu F$ (X5R or X7R), $C_{BYPASS} = 0 \, pF$, $SHDN1 > V_{IH}$, $SHDN2 > V_{IH}$. For the TC1301A, $V_{DET} = V_{OUT1}$, $RESET = OPEN$, $T_A = +25^\circ C$.

**FIGURE 2-13:** $V_{OUT1}$ vs. Junction Temperature.

**FIGURE 2-14:** $V_{OUT2}$ vs. Junction Temperature.

**FIGURE 2-15:** $V_{OUT2}$ vs. Junction Temperature.

**FIGURE 2-16:** $I_{DET}$ current vs. Junction Temperature.

**FIGURE 2-17:** $R_{ESET}$ Active Time vs. Junction Temperature.

**FIGURE 2-18:** $V_{DET}$ Trip Point vs. Junction Temperature.
Note: Unless otherwise indicated, $V_{IN} = V_R + 1V$, $I_{OUT1} = I_{OUT2} = 100 \mu A$, $C_{IN} = 4.7 \mu F$, $C_{OUT1} = C_{OUT2} = 1 \mu F$ (X5R or X7R), $C_{BYPASS} = 0 \mu F$, $SHDN1 = SHDN2 = VH$. For the TC1301A, $V_{DET} = V_{OUT1}$, $RESET = OPEN$, $T_A = +25^\circ C$.

**FIGURE 2-19:** Power Supply Rejection Ratio vs. Frequency (without bypass capacitor).

**FIGURE 2-20:** Power Supply Rejection Ratio vs. Frequency (with bypass capacitor).

**FIGURE 2-21:** $V_{OUT1}$ and $V_{OUT2}$ Noise vs. Frequency (without bypass capacitor).

**FIGURE 2-22:** $V_{OUT1}$ and $V_{OUT2}$ Noise vs. Frequency (with bypass capacitor).

**FIGURE 2-23:** $V_{OUT1}$ and $V_{OUT2}$ Power-up from Shutdown TC1301B.

**FIGURE 2-24:** $V_{OUT2}$ Power-up from Shutdown Input TC1301A.
Note: Unless otherwise indicated, $V_{\text{IN}} = V_R + 1V$, $I_{\text{OUT1}} = I_{\text{OUT2}} = 100 \mu A$, $C_{\text{IN}} = 4.7 \mu F$, $C_{\text{OUT1}} = C_{\text{OUT2}} = 1 \mu F$ (X5R or X7R), $C_{\text{BYPASS}} = 0 \, pF$, $\text{SHDN1} = \text{SHDN2} > V_{\text{IH}}$. For the TC1301A, $V_{\text{DET}} = V_{\text{OUT1}}$, $\text{RESET} = \text{OPEN}$, $T_A = +25^\circ C$.

**FIGURE 2-25:** $V_{\text{OUT1}}$ and $V_{\text{OUT2}}$ Power-up from Input Voltage TC1301B.

**FIGURE 2-26:** Dynamic Line Response.

**FIGURE 2-27:** 300 mA Dynamic Load Step $V_{\text{OUT1}}$.

**FIGURE 2-28:** 150 mA Dynamic Load Step $V_{\text{OUT2}}$.

**FIGURE 2-29:** RESET Power-Up From $V_{\text{IN}}$ TC1301B.

**FIGURE 2-30:** TC1301A RESET Power-Down.
Note: Unless otherwise indicated, $V_{IN} = V_R + 1V$, $I_{OUT1} = I_{OUT2} = 100 \mu A$, $C_{IN} = 4.7 \mu F$, $C_{OUT1} = C_{OUT2} = 1 \mu F$ (X5R or X7R), $C_{BYPASS} = 0 \mu F$, $SHDN1 = SHDN2 > VIH$. For the TC1301A, $V_{DET} = V_{OUT1}$, $RESET = OPEN$, $T_A = +25^\circ C$. 

**FIGURE 2-31:** $RESET$ Output Voltage Low vs. Junction Temperature.

**FIGURE 2-32:** $RESET$ Output Voltage High vs. Junction Temperature.
### 3.0 TC1301A PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RESET</td>
<td>Push-pull output pin that will remain low while ( V_{DET} ) is below the reset threshold and for 300 ms after ( V_{DET} ) rises above the reset threshold.</td>
</tr>
<tr>
<td>2</td>
<td>( V_{OUT1} )</td>
<td>Regulated output voltage #1 capable of 300 mA.</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Circuit ground pin.</td>
</tr>
<tr>
<td>4</td>
<td>Bypass</td>
<td>Internal reference bypass pin. A 10 nF external capacitor can be used to further reduce output noise and improve PSRR performance.</td>
</tr>
<tr>
<td>5</td>
<td>SHDN2</td>
<td>Output #2 shutdown control input.</td>
</tr>
<tr>
<td>6</td>
<td>( V_{OUT2} )</td>
<td>Regulated output voltage #2 capable of 150 mA.</td>
</tr>
<tr>
<td>7</td>
<td>( V_{IN} )</td>
<td>Unregulated input voltage pin.</td>
</tr>
<tr>
<td>8</td>
<td>( V_{DET} )</td>
<td>Input pin for Voltage Detector ( (V_{DET}) ).</td>
</tr>
</tbody>
</table>

#### 3.1 RESET Output Pin

The push-pull output pin is used to monitor the voltage on the \( V_{DET} \) pin. If the \( V_{DET} \) voltage is less than the threshold voltage, the RESET output will be held in the low state. As the \( V_{DET} \) pin rises above the threshold, the RESET output will remain in the low state for 300 ms and then change to the high state, indicating that the voltage on the \( V_{DET} \) pin is above the threshold.

#### 3.2 Regulated Output Voltage #1 \( (V_{OUT1}) \)

Connect \( V_{OUT1} \) to the positive side of the \( V_{OUT1} \) capacitor and load. It is capable of 300 mA maximum output current. \( V_{OUT1} \) output is available when \( V_{IN} \) is available; there is no pin to turn it OFF. See TC1301B if ON/OFF control of \( V_{OUT1} \) is desired.

#### 3.3 Circuit Ground Pin \( (GND) \)

Connect GND to the negative side of the input and output capacitor. Only the LDO internal circuitry bias current flows out of this pin (200 \( \mu \)A maximum).

#### 3.4 Reference Bypass Input

By connecting an external 10 nF capacitor (typical) to the bypass input, both outputs (\( V_{OUT1} \) and \( V_{OUT2} \)) will have less noise and improved Power Supply Ripple Rejection (PSRR) performance. The LDO output voltage start-up time will increase with the addition of an external bypass capacitor. By leaving this pin unconnected, the start-up time will be minimized.

#### 3.5 Output Voltage #2 Shutdown \( (SHDN2) \)

ON/OFF control is performed by connecting SHDN2 to its proper level. When the input of this pin is connected to a voltage less than 15% of \( V_{IN} \), \( V_{OUT2} \) will be OFF. If this pin is connected to a voltage that is greater than 45% of \( V_{IN} \), \( V_{OUT2} \) will be turned ON.

#### 3.6 Regulated Output Voltage #2 \( (V_{OUT2}) \)

Connect \( V_{OUT2} \) to the positive side of the \( V_{OUT2} \) capacitor and load. This pin is capable of a maximum output current of 150 mA. \( V_{OUT2} \) can be turned ON and OFF using SHDN2.

#### 3.7 Unregulated Input Voltage Pin \( (V_{IN}) \)

Connect the unregulated input voltage source to \( V_{IN} \). If the input voltage source is located more than several inches away, or is a battery, a typical input capacitance of 1 \( \mu \)F to 4.7 \( \mu \)F is recommended.

#### 3.8 Input Pin for Voltage Detector \( (V_{DET}) \)

The voltage on the input of \( V_{DET} \) is compared with the preset \( V_{DET} \) threshold voltage. If the voltage is below the threshold, the RESET output will be low. If the voltage is above the \( V_{DET} \) threshold, the RESET output will be high after the RESET time period. The \( I_{DET} \) supply current is typically 9 \( \mu \)A at room temperature, with \( V_{DET} = 3.8 \) V.
4.0 TC1301B PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

TABLE 4-1: TC1301B PIN FUNCTION TABLE

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RESET</td>
<td>Push-pull output pin that will remain low while VDET is below the reset threshold and for 300 ms after VOUT1 rises above the reset threshold</td>
</tr>
<tr>
<td>2</td>
<td>VOUT1</td>
<td>Regulated output voltage #1 capable of 300 mA</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Circuit ground pin</td>
</tr>
<tr>
<td>4</td>
<td>Bypass</td>
<td>Internal reference bypass pin. A 10 nF external capacitor can be used to further reduce output noise and improve PSRR performance</td>
</tr>
<tr>
<td>5</td>
<td>SHDN2</td>
<td>Output #2 shutdown control input</td>
</tr>
<tr>
<td>6</td>
<td>VOUT2</td>
<td>Regulated output voltage #2 capable of 150 mA</td>
</tr>
<tr>
<td>7</td>
<td>VIN</td>
<td>Unregulated input voltage pin</td>
</tr>
<tr>
<td>8</td>
<td>SHDN1</td>
<td>Output #1 shutdown control input</td>
</tr>
</tbody>
</table>

4.1 RESET Output Pin

The push-pull output pin is used to monitor the output voltage (VOUT1). If VOUT1 is less than the threshold voltage, the RESET output will be held in the low state. As VOUT1 rises above the threshold, the RESET output will remain in the low state for 300 ms and then change to the high state, indicating that the voltage on VOUT1 is above the threshold.

4.2 Regulated Output Voltage #1 (VOUT1)

Connect VOUT1 to the positive side of the VOUT1 capacitor and load. It is capable of 300 mA maximum output current. For the TC1301B, VOUT1 can be turned ON and OFF using the SHDN1 input pin.

4.3 Circuit Ground Pin (GND)

Connect GND to the negative side of the input and output capacitor. Only the LDO internal circuitry bias current flows out of this pin (200 µA maximum).

4.4 Reference Bypass Input

By connecting an external 10 nF capacitor (typical) to bypass, both outputs (VOUT1 and VOUT2) will have less noise and improved Power Supply Ripple Rejection (PSRR) performance. The LDO output voltage start-up time will increase with the addition of an external bypass capacitor. By leaving this pin unconnected, the start-up time will be minimized.

4.5 Output Voltage #2 Shutdown (SHDN2)

ON/OFF control is performed by connecting SHDN2 to its proper level. When this pin is connected to a voltage less than 15% of VIN, VOUT2 will be OFF. If this pin is connected to a voltage that is greater than 45% of VIN, VOUT2 will be turned ON.

4.6 Regulated Output Voltage #2 (VOUT2)

Connect VOUT2 to the positive side of the VOUT2 capacitor and load. This pin is capable of a maximum output current of 150 mA. VOUT2 can be turned ON and OFF using SHDN2.

4.7 Unregulated Input Voltage Pin (VIN)

Connect the unregulated input voltage source to VIN. If the input voltage source is located more than several inches away or is a battery, a typical minimum input capacitance of 1 µF and 4.7 µF is recommended.

4.8 Output Voltage #1 Shutdown (SHDN1)

ON/OFF control is performed by connecting SHDN1 to its proper level. When this pin is connected to a voltage less than 15% of VIN, VOUT1 will be OFF. If this pin is connected to a voltage that is greater than 45% of VIN, VOUT1 will be turned ON.
5.0 DETAILED DESCRIPTION

5.1 Device Overview

The TC1301A/B is a combination device consisting of one 300 mA LDO regulator with a fixed output voltage, \( V_{\text{OUT1}} \) (1.5V – 3.3V), one 150 mA LDO regulator with a fixed output voltage, \( V_{\text{OUT2}} \) (1.5V – 3.3V), and a microcontroller voltage monitor/RESET (2.2V to 3.2V).

For the TC1301A, the 300 mA output (\( V_{\text{OUT1}} \)) is always present, independent of the level of SHDN2. The 150 mA output (\( V_{\text{OUT2}} \)) can be turned on/off by controlling the level of SHDN2.

For the TC1301B, \( V_{\text{OUT1}} \) and \( V_{\text{OUT2}} \) each have independent shutdown input pins (SHDN1 and SHDN2) to control their respective outputs. In the case of the TC1301B, the voltage detect input of the microcontroller RESET function is internally connected to the \( V_{\text{OUT1}} \) output of the device.

5.2 LDO Output #1

LDO output #1 is rated for 300 mA of output current. The typical dropout voltage for \( V_{\text{OUT1}} = 104 \text{ mV} @ 300 \text{ mA} \). A 1 µF (minimum) output capacitor is needed for stability and should be located as close to the \( V_{\text{OUT1}} \) pin and ground as possible.

5.3 LDO Output #2

LDO output #2 is rated for 150 mA of output current. The typical dropout voltage for \( V_{\text{OUT2}} = 150 \text{ mV} \). A 1 µF (minimum) capacitor is needed for stability and should be located as close to the \( V_{\text{OUT2}} \) pin and ground as possible.

5.4 RESET Output

The \( \text{RESET} \) output is used to detect whether the level on the input of \( V_{\text{DET}} \) (TC1301A) or \( V_{\text{OUT1}} \) (TC1301B) is above or below a preset threshold. If the voltage detected is below the preset threshold, the \( \text{RESET} \) output is capable of sinking 1.2 mA (\( V_{\text{RESET}} < 0.2 \text{V} \) maximum). Once the voltage being monitored is above the preset threshold, the \( \text{RESET} \) output pin will transition from a logic-low to a logic-high after a 300 ms delay. The \( \text{RESET} \) output is a push-pull configuration and will actively pull the \( \text{RESET} \) output up to \( V_{\text{DET}} \) when not in \( \text{RESET} \).

5.5 Input Capacitor

Low input source impedance is necessary for the two LDO outputs to operate properly. When operating from batteries or in applications with long lead length (> 10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 1.0 µF to 4.7 µF is recommended for most applications. When using large capacitors on the LDO outputs, larger capacitance is recommended on the LDO input. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will help reduce the input impedance and further reduce any high-frequency noise on the input and output of the LDO.

5.6 Output Capacitor

A minimum output capacitance of 1 µF for each of the TC1301A/B LDO outputs is necessary for stability. Ceramic capacitors are recommended because of their size, cost and environmental robustness qualities. Electrolytic (Tantalum or Aluminum) capacitors can be used on the LDO outputs as well. The Equivalent Series Resistance (ESR) requirements on the electrolytic output capacitors are between 0 and 2 ohms. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials, X7R and X5R, have low temperature coefficients and are well within the acceptable ESR range required. A typical 1 uF X5R 0805 capacitor has an ESR of 50 milli-ohms. Larger LDO output capacitors can be used with the TC1301A/B to improve dynamic performance and power supply ripple rejection performance. A maximum of 10 µF is recommended. Aluminum electrolytic capacitors are not recommended for low temperature applications of < -25°C.

5.7 Bypass Input

The bypass pin is connected to the internal LDO reference. By adding capacitance to this pin, the LDO ripple rejection, input voltage transient response and output noise performance are all increased. A typical bypass capacitor between 470 pF to 10 nF is recommended. Larger bypass capacitors can be used, but results in a longer time-period for the LDO outputs to reach their rated output voltage when started from SHDN or \( V_{\text{IN}} \).

5.8 GND

For the optimal noise and PSRR performance, the GND pin of the TC1301A/B should be tied to a quiet circuit ground. For applications that have switching or noisy inputs, tie the GND pin to the return of the output capacitor. Ground planes help lower inductance and voltage spikes caused by fast transient load currents and are recommended for applications that are subjected to fast load transients.

5.9 SHDN1/SHDN2 Operation

The TC1301A SHDN2 pin is used to turn \( V_{\text{OUT2}} \) ON and OFF. A logic-high level on SHDN2 will enable the \( V_{\text{OUT2}} \) output, while a logic-low on the SHDN2 pin will disable the \( V_{\text{OUT2}} \) output. For the TC1301A, \( V_{\text{OUT1}} \) is not affected by SHDN2 and will be enabled as long as the input voltage is present.

The TC1301B SHDN1 and SHDN2 pins are used to turn \( V_{\text{OUT1}} \) and \( V_{\text{OUT2}} \) ON and OFF. They operate independent of each other.
5.10 **TC1301A SHDN2 Timing**

$V_{OUT1}$ will rise independent of the level of $SHDN2$ for the TC1301A. Figure 5-1 is used to define the wake-up time from shutdown ($t_{WK}$) and the settling time ($t_s$). The wake-up time is dependant upon the frequency of operation. The faster the $SHDN$ pin is pulsed, the shorter the wake-up time will be.

![FIGURE 5-1: TC1301A Timing.](image)

5.11 **TC1301B SHDN1 / SHDN2 Timing**

For the TC1301B, the $SHDN1$ input pin is used to control $V_{OUT1}$. The $SHDN2$ input pin is used to control $V_{OUT2}$, independent of the logic input on $SHDN1$.

![FIGURE 5-2: TC1301B Timing.](image)

5.12 **$V_{DET}$ and RESET Operation**

The TC1301A/B integrates an independent voltage reset monitor that can be used for low-battery input voltage detection or a microprocessor Power-On Reset (POR) function. The input voltage for the detector is different for the TC1301A than it is for the TC1301B.

For the TC1301A, the input voltage to the detector is pin 8 ($V_{DET}$). For the TC1301B, the input voltage to the detector is internally connected to the output of LDO #1 ($V_{OUT1}$). The detected voltage is sensed and compared to an internal threshold. When the voltage on the $V_{DET}$ pin is below the threshold voltage, the RESET output pin is low. When the voltage on the $V_{DET}$ pin rises above the voltage threshold, the RESET output will remain low for typically 300 ms (RESET time-out period). After the RESET time-out period, the RESET output voltage will transition from the low output state to the high output state if the detected voltage pin remains above the threshold voltage.

The RESET output will be driven low within 180 µs of $V_{DET}$ going below the RESET voltage threshold. The RESET output will remain valid for detected voltages greater than 1.2V overtemperature.

5.13 **TC1301A RESET Timing**

Figure 5-3 shows the RESET timing waveforms for the TC1301A. This diagram is also used to define the RESET active time-out period ($t_{RPU}$) and the $V_{DET}$ RESET delay time ($t_{RPD}$).

![FIGURE 5-3: TC1301A RESET Timing.](image)
5.14 TC1301B RESET Timing

The timing waveforms for the TC1301B RESET output are shown in Figure 5-4. Note that the RESET threshold input for the TC1301B is $V_{OUT1}$. The $V_{OUT1}$ to RESET threshold detector connection is made internal in the case of the TC1301B.

![TC1301B RESET Timing](image)

FIGURE 5-4: TC1301B RESET Timing.

5.15 Device Protection

5.15.1 OVERCURRENT LIMIT

In the event of a faulted output load, the maximum current the LDO output will permit to flow is limited internally for each of the TC1301A/B outputs. The peak current limit for $V_{OUT1}$ is typically 1.1A, while the peak current limit for $V_{OUT2}$ is typically 0.5A. During short-circuit operation, the average current is limited to 200 mA for $V_{OUT1}$ and 140 mA for $V_{OUT2}$. The $V_{DET}$ and RESET circuit will continue to operate in the event of an overcurrent on either output for the TC1301A. The voltage detect and RESET circuit will continue to operate in the event of an overcurrent on $V_{OUT1}$ (or $V_{OUT2}$) for the TC1301B. In the event of an overcurrent on $V_{OUT1}$, the RESET will detect the absence of $V_{OUT1}$.

5.15.2 OVERTEMPERATURE PROTECTION

If the internal power dissipation within the TC1301A/B is excessive due to a faulted load or higher-than-specified line voltage, an internal temperature-sensing element will prevent the junction temperature from exceeding approximately 150°C. If the junction temperature does reach 150°C, both outputs will be disabled until the junction temperature cools to approximately 140°C. The device will resume normal operation. If the internal power dissipation continues to be excessive, the device will again shut off. The $V_{DET}$ and RESET circuit will continue to operate normally during an overtemperature fault condition for both the TC1301A and TC1301B.
6.0 APPLICATION CIRCUITS/ISSUES

6.1 Typical Application
The TC1301A/B is used for applications that require the integration of two LDO’s and a microcontroller RESET.

![Typical Application Circuit TC1301A/B](image)

**FIGURE 6-1:** Typical Application Circuit TC1301A/B.

6.1.1 APPLICATION INPUT CONDITIONS
- Package Type = 3x3 DFN8
- Input Voltage Range = 2.7V to 4.2V
- \( V_{\text{IN}} \) maximum = 4.2V
- \( V_{\text{IN}} \) typical = 3.6V
- \( V_{\text{OUT1}} \) = 300 mA maximum
- \( V_{\text{OUT2}} \) = 150 mA maximum
- System RESET Load = 10 kΩ

6.2 Power Calculations
6.2.1 POWER DISSIPATION
The internal power dissipation within the TC1301A/B is a function of input voltage, output voltage, output current and quiescent current. The following equation can be used to calculate the internal power dissipation for each LDO.

**EQUATION 6-1:**

\[
P_{\text{LDO}} = (V_{\text{IN(MAX)}} - V_{\text{OUT(MIN)}}) \times I_{\text{OUT(MAX)}}
\]

Where:
- \( P_{\text{LDO}} \) = LDO Pass device internal power dissipation
- \( V_{\text{IN(MAX)}} \) = Maximum input voltage
- \( V_{\text{OUT(MIN)}} \) = LDO minimum output voltage

In addition to the LDO pass element power dissipation, there is power dissipation within the TC1301A/B as a result of quiescent or ground current. The power dissipation as a result of the ground current can be calculated using the following equation. The \( V_{\text{IN}} \) pin quiescent current and the \( V_{\text{DET}} \) pin current are both considered. The \( V_{\text{IN}} \) current is a result of LDO quiescent current, while the \( V_{\text{DET}} \) current is a result of the voltage detector current.

**EQUATION 6-2:**

\[
P_{\text{GND}} = V_{\text{IN(MAX)}} \times (I_{\text{IN}} + I_{\text{DET}})
\]

Where:
- \( P_{\text{GND}} \) = Total current in ground pin
- \( V_{\text{IN(MAX)}} \) = Maximum input voltage
- \( I_{\text{IN}} \) = Current flowing in the \( V_{\text{IN}} \) pin with no output current on either LDO output
- \( I_{\text{DET}} \) = Current in the \( V_{\text{DET}} \) pin with \( \text{RESET} \) loaded

The total power dissipated within the TC1301A/B is the sum of the power dissipated in both of the LDO’s and the \( P_{\text{GND}} \) term. Because of the CMOS construction, the typical \( I_{\text{GND}} \) for the TC1301A/B is 116 µA. Operating at a maximum of 4.2V results in a power dissipation of 0.5 milliWatts. For most applications, this is small compared to the LDO pass device power dissipation and can be neglected.

The maximum continuous operating junction temperature specified for the TC1301A/B is 125°C. To estimate the internal junction temperature of the TC1301A/B, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient \( (R_{\text{JA}}) \) of the device. The thermal resistance from junction to ambient for the 3x3 DFN8 pin package is estimated at 41°C/W.
EQUATION 6-3:

\[ T_{J(MAX)} = P_{TOTAL} \times R_{\theta JA} + T_{AMAX} \]

Where:
- \( T_{J(MAX)} \) = Maximum continuous junction temperature
- \( P_{TOTAL} \) = Total device power dissipation
- \( R_{\theta JA} \) = Thermal resistance from junction-to-ambient
- \( T_{AMAX} \) = Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction to ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the package maximum internal power dissipation.

EQUATION 6-4:

\[ P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX))})}{R_{\theta JA}} \]

Where:
- \( P_{D(MAX)} \) = Maximum device power dissipation
- \( T_{J(MAX)} \) = Maximum continuous junction temperature
- \( T_{A(MAX)} \) = Maximum ambient temperature
- \( R_{\theta JA} \) = Thermal resistance from junction-to-ambient

EQUATION 6-5:

\[ T_{J(RISE)} = P_{D(MAX)} \times R_{\theta JA} \]

Where:
- \( T_{J(RISE)} \) = Rise in device junction temperature over the ambient temperature
- \( P_{D(MAX)} \) = Maximum device power dissipation
- \( R_{\theta JA} \) = Thermal resistance from junction-to-ambient

EQUATION 6-6:

\[ T_{J} = T_{J(RISE)} + T_{A} \]

Where:
- \( T_{J} \) = Junction Temperature
- \( T_{J(RISE)} \) = Rise in device junction temperature over the ambient temperature
- \( T_{A} \) = Ambient Temperature

6.3 Typical Application

Internal power dissipation, junction temperature rise, junction temperature, and maximum power dissipation are calculated in the following example. The power dissipation as a result of ground current is small enough to be neglected.

6.3.1 POWER DISSIPATION EXAMPLE

Package

Package Type = 3x3 DFN8

Input Voltage

\( V_{IN} = 2.7 \text{V to } 4.2 \text{V} \)

LDO Output Voltages and Currents

\( V_{OUT1} = 2.8 \text{V} \)
\( I_{OUT1} = 300 \text{ mA} \)
\( V_{OUT2} = 1.8 \text{V} \)
\( I_{OUT2} = 150 \text{ mA} \)

Maximum Ambient Temperature

\( T_{A(MAX)} = 50^\circ \text{C} \)

Internal Power Dissipation

Internal power dissipation is the sum of the power dissipation for each LDO pass device.

\[ P_{LDO1(MAX)} = (V_{IN(MAX)} - V_{OUT1(MIN)}) \times I_{OUT1(MAX)} \]
\[ P_{LDO1} = (4.2 \text{V} - (0.975 \times 2.8 \text{V})) \times 300 \text{ mA} \]
\[ P_{LDO1} = 441.0 \text{milliWatts} \]
\[ P_{LDO2} = (4.2 \text{V} - (0.975 \times 1.8 \text{V})) \times 150 \text{ mA} \]
\[ P_{LDO2} = 366.8 \text{milliWatts} \]

\[ P_{TOTAL} = P_{LDO1} + P_{LDO2} \]
\[ P_{TOTAL} = 807.8 \text{milliWatts} \]

Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient (\( R_{\theta JA} \)) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface-mount packages. The EIA/JEDEC specification is JESD51-7, “High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages”. The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors such as copper area and thickness. Refer to AN792, “A Method To Determine How Much Power a SOT-23 Can Dissipate in Your Application” (DS00792), for more information regarding this subject.

\[ T_{J(RISE)} = P_{TOTAL} \times R_{\theta JA} \]
\[ 807.8 \text{milliWatts} \times 41.0^\circ \text{C/W} \]
\[ T_{J(RISE)} = 33.1^\circ \text{C} \]
Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below:

\[ T_J = T_{JRISE} + T_{A(MAX)} \]
\[ T_J = 83.1°C \]

Maximum Package Power Dissipation at 50°C Ambient Temperature

3X3DFN8 (41° C/W RθJA)

\[ P_D(MAX) = \frac{(125°C - 50°C)}{41° C/W} \]
\[ P_D(MAX) = 1.83 \text{ Watts} \]

MSOP8 (208° C/W RθJA)

\[ P_D(MAX) = \frac{(125°C - 50°C)}{208° C/W} \]
\[ P_D(MAX) = 0.360 \text{ Watts} \]

7.0 TYPICAL LAYOUT TC1301A

When doing the physical layout for the TC1301A/B, the highest priority is placing the input and output capacitors as close to the device pins as is practical. Figure 7-1 above represents a typical placement of the components when using SMT0805 capacitors.

A wiring example for the TC1301A is shown. The vias represent the connection to a ground plane that is below the wiring layer.

8.0 ADDITIONAL OUTPUT VOLTAGE AND THRESHOLD VOLTAGE OPTIONS

8.1 Output Voltage and Threshold Voltage Range

Table 8-1 describes the range of output voltage options available for the TC1301A/B. VOUT1 and VOUT2 can be factory preset from 1.5V to 3.3V in 100 mV increments. The VDET (TC1301A) or threshold voltage (TC1301B) can be preset from 2.2V to 3.2V in 10 mV increments.

<table>
<thead>
<tr>
<th>VOUT1</th>
<th>VOUT2</th>
<th>VDET Threshold</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5V to 3.3V</td>
<td>1.5V to 3.3V</td>
<td>2.2V to 3.2V</td>
</tr>
</tbody>
</table>

For a listing of TC1301A/B standard parts, refer to the Product Identification System on page 25.
## 9.0 PACKAGING INFORMATION

### 9.1 Package Marking Information

#### 8-Lead MSOP

Example:

<table>
<thead>
<tr>
<th>X1</th>
<th>Code V\text{OUT}\text{1}</th>
<th>Code V\text{OUT}\text{2}</th>
<th>Code V\text{OUT}\text{1}</th>
<th>Code V\text{OUT}\text{2}</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3.3V</td>
<td>J</td>
<td>2.4V</td>
<td>S</td>
</tr>
<tr>
<td>B</td>
<td>3.2V</td>
<td>K</td>
<td>2.3V</td>
<td>T</td>
</tr>
<tr>
<td>C</td>
<td>3.1V</td>
<td>L</td>
<td>2.2V</td>
<td>U</td>
</tr>
<tr>
<td>D</td>
<td>3.0V</td>
<td>M</td>
<td>2.1V</td>
<td>V</td>
</tr>
<tr>
<td>E</td>
<td>2.9V</td>
<td>N</td>
<td>2.0V</td>
<td>W</td>
</tr>
<tr>
<td>F</td>
<td>2.8V</td>
<td>O</td>
<td>1.9V</td>
<td>X</td>
</tr>
<tr>
<td>G</td>
<td>2.7V</td>
<td>P</td>
<td>1.8V</td>
<td>Y</td>
</tr>
<tr>
<td>H</td>
<td>2.6V</td>
<td>Q</td>
<td>1.7V</td>
<td>Z</td>
</tr>
<tr>
<td>I</td>
<td>2.5V</td>
<td>R</td>
<td>1.6V</td>
<td>—</td>
</tr>
</tbody>
</table>

#### 8-Lead DFN

Example:

<table>
<thead>
<tr>
<th>Xr</th>
<th>Code Voltage</th>
<th>Code Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>2.63V</td>
<td>J</td>
</tr>
<tr>
<td>B</td>
<td>2.2V</td>
<td>K</td>
</tr>
<tr>
<td>C</td>
<td>2.32V</td>
<td>L</td>
</tr>
<tr>
<td>D</td>
<td>2.5V</td>
<td>M</td>
</tr>
<tr>
<td>E</td>
<td>2.4V</td>
<td>N</td>
</tr>
<tr>
<td>F</td>
<td>2.6V</td>
<td>O</td>
</tr>
<tr>
<td>G</td>
<td>—</td>
<td>P</td>
</tr>
<tr>
<td>H</td>
<td>—</td>
<td>Q</td>
</tr>
<tr>
<td>I</td>
<td>—</td>
<td>R</td>
</tr>
</tbody>
</table>

#### Legend:

- XX...X Customer-specific information
- Y Year code (last digit of calendar year)
- YY Year code (last 2 digits of calendar year)
- WW Week code (week of January 1 is week ’01’)
- NNN Alphanumeric traceability code
- Pb-free JEDEC designator for Matte Tin (Sn)

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

For a listing of TC1301A/B standard parts, refer to the Product Identification System section on page 25.
8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B
8-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

### Units MILLIMETERS

<table>
<thead>
<tr>
<th>Dimension Limits</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Pins</td>
<td>N</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
<td>0.65 BSC</td>
<td></td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
<td>0.80</td>
<td>0.90</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
<td>0.00</td>
<td>0.02</td>
</tr>
<tr>
<td>Contact Thickness</td>
<td>A3</td>
<td>0.20 REF</td>
<td></td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
<td>3.00 BSC</td>
<td></td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E2</td>
<td>0.00</td>
<td>–</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
<td>3.00 BSC</td>
<td></td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D2</td>
<td>0.00</td>
<td>–</td>
</tr>
<tr>
<td>Contact Width</td>
<td>b</td>
<td>0.25</td>
<td>0.30</td>
</tr>
<tr>
<td>Contact Length</td>
<td>L</td>
<td>0.20</td>
<td>0.30</td>
</tr>
<tr>
<td>Contact-to-Exposed Pad</td>
<td>K</td>
<td>0.20</td>
<td>–</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-062B
APPENDIX A: REVISION HISTORY

Revision C (February 2008)
The following is the list of modifications.
1. Updated Section 9.0 “Packaging Information”.

Revision B (January 2005)
The following is the list of modifications.
1. Corrected the incorrect part number options shown on the Product Identification System page and changed the "standard" output voltage and reset voltage combinations.
2. Added Appendix A: Revision History.

Revision A (September 2003)
• Original data sheet release.
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>X-</th>
<th>Type A/B</th>
<th>VOUT1</th>
<th>VOUT2</th>
<th>Reset Voltage</th>
<th>Temp Range</th>
<th>Package</th>
<th>Tube or Tape &amp; Reel</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC1301</td>
<td>X</td>
<td>A/B</td>
<td>X</td>
<td>X</td>
<td>XX</td>
<td>XX</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Standard Configurations**: *

| Device: | TC1301A: Dual LDO with microcontroller RESET function and single shutdown input. | TC1301B: Dual LDO with microcontroller RESET function and dual shutdown inputs. |

<table>
<thead>
<tr>
<th>Standard Configurations: *</th>
<th>VOUT1/VOUT2/Reset</th>
<th>Configuration Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC1301A</td>
<td>3.3 / 3.0 / 2.63</td>
<td>ADA</td>
</tr>
<tr>
<td></td>
<td>3.3 / 1.8 / 2.63</td>
<td>APA</td>
</tr>
<tr>
<td></td>
<td>3.0 / 2.8 / 2.63</td>
<td>DAA</td>
</tr>
<tr>
<td></td>
<td>3.0 / 1.8 / 2.63</td>
<td>DPA</td>
</tr>
<tr>
<td></td>
<td>2.8 / 3.0 / 2.63</td>
<td>FDA</td>
</tr>
<tr>
<td></td>
<td>2.8 / 2.6 / 2.63</td>
<td>FHD</td>
</tr>
<tr>
<td></td>
<td>1.8 / 2.8 / 2.32</td>
<td>PFC</td>
</tr>
<tr>
<td></td>
<td>1.5 / 2.8 / 2.32</td>
<td>SFC</td>
</tr>
<tr>
<td></td>
<td>2.85 / 1.85 / 2.63</td>
<td>UWA</td>
</tr>
<tr>
<td>TC1301B</td>
<td>3.3 / 3.0 / 2.63</td>
<td>ADA</td>
</tr>
<tr>
<td></td>
<td>3.3 / 1.8 / 2.63</td>
<td>APA</td>
</tr>
<tr>
<td></td>
<td>3.0 / 2.8 / 2.63</td>
<td>DAA</td>
</tr>
<tr>
<td></td>
<td>3.0 / 1.8 / 2.63</td>
<td>DPA</td>
</tr>
<tr>
<td></td>
<td>2.8 / 3.0 / 2.63</td>
<td>FDA</td>
</tr>
<tr>
<td></td>
<td>2.8 / 2.6 / 2.63</td>
<td>FHD</td>
</tr>
<tr>
<td></td>
<td>2.7 / 2.8 / 2.5</td>
<td>GFD</td>
</tr>
<tr>
<td></td>
<td>2.7 / 3.0 / 2.50</td>
<td>GDD</td>
</tr>
<tr>
<td></td>
<td>2.85 / 1.85 / 2.63</td>
<td>UWA</td>
</tr>
</tbody>
</table>

* Contact Factory for Alternate Output Voltage and Reset Voltage Configurations.

Temperature Range: $V = -40^\circ C$ to $+125^\circ C$

Package: MF = Dual Flat, No Lead (3x3 mm body), 8-lead
         UA = Plastic Micro Small Outline (MSOP), 8-lead
Tube or Tape and Reel: Blank = Tube
                      TR = Tape and Reel

Examples:

- TC1301A-ADAVUA: 3.3, 3.0, 2.63, MSOP pkg.
- TC1301A-APAVMFTR: 3.3, 1.8, 2.63, 8LD DFN pkg.
- TC1301A-DFAVUATR: 3.0, 2.8, 2.63, MSOP pkg.
- TC1301A-DPAVMF: 3.0, 1.8, 2.63, 8LD DFN pkg.
- TC1301A-FDAVMF: 2.8, 3.0, 2.63, 8LD DFN pkg.
- TC1301A-FHAVMF: 2.8, 2.6, 2.63, DFN pkg.
- TC1301A-PFCVUA: 1.8, 2.8, 2.32, MSOP pkg.
- TC1301A-SFCVMFTR: 1.5, 2.8, 2.32, DFN pkg.
- TC1301A-UWAVUATR: 2.85, 1.85, 2.63, MSOP pkg.
- TC1301B-ADAVMF: 3.3, 3.0, 2.63, 8LD DFN pkg.
- TC1301B-APAVMFTR: 3.3, 1.8, 2.63, 8LD DFN pkg.
- TC1301B-DFAVUA: 3.0, 2.8, 2.63, MSOP pkg.
- TC1301B-DPAVUATR: 3.0, 1.8, 2.63, MSOP pkg.
- TC1301B-FDAVMF: 2.8, 3.0, 2.63, 8LD DFN pkg.
- TC1301B-FHAVMF: 2.8, 2.6, 2.63, 8LD DFN pkg.
- TC1301B-GDDVUA: 2.7, 3.0, 2.50, MSOP pkg.
- TC1301B-GFDVMF: 2.7, 2.8, 2.5, 8LD DFN pkg.
- TC1301B-UWAVUATR: 2.85, 1.85, 2.63, MSOP pkg.
Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademark

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOG, KEELOG logo, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, rfPIC and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Linear Active Thermistor, MXDEV, MXLAB, SSEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICWorks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, In-Circuit Serial Programming, ICSP, ICEPIC, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, PICkit, PICDEM, PICDEM.net, PicTail, PIC26 logo, PowerCal, PowerInfo, PowerMate, PowerTool, REAL ICE, rFLAB, Select Mode, Total Endurance, UNI/O, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.
© 2008, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.