MCP6541/1R/1U/2/3/4
Push-Pull Output Sub-Microamp Comparators

Features:
- Low Quiescent Current: 600 nA/Comparator (typ.)
- Rail-to-Rail Input: V_{SS} - 0.3V to V_{DD} + 0.3V
- CMOS/TTL-Compatible Output
- Propagation Delay: 4 µs (typical, 100 mV Overdrive)
- Wide Supply Voltage Range: 1.6V to 5.5V
- Available in Single, Dual and Quad
- Single Available in SOT-23-5, SC-70-5 Packages
- Chip Select (CS) with MCP6543
- Low Switching Current
- Internal Hysteresis: 3.3 mV (typ.)
- Temperature Ranges:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

Typical Applications:
- Laptop Computers
- Mobile Phones
- Metering Systems
- Hand-held Electronics
- RC Timers
- Alarm and Monitoring Circuits
- Windowed Comparators
- Multivibrators

Description:
The Microchip Technology Inc. MCP6541/1R/1U/2/3/4 family of comparators is offered in single (MCP6541, MCP6541R, MCP6541U), single with Chip Select (CS) (MCP6543), dual (MCP6542) and quad (MCP6544) configurations. The outputs are push-pull (CMOS/TTL-compatible) and are capable of driving heavy DC or capacitive loads.

These comparators are optimized for low-power, single-supply operation with greater than rail-to-rail input operation. The push-pull output of the MCP6541/1R/1U/2/3/4 family supports rail-to-rail output swing and interfaces with TTL/CMOS logic. The internal input hysteresis eliminates output switching due to internal input noise voltage, reducing current draw. The output limits supply current surges and dynamic power consumption while switching. This product family operates with a single-supply voltage as low as 1.6V and draws less than 1 µA/comparator of quiescent current.

The related MCP6546/7/8/9 family of comparators from Microchip has an open-drain output. Used with a pull-up resistor, these devices can be used as level-shifters for any desired voltage up to 10V and in wired-OR logic.

* SC-70-5 E-Temp parts not available at this release of the data sheet.

MCP6541U SOT-23-5 is E-Temp only.

Related Devices:
- Open-Drain Output: MCP6546/7/8/9

Package Types:

<table>
<thead>
<tr>
<th>MCP6541</th>
<th>MCP6541R</th>
<th>MCP6542</th>
<th>MCP6544</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDIP, SOIC, MSOP</td>
<td>PDIP, SOIC, SOT-23-5</td>
<td>PDIP, SOIC, MSOP</td>
<td>PDIP, SOIC, TSSOP</td>
</tr>
<tr>
<td>NC 1</td>
<td>OUT 1</td>
<td>OUTA 1</td>
<td>OUTD 1</td>
</tr>
<tr>
<td>V_{IN}^- 2</td>
<td>V_{DD} 7</td>
<td>V_{IN}^- 2</td>
<td>V_{IND}^- 4</td>
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<tr>
<td>V_{INA}^+ 3</td>
<td>V_{IN}^- 4</td>
<td>V_{IN}^- 2</td>
<td>V_{IND}^- 2</td>
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<tr>
<td>V_{SS} 4</td>
<td>OUT 3</td>
<td>OUTB 4</td>
<td>V_{SS} 4</td>
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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

- $V_{DD} - V_{SS}$ ................................................................. 7.0V
- Current at Analog Input Pin ($V_{IN+}$, $V_{IN-}$) .................. ±2 mA
- Analog Input ($V_{IN}$) †† .......................... $V_{SS} - 1.0\text{V}$ to $V_{DD} + 1.0\text{V}$
- All other Inputs and Outputs........... $V_{SS} - 0.3\text{V}$ to $V_{DD} + 0.3\text{V}$
- Difference Input Voltage ................................. $|V_{DD} - V_{SS}|$
- Output Short-Circuit Current ............................ Continuous
- Current at Input Pins ................................................. ±2 mA
- Current at Output and Supply Pins ................. ±30 mA
- Storage Temperature ................................. -65°C to +150°C
- Maximum Junction Temperature ($T_{J}$)................. +150°C
- ESD Protection on all Pins (HBM:MM) ............. 4 kV, 400V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See Section 4.1.2 “Input Voltage and Current Limits”

DC CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated, $V_{DD} = +1.6\text{V}$ to +5.5V, $V_{SS} = \text{GND}$, $T_{A} = +25°C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = V_{SS}$, and $R_L = 100\ \text{k\Omega}$ to $V_{DD}/2$ (Refer to Figure 1-3).

<table>
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<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
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<td>Supply Voltage</td>
<td>$V_{DD}$</td>
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<td>—</td>
<td>5.5</td>
<td>V</td>
<td>I_{OUT} = 0</td>
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<td>Quiescent Current per comparator</td>
<td>$I_Q$</td>
<td>0.3</td>
<td>0.6</td>
<td>1.0</td>
<td>μA</td>
<td>$I_{OUT} = 0$</td>
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<td>Input</td>
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<td>Input Voltage Range</td>
<td>$V_{CMR}$</td>
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<td>—</td>
<td>—</td>
<td>V</td>
<td>$V_{SS} - 0.3$</td>
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<td>Common Mode Rejection Ratio</td>
<td>$CMRR$</td>
<td>55</td>
<td>70</td>
<td>—</td>
<td>dB</td>
<td>$V_{DD} = 5\text{V}, V_{CM} = -0.3\text{V}$ to +5.3V</td>
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<td>Common Mode Rejection Ratio</td>
<td>$CMRR$</td>
<td>50</td>
<td>65</td>
<td>—</td>
<td>dB</td>
<td>$V_{DD} = 5\text{V}, V_{CM} = +2.5\text{V}$ to +5.3V</td>
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<td>Common Mode Rejection Ratio</td>
<td>$CMRR$</td>
<td>55</td>
<td>70</td>
<td>—</td>
<td>dB</td>
<td>$V_{DD} = 5\text{V}, V_{CM} = -0.3\text{V}$ to +2.5V</td>
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<td>Power Supply Rejection Ratio</td>
<td>$PSRR$</td>
<td>63</td>
<td>80</td>
<td>—</td>
<td>dB</td>
<td>$V_{CM} = V_{SS}$</td>
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<tr>
<td>Input Offset Voltage</td>
<td>$V_{OS}$</td>
<td>-1.7</td>
<td>±1.5</td>
<td>+7.0</td>
<td>mV</td>
<td>$V_{CM} = V_{SS}$ (Note 1)</td>
</tr>
<tr>
<td>Drift with Temperature</td>
<td>$\Delta V_{OS}/\Delta T_A$</td>
<td>—</td>
<td>±3</td>
<td>—</td>
<td>μV/°C</td>
<td>$T_A = -40°C$ to +125°C, $V_{CM} = V_{SS}$</td>
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<tr>
<td>Input Hysteresis Voltage</td>
<td>$V_{HYST}$</td>
<td>1.5</td>
<td>3.3</td>
<td>6.5</td>
<td>mV</td>
<td>$V_{CM} = V_{SS}$ (Note 1)</td>
</tr>
<tr>
<td>Linear Temp. Co. (Note 2)</td>
<td>$TC_1$</td>
<td>—</td>
<td>6.7</td>
<td>—</td>
<td>μV/°C</td>
<td>$T_A = -40°C$ to +125°C, $V_{CM} = V_{SS}$</td>
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<tr>
<td>Quadratic Temp. Co. (Note 2)</td>
<td>$TC_2$</td>
<td>—</td>
<td>-0.035</td>
<td>—</td>
<td>μV/°C²</td>
<td>$T_A = -40°C$ to +125°C, $V_{CM} = V_{SS}$</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>$I_B$</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>pA</td>
<td>$V_{CM} = V_{SS}$</td>
</tr>
<tr>
<td>At Temperature (I-Temp parts)</td>
<td>$I_B$</td>
<td>—</td>
<td>25</td>
<td>100</td>
<td>pA</td>
<td>$T_A = +85°C, V_{CM} = V_{SS}$ (Note 3)</td>
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<tr>
<td>At Temperature (E-Temp parts)</td>
<td>$I_B$</td>
<td>—</td>
<td>1200</td>
<td>5000</td>
<td>pA</td>
<td>$T_A = +125°C, V_{CM} = V_{SS}$ (Note 3)</td>
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<tr>
<td>Input Offset Current</td>
<td>$I_{OS}$</td>
<td>—</td>
<td>±1</td>
<td>—</td>
<td>pA</td>
<td>$V_{CM} = V_{SS}$</td>
</tr>
<tr>
<td>Common Mode Input Impedance</td>
<td>$Z_{CM}$</td>
<td>—</td>
<td>$10^{13}$</td>
<td>4</td>
<td>Ω</td>
<td>$</td>
</tr>
<tr>
<td>Differential Input Impedance</td>
<td>$Z_{DIFF}$</td>
<td>—</td>
<td>$10^{13}$</td>
<td>2</td>
<td>Ω</td>
<td>$</td>
</tr>
</tbody>
</table>

**Note 1:** The input offset voltage is the center (average) of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

**Note 2:** $V_{HYST}$ at different temperatures is estimated using $V_{HYST}(T_A) = V_{HYST} + (T_A - 25°C) TC_1 + (T_A - 25°C)^2 TC_2$.

**Note 3:** Input bias current at temperature is not tested for SC-70-5 package.

**Note 4:** Limit the output current to Absolute Maximum Rating of 30 mA.
## DC CHARACTERISTICS (CONTINUED)

### Electrical Specifications:
Unless otherwise indicated, \( V_{DD} = +1.6V \) to +5.5V, \( V_{SS} = GND, \) \( T_A = +25^\circ C, \) \( V_{IN+} = V_{DD}/2, \) \( V_{IN-} = V_{SS}, \) and \( R_L = 100 \, k\Omega \) to \( V_{DD}/2 \) (Refer to Figure 1-3).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-Level Output Voltage</td>
<td>( V_{OH} )</td>
<td>( V_{DD} - 0.2 )</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>( I_{OUT} = -2 , mA, ) ( V_{DD} = 5V )</td>
</tr>
<tr>
<td>Low-Level Output Voltage</td>
<td>( V_{OL} )</td>
<td>—</td>
<td>—</td>
<td>( V_{SS} + 0.2 )</td>
<td>V</td>
<td>( I_{OUT} = 2 , mA, ) ( V_{DD} = 5V )</td>
</tr>
<tr>
<td>Short-Circuit Current</td>
<td>( I_{SC} )</td>
<td>—</td>
<td>( -2.5, +1.5 )</td>
<td>—</td>
<td>mA</td>
<td>( V_{DD} = 1.6V ) (Note 4)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>( I_{SC} )</td>
<td>±30</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Note 1:** The input offset voltage is the center (average) of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

**Note 2:** \( V_{HYST} \) at different temperatures is estimated using \( V_{HYST} (T_A) = V_{HYST} + (T_A - 25^\circ C) \, TC_1 + (T_A - 25^\circ C)^2 \, TC_2. \)

**Note 3:** Input bias current at temperature is not tested for SC-70-5 package.

**Note 4:** Limit the output current to Absolute Maximum Rating of 30 mA.

## AC CHARACTERISTICS

### Electrical Specifications:
Unless otherwise indicated, \( V_{DD} = +1.6V \) to +5.5V, \( V_{SS} = GND, \) \( T_A = +25^\circ C, \) \( V_{IN+} = V_{DD}/2, \) Step = 200 mV, Overdrive = 100 mV, and \( C_L = 36 \, pF \) (Refer to Figure 1-2 and Figure 1-3).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
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<tbody>
<tr>
<td>Rise Time</td>
<td>( t_R )</td>
<td>—</td>
<td>0.85</td>
<td>—</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td>Fall Time</td>
<td>( t_F )</td>
<td>—</td>
<td>0.85</td>
<td>—</td>
<td>( \mu s )</td>
<td></td>
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<tr>
<td>Propagation Delay (High-to-Low)</td>
<td>( t_{PHL} )</td>
<td>—</td>
<td>4</td>
<td>8</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td>Propagation Delay (Low-to-High)</td>
<td>( t_{PLH} )</td>
<td>—</td>
<td>4</td>
<td>8</td>
<td>( \mu s )</td>
<td></td>
</tr>
<tr>
<td>Propagation Delay Skew</td>
<td>( t_{PDS} )</td>
<td>—</td>
<td>±0.2</td>
<td>—</td>
<td>( \mu s )</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>Maximum Toggle Frequency</td>
<td>( f_{MAX} )</td>
<td>—</td>
<td>160</td>
<td>—</td>
<td>kHz</td>
<td>( V_{DD} = 1.6V )</td>
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<td></td>
<td>( f_{MAX} )</td>
<td>—</td>
<td>120</td>
<td>—</td>
<td>kHz</td>
<td>( V_{DD} = 5.5V )</td>
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<tr>
<td>Input Noise Voltage</td>
<td>( E_{ni} )</td>
<td>—</td>
<td>200</td>
<td>—</td>
<td>( \mu V_{P-P} )</td>
<td>10 Hz to 100 kHz</td>
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</table>

**Note 1:** Propagation Delay Skew is defined as: \( t_{PDS} = t_{PLH} - t_{PHL}. \)
## MCP6543 CHIP SELECT (CS) CHARACTERISTICS

### Electrical Specifications

Unless otherwise indicated, $\text{V}_{\text{DD}} = +1.6\text{V}$ to $+5.5\text{V}$, $\text{V}_{\text{SS}} = \text{GND}$, $\text{T}_\text{A} = +25\text{°C}$, $\text{V}_{\text{IN}^+} = \text{V}_{\text{DD}}/2$, $\text{V}_{\text{IN}^-} = \text{V}_{\text{SS}}$, and $C_L = 36 \text{ pF}$ (Refer to Figures 1-1 and 1-3).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
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<tr>
<td><strong>CS Low Specifications</strong></td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>CS Logic Threshold, Low</td>
<td>$V_{\text{IL}}$</td>
<td>$V_{\text{SS}}$</td>
<td>—</td>
<td>0.2 $V_{\text{DD}}$</td>
<td>V</td>
<td>$\text{CS} = V_{\text{SS}}$</td>
</tr>
<tr>
<td>CS Input Current, Low</td>
<td>$I_{\text{CSL}}$</td>
<td>—</td>
<td>5.0</td>
<td>—</td>
<td>pA</td>
<td>$\text{CS} = V_{\text{SS}}$</td>
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<td><strong>CS High Specifications</strong></td>
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<tr>
<td>CS Logic Threshold, High</td>
<td>$V_{\text{IH}}$</td>
<td>0.8 $V_{\text{DD}}$</td>
<td>—</td>
<td>$V_{\text{DD}}$</td>
<td>V</td>
<td>$\text{CS} = V_{\text{DD}}$</td>
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<tr>
<td>CS Input Current, High</td>
<td>$I_{\text{CSH}}$</td>
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<td>1</td>
<td>—</td>
<td>pA</td>
<td>$\text{CS} = V_{\text{DD}}$</td>
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<td>CS Input High, $V_{\text{DD}}$ Current</td>
<td>$I_{\text{OD}}$</td>
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<td>18</td>
<td>—</td>
<td>pA</td>
<td>$\text{CS} = V_{\text{DD}}$</td>
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<td>CS Input High, GND Current</td>
<td>$I_{\text{OS}}$</td>
<td>—</td>
<td>—20</td>
<td>—</td>
<td>pA</td>
<td>$\text{CS} = V_{\text{DD}}$</td>
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<tr>
<td>Comparator Output Leakage</td>
<td>$I_{\text{O(LEAK)}}$</td>
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<td>1</td>
<td>—</td>
<td>pA</td>
<td>$V_{\text{OUT}} = V_{\text{OD}}, \text{CS} = V_{\text{DD}}$</td>
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<td><strong>CS Dynamic Specifications</strong></td>
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<td>CS Low to Comparator Output Low Turn-on Time</td>
<td>$t_{\text{ON}}$</td>
<td>—</td>
<td>2</td>
<td>50</td>
<td>ms</td>
<td>$\text{CS} = 0.2 \text{V}<em>{\text{DD}}$ to $V</em>{\text{OUT}} = \text{V}<em>{\text{OD}}/2$, $\text{V}</em>{\text{IN}^-} = \text{V}_{\text{DD}}$</td>
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<tr>
<td>CS High to Comparator Output High Z Turn-off Time</td>
<td>$t_{\text{OFF}}$</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>$\mu$s</td>
<td>$\text{CS} = 0.8 \text{V}<em>{\text{DD}}$ to $V</em>{\text{OUT}} = \text{V}<em>{\text{OD}}/2$, $\text{V}</em>{\text{IN}^-} = \text{V}_{\text{OD}}$</td>
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<td>CS Hysteresis</td>
<td>$V_{\text{CS,HYS}}$</td>
<td>—</td>
<td>0.6</td>
<td>—</td>
<td>V</td>
<td>$\text{V}_{\text{DD}} = 5\text{V}$</td>
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**FIGURE 1-1:** Timing Diagram for the CS Pin on the MCP6543.

**FIGURE 1-2:** Propagation Delay Timing Diagram.
TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{DD} = +1.6V$ to $+5.5V$ and $V_{SS} = GND$.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
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<td>Specified Temperature Range</td>
<td>$T_A$</td>
<td>-40</td>
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<td>+85</td>
<td>°C</td>
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<td>Operating Temperature Range</td>
<td>$T_A$</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
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<td>+150</td>
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<td>Thermal Resistance, 5L-SC-70</td>
<td>$\theta_{JA}$</td>
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<td>331</td>
<td>—</td>
<td>°C/W</td>
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<td>Thermal Resistance, 5L-SOT-23</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>220.7</td>
<td>—</td>
<td>°C/W</td>
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<tr>
<td>Thermal Resistance, 8L-PDIP</td>
<td>$\theta_{JA}$</td>
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<td>89.3</td>
<td>—</td>
<td>°C/W</td>
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<td>Thermal Resistance, 8L-SOIC</td>
<td>$\theta_{JA}$</td>
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<td>149.5</td>
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<td>°C/W</td>
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<td>Thermal Resistance, 8L-MSOP</td>
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<td>211</td>
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<td>°C/W</td>
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<td>Thermal Resistance, 14L-PDIP</td>
<td>$\theta_{JA}$</td>
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<td>—</td>
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<td>Thermal Resistance, 14L-SOIC</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>95.3</td>
<td>—</td>
<td>°C/W</td>
<td></td>
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<tr>
<td>Thermal Resistance, 14L-TSSOP</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

Note: The MCP6541/1R/1U/2/3/4 I-Temp parts operate over this extended temperature range, but with reduced performance. In any case, the Junction Temperature ($T_J$) must not exceed the Absolute Maximum specification of +150°C.

1.1 Test Circuit Configuration

This test circuit configuration is used to determine the AC and DC specifications.

**FIGURE 1-3:** AC and DC Test Circuit for the Push-Pull Output Comparators.
2.0  TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, \( V_{\text{DD}} = +1.6 \text{V to } +5.5 \text{V} \), \( V_{\text{SS}} = \text{GND} \), \( T_A = +25^\circ \text{C} \), \( V_{\text{IN+}} = V_{\text{DD}}/2 \), \( V_{\text{IN–}} = \text{GND} \), \( R_L = 100 \text{k}\Omega \) to \( V_{\text{DD}}/2 \), and \( C_L = 36 \text{ pF} \).

**FIGURE 2-1:** Input Offset Voltage at \( V_{\text{CM}} = V_{\text{SS}} \).

**FIGURE 2-2:** Input Offset Voltage Drift at \( V_{\text{CM}} = V_{\text{SS}} \).

**FIGURE 2-3:** The MCP6541/1R/1U/2/3/4 Comparators Show No Phase Reversal.

**FIGURE 2-4:** Input Hysteresis Voltage at \( V_{\text{CM}} = V_{\text{SS}} \).

**FIGURE 2-5:** Input Hysteresis Voltage Linear Temp. Co. (TC1) at \( V_{\text{CM}} = V_{\text{SS}} \).

**FIGURE 2-6:** Input Hysteresis Voltage Quadratic Temp. Co. (TC2) at \( V_{\text{CM}} = V_{\text{SS}} \).
Note: Unless otherwise indicated, $V_{DD} = +1.6V$ to +5.5V, $V_{SS} = GND$, $T_A = +25°C$, $V_{IN^+} = V_{DD}/2$, $V_{IN^-} = GND$, $R_L = 100 \, k\Omega$ to $V_{DD}/2$, and $C_L = 36 \, pF$.

**FIGURE 2-7:** Input Offset Voltage vs. Ambient Temperature at $V_{CM} = V_{SS}$.

**FIGURE 2-8:** Input Offset Voltage vs. Common Mode Input Voltage at $V_{DD} = 1.6V$.

**FIGURE 2-9:** Input Offset Voltage vs. Common Mode Input Voltage at $V_{DD} = 5.5V$.

**FIGURE 2-10:** Input Hysteresis Voltage vs. Ambient Temperature at $V_{CM} = V_{SS}$.

**FIGURE 2-11:** Input Hysteresis Voltage vs. Common Mode Input Voltage at $V_{DD} = 1.6V$.

**FIGURE 2-12:** Input Hysteresis Voltage vs. Common Mode Input Voltage at $V_{DD} = 5.5V$. 
**MCP6541/1R/1U/2/3/4**

**Note:** Unless otherwise indicated, $V_{DD} = +1.6V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25°C$, $V_{IN+} = V_{DD}/2$, $V_{IN-} = GND$, $R_L = 100 \, k\Omega$ to $V_{DD}/2$, and $C_L = 36 \, pF$.

**FIGURE 2-13:** CMRR, PSRR vs. Ambient Temperature.

**FIGURE 2-14:** Input Bias Current, Input Offset Current vs. Ambient Temperature.

**FIGURE 2-15:** Quiescent Current vs. Common Mode Input Voltage at $V_{DD} = 1.6V$.

**FIGURE 2-16:** Input Bias Current, Input Offset Current vs. Common Mode Input Voltage.

**FIGURE 2-17:** Quiescent Current vs. Power Supply Voltage.

**FIGURE 2-18:** Quiescent Current vs. Common Mode Input Voltage at $V_{DD} = 5.5V$. 
Note: Unless otherwise indicated, \( V_{DD} = +1.6V \) to +5.5V, \( V_{SS} = \text{GND} \), \( T_A = +25^\circ C \), \( V_{IN^+} = V_{DD}/2 \), \( V_{IN^-} = \text{GND} \), \( R_L = 100 \, \text{k}\Omega \) to \( V_{DD}/2 \), and \( C_L = 36 \, \text{pF} \).

**FIGURE 2-19:** Supply Current vs. Toggle Frequency.

**FIGURE 2-20:** Output Voltage Headroom vs. Output Current at \( V_{DD} = 1.6V \).

**FIGURE 2-21:** High-to-Low Propagation Delay.

**FIGURE 2-22:** Output Short Circuit Current Magnitude vs. Power Supply Voltage.

**FIGURE 2-23:** Output Voltage Headroom vs. Output Current at \( V_{DD} = 5.5V \).

**FIGURE 2-24:** Low-to-High Propagation Delay.
Note: Unless otherwise indicated, $V_{DD} = +1.6V$ to $+5.5V$, $V_{SS} = GND$, $T_A = +25^\circ C$, $V_{IN^+} = V_{DD}/2$, $V_{IN^-} = GND$, $R_L = 100 \, k\Omega$ to $V_{DD}/2$, and $C_L = 36 \, pF$.

**FIGURE 2-25:** Propagation Delay Skew.

**FIGURE 2-26:** Propagation Delay vs. Power Supply Voltage.

**FIGURE 2-27:** Propagation Delay vs. Common Mode Input Voltage at $V_{DD} = 1.6V$.

**FIGURE 2-28:** Propagation Delay vs. Ambient Temperature.

**FIGURE 2-29:** Propagation Delay vs. Input Overdrive.

**FIGURE 2-30:** Propagation Delay vs. Common Mode Input Voltage at $V_{DD} = 5.5V$. 
Note: Unless otherwise indicated, $V_{DD} = +1.6$V to $+5.5$V, $V_{SS} = \text{GND}$, $T_A = +25^\circ$C, $V_{IN^+} = V_{DD}/2$, $V_{IN^-} = \text{GND}$, $R_L = 100 \text{ k}\Omega$ to $V_{DD}/2$, and $C_L = 36 \text{ pF}$.

**FIGURE 2-31:** Propagation Delay vs. Load Capacitance.

**FIGURE 2-32:** Supply Current (shoot through current) vs. Chip Select (CS) Voltage at $V_{DD} = 1.6$V (MCP6543 only).

**FIGURE 2-33:** Supply Current (charging current) vs. Chip Select (CS) pulse at $V_{DD} = 1.6$V (MCP6543 only).

**FIGURE 2-34:** Chip Select (CS) Step Response (MCP6543 only).

**FIGURE 2-35:** Supply Current (shoot through current) vs. Chip Select (CS) Voltage at $V_{DD} = 5.5$V (MCP6543 only).

**FIGURE 2-36:** Supply Current (charging current) vs. Chip Select (CS) pulse at $V_{DD} = 5.5$V (MCP6543 only).
Note: Unless otherwise indicated, \( V_{DD} = +1.6 \)V to +5.5V, \( V_{SS} = GND \), \( T_A = +25^\circ C \), \( V_{IN^+} = V_{DD}/2 \), \( V_{IN^-} = GND \), \( R_L = 100 \Omega \) to \( V_{DD}/2 \), and \( C_L = 36 \text{ pF} \).

**FIGURE 2-37:** Input Bias Current vs. Input Voltage.
3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

### TABLE 3-1: PIN FUNCTION TABLE

<table>
<thead>
<tr>
<th>MCP6541 Symbol</th>
<th>Description</th>
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<tbody>
<tr>
<td>MCP6541</td>
<td>VDD Positive Power Supply</td>
</tr>
<tr>
<td>PDIP, SOIC, MSOP</td>
<td>MCP6541R</td>
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<td>1, 5, 8</td>
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</tr>
</tbody>
</table>

3.1 Analog Inputs

The comparator non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.2 CS Digital Input

This is a CMOS, Schmitt-triggered input that places the part into a low-power mode of operation.

3.3 Digital Outputs

The comparator outputs are CMOS, push-pull digital outputs. They are designed to be compatible with CMOS and TTL logic and are capable of driving heavy DC or capacitive loads.

3.4 Power Supply (VSS and VDD)

The positive power supply pin (VDD) is 1.6V to 5.5V higher than the negative power supply pin (VSS). For normal operation, the other pins are at voltages between VSS and VDD.

Typically, these parts are used in a single (positive) supply configuration. In this case, VSS is connected to ground and VDD is connected to the supply. VDD will need a local bypass capacitor (typically 0.01 µF to 0.1 µF) within 2 mm of the VDD pin. These can share a bulk capacitor with nearby analog parts (within 100 mm), but it is not required.
4.0 APPLICATIONS INFORMATION

The MCP6541/1R/1U/2/3/4 family of push-pull output comparators are fabricated on Microchip’s state-of-the-art CMOS process. They are suitable for a wide range of applications requiring very low-power consumption.

4.1 Comparator Inputs

4.1.1 PHASE REVERSAL

The MCP6541/1R/1U/2/3/4 comparator family uses CMOS transistors at the input. They are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-3 shows an input voltage exceeding both supplies with no resulting phase inversion.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current (IB). The input ESD diodes clamp the inputs when they try to go more than one diode drop below VSS. They also clamp any voltages that go too far above VDD; their breakdown voltage is high enough to allow normal operation, and low enough to bypass ESD events within the specified limits.

![Fig 4-1](image)

FIGURE 4-1: Simplified Analog Input ESD Structures.

In order to prevent damage and/or improper operation of these amplifiers, the circuits they are in must limit the currents (and voltages) at the VIN+ and VIN– pins (see Absolute Maximum Ratings † at the beginning of Section 1.0 “Electrical Characteristics”). Figure 4-3 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (VIN+ and VIN–) from going too far below ground, and the resistors R1 and R2, limit the possible current drawn out of the input pin. Diodes D1 and D2 prevent the input pin (VIN+ and VIN–) from going too far above VDD. When implemented as shown, resistors R1 and R2 also limit the current through D1 and D2.

![Fig 4-2](image)

FIGURE 4-2: Protecting the Analog Inputs.

It is also possible to connect the diodes to the left of the resistors R1 and R2. In this case, the currents through the diodes D1 and D2 need to be limited by some other mechanism. The resistor then serves as in-rush current limiter; the DC current into the input pins (VIN+ and VIN–) should be very small.

A significant amount of current can flow out of the inputs when the common mode voltage (VCM) is below ground (VSS); see Figure 2-37. Applications that are high-impedance may need to limit the usable voltage range.

4.1.3 NORMAL OPERATION

The input stage of this family of devices uses two differential input stages in parallel: one operates at low input voltages and the other at high input voltages. With this topology, the input voltage is 0.3V above VDD and 0.3V below VSS. Therefore, the input offset voltage is measured at both VSS - 0.3V and VDD + 0.3V to ensure proper operation.

The MCP6541/1R/1U/2/3/4 family has internally-set hysteresis that is small enough to maintain input offset accuracy (<7 mV) and large enough to eliminate output chattering caused by the comparator’s own input noise voltage (200 μVp-p). Figure 4-3 depicts this behavior.
4.2 Push-Pull Output

The push-pull output is designed to be compatible with CMOS and TTL logic, while the output transistors are configured to give rail-to-rail output performance. They are driven with circuitry that minimizes any switching current (shoot-through current from supply-to-supply) when the output is transitioned from high-to-low, or from low-to-high (see Figures 2-15, 2-18, and 2-32 — 2-36 for more information).

4.3 MCP6543 Chip Select (CS)

The MCP6543 is a single comparator with Chip Select (CS). When CS is pulled high, the total current consumption drops to 20 pA (typ.); 1 pA (typ.) flows through the CS pin, 1 pA (typ.) flows through the output pin and 18 pA (typ.) flows through the VDD pin, as shown in Figure 1-1. When this happens, the comparator output is put into a high-impedance state. By pulling CS low, the comparator is enabled. If the CS pin is left floating, the comparator will not operate properly. Figure 1-1 shows the output voltage and supply current response to a CS pulse.

The internal CS circuitry is designed to minimize glitches when cycling the CS pin. This helps conserve power, which is especially important in battery-powered applications.

4.4 Externally Set Hysteresis

Greater flexibility in selecting hysteresis (or input trip points) is achieved by using external resistors.

Input offset voltage (V_{OS}) is the center (average) of the (input-referred) low-high and high-low trip points. Input hysteresis voltage (V_{HYST}) is the difference between the same trip points. Hysteresis reduces output chattering when one input is slowly moving past the other and thus reduces dynamic supply current. It also helps in systems where it is best not to cycle between states too frequently (e.g., air conditioner thermostatic control).

4.4.1 NON-INVERTING CIRCUIT

Figure 4-4 shows a non-inverting circuit for single-supply applications using just two resistors. The resulting hysteresis diagram is shown in Figure 4-5.

The trip points for Figures 4-4 and 4-5 are:

\[
\begin{align*}
V_{THL} &= V_{REF} \left(1 + \frac{R_1}{R_F}\right) - V_{OL} \left(\frac{R_1}{R_F}\right) \\
V_{TILH} &= V_{REF} \left(1 + \frac{R_1}{R_F}\right) - V_{OH} \left(\frac{R_1}{R_F}\right)
\end{align*}
\]

Where:
- \(V_{THL}\) = trip voltage from low-to-high
- \(V_{TILH}\) = trip voltage from high-to-low
4.4.2 INVERTING CIRCUIT

Figure 4-6 shows an inverting circuit for single-supply using three resistors. The resulting hysteresis diagram is shown in Figure 4-7.

**Figure 4-6:** Inverting Circuit With Hysteresis.

In order to determine the trip voltages (V\text{THL} and V\text{TLH}) for the circuit shown in Figure 4-6, R\textsubscript{2} and R\textsubscript{3} can be simplified to the Thevenin equivalent circuit with respect to V\textsubscript{DD}, as shown in Figure 4-8.

**Figure 4-7:** Hysteresis Diagram for the Inverting Circuit.

**Figure 4-8:** Thevenin Equivalent Circuit.

Using this simplified circuit, the trip voltage can be calculated using the following equation:

\begin{equation}
V_{\text{TLH}} = \frac{R_{23}}{R_{23} + R_{F}} V_{\text{DD}} + V_{23}
\end{equation}

\begin{equation}
V_{\text{THL}} = \frac{R_{23}}{R_{23} + R_{F}} V_{\text{DD}} + V_{23}
\end{equation}

V\text{TLH} = trip voltage from low-to-high
V\text{THL} = trip voltage from high-to-low

Figure 2-20 and Figure 2-23 can be used to determine typical values for V\text{OH} and V\text{OL}.

4.5 Bypass Capacitors

With this family of comparators, the power supply pin (V\text{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good edge rate performance.

4.6 Capacitive Loads

Reasonable capacitive loads (e.g., logic gates) have little impact on propagation delay (see Figure 2-31). The supply current increases with increasing toggle frequency (Figure 2-19), especially with higher capacitive loads.

4.7 Battery Life

In order to maximize battery life in portable applications, use large resistors and small capacitive loads. Avoid toggling the output more than necessary. Do not use Chip Select (CS) frequently to conserve start-up power. Capacitive loads will draw additional power at start-up.

4.8 PCB Surface Leakage

In applications where low input bias current is critical, PCB (Printed Circuit Board) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is 10\textsuperscript{12} Ω. A 5V difference would cause 5 pA of current to flow. This is greater than the MCP6541/1R/1U/2/3/4 family's bias current at 25°C (1 pA, typ.).
The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-9.

![Guard Ring Layout](image)

**FIGURE 4-9:** Example Guard Ring Layout for Inverting Circuit.

1. Inverting Configuration (Figures 4-6 and 4-9):
   a. Connect the guard ring to the non-inverting input pin (V\text{IN}^+). This biases the guard ring to the same reference voltage as the comparator (e.g., V\text{DD}/2 or ground).
   b. Connect the inverting pin (V\text{IN}–) to the input pad without touching the guard ring.

2. Non-inverting Configuration (Figure 4-4):
   a. Connect the non-inverting pin (V\text{IN}+) to the input pad without touching the guard ring.
   b. Connect the guard ring to the inverting input pin (V\text{IN}–).

### 4.9 Unused Comparators

An unused amplifier in a quad package (MCP6544) should be configured as shown in Figure 4-10. This circuit prevents the output from toggling and causing crosstalk. It uses the minimum number of components and draws minimal current (see Figure 2-15 and Figure 2-18).

![Unused Comparators](image)

**FIGURE 4-10:** Unused Comparators.

### 4.10 Typical Applications

#### 4.10.1 Precise Comparator

Some applications require higher DC precision. An easy way to solve this problem is to use an amplifier (such as the MCP6041) to gain-up the input signal before it reaches the comparator. Figure 4-11 shows an example of this approach.

![Precise Inverting Comparator](image)

**FIGURE 4-11:** Precise Inverting Comparator.

#### 4.10.2 Windowed Comparator

Figure 4-12 shows one approach to designing a windowed comparator. The AND gate produces a logic ‘1’ when the input voltage is between V\text{RB} and V\text{RT} (where V\text{RT} > V\text{RB}).

![Windowed Comparator](image)

**FIGURE 4-12:** Windowed Comparator.

#### 4.10.3 Astable Multivibrator

A simple astable multivibrator design is shown in Figure 4-13. V\text{REF} needs to be between the power supplies (V\text{SS} = GND and V\text{DD}) to achieve oscillation. The output duty cycle changes with V\text{REF}.

![Astable Multivibrator](image)

**FIGURE 4-13:** Astable Multivibrator.
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

5-Lead SC-70 (MCP6541, MCP6541U)

- Device: MCP6541, MCP6541R, MCP6541U
- I-Temp Code: ABNN
- E-Temp Code: GTNN

Example:

8-Lead PDIP (300 mil) (MCP6541, MCP6542, MCP6543, MCP6544)

- Device: MCP6541, MCP6541R, MCP6541U
- I-Temp Code: ABNN
- E-Temp Code: ATNN

Example:

5-Lead SOT-23 (MCP6541, MCP6541R, MCP6541U)

- Device: MCP6541, MCP6541R, MCP6541U
- I-Temp Code: ABNN
- E-Temp Code: GTNN

Example:

Legend: XX...X Customer-specific information
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
VWW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code
* Pb-free JEDEC designator for Matte Tin (Sn)
@3 Pb-free JEDEC designator for Matte Tin (Sn)
This package is Pb-free. The Pb-free JEDEC designator (@3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
Package Marking Information (Continued)

14-Lead PDIP (300 mil) (MCP6544)

Example:

- MCP6544-I/P
  - 114656
- MCP6544E/P
  - 1146256

OR

- MCP6544-I/P
  - 1146256

14-Lead SOIC (150 mil) (MCP6544)

Example:

- MCP6544I/SL
  - 1146256
- MCP6544E/SL
  - 1146256

OR

- MCP6544-I/SL
  - 1146256

14-Lead TSSOP (MCP6544)

Example:

- MCP6544I
  - 1146
  - 256
- MCP6544E
  - 1146
  - 256
5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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Notes:
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B
5-Lead Plastic Small Outline Transistor (LT) [SC70]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

![Recommended Land Pattern Diagram]

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**Notes:**
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061A
5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
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</table>

**Notes:**
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
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<td>E</td>
</tr>
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<td>Contact Pad Spacing</td>
<td>C</td>
</tr>
<tr>
<td>Contact Pad Width (X5)</td>
<td>X</td>
</tr>
<tr>
<td>Contact Pad Length (X5)</td>
<td>Y</td>
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<tr>
<td>Distance Between Pads</td>
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<tr>
<td>Distance Between Pads</td>
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<td>Overall Width</td>
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Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A
8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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<td>Number of Pins</td>
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</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Top to Seating Plane</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Base to Seating Plane</td>
<td>A1</td>
</tr>
<tr>
<td>Shoulder to Shoulder Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
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<tr>
<td>Tip to Seating Plane</td>
<td>L</td>
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<td>Lead Thickness</td>
<td>c</td>
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<td>b</td>
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<tr>
<td>Overall Row Spacing §</td>
<td>eB</td>
</tr>
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**Notes:**

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing No. C04-057C Sheet 1 of 2
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>§</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Chamfer (Optional)</td>
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<td>Foot Length</td>
<td>L</td>
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<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
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<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
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<td>Mold Draft Angle Top</td>
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<tr>
<td>Mold Draft Angle Bottom</td>
<td>β</td>
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Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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**Recommended Land Pattern**

---

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<th>Dimension Limits</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
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<td>E</td>
<td>1.27 BSC</td>
<td></td>
<td></td>
<td></td>
</tr>
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<td>Contact Pad Spacing</td>
<td>C</td>
<td>5.40</td>
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</tr>
<tr>
<td>Contact Pad Width (X8)</td>
<td>X1</td>
<td>0.60</td>
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</tr>
<tr>
<td>Contact Pad Length (X8)</td>
<td>Y1</td>
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**Notes:**
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
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<td>MIN</td>
<td>NOM</td>
<td>MAX</td>
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<td></td>
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<td>Pitch</td>
<td>e</td>
<td>0.65 BSC</td>
<td></td>
<td></td>
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<tr>
<td>Overall Height</td>
<td>A</td>
<td>-</td>
<td>-</td>
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<td>0.75</td>
<td>0.85</td>
<td>0.95</td>
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<tr>
<td>Standoff</td>
<td>A1</td>
<td>0.00</td>
<td>-</td>
<td>0.15</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
<td></td>
<td>4.90 BSC</td>
<td></td>
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<tr>
<td>Molded Package Width</td>
<td>E1</td>
<td>3.00 BSC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
<td>3.00 BSC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
<td>0.40</td>
<td>0.60</td>
<td>0.80</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
<td></td>
<td>0.95 REF</td>
<td></td>
</tr>
<tr>
<td>Foot Angle</td>
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<td>-</td>
<td>0.40</td>
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</table>

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

![Recommended Land Pattern Diagram]

<table>
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<tr>
<th>Units</th>
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<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
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<tr>
<td>Contact Pitch</td>
<td>E</td>
<td></td>
<td>0.65 BSC</td>
<td></td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
<td></td>
<td>4.40</td>
<td></td>
</tr>
<tr>
<td>Overall Width</td>
<td>Z</td>
<td></td>
<td>5.85</td>
<td></td>
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<td>Contact Pad Width (X8)</td>
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<td>0.45</td>
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</tr>
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<td>Y1</td>
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<td>1.45</td>
<td></td>
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<td>G1</td>
<td></td>
<td>2.95</td>
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</tr>
<tr>
<td>Distance Between Pads</td>
<td>GX</td>
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<td>0.20</td>
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</tr>
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Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A
14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

**Units** | **INCHES**
---|---
**Dimension Limits**
Number of Pins | N | 14
Pitch | e | .100 BSC
Top to Seating Plane | A | – | – | .210
Molded Package Thickness | A2 | .115 | .130 | .195
Base to Seating Plane | A1 | .015 | – | –
Shoulder to Shoulder Width | E | .290 | .310 | .325
Molded Package Width | E1 | .240 | .250 | .280
Overall Length | D | .735 | .750 | .775
Tip to Seating Plane | L | .115 | .130 | .150
Lead Thickness | c | .008 | .010 | .015
Upper Lead Width | b1 | .045 | .060 | .070
Lower Lead Width | b | .014 | .018 | .022
Overall Row Spacing § | eB | – | – | .430

**Notes:**
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.  
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing No. C04-065C Sheet 1 of 2
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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<td>N</td>
<td>14</td>
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<tr>
<td>e</td>
<td>1.27 BSC</td>
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<tr>
<td>A</td>
<td>-</td>
</tr>
<tr>
<td>A2</td>
<td>1.25</td>
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<tr>
<td>A1</td>
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<tr>
<td>E</td>
<td>6.00 BSC</td>
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<td>E1</td>
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<td>L1</td>
<td>1.04 REF</td>
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<tr>
<td>Θ</td>
<td>0°</td>
</tr>
<tr>
<td>φ</td>
<td>0°</td>
</tr>
<tr>
<td>c</td>
<td>0.10</td>
</tr>
<tr>
<td>b</td>
<td>0.31</td>
</tr>
<tr>
<td>α</td>
<td>5°</td>
</tr>
<tr>
<td>β</td>
<td>5°</td>
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Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

<table>
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<tr>
<th>Units</th>
<th>Dimension Limits</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
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</thead>
<tbody>
<tr>
<td>Contact Pitch</td>
<td>E</td>
<td></td>
<td>1.27 BSC</td>
<td></td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
<td></td>
<td>5.40</td>
<td></td>
</tr>
<tr>
<td>Contact Pad Width</td>
<td>X</td>
<td></td>
<td>0.60</td>
<td></td>
</tr>
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<td>Contact Pad Length</td>
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<td>Distance Between Pads Gx</td>
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<td>Distance Between Pads G</td>
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Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A
14-Lead Plastic Thin Shrink Small Outline (ST) · 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing C04-087C Sheet 1 of 2
14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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<td>Pitch</td>
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<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
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<tr>
<td>Molded Package Length</td>
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<td>Foot Length</td>
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<td>Footprint</td>
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<td>θ</td>
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</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
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**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2
14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com-packaging

RECOMMENDED LAND PATTERN

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<td>C1</td>
</tr>
<tr>
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<td>X1</td>
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<tr>
<td>Contact Pad Length (X14)</td>
<td>Y1</td>
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<tr>
<td>Distance Between Pads</td>
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Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A
APPENDIX A: REVISION HISTORY

Revision H (December 2011)
The following is the list of modifications:
1. Updated Package Types drawings to correctly show the device representation for the SC-70 package.
3. Corrected the marking information table for the 5-Lead SC-70 package (MCP6541 and MCP6541U) in Section 5.1 “Package Marking Information”.
4. Updated package outline drawings in Section 5.1 “Package Marking Information” to show all views for each package.
5. Minor editorial changes.

Revision G (March 2011)
The following is the list of modifications:
1. Updated the marking information for the 5-Lead SC-70 package in Section 5.1 “Package Marking Information”.

Revision F (September 2007)
1. Corrected polarity of MCP6541U SOT-23-5 pin out diagram on front page.
2. Section 5.0 “Packaging Information”: Updated package outline drawings per MarCom.

Revision E (September 2006)
The following is the list of modifications:
1. Added MCP6541U pinout for the SOT-23-5 package.
2. Clarified Absolute Maximum Analog Input Voltage and Current Specifications.
3. Added applications write-ups on unused comparators.
4. Added disclaimer to package outline drawings.

Revision D (May 2006)
The following is the list of modifications:
1. Added E-temp parts.
2. Changed $V_{HYST}$ temperature specification to linear and quadratic temperature coefficients.
3. Changed specifications and plots for E-Temp.
4. Added section 3.0 “Pin Descriptions”.
5. Corrected package marking (See Section 5.1 “Package Marking Information”).
6. Added Appendix A: “Revision History”.

Revision C (September 2003)
• Undocumented changes.

Revision B (November 2002)
• Undocumented changes.

Revision A (March 2002)
• Original Release of this Document.
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
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<tr>
<td>/XX</td>
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</table>

- **Device:**
  - MCP6541: Single Comparator
  - MCP6541T: Single Comparator (Tape and Reel) (SC-70, SOT-23, SOIC, MSOP)
  - MCP6541RT: Single Comparator (Rotated - Tape and Reel) (SOT-23 only)
  - MCP6541UT: Single Comparator (Tape and Reel) (SC-70, SOT-23; SOT-23-5 is E-Temp only)
  - MCP6542: Dual Comparator
  - MCP6542T: Dual Comparator (Tape and Reel for SOIC and MSOP)
  - MCP6543: Single Comparator with CS
  - MCP6543T: Single Comparator with CS (Tape and Reel for SOIC and MSOP)
  - MCP6544: Quad Comparator
  - MCP6544T: Quad Comparator (Tape and Reel for SOIC and TSSOP)

- **Temperature Range:**
  - I = -40°C to +85°C
  - E * = -40°C to +125°C
  - * SC-70-5 E-Temp parts not available at this release of the data sheet.

- **Package:**
  - LT = Plastic Package (SC-70), 5-lead
  - OT = Plastic Small Outline Transistor (SOT-23), 5-lead
  - MS = Plastic MSOP, 8-lead
  - P = Plastic DIP (300 mil Body), 8-lead, 14-lead
  - SN = Plastic SOIC (150 mil Body), 8-lead
  - SL = Plastic SOIC (150 mil Body), 14-lead (MCP6544)
  - ST = Plastic TSSOP (4.4mm Body), 14-lead (MCP6544)

**Examples:**

- a) MCP6541T-I/LT: Tape and Reel, Industrial Temperature, 5LD SC-70.
- b) MCP6541T-I/OT: Tape and Reel, Industrial Temperature, 5LD SOT-23.
- c) MCP6541T-I/MS: Tape and Reel, Industrial Temperature, 8LD MSOP.
- d) MCP6541T-E/P: Extended Temperature, 8LD PDIP.
- e) MCP6541T-E/SN: Extended Temperature, 8LD SOIC.
- f) MCP6541RT-I/OT: Tape and Reel, Industrial Temperature, 5LD SOT23.
- g) MCP6541UT-E/LT: Tape and Reel, Industrial Temperature, 5LD SC-70.
- h) MCP6541UT-E/OT: Tape and Reel, Extended Temperature, 5LD SOT23.
- i) MCP6542T-I/MS: Industrial Temperature, 8LD MSOP.
- j) MCP6542T-I/PT: Tape and Reel, Industrial Temperature, 8LD MSOP.
- k) MCP6542T-I/P: Industrial Temperature, 8LD PDIP.
- l) MCP6542T-E/SN: Extended Temperature, 8LD SOIC.
- m) MCP6543T-I/PT: Tape and Reel, Industrial Temperature, 8LD SOIC.
- n) MCP6543T-I/P: Industrial Temperature, 14LD PDIP.
- o) MCP6543T-E/ST: Tape and Reel, Extended Temperature, 14LD TSSOP.
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