Features
- Precision (up to 17-Bits) A/D Converter
- 3-Wire Serial Port
- Flexible: User Can Trade Off Conversion Speed For Resolution
- Single Supply Operation
- -5V Output Pin
- 4 Input, Differential Analog MUX (TC534)
- Automatic Input Polarity and Overrange Detection
- Low Operating Current: 5mA Max
- Wide Analog Input Range: ±4.2V Max
- Cost Effective

Applications
- Precision Analog Signal Processor
- Precision Sensor Interface
- High Accuracy DC Measurements

Device Selection Table

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC530COI</td>
<td>28-Pin SOIC</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>TC530CPJ</td>
<td>28-Pin PDIP (Narrow)</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>TC534CKW</td>
<td>44-Pin PQFP</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>TC534CPL</td>
<td>40-Pin PDIP</td>
<td>0°C to +70°C</td>
</tr>
</tbody>
</table>
General Description

The TC530/TC534 are serial analog data acquisition subsystems ideal for high precision measurements (up to 17-bits plus sign). The TC530 consists of a dual slope integrating A/D converter, negative power supply generator and 3 wire serial interface port. The TC534 is identical to the TC530, but adds a four channel differential input multiplexer. Key A/D converter operating parameters (Auto Zero and Integration time) are programmable, allowing the user to trade conversion time for resolution.

Data conversion is initiated when the RESET input is brought low. After conversion, data is loaded into the output shift register and EOC is asserted, indicating new data is available. The converted data (plus Over-range and polarity bits) is held in the output shift register until read by the processor or until the next conversion is completed, allowing the user to access data at any time.

The TC530/TC534 timebase can be derived from an external crystal of 2MHz (max) or from an external frequency source. The TC530/TC534 requires a single 5V power supply and features a -5V, 10mA output which can be used to supply negative bias to other components in the system.

Typical Application
1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage .................................................................+6V
Analog Input Voltage (VIN+ or VIN-)..................VDD to VSS
Logic Input Voltage...........(VDD + 0.3V) to (GND - 0.3V)

Ambient Operating Temperature Range:
PDIP Package (C)................. 0°C to +70°C
SOIC Package (C) ................ 0°C to +70°C
PQFP Package (C) ............... 0°C to +70°C

Storage Temperature Range.............. -65°C to +150°C

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC530/TC530A/TC534 ELECTRICAL SPECIFICATIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>TA = +25°C</th>
<th>TA = 0°C to +70°C</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Analog Power Supply Voltage</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>—</td>
</tr>
<tr>
<td>VCCD</td>
<td>Digital Power Supply Voltage</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>—</td>
</tr>
<tr>
<td>PD</td>
<td>TC530/TC534 Total Power Dissipation</td>
<td>—</td>
<td>—</td>
<td>25</td>
<td>—</td>
</tr>
<tr>
<td>IS</td>
<td>Supply Current (VS + PIN)</td>
<td>—</td>
<td>1.8</td>
<td>2.5</td>
<td>—</td>
</tr>
<tr>
<td>ICCD</td>
<td>Supply Current (VCCD PIN)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Analog

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Bits</th>
<th>Note 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>Resolution</td>
<td></td>
<td></td>
<td>±17</td>
<td></td>
<td></td>
<td>±17</td>
<td></td>
<td>Note 1</td>
</tr>
<tr>
<td>ZSE</td>
<td>Zero Scale Error with Auto Zero Phase</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±0.005</td>
<td>Note 1</td>
</tr>
<tr>
<td>ENL</td>
<td>End Point Linearity</td>
<td>—</td>
<td>0.15</td>
<td>0.30</td>
<td></td>
<td></td>
<td></td>
<td>±0.015</td>
<td>Note 1 and Note 2</td>
</tr>
<tr>
<td>NL</td>
<td>Max. Deviation from Best Straight Line Fit</td>
<td>—</td>
<td>0.008</td>
<td>0.015</td>
<td></td>
<td></td>
<td></td>
<td>±0.015</td>
<td>Note 1 and Note 2</td>
</tr>
<tr>
<td>ZSTC</td>
<td>Zero Scale Temperature Coefficient</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>2</td>
<td>µV/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SYE</td>
<td>Rollover Error</td>
<td>—</td>
<td>.012</td>
<td></td>
<td></td>
<td>.03</td>
<td></td>
<td>±0.03</td>
<td>Note 3</td>
</tr>
<tr>
<td>FSTC</td>
<td>Full Scale Temperature Coefficient</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td></td>
<td>ppm/°C</td>
<td>Ext. VREF, T.C. = 0 ppm/°C</td>
<td></td>
</tr>
<tr>
<td>IIN</td>
<td>Input Current</td>
<td>—</td>
<td>6</td>
<td></td>
<td></td>
<td>—</td>
<td></td>
<td>pA</td>
<td>V IN = 0V</td>
</tr>
<tr>
<td>VCMR</td>
<td>Common-Mode Voltage Range</td>
<td>VS + 1.5</td>
<td>—</td>
<td>VDD - 1.5</td>
<td>VSS + 1.5</td>
<td>—</td>
<td>VDD - 1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VINT</td>
<td>Integrator Output Swing</td>
<td>VS + 0.9</td>
<td>—</td>
<td>VDD - 0.9</td>
<td>VSS + 0.9</td>
<td>—</td>
<td>VDD - 0.9</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIN</td>
<td>Analog Input Signal Range</td>
<td>VS + 1.5</td>
<td>—</td>
<td>VDD - 1.5</td>
<td>VSS + 1.5</td>
<td>—</td>
<td>VDD - 1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VREF</td>
<td>Voltage Reference Range</td>
<td>VS + 1</td>
<td>—</td>
<td>VDD - 1</td>
<td>VDD + 1</td>
<td>—</td>
<td>VDD - 1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>TD</td>
<td>Zero Crossing Comparator Delay</td>
<td>—</td>
<td>2.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.0</td>
<td>µsec</td>
</tr>
</tbody>
</table>

Note 1: Integrate time ≥ 66msec, Auto Zero time ≥ 66msec, VIN (pk) = 4V.
2: End point linearity at ±1/4, ±1/2 ±3/4, F.S. after full scale adjustment.
3: Rollover error is related to capacitor used for CINT. See Table 5-2, Recommended Capacitor for CINT.
4: TC534 Only.
### TC530/TC530A/TC534 ELECTRICAL SPECIFICATIONS (CONTINUED)

**Electrical Characteristics:** $V_{DD} = V_{CCD}, C_{AZ} = C_{REF} = 0.47\mu F,$ unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>$T_{A} = +25^\circ C$</th>
<th>$T_{A} = 0^\circ C$ to $+70^\circ C$</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input Logic HIGH Level</td>
<td>2.5</td>
<td>—</td>
<td>—</td>
<td>2.5</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Logic LOW Level</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>—</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Input Current (DI, DO, DCLK)</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Logic LOW Output Voltage (EOC)</td>
<td>—</td>
<td>0.2</td>
<td>0.3</td>
<td>—</td>
</tr>
<tr>
<td>$T_{RI}, T_{RF}$</td>
<td>Rise and Fall Times (EOC, DI, DO)</td>
<td>—</td>
<td>—</td>
<td>250</td>
<td>—</td>
</tr>
<tr>
<td>$F_{XTL}$</td>
<td>Crystal Frequency</td>
<td>—</td>
<td>—</td>
<td>2.0</td>
<td>—</td>
</tr>
<tr>
<td>$F_{EXT}$</td>
<td>External Frequency on OSCIN</td>
<td>—</td>
<td>—</td>
<td>4.0</td>
<td>—</td>
</tr>
<tr>
<td>$T_{RS}$</td>
<td>Read Setup Time</td>
<td>1</td>
<td>—</td>
<td>—</td>
<td>1</td>
</tr>
<tr>
<td>$T_{RD}$</td>
<td>Read Delay Time</td>
<td>250</td>
<td>—</td>
<td>—</td>
<td>250</td>
</tr>
<tr>
<td>$T_{DRS}$</td>
<td>DCLK to DOUT Delay</td>
<td>450</td>
<td>—</td>
<td>—</td>
<td>450</td>
</tr>
<tr>
<td>$T_{PWL}$</td>
<td>DCLK LOW Pulse Width</td>
<td>150</td>
<td>—</td>
<td>—</td>
<td>150</td>
</tr>
<tr>
<td>$T_{PWH}$</td>
<td>DCLK HIGH Pulse Width</td>
<td>150</td>
<td>—</td>
<td>—</td>
<td>150</td>
</tr>
<tr>
<td>$T_{DR}$</td>
<td>Data Ready Delay</td>
<td>200</td>
<td>—</td>
<td>—</td>
<td>200</td>
</tr>
<tr>
<td>$R_{OUT}$</td>
<td>Output Resistance</td>
<td>—</td>
<td>65</td>
<td>85</td>
<td>—</td>
</tr>
<tr>
<td>$F_{CLK}$</td>
<td>Oscillator Frequency</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>VSS Output Current</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>—</td>
</tr>
</tbody>
</table>

**Multiplexer**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>$T_{A} = +25^\circ C$</th>
<th>$T_{A} = 0^\circ C$ to $+70^\circ C$</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>$V_{IMAX}$</td>
<td>Maximum Input Voltage</td>
<td>-2.5</td>
<td>—</td>
<td>2.5</td>
<td>-2.5</td>
</tr>
<tr>
<td>$R_{DSON}$</td>
<td>Drain/Source ON Resistance</td>
<td>6</td>
<td>10</td>
<td>—</td>
<td>6</td>
</tr>
</tbody>
</table>

**Note**

1. Integrate time $\geq 66\text{msec}$, Auto Zero time $\geq 66\text{msec}$, $V_{\text{INT (pk)}} = 4V$.
2. End point linearity at $\pm 1/4$, $\pm 1/2$, $\pm 3/4$, F.S. after full scale adjustment.
3. Rollover error is related to capacitor used for $C_{\text{INT}}$. See Table 5-2, Recommended Capacitor for $C_{\text{INT}}$.
4. TC534 Only.
## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

<table>
<thead>
<tr>
<th>Pin Number (TC530) 28-Pin PDIP</th>
<th>Pin Number (TC530) 28-Pin SOIC</th>
<th>Pin Number (TC534) 40-Pin PDIP</th>
<th>Pin Number (TC534) 44-Pin PQFP</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>40</td>
<td>V&lt;sub&gt;SS&lt;/sub&gt;</td>
<td>Analog output. Negative power supply converter output and reservoir capacitor connection. This output can be used to provide negative bias to other devices in the system.</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>2</td>
<td>41</td>
<td>C&lt;sub&gt;INT&lt;/sub&gt;</td>
<td>Analog output. Integrator capacitor connection and integrator output.</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>3</td>
<td>42</td>
<td>C&lt;sub&gt;AZ&lt;/sub&gt;</td>
<td>Analog input. Auto Zero capacitor connection.</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>4</td>
<td>43</td>
<td>BUF</td>
<td>Analog output. Integrator capacitor connection and voltage buffer output.</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>5</td>
<td>2</td>
<td>ACOM</td>
<td>Analog input. This pin is ground for all of the analog switches in the A/D converter. It is grounded for most applications. ACOM and the input common pin (V&lt;sub&gt;IN&lt;/sub&gt;- or CHX-) should be within the common mode range, CMR.</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>6</td>
<td>3</td>
<td>C&lt;sub&gt;REF-&lt;/sub&gt;</td>
<td>Analog Input. Reference cap negative connection.</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td>7</td>
<td>4</td>
<td>C&lt;sub&gt;REF+&lt;/sub&gt;</td>
<td>Analog Input. Reference cap positive connection.</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>8</td>
<td>5</td>
<td>V&lt;sub&gt;REF+&lt;/sub&gt;</td>
<td>Analog Input. External voltage reference positive connection.</td>
</tr>
<tr>
<td>9</td>
<td>9</td>
<td>9</td>
<td>6</td>
<td>V&lt;sub&gt;REF+&lt;/sub&gt;</td>
<td>Analog Input. External voltage reference positive connection.</td>
</tr>
<tr>
<td>Not Used</td>
<td>Not Used</td>
<td>10</td>
<td>7</td>
<td>CH4-</td>
<td>Analog Input. Multiplexer channel 4 negative differential</td>
</tr>
<tr>
<td>Not Used</td>
<td>Not Used</td>
<td>11</td>
<td>8</td>
<td>CH3-</td>
<td>Analog Input. Multiplexer channel 3 negative differential</td>
</tr>
<tr>
<td>Not Used</td>
<td>Not Used</td>
<td>12</td>
<td>9</td>
<td>CH2-</td>
<td>Analog Input. Multiplexer channel 2 negative differential</td>
</tr>
<tr>
<td>Not Used</td>
<td>Not Used</td>
<td>13</td>
<td>10</td>
<td>CH1-</td>
<td>Analog Input. Multiplexer channel 1 negative differential</td>
</tr>
<tr>
<td>Not Used</td>
<td>Not Used</td>
<td>14</td>
<td>11</td>
<td>CH4+</td>
<td>Analog Input. Multiplexer channel 4 positive differential</td>
</tr>
<tr>
<td>Not Used</td>
<td>Not Used</td>
<td>15</td>
<td>12</td>
<td>CH3+</td>
<td>Analog Input. Multiplexer channel 3 positive differential</td>
</tr>
<tr>
<td>Not Used</td>
<td>Not Used</td>
<td>16</td>
<td>13</td>
<td>CH2+</td>
<td>Analog Input. Multiplexer channel 2 positive differential</td>
</tr>
<tr>
<td>Not Used</td>
<td>Not Used</td>
<td>17</td>
<td>14</td>
<td>CH1+</td>
<td>Analog Input. Multiplexer channel 1 positive differential</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>Not Used</td>
<td>Not Used</td>
<td>V&lt;sub&gt;N-&lt;/sub&gt;</td>
<td>Analog Input. Negative differential analog voltage input.</td>
</tr>
<tr>
<td>11</td>
<td>11</td>
<td>Not Used</td>
<td>Not Used</td>
<td>V&lt;sub&gt;N+&lt;/sub&gt;</td>
<td>Analog Input. Positive differential analog voltage input.</td>
</tr>
<tr>
<td>12</td>
<td>12</td>
<td>18</td>
<td>15</td>
<td>DGND</td>
<td>Analog Input. Ground connection for serial port circuit.</td>
</tr>
<tr>
<td>Not Used</td>
<td>Not Used</td>
<td>19</td>
<td>16</td>
<td>A1</td>
<td>Logic Level Input. Multiplexer address MSB.</td>
</tr>
<tr>
<td>Not Used</td>
<td>Not Used</td>
<td>20</td>
<td>17</td>
<td>A0</td>
<td>Logic Level Input. Multiplexer address LSB.</td>
</tr>
<tr>
<td>14</td>
<td>14</td>
<td>21</td>
<td>18</td>
<td>OSC&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>Analog Input. Timebase for state machine. This pin connects to one side of an AT-cut crystal having an effective series resistance of 100Ω (typ) and a parallel capacitance of 20pF. If an external frequency source is used to clock the TC530/TC534 this pin must be left floating.</td>
</tr>
<tr>
<td>15</td>
<td>15</td>
<td>22</td>
<td>19</td>
<td>OSC&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Analog Input. This pin connects to the other side of the crystal described in OSC&lt;sub&gt;OUT&lt;/sub&gt; above. The TC530/TC534 may also be clocked from an external frequency source connected to this pin. The external frequency source must be a pulse wave form with a minimum 30% duty cycle and rise and fall times 15nsec (Max). If an external frequency source is used, OSC&lt;sub&gt;OUT&lt;/sub&gt; must be left floating. A maximum operating frequency of 2MHz (crystal) or 4MHz (external clock source) is permitted.</td>
</tr>
</tbody>
</table>
TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

<table>
<thead>
<tr>
<th>Pin Number (TC530) 28-Pin PDIP</th>
<th>Pin Number (TC530) 28-Pin SOIC</th>
<th>Pin Number (TC534) 40-Pin PDIP</th>
<th>Pin Number (TC534) 44-Pin PQFP</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>16</td>
<td>23</td>
<td>20</td>
<td>D&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>Logic Level Output. Serial port data output pin. This pin is enabled only when R/W is high.</td>
</tr>
<tr>
<td>17</td>
<td>17</td>
<td>24</td>
<td>21</td>
<td>D&lt;sub&gt;CLK&lt;/sub&gt;</td>
<td>Logic Input, Positive and Negative Edge Triggered. Serial port clock. When R/W is high, serial data is clocked out of the TC530/TC534A (on D&lt;sub&gt;OUT&lt;/sub&gt;) at each high-to-low transition of D&lt;sub&gt;CLK&lt;/sub&gt;. A maximum serial port D&lt;sub&gt;CLK&lt;/sub&gt; frequency of 3MHz is permitted.</td>
</tr>
<tr>
<td>18</td>
<td>18</td>
<td>25</td>
<td>22</td>
<td>D&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Logic Level Input. Serial port input pin. The A/D converter integration time (T&lt;sub&gt;INT&lt;/sub&gt;) and Auto Zero time (T&lt;sub&gt;AZ&lt;/sub&gt;) values are determined by the LOAD VALUE byte clocked into this pin. This initialization must take place at power up, and can be rewritten (or modified and rewritten) at any time. The LOAD VALUE is clocked into D&lt;sub&gt;N&lt;/sub&gt; MSB first.</td>
</tr>
<tr>
<td>19</td>
<td>19</td>
<td>26</td>
<td>23</td>
<td>R/W</td>
<td>Logic Level Input. This pin must be brought low to perform a write to the serial port (e.g. initialize the A/D converter). The D&lt;sub&gt;OUT&lt;/sub&gt; pin of the serial port is enabled only when this pin is high.</td>
</tr>
<tr>
<td>20</td>
<td>20</td>
<td>27</td>
<td>24</td>
<td>EOC</td>
<td>Open Drain Output. End-of-Conversion (EOC) is asserted any time the TC530/TC534 is in the AZ phase of conversion. This occurs when either the TC530/TC534 initiates a normal AZ phase or when RESET is pulled high. EOC is returned high when the TC530/TC534 exits AZ. Since EOC is driven low immediately following completion of a conversion cycle, it can be used as a DATA READY processor interrupt.</td>
</tr>
<tr>
<td>21</td>
<td>21</td>
<td>30</td>
<td>28</td>
<td>RESET</td>
<td>Logic Level Input. It is necessary to force the TC530/TC534 into the Auto Zero phase when power is initially applied. This is accomplished by momentarily taking RESET high. Using an I/O port line from the microprocessor or by applying an external system reset signal or by connecting a 0.01µF capacitor from the RESET input to V&lt;sub&gt;DD&lt;/sub&gt;. Conversions are performed continuously as long as RESET is low and conversion is halted when RESET is high. RESET may therefore be used in a complex system to momentarily suspend conversion (for example, while the address lines of an input multiplexer are changing state). In this case, RESET should be pulled high only when the EOC is LOW to avoid excessively long integrator discharge times which could result in erroneous conversion. (See Applications Section).</td>
</tr>
<tr>
<td>22</td>
<td>22</td>
<td>32</td>
<td>30</td>
<td>V&lt;sub&gt;CCD&lt;/sub&gt;</td>
<td>Analog Input. Power supply connection for digital logic and serial port. Proper power-up sequencing is critical, see the Applications section.</td>
</tr>
<tr>
<td>23</td>
<td>23</td>
<td>34</td>
<td>32</td>
<td>OSC</td>
<td>Input. The negative power supply converter normally runs at a frequency of 100kHz. This frequency can be slowed down to reduce quiescent current by connecting an external capacitor between this pin and V&lt;sup&gt;+&lt;/sup&gt;DD. See Section 6.0, Typical Characteristics.</td>
</tr>
<tr>
<td>25</td>
<td>25</td>
<td>37</td>
<td>35</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>Analog Input. Power supply connection for the A/D analog section and DC-DC converter. Proper power-up sequencing is critical, (See the Applications section).</td>
</tr>
<tr>
<td>Pin Number (TC530) 28-Pin PDIP</td>
<td>Pin Number (TC530) 28-Pin SOIC</td>
<td>Pin Number (TC534) 40-Pin PDIP</td>
<td>Symbol</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>-------------------------------</td>
<td>---------------------------------</td>
<td>--------------------------------</td>
<td>--------</td>
<td>-------------</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>26</td>
<td>38</td>
<td>36</td>
<td>CAP+</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Analog Input. Storage capacitor positive connection for the DC/DC converter.</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>27</td>
<td>39</td>
<td>37</td>
<td>AGND</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Analog Input. Ground connection for DC/DC converter.</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>28</td>
<td>40</td>
<td>38</td>
<td>CAP-</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Analog Input. Storage capacitor negative connection for the DC/DC converter.</td>
<td></td>
</tr>
<tr>
<td>13, 24</td>
<td>13, 24</td>
<td>28, 29, 31, 33, 35, 36</td>
<td>1, 25, 26, 27, 29, 31, 33, 34, 39, 44</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>No connect. Do not connect any signal to these pins.</td>
<td></td>
</tr>
</tbody>
</table>
3.0 DETAILED DESCRIPTION

3.1 Dual Slope Integrating Converter

The TC530/TC534 dual slope converter operates by integrating the input signal for a fixed time period, then applying an opposite polarity reference voltage while timing the period (counting clock pulses) for the integrator output to cross 0V (deintegrating). The resulting count is read as conversion data.

A simple mathematical expression that describes dual slope conversion is:

\[
\text{Integrate Voltage} = \text{De-integrate Voltage}
\]

\[
\frac{1}{R_{\text{INT}}C_{\text{INT}}} \int_0^{T_{\text{INT}}} V_{\text{IN}}(t) \, dt = \frac{1}{R_{\text{INT}}C_{\text{INT}}} \int_0^{T_{\text{DEINT}}} V_{\text{REF}} \, dt
\]

from which:

\[
(V_{\text{IN}}) \frac{(T_{\text{INT}})}{(R_{\text{INT}})(C_{\text{INT}})} = (V_{\text{REF}}) \frac{(T_{\text{DEINT}})}{(R_{\text{INT}})(C_{\text{INT}})}
\]

And therefore:

\[
V_{\text{IN}} = V_{\text{REF}} \frac{T_{\text{DEINT}}}{T_{\text{INT}}}
\]

where:

- \(V_{\text{REF}}\) = Reference Voltage
- \(T_{\text{INT}}\) = Integrate Time
- \(T_{\text{DEINT}}\) = Reference Voltage De-integrate Time

Inspection of Equation 3-4 shows dual slope converter accuracy is unrelated to integrating resistor and capacitor values, as long as they are stable throughout the measurement cycle. This measurement technique is inherently ratiometric (i.e., the ratio between the \(T_{\text{INT}}\) and \(T_{\text{DEINT}}\) times is equal to the ratio between \(V_{\text{IN}}\) and \(V_{\text{REF}}\)).

Another inherent benefit is noise immunity. Input noise spikes are integrated, or averaged to zero, during the integration period. The integrating converter has a noise immunity with an attenuation rate of at least -20dB per decade. Interference signals with frequencies at integral multiples of the integration period are, for the most part, completely removed. For this reason, the integration period of the converter is often established to reject 50/60Hz line noise. The ability to reject such noise is shown by the plot of Figure 3-1.

In addition to the two phases required for dual slope measurement (Integrate and De-integrate), the TC530/TC534 performs two additional adjustments to minimize measurement error due to system offset voltages. The resulting four internal operations (conversion phases) performed each measurement cycle are: Auto Zero (AZ), Integrator Output Zero (IZ), Input Integrate (INT) and Reference De-integrate (DINT). The AZ and IZ phases compensate for system offset errors and the INT and DINT phases perform the actual A/D conversion.

FIGURE 3-1: INTEGRATING CONVERTER NORMAL MODE REJECTION

3.2 Auto Zero Phase (AZ)

This phase compensates for errors due to buffer, integrator and comparator offset voltages. During this phase, an internal feedback loop forces a compensating error voltage on auto zero capacitor (\(C_{\text{AZ}}\)). The duration of the AZ phase is programmable via the serial port (see Section 4.1.1, AZ and INT Phase Duration).
3.3 Input Integrate Phase (INT)

In this phase, a current directly proportional to differential input voltage is sourced into integrating capacitor $C_{\text{INT}}$. The amount of voltage stored on $C_{\text{INT}}$ at the end of the INT phase is directly proportional to the applied differential input voltage. Input signal polarity (sign bit) is determined at the end of this phase. Converter resolution and speed is a function of the duration of the INT phase, which is programmable by the user via the serial port (see Section 4.1.1, AZ and INT Phase Duration). The shorter the integration time, the faster the speed of conversion (but the lower the resolution). Conversely, the longer the integration time, the greater the resolution (but at slower the speed of conversion).
3.4 Reference De-integrate Phase (DINT)

This phase consists of measuring the time for the integrator output to return (at a rate determined by the external reference voltage) from its initial voltage to 0V. The resulting timer data is stored in the output shift register as converted analog data.

3.5 Integrator Output Zero Phase (IZ)

This phase ensures the integrator output is at zero volts when the AZ phase is entered so that only true system offset voltages will be compensated for.

All internal converter timing is derived from the frequency source at OSCIN and OSCOUT. This frequency source must be either an externally provided clock signal or an external crystal. If an external clock is used, it must be connected to the OSCIN pin and the OSCOUT pin must remain floating. If a crystal is used, it must be connected between OSCIN and OSCOUT and be physically located as close to the OSCIN and OSCOUT pins as possible. In either case, the incoming clock frequency is divided by four, with the resulting clock serving as the internal TC530/TC534 timebase.

4.0 TYPICAL APPLICATIONS

4.1 Programming the TC530/TC534

4.1.1 AZ AND INT PHASE DURATION

These two phases have equal duration determined by the crystal (or external) frequency and the timer initialization byte (LOAD VALUE). Timing is selected as follows:

1. Select Integration Time
   - Integration time must be picked as a multiple of the period of the line frequency. For example, TINT times of 33msec, 66msec and 132msec maximize 60Hz line rejection.

2. Estimate Crystal Frequency
   - Crystal frequencies as high as 2MHz are allowed.
   - Crystal frequency is estimated using:

   \[ \text{FIN} = \frac{2 \times R}{T_{\text{INT}}} \]

   where:
   - \( R \) = Desired Converter Resolution (in counts)
   - \( F_{\text{IN}} \) = Input Frequency (in MHz)
   - \( T_{\text{INT}} \) = Integration Time (in seconds)

3. Calculate LOAD VALUE

   \[ \text{LOAD VALUE}_{10} = \frac{256 \times (T_{\text{INT}})(F_{\text{IN}})}{1024} \]

   \( F_{\text{IN}} \) can be adjusted to a standard value during this step. The resulting base, -10 LOAD VALUE, must be converted to a hexadecimal number and then loaded into the serial port prior to initiating A/D conversion.

4.2 DINT and IZ Phase Timing

The duration of the DINT phase is a function of the amount of voltage stored on the integrator capacitor during INT and the value of \( V_{\text{REF}} \). The DINT phase is initiated immediately following INT and terminated when an integrator output zero crossing is detected. In general, the maximum number of counts chosen for DINT is twice that of INT (with \( V_{\text{REF}} \) chosen at \( V_{\text{IN\_MAX}}/2 \)).

4.3 System RESET

The TC530/TC534 must be forced into the AZ state when power is first applied. A .01\( \mu \)F capacitor connected from RESET to VDD (or external system reset logic signal) can be used to momentarily drive RESET high for a minimum of 100msec.

4.4 Design Example

Figure 4-1 shows a typical TC534 interrupt-driven application. Timing and component values are calculated from equations and recommendations made in Section 3.1 and Section 4.1 of this document. The EOC connection to the processor INT input is for interrupt-driven applications only. (In polled systems, the EOC output is available on DOUT).

Given:
- Required resolution: 16-bits (65,536 counts.)
- Maximum: \( V_{\text{IN}} \leq 2V \)
- Power supply voltage: +5V
- 60Hz system

1. Pick Integration time (\( T_{\text{INT}} \)): 66msec
2. Estimate crystal frequency.

   \[ F_{\text{IN}} = \frac{2R}{T_{\text{INT}}} = 2 \times 65536/66 \times 10^{-3} = 1.98MHz \]

   (use 2MHz)

3. Calculate LOAD VALUE

   \[ \text{LOAD VALUE} = 256 - \frac{(T_{\text{INT}})(F_{\text{IN}})}{1024} = [128]_{10} \]

   \[ [128]_{10} = 80 \text{ hex} \]
4. Calculate $R_{INT}$

**EXAMPLE 4-3:**

$$R_{INT} = \frac{V_{INMAX}}{20} = \frac{2}{20} = 100\,\Omega$$

5. Calculate $C_{INT}$ for maximum (4V) integrator output swing:

**EXAMPLE 4-4:**

$$C_{INT} = \frac{(T_{INT})(20 \times 10^{-6})}{(V_S - 0.9)}$$

$$= \frac{0.066(20 \times 10^{-6})}{(4.1)}$$

$$= 0.32\,\mu F \text{ (use closest value: 0.33}\,\mu F)$$

Note: Microchip recommended capacitor: Evox-Rifa p/n: SMR5 334K50J03L

6. Choose $C_{REF}$ and $C_{AZ}$ based on conversion rate:

**EXAMPLE 4-5:**

Conversions/sec $= \frac{1}{(T_{AZ} + T_{INT} + 2T_{INT} + 2\,\text{msec})}$

$= \frac{1}{(66\,\text{msec} + 66\,\text{msec} + 132\,\text{msec} + 2\,\text{msec})}$

$= 3.7 \text{ conversions/sec}$

from which $C_{AZ} = C_{REF} = 0.22\,\mu F$ (Table 5-1)

Note: Microchip recommended capacitor: Evox-Rifa p/n: SMR5 224K50J02L4

7. Calculate $V_{REF}$

**EXAMPLE 4-6:**

$$V_{REF} = \frac{(V_S - 0.9)(C_{INT})(R_{INT})}{2(T_{INT})}$$

$$= \frac{(4.1)(0.33 \times 10^{-6})(10^5)}{2(0.066)}$$

$$= 1.025V$$

4.5 Power Supply Sequencing

Improper sequencing of the power supply inputs ($V_{DD}$ vs. $V_{CCD}$) can potentially cause an improper power-up sequence to occur. See Section 4.6, Circuit Design/Layout Considerations. Failing to insure a proper power-up sequence can cause spurious operation.

4.6 Circuit Design/Layout Considerations

1. Separate ground return paths should be used for the analog and digital circuitry. Use of ground planes and trace fill on analog circuit sections is highly recommended EXCEPT for in and around the integrator section and $C_{REF}$, $C_{AZ}$, ($C_{INT}$, $C_{REF}$, $C_{AZ}$, $R_{INT}$). Stray capacitance between these nodes and ground appears in parallel with the components themselves and can affect measurement accuracy.

2. Improper sequencing of the power supply inputs ($V_{DD}$ vs. $V_{CCD}$) can potentially cause an improper power-up sequence to occur in the internal state machines. It is recommended that the digital supply, $V_{CCD}$, be powered up first. One method of insuring the correct power-up sequence is to delay the analog supply using a series resistor and a capacitor. See Figure 4-1, TC530/TC534 Typical Application.

3. Decoupling capacitors, preferably a higher value electrolytic or tantalum in parallel with a small ceramic or tantalum, should be used liberally. This includes bypassing the supply connections of all active components and the voltage reference.

4. Critical components should be chosen for stability and low noise. The use of a metal-film resistor for $R_{INT}$ and Polypropylene or Polyphenylene Sulfide (PPS) capacitors for $C_{INT}$, $C_{AZ}$ and $C_{REF}$ is highly recommended.

5. The inputs and integrator section are very high impedance nodes. Leakage to or from these critical nodes can contribute measurement error. A guard-ring should be used to protect the integrator section from stray leakage.

6. Circuit assemblies should be exceptionally clean to prevent the presence of contamination from assembly, handling or the cleaning itself. Minute conductive trace contaminants, easily ignored in most applications, can adversely affect the performance of high impedance circuits. The input and integrator sections should be made as compact and close to the TC53X as possible.

7. Digital and other dynamic signal conductors should be kept as far from the TC53X’s analog section as possible. The microcontroller or other host logic should be kept quiet during a measurement cycle. Background activities such as keypad scanning, display refreshing and power switching can introduce noise.
FIGURE 4-1: TC530/TC534 TYPICAL APPLICATION

[Diagram showing the typical application of the TC530/TC534 with labeled components such as VDD, VCCD, RESET, Oscillator inputs/outputs, Analog inputs, Processor interface, and associated components like R1, R2, C1, C2, and C3.]
5.0 SELECTING COMPONENT VALUES FOR THE TC530/TC534

1. Calculate Integrating Resistor (\(R_{\text{INT}}\))
   The desired full scale input voltage and amplifier output current capability determine the value of \(R_{\text{INT}}\). The buffer and integrator amplifiers each have a full scale current of 20\(\mu\)A. The value of \(R_{\text{INT}}\) is therefore directly calculated as follows:

   \[
   R_{\text{INT}} = \frac{V_{\text{IN(MAX)}}}{20}\ m\Omega
   \]

   where:
   \(V_{\text{IN(MAX)}}\) = Maximum Input Voltage (full count voltage)
   \(R_{\text{INT}}\) = Integrating Resistor (in m\(\Omega\))
   For loop stability, \(R_{\text{INT}}\) should be \(\geq 50\k\Omega\).

2. Select Reference (\(C_{\text{REF}}\)) and Auto Zero (\(C_{\text{AZ}}\)) Capacitors
   \(C_{\text{REF}}\) and \(C_{\text{AZ}}\) must be low leakage capacitors (such as polypropylene). The slower the conversion rate, the larger the value \(C_{\text{REF}}\) must be. Recommended capacitors for \(C_{\text{REF}}\) and \(C_{\text{AZ}}\) are shown in Table 5-1. Larger values for \(C_{\text{AZ}}\) and \(C_{\text{REF}}\) may also be used to limit rollover errors.

   \[
   \frac{(V_S - 0.9)(C_{\text{INT}})(R_{\text{INT}})}{2(R_{\text{INT}})} V
   \]

   TABLE 5-1: C_{\text{REF}} AND C_{\text{AZ}} SELECTION

<table>
<thead>
<tr>
<th>Conversion Per Second</th>
<th>Typical Value of (C_{\text{REF}}, C_{\text{AZ}}) ((\mu)F)</th>
<th>Suggested Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt;7</td>
<td>0.1</td>
<td>SMR5 104K50J01L</td>
</tr>
<tr>
<td>2 to 7</td>
<td>0.22</td>
<td>SMR5 224K50J2L</td>
</tr>
<tr>
<td>2 or less</td>
<td>0.47</td>
<td>SMR5 474K50J04L</td>
</tr>
</tbody>
</table>

   Note: *Manufactured by Evox-Rifa, Inc.

3. Calculate Integrating Capacitor (\(C_{\text{INT}}\))
   The integrating capacitor must be selected to maximize integrator output voltage swing. The integrator output voltage swing is defined as the absolute value of \(V_{\text{DD}}\) (or \(V_{\text{SS}}\)) less 0.9V (i.e., \(|V_{\text{DD}}| - 0.9\text{V}\) or \(|V_{\text{SS}}| + 0.9\text{V}\)). Using the 20\(\mu\)A buffer maximum output current, the value of the integrating capacitor is calculated using the following equation:

   \[
   C_{\text{INT}} = \frac{(T_{\text{INT}})(20 \times 10^{-5})}{(V_S - 0.9)} \mu\text{F}
   \]

   where:
   \(T_{\text{INT}}\) = Integration Period
   \(V_S = |V_{\text{DD}}|\)
   \(C_{\text{INT}}\) = Integrated Capacitor Value (\(\mu\)F).

5.2 Calculate \(V_{\text{REF}}\)
   The reference de-integration voltage is calculated using the following equation:

   \[
   V_{\text{REF}} = \frac{(V_S - 0.9)(C_{\text{INT}})(R_{\text{INT}})}{2(R_{\text{INT}})} \]

5.3 Serial Port
   Communication with the TC530/TC534 is accomplished over a 3 wire serial port. Data is clocked into \(D_{\text{IN}}\) on the rising edge of \(D_{\text{CLK}}\) and clocked out of \(D_{\text{OUT}}\) on the falling edge of \(D_{\text{CLK}}\). \(R/W\) must be HIGH to read converted data from the serial port and LOW to write the LOAD VALUE to the TC530/TC534.

5.4 Data Read Cycle
   Data is shifted out of the serial port in the following order: End of Conversion (EOC), Overrange (OVR), Polarity (POL), conversion data (MSB first). When \(R/W\) is high, the state of the EOC bit can be polled by simply reading the state of \(D_{\text{OUT}}\). This allows the processor to determine if new data is available without connecting an additional wire to the EOC output pin (this is especially useful in a polled environment). See Figure 5-1.
5.5 Load Value Write Cycle

Following the power-up reset pulse, the LOAD VALUE (which sets the duration of AZ and INT) must next be transmitted to the serial port. To accomplish this, the processor monitors the state of EOC (which is available as a hardware output or at D[OUT]). R/W is taken low to initiate the write cycle only when EOC is low (during the AZ phase). (Failure to observe EOC low may cause an offset voltage to be developed across C[INT], resulting in erroneous readings). The 8-bit LOAD VALUE data on D[IN] is clocked in by DCLK. The processor then terminates the write cycle by taking R/W high. (Data is transferred from the serial input shift register to the time base counter on the rising edge of R/W and data conversion is initiated). See Figure 5-2.

5.6 Input Multiplexer (TC534 Only)

A 4-input, differential multiplexer is included in the TC534. The states of channel address lines A0 and A1 determine which differential V[IN] pair is routed to the converter input. A0 is the least significant address bit (i.e., channel 1 is selected when A0 = 0 and A1 = 0). The multiplexer is designed to be operated in a differential mode. For single-ended inputs, the CHx- input for the channel under selection must be connected to the ground reference associated with the input signal.

FIGURE 5-2: TC530/TC534 INITIALIZATION AND LOAD VALUE WRITE CYCLE

5.7 DC/DC Converter

An on-board, TC7660H-type charge pump supplies negative bias to the converter circuitry, as well as to external devices. The charge pump develops a negative output voltage by moving charge from the power supply to the reservoir capacitor at V[SS] by way of the commutating capacitor connected to the CAP+ and CAP- inputs.

The charge pump clock operates at a typical frequency of 100kHz. If lower quiescent current is desired, the charge pump clock can be slowed by connecting an external capacitor from the OSC pin to V[DD]. Reference typical characteristics curves.
6.0 TYPICAL CHARACTERISTICS

The graphs and tables following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range), and therefore outside the warranted range.
7.0 PACKAGING INFORMATION

7.1 Package Marking Information
Package marking data not available at this time.

7.2 Taping Forms

### Component Taping Orientation for 28-Pin SOIC (Wide) Devices

**User Direction of Feed**

- **PIN 1**
- **W**: Package Carrier Width
- **P**: Pitch
- **Reel Size**: 13 in

<table>
<thead>
<tr>
<th>Package</th>
<th>Carrier Width (W)</th>
<th>Pitch (P)</th>
<th>Part Per Full Reel</th>
<th>Reel Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>28-Pin SOIC (W)</td>
<td>24 mm</td>
<td>12 mm</td>
<td>1000</td>
<td>13 in</td>
</tr>
</tbody>
</table>

**NOTE:** Drawing does not represent total number of pins.

### Component Taping Orientation for 44-Pin PQFP Devices

**User Direction of Feed**

- **PIN 1**
- **W**: Package Carrier Width
- **P**: Pitch

<table>
<thead>
<tr>
<th>Package</th>
<th>Carrier Width (W)</th>
<th>Pitch (P)</th>
<th>Part Per Full Reel</th>
<th>Reel Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>44-Pin PQFP</td>
<td>24 mm</td>
<td>16 mm</td>
<td>500</td>
<td>13 in</td>
</tr>
</tbody>
</table>

**NOTE:** Drawing does not represent total number of pins.
7.3 Package Dimensions

28-Pin PDIP (Narrow)

Dimensions: inches (mm)

40-Pin PDIP (Wide)

Dimensions: inches (mm)
### 7.3 Package Dimensions (Continued)

**28-Pin SOIC (Wide)**

![28-Pin SOIC (Wide) Diagram]

Dimensions: inches (mm)

**44-Pin PQFP**

![44-Pin PQFP Diagram]

Dimensions: inches (mm)
SALES AND SUPPORT

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System
Register on our web site (www.microchip.com/cn) to receive the most current information on our products.
Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip’s products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, FilterLab, KEELOQ, microID, MPLAB, PIC, PICmicro, PICMASTER, PICSTART, PRO MATE, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

dsPIC, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, MXDEV, PICC, PICDEM, PICDEM.net, rPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2002, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.
### AMERICAS

**Corporate Office**
2335 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

**Rocky Mountain**
2335 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

**Atlanta**
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

**Boston**
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

**Chicago**
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

**Dallas**
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7923 Fax: 972-818-2924

**Detroit**
Tri-Aria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

**Kokomo**
2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

**Los Angeles**
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

**New York**
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

**San Jose**
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

**Toronto**
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

### ASIA/PACIFIC

**Australia**
Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

**China - Beijing**
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

**China - Chengdu**
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 3401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

**China - Fuzhou**
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Unit 71 Wuqia Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

**China - Hong Kong SAR**
Microchip Technology Hong Kong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

**India**
Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

**Japan**
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

**Korea**
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

**Singapore**
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

**Taiwan**
Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

### EUROPE

**Denmark**
Microchip Technology Nordic ApS
Regus Business Centre
Lautrup høj 1-3
Ballrup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

**France**
Microchip Technology SARL
Parc d’Activite du Moulin de Massy
43 Rue du Saule Trapu
Bâtiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

**Germany**
Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

**Italy**
Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

**United Kingdom**
Microchip Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

04/20/02