Features
- High Peak Output Current: 1.2 A
- Wide Operating Range:
  - 4.5 V to 18 V
- Symmetrical Rise/Fall Times: 25 nsec
- Short, Equal Delay Times: 75 nsec
- Latch-proof. Will Withstand 500 mA Inductive Kickback
- 3 Input Logic Choices:
  - AND / NAND / AND + Inv
- ESD Protection on All Pins: 2 kV

Applications
- General Purpose CMOS Logic Buffer
- Driving All Four MOSFETs in an H-Bridge
- Direct Small Motor Driver
- Relay or Peripheral Drivers
- CCD Driver
- Pin-Switching Network Driver

General Description
The TC4467/TC4468/TC4469 devices are a family of four-output CMOS buffers/MOSFET drivers with 1.2 A peak drive capability. Unlike other MOSFET drivers, these devices have two inputs for each output. The inputs are configured as logic gates: NAND (TC4467), AND (TC4468) and AND/INV (TC4469).

The TC4467/TC4468/TC4469 drivers can continuously source up to 250 mA into ground referenced loads. These devices are ideal for direct driving low current motors or driving MOSFETs in a H-bridge configuration for higher current motor drive (see Section 5.0 for details). Having the logic gates onboard the driver can help to reduce component count in many designs.

The TC4467/TC4468/TC4469 devices are very robust and highly latch-up resistant. They can tolerate up to 5 V of noise spiking on the ground line and can handle up to 0.5 A of reverse current on the driver outputs.

The TC4467/4468/4469 devices are available in commercial, industrial and military temperature ranges.
Logic Diagrams

<table>
<thead>
<tr>
<th>TC4467</th>
<th>TC4468</th>
<th>TC4469</th>
<th>TC446X</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>VDD</td>
<td>VDD</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>14</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>1A 1</td>
<td>1A 1</td>
<td>1A 1</td>
<td>1Y</td>
</tr>
<tr>
<td>1B 2</td>
<td>1B 2</td>
<td>1B 2</td>
<td></td>
</tr>
<tr>
<td>2A 3</td>
<td>2A 3</td>
<td>2A 3</td>
<td>2Y</td>
</tr>
<tr>
<td>2B 4</td>
<td>2B 4</td>
<td>2B 4</td>
<td></td>
</tr>
<tr>
<td>3A 5</td>
<td>3A 5</td>
<td>3A 5</td>
<td>3Y</td>
</tr>
<tr>
<td>3B 6</td>
<td>3B 6</td>
<td>3B 6</td>
<td></td>
</tr>
<tr>
<td>4A 8</td>
<td>4A 8</td>
<td>4A 8</td>
<td>4Y</td>
</tr>
<tr>
<td>4B 9</td>
<td>4B 9</td>
<td>4B 9</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>Output</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

© 2001-2012 Microchip Technology Inc.
1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage ...............................................................+20 V
Input Voltage ...............................................................(GND – 5 V) to (V DD + 0.3 V)
Package Power Dissipation: (T A ≤ 70°C)
  PDIP ...................................................................800 mW
  CERDIP .............................................................840 mW
  SOIC ..................................................................760 mW
Package Thermal Resistance:
  CERDIP R θ JA ...................................................100°C/W
  CERDIP R θ JC .....................................................23°C/W
  PDIP R θ JA ..........................................................80°C/W
  PDIP R θ JC ..........................................................35°C/W
  SOIC R θ JA ..........................................................95°C/W
  SOIC R θ JC ..........................................................28°C/W
Operating Temperature Range:
  C Version ...................................................0°C to +70°C
  E Version ...................................................-40°C to +85°C
  M Version ..............................................-55°C to +125°C
Maximum Chip Temperature.......................................+150°C
Storage Temperature Range.........................-65°C to +150°C

†Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic 1, High Input Voltage</td>
<td>V IH</td>
<td>2.4</td>
<td>—</td>
<td>V DD</td>
<td>V</td>
<td>Note 3</td>
</tr>
<tr>
<td>Logic 0, Low Input Voltage</td>
<td>V IL</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>Note 3</td>
</tr>
<tr>
<td>Input Current</td>
<td>I IN</td>
<td>-1.0</td>
<td>—</td>
<td>+1.0</td>
<td>µA</td>
<td>0 V ≤ V IN ≤ V DD</td>
</tr>
<tr>
<td>Output</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High Output Voltage</td>
<td>V OH</td>
<td>V DD – 0.025</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>I LOAD = 100 µA (Note 1)</td>
</tr>
<tr>
<td>Low Output Voltage</td>
<td>V OL</td>
<td>—</td>
<td>—</td>
<td>0.15</td>
<td>V</td>
<td>I LOAD = 10 mA (Note 1)</td>
</tr>
<tr>
<td>Output Resistance</td>
<td>R O</td>
<td>—</td>
<td>10</td>
<td>15</td>
<td>Ω</td>
<td>I OUT = 10 mA, V DD = 18 V</td>
</tr>
<tr>
<td>Peak Output Current</td>
<td>I PK</td>
<td>—</td>
<td>1.2</td>
<td>—</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Continuous Output Current</td>
<td>I DC</td>
<td>—</td>
<td>—</td>
<td>300</td>
<td>mA</td>
<td>Single Output</td>
</tr>
<tr>
<td>Reverse Current</td>
<td>I</td>
<td>—</td>
<td>500</td>
<td>—</td>
<td>mA</td>
<td>4.5 V ≤ V DD ≤ 16 V</td>
</tr>
<tr>
<td>Latch-Up Protection Withstand</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching Time (Note 1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rise Time</td>
<td>t R</td>
<td>—</td>
<td>15</td>
<td>25</td>
<td>nsec</td>
<td>Figure 4-1</td>
</tr>
<tr>
<td>Fall Time</td>
<td>t F</td>
<td>—</td>
<td>15</td>
<td>25</td>
<td>nsec</td>
<td>Figure 4-1</td>
</tr>
<tr>
<td>Delay Time</td>
<td>I D1</td>
<td>—</td>
<td>40</td>
<td>75</td>
<td>nsec</td>
<td>Figure 4-1</td>
</tr>
<tr>
<td>Delay Time</td>
<td>I D2</td>
<td>—</td>
<td>40</td>
<td>75</td>
<td>nsec</td>
<td>Figure 4-1</td>
</tr>
<tr>
<td>Power Supply</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply Current</td>
<td>I S</td>
<td>—</td>
<td>1.5</td>
<td>4</td>
<td>mA</td>
<td>Note 2</td>
</tr>
<tr>
<td>Power Supply Voltage</td>
<td>V DD</td>
<td>4.5</td>
<td>—</td>
<td>18</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Totem pole outputs should not be paralleled because the propagation delay differences from one to the other could cause one driver to drive high a few nanoseconds before another. The resulting current spike, although short, may decrease the life of the device. Switching times are ensured by design.

2: When driving all four outputs simultaneously in the same direction, V DD will be limited to 16 V. This reduces the chance that internal dv/dt will cause high-power dissipation in the device.

3: The input threshold has approximately 50 mV of hysteresis centered at approximately 1.5 V. Input rise times should be kept below 5 µsec to avoid high internal peak currents during input transitions. Static input levels should also be maintained above the maximum, or below the minimum, input levels specified in the "Electrical Characteristics" to avoid increased power dissipation in the device.
### ELECTRICAL SPECIFICATIONS (OPERATING TEMPERATURES)

Electrical Characteristics: Unless otherwise noted, over operating temperature range with $4.5 \, \text{V} \leq V_{\text{DD}} \leq 18 \, \text{V}$.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic 1, High Input Voltage</td>
<td>$V_{\text{IH}}$</td>
<td>2.4</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>Note 3</td>
</tr>
<tr>
<td>Logic 0, Low Input Voltage</td>
<td>$V_{\text{IL}}$</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>Note 3</td>
</tr>
<tr>
<td>Input Current</td>
<td>$I_{\text{IN}}$</td>
<td>-10</td>
<td>—</td>
<td>10</td>
<td>$\mu$A</td>
<td>0 $, \text{V} \leq I_{\text{IN}} \leq V_{\text{DD}}$</td>
</tr>
<tr>
<td><strong>Output</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High Output Voltage</td>
<td>$V_{\text{OH}}$</td>
<td>$V_{\text{DD}} - 0.025$</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>$I_{\text{LOAD}} = 100 , \mu$A (Note 1)</td>
</tr>
<tr>
<td>Low Output Voltage</td>
<td>$V_{\text{OL}}$</td>
<td>—</td>
<td>—</td>
<td>0.30</td>
<td>V</td>
<td>$I_{\text{LOAD}} = 10 , mA$ (Note 1)</td>
</tr>
<tr>
<td>Output Resistance</td>
<td>$R_{\text{O}}$</td>
<td>—</td>
<td>20</td>
<td>30</td>
<td>$\Omega$</td>
<td>$I_{\text{OUT}} = 10 , mA, V_{\text{DD}} = 18 , \text{V}$</td>
</tr>
<tr>
<td>Peak Output Current</td>
<td>$I_{\text{PK}}$</td>
<td>—</td>
<td>1.2</td>
<td>—</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Continuous Output Current</td>
<td>$I_{\text{DC}}$</td>
<td>—</td>
<td>—</td>
<td>300</td>
<td>mA</td>
<td>Single Output</td>
</tr>
<tr>
<td>Latch-Up Protection Withstand Reverse Current</td>
<td>$I$</td>
<td>—</td>
<td>500</td>
<td>—</td>
<td>mA</td>
<td>4.5 $, \text{V} \leq V_{\text{DD}} \leq 16 , \text{V}$</td>
</tr>
<tr>
<td><strong>Switching Time (Note 1)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rise Time</td>
<td>$t_{\text{R}}$</td>
<td>—</td>
<td>15</td>
<td>50</td>
<td>nsec</td>
<td>Figure 4-1</td>
</tr>
<tr>
<td>Fall Time</td>
<td>$t_{\text{F}}$</td>
<td>—</td>
<td>15</td>
<td>50</td>
<td>nsec</td>
<td>Figure 4-1</td>
</tr>
<tr>
<td>Delay Time</td>
<td>$t_{\text{D1}}$</td>
<td>—</td>
<td>40</td>
<td>100</td>
<td>nsec</td>
<td>Figure 4-1</td>
</tr>
<tr>
<td>Delay Time</td>
<td>$t_{\text{D2}}$</td>
<td>—</td>
<td>40</td>
<td>100</td>
<td>nsec</td>
<td>Figure 4-1</td>
</tr>
<tr>
<td><strong>Power Supply</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply Current</td>
<td>$I_{\text{S}}$</td>
<td>—</td>
<td>—</td>
<td>8</td>
<td>mA</td>
<td>Note 2</td>
</tr>
<tr>
<td>Power Supply Voltage</td>
<td>$V_{\text{DD}}$</td>
<td>—</td>
<td>4.5</td>
<td>18</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Totem pole outputs should not be paralleled because the propagation delay differences from one to the other could cause one driver to drive high a few nanoseconds before another. The resulting current spike, although short, may decrease the life of the device. Switching times are ensured by design.

Note 2: When driving all four outputs simultaneously in the same direction, $V_{\text{DD}}$ will be limited to 16 V. This reduces the chance that internal $dv/dt$ will cause high-power dissipation in the device.

Note 3: The input threshold has approximately 50 mV of hysteresis centered at approximately 1.5 V. Input rise times should be kept below 5 µsec to avoid high internal peak currents during input transitions. Static input levels should also be maintained above the maximum, or below the minimum, input levels specified in the "Electrical Characteristics" to avoid increased power dissipation in the device.

### TRUTH TABLE

<table>
<thead>
<tr>
<th>Part No.</th>
<th>TC4467 NAND</th>
<th>TC4468 AND</th>
<th>TC4469 AND/INV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inputs A</td>
<td>H H L L L</td>
<td>H H L L L</td>
<td>H H L L L</td>
</tr>
<tr>
<td>Inputs B</td>
<td>H L H L L</td>
<td>H L H L L</td>
<td>H L H L L</td>
</tr>
<tr>
<td>Outputs TC446X</td>
<td>L H H H</td>
<td>L H H H</td>
<td>L H H H</td>
</tr>
</tbody>
</table>

Legend: $H =$ High $\quad L =$ Low
2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** $T_A = +25^\circ C$, with $4.5 \text{ V} \leq V_{DD} \leq 18 \text{ V}$.

**FIGURE 2-1:** Rise Time vs. Supply Voltage.

**FIGURE 2-2:** Rise Time vs. Capacitive Load.

**FIGURE 2-3:** Rise/Fall Times vs. Temperature.

**FIGURE 2-4:** Fall Time vs. Supply Voltage.

**FIGURE 2-5:** Fall Time vs. Capacitive Load.

**FIGURE 2-6:** Propagation Delay Time vs. Supply Voltage.
2.0 TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: \( T_A = +25^\circ C \), with \( 4.5 \leq V_{DD} \leq 18 \) V.

**FIGURE 2-7:** Input Amplitude vs. Delay Times.

**FIGURE 2-8:** Quiescent Supply Current vs. Supply Voltage.

**FIGURE 2-9:** High-State Output Resistance.

**FIGURE 2-10:** Propagation Delay Times vs. Temperatures.

**FIGURE 2-11:** Quiescent Supply Current vs. Temperature.

**FIGURE 2-12:** Low-State Output Resistance.
2.0  TYPICAL PERFORMANCE CURVES (CONTINUED)

Note:  (Load on single output only).


FIGURE 2-14: Supply Current vs. Capacitive Load.

FIGURE 2-15: Supply Current vs. Capacitive Load.

FIGURE 2-16: Supply Current vs. Frequency.

FIGURE 2-17: Supply Current vs. Frequency.

FIGURE 2-18: Supply Current vs. Frequency.
3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

<table>
<thead>
<tr>
<th>14-Pin PDIP, CERDIP</th>
<th>16-Pin SOIC (Wide)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol</td>
<td>Symbol</td>
<td></td>
</tr>
<tr>
<td>1A</td>
<td>1A</td>
<td>Input A for Driver 1, TTL/CMOS Compatible Input</td>
</tr>
<tr>
<td>1B</td>
<td>1B</td>
<td>Input B for Driver 1, TTL/CMOS Compatible Input</td>
</tr>
<tr>
<td>2A</td>
<td>2A</td>
<td>Input A for Driver 2, TTL/CMOS Compatible Input</td>
</tr>
<tr>
<td>2B</td>
<td>2B</td>
<td>Input B for Driver 2, TTL/CMOS Compatible Input</td>
</tr>
<tr>
<td>3A</td>
<td>3A</td>
<td>Input A for Driver 3, TTL/CMOS Compatible Input</td>
</tr>
<tr>
<td>3B</td>
<td>3B</td>
<td>Input B for Driver 3, TTL/CMOS Compatible Input</td>
</tr>
<tr>
<td>GND</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>—</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>4A</td>
<td>4A</td>
<td>Input A for Driver 4, TTL/CMOS Compatible Input</td>
</tr>
<tr>
<td>4B</td>
<td>4B</td>
<td>Input B for Driver 4, TTL/CMOS Compatible Input</td>
</tr>
<tr>
<td>4Y</td>
<td>4Y</td>
<td>Output for Driver 4, CMOS Push-Pull Output</td>
</tr>
<tr>
<td>3Y</td>
<td>3Y</td>
<td>Output for Driver 3, CMOS Push-Pull Output</td>
</tr>
<tr>
<td>2Y</td>
<td>2Y</td>
<td>Output for Driver 2, CMOS Push-Pull Output</td>
</tr>
<tr>
<td>1Y</td>
<td>1Y</td>
<td>Output for Driver 1, CMOS Push-Pull Output</td>
</tr>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>Supply Input, 4.5 V to 18 V</td>
</tr>
<tr>
<td>—</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>Supply Input, 4.5 V to 18 V</td>
</tr>
</tbody>
</table>
4.0 DETAILED DESCRIPTION

4.1 Supply Bypassing

Large currents are required to charge and discharge large capacitive loads quickly. For example, charging a 1000 pF load to 18 V in 25 nsec requires 0.72 A from the device's power supply.

To ensure low supply impedance over a wide frequency range, a 1 µF film capacitor in parallel with one or two low-inductance, 0.1 µF ceramic disk capacitors with short lead lengths (<0.5 in.) normally provide adequate bypassing.

4.2 Grounding

The TC4467 and TC4469 contain inverting drivers. Potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics. Instead, individual ground returns for input and output circuits, or a ground plane, should be used.

4.3 Input Stage

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5 mA current source load. With logic "0" outputs, maximum quiescent supply current is 4 mA. Logic "1" output level signals reduce quiescent current to 1.4 mA, maximum. Unused driver inputs must be connected to VDD or VSS. Minimum power dissipation occurs for logic "1" outputs.

The drivers are designed with 50 mV of hysteresis, which provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5 V, making any voltage greater than 1.5 V, up to VDD, a logic "1" input. Input current is less than 1 µA over this range.

4.4 Power Dissipation

The supply current versus frequency and supply current versus capacitive load characteristic curves will aid in determining power dissipation calculations. Microchip Technology’s CMOS drivers have greatly reduced quiescent DC power consumption.

Input signal duty cycle, power supply voltage and load type influence package power dissipation. Given power dissipation and package thermal resistance, the maximum ambient operating temperature is easily calculated. The 14-pin plastic package junction-to-ambient thermal resistance is 83.3°C/W. At +70°C, the package is rated at 800 mW maximum dissipation. Maximum allowable chip temperature is +150°C.

Three components make up total package power dissipation:
1. Load-caused dissipation (PL).
2. Quiescent power (PQ).
3. Transition power (PT).

A capacitive-load-caused dissipation (driving MOSFET gates), is a direct function of frequency, capacitive load and supply voltage. The power dissipation is:

\[ P_L = fCV_S^2 \]

\[ f = \text{Switching Frequency} \]
\[ C = \text{Capacitive Load} \]
\[ V_S = \text{Supply Voltage} \]

A resistive-load-caused dissipation for ground-referenced loads is a function of duty cycle, load current and load voltage. The power dissipation is:

\[ P_L = D(V_S - V_L)I_L \]

\[ D = \text{Duty Cycle} \]
\[ V_S = \text{Supply Voltage} \]
\[ V_L = \text{Load Voltage} \]
\[ I_L = \text{Load Current} \]
A resistive-load-caused dissipation for supply-referenced loads is a function of duty cycle, load current and output voltage. The power dissipation is

**EQUATION**

\[ P_L = DV_O I_L \]

\[ D = \text{Duty Cycle} \]
\[ V_O = \text{Device Output Voltage} \]
\[ I_L = \text{Load Current} \]

Quiescent power dissipation depends on input signal duty cycle. Logic HIGH outputs result in a lower power dissipation mode, with only 0.6 mA total current drain (all devices driven). Logic LOW outputs raise the current to 4 mA maximum. The quiescent power dissipation is:

**EQUATION**

\[ P_Q = V_S(D(I_H) + (1 - D)I_L) \]

\[ I_H = \text{Quiescent Current with all outputs LOW} \]
\[ (4 \text{ mA max.}) \]
\[ I_L = \text{Quiescent Current with all outputs HIGH} \]
\[ (0.6 \text{ mA max.}) \]
\[ D = \text{Duty Cycle} \]
\[ V_S = \text{Supply Voltage} \]

Transition power dissipation arises in the complimentary configuration (TC446X) because the output stage N-channel and P-channel MOS transistors are ON simultaneously for a very short period when the output changes. The transition power dissipation is approximately:

**EQUATION**

\[ P_T = fV_S(10 \times 10^{-9}) \]

\[ C = 1000 \text{ pF Capacitive Load} \]
\[ V_S = 15 \text{ V} \]
\[ D = 50\% \]
\[ f = 200 \text{ kHz} \]
\[ P_D = \text{Package Power Dissipation} \]
\[ = P_L + P_Q + P_T \]
\[ = 45\text{mW} + 35\text{mW} + 30\text{mW} \]
\[ = 110\text{mW} \]

Package power dissipation is the sum of load, quiescent and transition power dissipations. An example shows the relative magnitude for each term: Maximum operating temperature is:

**EQUATION**

\[ T_J - \theta_{JA}(P_D) = 141^\circ\text{C} \]

\[ T_J = \text{Maximum allowable junction temperature} \]
\[ (+150^\circ\text{C}) \]
\[ \theta_{JA} = \text{Junction-to-ambient thermal resistance} \]
\[ (83.3^\circ\text{C/W}) 14\text{-pin plastic package} \]

**Note:** Ambient operating temperature should not exceed +85°C for "EJD" device or +125°C for "MJD" device.

**FIGURE 4-1:** Switching Time Test Circuit.
5.0 APPLICATIONS INFORMATION

**FIGURE 5-1:** Stepper Motor Drive.

**FIGURE 5-2:** Quad Driver For H-bridge Motor Control.
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

14-Lead PDIP (300 mil)

Example:

```
XXXXXXXXXXXXXX
XXXXXXXXXXXXXX
YYWWNNNN
```

14-Lead CERDIP (300 mil)

Example:

```
XXXXXXXXXXXXXX
XXXXXXXXXXXXXX
YYWWNNNN
```

16-Lead SOIC (300 mil)

Example:

```
XXXXXXXXXX
XXXXXXXXXX
YYYYYYYY
```

Legend:

- XX...X Customer-specific information
- Y Year code (last digit of calendar year)
- YY Year code (last 2 digits of calendar year)
- WW Week code (week of January 1 is week '01')
- NNN Alphanumeric traceability code
- (e3) Pb-free JEDEC designator for Matte Tin (Sn)
- * This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

**Dimensions and Notes:**

- **Dimensions:**
  - Number of Pins: 14
  - Pitch: 0.100
  - Top to Seating Plane:
    - A: Min: 0.140, Nom: 0.155, Max: 0.170
    - A1: Min: 0.015
  - Molded Package Thickness: A2: Min: 0.084, Nom: 0.095, Max: 0.106
  - Base to Seating Plane: A1: Min: 0.015
  - Shoulder to Shoulder Width: E: Min: 0.300, Nom: 0.313, Max: 0.325
  - Molded Package Width: E1: Min: 0.240, Nom: 0.250, Max: 0.260
  - Overall Length: D: Min: 0.740, Nom: 0.750, Max: 0.760
  - Tip to Seating Plane: L: Min: 0.125, Nom: 0.130, Max: 0.135
  - Lead Thickness: c: Min: 0.008, Nom: 0.012, Max: 0.015
  - Upper Lead Width: B1: Min: 0.045, Nom: 0.050, Max: 0.055
  - Lower Lead Width: B: Min: 0.014, Nom: 0.018, Max: 0.022
  - Overall Row Spacing: eB: Min: 0.310, Nom: 0.370, Max: 0.430
  - Mold Draft Angle Top: α: Min: 5, Nom: 10, Max: 15
  - Mold Draft Angle Bottom: β: Min: 5, Nom: 10, Max: 15

- **Notes:**
  - Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010” (0.254mm) per side.
  - JEDEC Equivalent: MS-001
  - Drawing No. C04-005

- **Units:**
  - INCHES: MIN, NOM, MAX
  - MILLIMETERS: MIN, NOM, MAX

- **Controlling Parameter:**
  - Significant Characteristic

- **Notes:**
  - Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010” (0.254mm) per side.
  - JEDEC Equivalent: MS-001
  - Drawing No. C04-005
14-Lead Ceramic Dual In-line – 300 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

14-Pin CERDIP (Narrow)
TC4467/TC4468/TC4469

16-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

**Units**

<table>
<thead>
<tr>
<th>Dimension Limits</th>
<th>INCHES*</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Pins</td>
<td>n</td>
<td>16</td>
</tr>
<tr>
<td>Pitch</td>
<td>p</td>
<td>.050</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
<td>.093 .099 .104</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
<td>.088 .091 .094</td>
</tr>
<tr>
<td>Standoff §</td>
<td>A1</td>
<td>.004 .008 .012</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
<td>.394 .407 .420</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
<td>.291 .295 .299</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
<td>.398 .406 .413</td>
</tr>
<tr>
<td>Chamfer Distance</td>
<td>H</td>
<td>.010 .020 .029</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
<td>.016 .033 .050</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>e</td>
<td>0 4 8</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
<td>.009 .011 .013</td>
</tr>
<tr>
<td>Lead Width</td>
<td>B</td>
<td>.014 .017 .020</td>
</tr>
<tr>
<td>Mold Draft Angle Top</td>
<td>α</td>
<td>0 12 15</td>
</tr>
<tr>
<td>Mold Draft Angle Bottom</td>
<td>β</td>
<td>0 12 15</td>
</tr>
</tbody>
</table>

*Controlling Parameter

§ Significant Characteristic

**Notes:**

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-013

Drawing No. C04-102

© 2001-2012 Microchip Technology Inc.
7.0 REVISION HISTORY

Revision C (December 2012)

Added a note to each package outline drawing.
THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user’s guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip’s customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under “Support”, click on “Customer Change Notification” and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://microchip.com/support
READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

TO: Technical Publications Manager
RE: Reader Response
From: Name ____________________________
Company _______________________________________
Address _______________________________________
City / State / ZIP / Country ___________________________
Telephone: (_____ ) _________ - _________ FAX: (_____ ) _________ - _________

Application (optional):

Would you like a reply?       Y         N

Device: TC4467/4468/4469

Questions:
1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>Device</th>
<th>Temperature Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC4467</td>
<td>0°C to +70°C</td>
<td>PD = Plastic DIP, (300 mil body), 14-lead</td>
</tr>
<tr>
<td>TC4468</td>
<td>-40°C to +85°C (CERDIP only)</td>
<td>JD = Ceramic DIP, (300 mil body), 14-lead</td>
</tr>
<tr>
<td>TC4469</td>
<td>-55°C to +125°C (CERDIP only)</td>
<td>OE = SOIC (Wide), 16-lead</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OE713 = SOIC (Wide), 16-lead (Tape and Reel)</td>
</tr>
</tbody>
</table>

Examples:

a) TC4467COE: Commercial Temperature, SOIC package.
b) TC4467CPD: Commercial Temperature, PDIP package.
c) TC4467MJD: Military Temperature, Ceramic DIP package.
a) TC4468COE713: Tape and Reel, Commercial Temp., SOIC package.
b) TC4468CPD: Commercial Temperature, PDIP package.
a) TC4469COE: Commercial Temperature, SOIC package.
b) TC4469CPD: Commercial Temperature, PDIP package.

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System
Register on our web site (www.microchip.com/cn) to receive the most current information on our products.
Note the following details of the code protection feature on Microchip devices:

• Microchip products meet the specification contained in their particular Microchip Data Sheet.
• Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
• There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
• Microchip is willing to work with the customer who is concerned about the integrity of their code.
• Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Microchip makes no representations or warranties of any kind, whether express or implied, written or oral, statutory or otherwise, related to the information, including but not limited to its condition, quality, performance, merchantability or fitness for purpose. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks
The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELoo, KEELoo logo, MPLAB, PIC, PICmicro, PICSTART, PIC32 logo, rPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, Hi-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, Hi-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rLAB, Select Mode, SQI, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. & KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2001-2012, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.
Printed on recycled paper.
ISBN: 9781620767993

QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV

ISO/TS 16949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company’s quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001:2000 certified.
Worldwide Sales and Service

AMERICAS
Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0086
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0484
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-9323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario, Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC
Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2943-5131

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8664-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC
India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Osaka
Tel: 81-66-152-7160
Fax: 81-66-152-9310

Japan - Yokohama
Tel: 81-45-471-6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or 82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5777-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7628
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE
Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

11/27/12