16-Bit Low Cost, Low Power Sigma-Delta A/D Converter

Features

• 16-bit Resolution at Eight Conversions Per Second, Adjustable Down to 10-bit Resolution at 512 Conversions Per Second
• 1.8V – 5.5V Operation, Low Power Operating 300µA; Sleep: 50µA
• microPort™ Serial Bus Requires only two Interface Lines
• Uses Internal or External Reference
• Automatically Enters Sleep Mode when not in use
• True Differential Inputs with Built-In Multiplexer Provide Ratiometric Conversions
• Early Warning Power Fail Detector, also suitable as Wake-Up Timer Operational in Shutdown Mode
• \( V_{DD} \) Monitor and Reset Generator Operational in Shutdown Mode

Applications

• Consumer Electronics, Thermostats, CO Monitors, Humidity Meters, Security Sensors
• Embedded Systems, Data Loggers, Portable Equipment
• Medical Instruments

Device Selection Table

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC3401VPE</td>
<td>16-Pin PDIP (Narrow)</td>
<td>0°C to +85°C</td>
</tr>
<tr>
<td>TC3401VQR</td>
<td>16-Pin QSOP Narrow</td>
<td>0°C to +85°C</td>
</tr>
</tbody>
</table>

General Description

The TC3401 is a low cost, low power analog-to-digital converter based on Microchip’s Sigma-Delta technology. It will perform 16-bit conversions (15-bit plus sign) at up to eight per second. The TC3401 is optimized for use as a microcontroller peripheral in low cost, battery operated systems. A voltage reference is included, or an external reference can be used. A \( V_{DD} \) monitor with a reset generator provides Power-on Reset and Brown-out protection while an extra threshold detector is suitable for use as an early warning Power Fail detector, or as a Wake-up Timer.

The TC3401’s 2-wire microPort™ digital interface is used for starting conversions and for reading out the data. Driving the SCLK line low starts a conversion. After the conversion starts, each additional falling edge (up to six) detected on SCLK for \( t_4 \) seconds reduces the A/D resolution by one bit and cuts conversion time in half. After a conversion is completed, clocking the SCLK line puts the MSB through LSB of the resulting data word onto the SDAT line, much like a shift register. The part automatically sleeps when not performing a data conversion.

The TC3401 is available in a 16-Pin PDIP and a 16-Pin QSOP package.
1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage ................................................. 6.0V
Voltage on Pins:
    PFO, RESET ................................. (GND – 0.3V) to 5.5V
Input Voltage (All Other Pins):
    .................................. (GND – 0.3V) to (VDD + 0.3V)
Operating Temperature Range ................. 0°C to 85°C
Storage Temperature ......................... -65°C to +150°C

TC3401 DC ELECTRICAL SPECIFICATIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply Voltage</td>
<td>1.8</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IDD</td>
<td>Supply Current, During Data Conversion</td>
<td>—</td>
<td>300</td>
<td>—</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>IDD Sleep</td>
<td>Supply Current, Sleep Mode</td>
<td>—</td>
<td>50</td>
<td>80</td>
<td>µA</td>
<td>TA = +25°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>50</td>
<td>130</td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

Accuracy (Differential Inputs)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES</td>
<td>Resolution</td>
<td>—</td>
<td>16</td>
<td>—</td>
<td>Bits</td>
<td></td>
</tr>
<tr>
<td>INL</td>
<td>Integral Non-Linearity</td>
<td>—</td>
<td>0.0038</td>
<td>—</td>
<td>%FSR</td>
<td>VDD = 2.7V</td>
</tr>
<tr>
<td>VOS</td>
<td>Offset Error</td>
<td>—</td>
<td>—</td>
<td>±0.9%FSR</td>
<td>—</td>
<td>%FSR</td>
</tr>
<tr>
<td>VNOISE</td>
<td>Referred to input</td>
<td>—</td>
<td>60</td>
<td>—</td>
<td>µVRms</td>
<td></td>
</tr>
<tr>
<td>CMR</td>
<td>Common Mode Rejection</td>
<td>—</td>
<td>75</td>
<td>—</td>
<td>dB</td>
<td>At DC</td>
</tr>
<tr>
<td>FSE</td>
<td>Full Scale Error</td>
<td>—</td>
<td>0.4%</td>
<td>—</td>
<td>%FS</td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>—</td>
<td>75</td>
<td>—</td>
<td>dB</td>
<td>VDD = 2.5V to 3.5V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN+, IN-</td>
<td>Differential Input Voltage</td>
<td>—</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Absolute Voltage Range on IN+, IN-</td>
<td>—</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Bias Current</td>
<td>—</td>
<td>1</td>
<td>100</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>CIN</td>
<td>Input Sampling Capacitance</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Rin</td>
<td>Differential Input Resistance</td>
<td>—</td>
<td>2.0</td>
<td>—</td>
<td>MΩ</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>VREF</td>
<td>REF IN Voltage Range</td>
<td>0</td>
<td>—</td>
<td>1.25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IREF</td>
<td>REF IN Input Current</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>VREFOUT</td>
<td>REF OUT Voltage</td>
<td>—</td>
<td>1.193</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>REF SINK</td>
<td>REF OUT Current Sink Capability</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>REF SRC</td>
<td>REF OUT Current Source Capability</td>
<td>—</td>
<td>300</td>
<td>—</td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Differential input voltage defined as (VIN+ – VIN-).
Note 2: Resistance from IN+ to IN- or IN- to GND.
Note 3: @ VDD = 1.8V, ISOURCE ≤ 200µA.
TC3401 AC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: $T_A = 25^\circ C$ and $V_{DD} = 2.7V$, unless otherwise specified. **Boldface** type specifications apply for temperatures of 0°C to 85°C. $V_{REF} = 1.25V$, Internal Clock Frequency = 520kHz.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SCLK, ADDR, ENABLE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td></td>
<td></td>
<td></td>
<td>0.3x$V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td></td>
<td>$0.7xV_{DD}$</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{LEAK}$</td>
<td>Leakage Current</td>
<td>1</td>
<td></td>
<td></td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td></td>
<td></td>
<td></td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage (SDAT)</td>
<td></td>
<td></td>
<td></td>
<td>$0.9xV_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDmin}$</td>
<td>Minimum $V_{DD}$ for PFO, RESET Valid</td>
<td></td>
<td>1.1</td>
<td>1.3</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$V_{TH,PFI}$</td>
<td>PFI Input Voltage Range</td>
<td></td>
<td></td>
<td></td>
<td>$V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{TH,PFI}$</td>
<td>PFI Input Current</td>
<td>-0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$V_{THR}$</td>
<td>Threshold ($V_{TH,PFI}$)</td>
<td></td>
<td>1.23</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{THH}$</td>
<td>Threshold Hysteresis</td>
<td></td>
<td>30</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Threshold Tempco</td>
<td></td>
<td>30</td>
<td></td>
<td>ppm/°C</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Differential input voltage defined as $(V_{IN+} - V_{IN-})$.

**Note 2:** Resistance from INn+ to INn- or INn to GND.

**Note 3:** @ $V_{DD} = 1.8V$,ADVERTISEMENT = 200µA.

TC3401 DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: $T_A = 25^\circ C$ and $V_{DD} = 2.7V$, unless otherwise specified. **Boldface** type specifications apply for temperatures of 0°C to 85°C. $V_{REF} = 1.25V$, Internal Clock Frequency = 520kHz.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
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<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Symbol</strong></td>
<td><strong>Parameter</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td>Output Low Voltage</td>
<td></td>
<td></td>
<td></td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>$I_{SOURCE}$</td>
<td>Source Current</td>
<td></td>
<td></td>
<td></td>
<td>400 $\mu A$</td>
<td>(Note 3)</td>
</tr>
<tr>
<td>$V_{DDmin}$</td>
<td>Minimum $V_{DD}$ for PFO, RESET Valid</td>
<td></td>
<td>1.1</td>
<td>1.3</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$V_{TH,PFI}$</td>
<td>PFI Input Voltage Range</td>
<td></td>
<td></td>
<td></td>
<td>$V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{TH,PFI}$</td>
<td>PFI Input Current</td>
<td>-0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$V_{THR}$</td>
<td>Threshold ($V_{TH,PFI}$)</td>
<td></td>
<td>1.23</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{THH}$</td>
<td>Threshold Hysteresis</td>
<td></td>
<td>30</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Threshold Tempco</td>
<td></td>
<td>30</td>
<td></td>
<td>ppm/°C</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Nominal temperature drift is -2830ppm/C° for temperature less than 25°C and -1340ppm/C° for temperatures greater than 25°C.
2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

<table>
<thead>
<tr>
<th>Pin No. (16-Pin PDIP) (16-Pin QSOP)</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1</strong></td>
<td>IN1+</td>
<td>Analog Input. This is the positive terminal of a true differential input consisting of IN1+ and IN1-. V&lt;sub&gt;IN1&lt;/sub&gt; = (IN1+ – IN-). See Section 1.0, Electrical Characteristics.</td>
</tr>
<tr>
<td><strong>2</strong></td>
<td>IN1-</td>
<td>Analog Input. This is the negative terminal of a true differential input consisting of IN1+ and IN1-. V&lt;sub&gt;IN1&lt;/sub&gt; = (IN+ - IN-) IN1- can swing to, but not below, ground. See Section 1.0, Electrical Characteristics.</td>
</tr>
<tr>
<td><strong>3</strong></td>
<td>IN2+</td>
<td>Analog Input. This is the positive terminal of a true differential input consisting of IN2+ and IN2-. V&lt;sub&gt;IN2&lt;/sub&gt; = (IN2+ – IN-). See Section 1.0, Electrical Characteristics.</td>
</tr>
<tr>
<td><strong>4</strong></td>
<td>IN2-</td>
<td>Analog Input. This is the negative terminal of a true differential input consisting of IN2+ and IN2-. V&lt;sub&gt;IN2&lt;/sub&gt; = (IN+ – IN-) IN2- can swing to, but not below, ground. See Section 1.0, Electrical Characteristics.</td>
</tr>
<tr>
<td><strong>5</strong></td>
<td>PFI</td>
<td>Analog Input. This is the positive input to an internal comparator used as a threshold detector. The negative input is tied to an internal reference.</td>
</tr>
<tr>
<td><strong>6</strong></td>
<td>V&lt;sub&gt;TH&lt;/sub&gt;</td>
<td>Analog Input. This is the positive input to the internal comparator used to monitor the voltage supply. The negative input is tied to an internal reference. When V&lt;sub&gt;TH&lt;/sub&gt; falls below the internal reference, the reset generator drives RESET low. See Section 1.0, Electrical Characteristics.</td>
</tr>
<tr>
<td><strong>7</strong></td>
<td>REF&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Analog Input. The converter’s reference voltage is the differential between this pin and ground times two. It may be tied directly to REF&lt;sub&gt;OUT&lt;/sub&gt; or scaled using a resistor divider. Any user supplied reference voltage less than 1.25 may be used in place of REF&lt;sub&gt;OUT&lt;/sub&gt;.</td>
</tr>
<tr>
<td><strong>8</strong></td>
<td>GND</td>
<td>Ground Terminal.</td>
</tr>
<tr>
<td><strong>9</strong></td>
<td>REF&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>Analog Output. The internal reference connects to this pin. It may be scaled externally and tied to the REF&lt;sub&gt;IN&lt;/sub&gt; input to provide the converter’s reference voltage. Care must be taken in connecting external circuitry to this pin. This pin is in a high impedance state during Sleep mode.</td>
</tr>
<tr>
<td><strong>10</strong></td>
<td>SDAT</td>
<td>Digital Output (push-pull). This is the microPort™ serial data output. SDAT is driven low while the TC3401 is converting data, effectively providing a “busy” signal. After the conversion is complete, every high to low transition on the SCLK pin puts a bit from the resulting data word on the SDAT pin (from MSB to LSB).</td>
</tr>
<tr>
<td><strong>11</strong></td>
<td>PFO</td>
<td>Digital Output (open drain). This is the output of the internal threshold detector. When PFI is less than the internal reference, PFO is driven low.</td>
</tr>
<tr>
<td><strong>12</strong></td>
<td>ENABLE</td>
<td>Digital Input. When this input control is pulled low, the part is internally restarted. That is, any data conversion or data read sequence is cleared and the part goes into Sleep mode. When ENABLE returns high, the part resumes normal operation.</td>
</tr>
<tr>
<td><strong>13</strong></td>
<td>RESET</td>
<td>Digital Output (open drain). This is the output of the V&lt;sub&gt;DD&lt;/sub&gt; monitor reset generator. RESET is driven low when a Power-on Reset or Brown-out condition is detected. See Section 1.0, AC Electrical Characteristics.</td>
</tr>
<tr>
<td><strong>14</strong></td>
<td>ADDR</td>
<td>Digital Input. This input controls the analog input multiplexer to select one of two input channels. This address is latched at the falling edge of the SCLK, which starts an A/D conversion. (0 = Input 1, 1 = Input 2).</td>
</tr>
<tr>
<td><strong>15</strong></td>
<td>SCLK</td>
<td>Digital Input. This is the microPort™ serial clock input. The TC3401 comes out of Sleep mode and a conversion cycle begins when this pin is driven low. After the conversion starts, each additional falling edge (up to six) detected on SCLK for t&lt;sub&gt;s&lt;/sub&gt; seconds reduces the A/D resolution by one bit. When the conversion is complete, the data word can be shifted out on the SDAT pin by clocking the SCLK pin.</td>
</tr>
<tr>
<td><strong>16</strong></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>Power Supply Input.</td>
</tr>
</tbody>
</table>
3.0 DETAILED DESCRIPTION

The TC3401 has a 16-bit sigma-delta A/D converter. It has two differential inputs, an analog multiplexer, a VDD monitor with reset generator and an early warning Power Fail detector. See the Typical Application circuit and the Functional Block diagram. The key components of the TC3401 are described below.

Also refer to Figure 3-5, A/D Operational Flowchart and the Timing Diagrams, Figure 3-1, Figure 3-2 and Figure 3-3.

3.1 A/D Converter Operation

When the TC3401 is not converting, it is in Sleep mode with both the SCLK and SDAT lines high. An A/D conversion is initiated by a high to low transition on the SCLK line at which time the internal clock of the TC3401 is started and the address value (ADDR) is internally latched. The address value steers the analog multiplexer to select the input channel to be converted. Each additional high to low transition of SCLK (following the initial SCLK falling edge) during the time interval \( t_4 \) will decrement the conversion resolution by one bit and reduce the conversion time by one half. The time interval \( t_4 \) is referred to as the resolution reduction window. The minimum conversion resolution is 10-bits so any more than 6 SCLK transitions during \( t_4 \) will be ignored.

After each high to low transition of SCLK, in the \( t_4 \) interval, the SDAT output is driven high by the TC3401 to acknowledge that the resolution has been decremented. When the SCLK returns high or the \( t_4 \) interval ends, the SDAT line returns low (see Figure 3-2). When the conversion is complete SDAT is driven high. The TC3401 now enters Sleep mode and the conversion value can be read as a serial data word on the SDAT line.

3.2 Reading the Data Word

After the conversion is complete and SDAT goes high, the conversion value can be clocked serially onto the SDAT line by high to low transitions of the SCLK. The data word is in two's compliment format with the sign bit clocked onto the SDAT line, first followed by the MSB and ending in the LSB. For a 16-bit conversion the data word would consist of a sign bit followed by 15 magnitude bits, Table 3-1 shows the data word versus input voltage for a 16-bit conversion. Note that the full scale input voltage range is \( \pm (2 \cdot \text{REF}_{\text{IN}} - 1 \text{LSB}) \). When \( \text{REF}_{\text{OUT}} \) is fed back directly to \( \text{REF}_{\text{IN}} \), an LSB is 73\,\mu V for a 16-bit conversion, as \( \text{REF}_{\text{OUT}} \) is typically 1.193\,V.

Figure 3-4 shows typical SCLK and SDAT waveforms for 16, 12 and 10-bit conversions. Note that any complete convert and read cycle requires 17 negative edge clock pulses. The first is the convert command. Then, up to six of these can occur in the resolution reduction window, \( t_4 \), to decrement resolution. The remaining pulses clock out the conversion data word.

<table>
<thead>
<tr>
<th>Data Word</th>
<th>( \text{IN}^+ - \text{IN}^- ) (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 0000 0000 0001</td>
<td>72.8 E-6</td>
</tr>
<tr>
<td>1111 1111 1111 1111</td>
<td>2.38596 (Positive Full Scale)</td>
</tr>
<tr>
<td>1000 0000 0000 0000</td>
<td>0</td>
</tr>
<tr>
<td>0000 0000 0000 0000</td>
<td>-72.8 E-6</td>
</tr>
<tr>
<td>0111 1111 1111 1111</td>
<td>-2.38596 (Negative Full Scale)</td>
</tr>
<tr>
<td>1000 0000 0000 0000</td>
<td>Reserved Code</td>
</tr>
</tbody>
</table>

The SCLK input has a filter which rejects any positive or negative pulse of width less than 50\,nsec to reduce noise. The rejection width of this pulse can vary between 50\,nsec and 750\,nsec depending on processing parameters and supply voltage.

Figure 3-1 and Table 3-2 show information for determining the mode of operation for the TC3401 part by recording the value of SDAT for SCLK in a high, then low, then high state. For example, if SCLK goes through a 1-0-1 transition and the corresponding values of SDAT are 1-1-0, then the SCLK falling edge started a new data conversion. A 0-1-0 for SDAT would have indicated a resolution reduction had occurred. This is useful if the microcontroller has a Watchdog Reset or otherwise loses track of where the TC3401 is in the conversion and data readout sequence. The microcontroller can simply transition SCLK until it “finds” a Start Conversion condition.

**TABLE 3-1: DATA CONVERSION WORD VS. VOLTAGE INPUT (\( \text{REF}_{\text{IN}} = 1.193 \))**

**FIGURE 3-1: SCLK, SDAT LOGIC STATE DIAGRAM**

**TABLE 3-2: SCLK, SDAT LOGIC STATE**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>x</td>
<td>1</td>
<td>1</td>
<td>Data Transfer</td>
</tr>
<tr>
<td>x</td>
<td>0</td>
<td>0</td>
<td>Data Transfer or Busy*</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Start Conversion</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Resolution Reduction</td>
</tr>
</tbody>
</table>

*Note: The code X00 has a dual meaning: Data Transfer or Busy converting. To avoid confusion, the user should send only the required number of pulses for the desired resolution, then wait for SDAT to rise to 1, indicating conversion is complete before clocking SCLK again to read out data bits.*
FIGURE 3-2: CONVERSION AND DATA OUTPUT TIMING

FIGURE 3-3: RESET AND POWER FAIL TIMING
FIGURE 3-4: SCLK AND SDAT WAVEFORMS FOR 16, 12 AND 10-BIT CONVERSIONS

16-bit Data Conversion, Data Word A5A5h

SCLK

SDAT
t3a

Data Conversion Complete

16-bit Data Conversion, Long Start Pulse, Data Word 5A5Ah

SCLK

SDAT	> t3a

Data Conversion Complete

12-bit Conversion, Data Word = AB3h

SCLK

SDAT	< t4< t3e

Data Conversion Complete

10-bit Conversion with “Extra” Data Reduction Clocks, Data Word = 3A4h

SCLK

SDAT	< t4< t3g

Data Conversion Complete
FIGURE 3-5: A/D OPERATIONAL FLOWCHART

POR

Sleep
SDAT = High

SCLK
Hgh to Low?
Yes

Power Up Analog,
Start CONVCLK (= 0),
Start Conversion,
Resolution = 2m
(m = 16), Latch Input
Channel Address (if applicable).

SCLK
Low to High
transition?
Yes
SDAT = Low

CONVCLK < 2^9?
Yes

SDAT = High

A/D
Resolution
> 2^10?
Yes

Reduce A/D
Resolution by 1-bit
(m = m - 1);
SDAT = High

No

CONVCLK = 2^m?
(Conversion Done?)
Yes

Power Down Analog,
Conversion Complete,
SDAT = High

SCLK
Hgh to Low?
Yes

SDAT = Dm;
m = m - 1

m ≥ 0?
Yes

SDAT = High
Internal Reset

No

Sleep
3.3  $V_{DD}$ Monitor

The TC3401 RESET output is in high impedance provided the voltage at $V_{TH}$ is greater than the internal voltage reference. This reference is approximately the same value as the voltage appearing at REFOUT. When $V_{TH}$ is less than the internal reference, RESET is pulled low. When $V_{TH}$ rises above the internal reference voltage again, RESET is held low for the reset active time-out period, $t_9$, before being released. The RESET output is ensured to be valid for $V_{DD} = 1.3V$ to 5.5V.

When used to generate a Power-on or Brown-out Reset, an external resistor network is required to divide the appropriate $V_{DD}$ threshold down to 1.23V at the $V_{TH}$ input, (See the Typical Application circuit). For example, to generate a POR for a $V_{DD}$ at 3V -10%, the values of $R1$ and $R2$ should be 137k$\Omega$ and 115k$\Omega$ respectively.

Since RESET is an open drain, it can be wired-OR’ed with another open drain or external switch if desired.

3.4  Power Fail Detector

The Power Fail detector is a comparator in which the inverting input is connected to the internal voltage reference. The non-inverting input is the PFI pin of the TC3401 and the PFO pin is the active low, open drain output. This comparator is suitable as an early warning fail or low battery indicator. In a typical application, where a voltage regulator is being used to supply power to a system, the Power Fail comparator would monitor the input voltage to the regulator while the $V_{DD}$ monitor would measure the output voltage of the regulator. Both PFO and RESET would drive interrupt pins of a microcontroller.

The Power Fail detector may be used as a Wake-up or Watchdog Timer. The Typical Application circuit shows an RC network on PFI with the capacitor tied to a tristated $\mu$C I/O pin. If $R4$ is 1 M$\Omega$ and $C2$ is 10$\mu$F, the time constant is roughly ten seconds. The $\mu$C resets the RC network by driving the I/O tied to PFI low and then tristating it. The RC network will ramp to 1.23V in roughly 9 seconds, assuming a $V_{BATT}$ of 3.0V. With PFO tied to a $\mu$C input or interrupt, the $\mu$C will see a low to high transition on PFO when the voltage on PFI exceeds 1.23V. The PFO output is specified to be valid for $V_{DD} = 1.3$ to 5.5V.
4.0 PACKAGING INFORMATION

4.1 Package Marking Information
Package marking data not available at this time.

4.2 Taping Forms

Component Taping Orientation for 16-Pin QSOP (Narrow) Devices

<table>
<thead>
<tr>
<th>Package</th>
<th>Carrier Width (W)</th>
<th>Pitch (P)</th>
<th>Part Per Full Reel</th>
<th>Reel Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-Pin QSOP (N)</td>
<td>12 mm</td>
<td>8 mm</td>
<td>2500</td>
<td>13 in</td>
</tr>
</tbody>
</table>
4.3 Package Dimensions

16-Pin PDIP (Narrow)

Dimensions: inches (mm)

16-Pin QSOP (Narrow)

Dimensions: inches (mm)
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