MCP18480

-48V Hot Swap Controller

Features

- Allows safe board removal and insertion from a live backplane
- Accurate (<1.5%) internal voltage reference for fault detection and precision timing
- Programmable foldback current limiting
- Programmable circuit breaker current limiting
- Auto restart option for all faults
- Adjustable Undervoltage lockout thresholds
- Adjustable Overvoltage protection threshold
- Adjustable Power Good delay
- Configurable Power Good output polarity
- Low-side drive of an external N-channel FET

CMOS Technology

- High-Voltage Operation
- Temperature range: Industrial (I): -40°C to +85°C

Packaging

- 20-lead SSOP

Package Type

<table>
<thead>
<tr>
<th>SSOP</th>
</tr>
</thead>
<tbody>
<tr>
<td>VPOS</td>
</tr>
<tr>
<td>OVT</td>
</tr>
<tr>
<td>UVTH</td>
</tr>
<tr>
<td>UVHYS</td>
</tr>
<tr>
<td>VDD</td>
</tr>
<tr>
<td>VREFOUT</td>
</tr>
<tr>
<td>VREFIN</td>
</tr>
<tr>
<td>CL</td>
</tr>
<tr>
<td>ISET</td>
</tr>
<tr>
<td>TIMER</td>
</tr>
<tr>
<td></td>
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</tr>
</tbody>
</table>

Description

The MCP18480 is a Hot Swap controller that allows boards to be safely removed or inserted from an active backplane using -48V.

When PCBs are inserted into a live backplane, high-peak or transient currents from the source are generated due to the charging of the bypass capacitors on the supply. The high transient currents can destroy connectors and capacitors. The high inrush current can pull the input voltage BUS down and reset the system.

The MCP18480 solves this problem by controlling the slew rate of the backplane voltage to the board so that these transients are eliminated. This allows boards to be removed and inserted without causing damage to connector pins and input bulk capacitors, in addition to preventing false resets to the other boards on the backplane.

The MCP18480 can be used in applications in several areas including:

- Telecom Line Cards
- Network Switches
- Network Routers and Servers
- Base Station Line Cards
- Power-Over-LAN
- Power-Over-MDI
- IP Phone Switches/Routers
- Mid-Span, Power-Over-MDI

Two forms of current limit are provided in the MCP18480. These are:

- Foldback
- Circuit breaker

The foldback current-limiting circuit uses an external sense resistor and a voltage that is proportional to the external MOSFET's drain voltage. These are used to keep the MOSFET in its Safe Operating Area (SOA).

If the device remains in current limit for a programmed time period, the external N-channel FET is turned off. The option exists to configure the device to automatically restart after a programmed time delay. A programmable catastrophic current limit threshold shuts down the switch (circuit breaker) if excessive current is sensed due to a short-circuit condition.
Internal comparators are incorporated to add hysteresis for adjusting the Undervoltage Lockout (UVLO) threshold. The external N-channel MOSFET is turned on when the input is below the user-programmable, Overvoltage threshold and above the user-programmable, Undervoltage threshold.

The PWRGOOD pin indicates the status of the MCP18480 and is active when the device has completed power-up and the system is not in an Undervoltage, Overvoltage or current-limit condition.

PWRGOOD can be externally configured to either active-high or active-low to accommodate external circuitry (power supplies) that have either enabling logic.

A block diagram of the MCP18480 is shown below.

**MCP18480 Block Diagram**

**Note 1:** The PWRGOOD output pin can be either active-high or active-low. This polarity is determined by the voltage (either the level on the VREFIN pin or level on the VNEG pin) on the ISET pin:
- Connecting the external RSET resistor to VREFIN configures the PWRGOOD pin as active-low
- Connecting the external RSET resistor to VNEG configures the PWRGOOD pin as active-high

(Section 6.8.1)
(Section 6.8.2)
(Section 6.8.3)
(Section 6.8.4)
(Section 6.8.5)
(Section 6.8.6)
(Section 6.8.7)
(Section 6.8.8)
(Section 6.8.9)
1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient Temperature under bias</td>
<td>–40°C to +85°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>–65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage on VPOS with respect to VNEG</td>
<td>–0.3V to +15.0V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage on DV_TH, UV_TH, V_FB, OVO and UV_HYS pins with respect to VNEG</td>
<td>VNEG – 0.3V to (VPOS + 0.3V)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage on VREFIN, CL, SENSE, DRAIN_TH, ENABLE and RESTART pins with respect to VNEG</td>
<td>VNEG – 0.3V to 6V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Power Dissipation (Note 1)</td>
<td>800 mW</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max. Current out of VNEG pin</td>
<td>80 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max. Current into VPOS pin</td>
<td>50 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max. Output Current sunk by Gate pin</td>
<td>80 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max. Output Current sunk by VREFOUT pin</td>
<td>5 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max. Output Current sunk by any other Output pin</td>
<td>25 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max. Output Current sourced by Gate pin</td>
<td>200 µA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max. Output Current sourced by VREFOUT pin</td>
<td>5 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max. Output Current sourced by any other Output pin</td>
<td>25 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Power Dissipation is calculated as follows:

\[ P_{DIS} = V_{DD} \times (I_{DD} - \sum I_{OH}) + \sum (V_{DD} - V_{OH}) \times I_{OH} + \sum (V_{OL} \times I_{OL}) \]

DC CHARACTERISTICS

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Parameter</th>
<th>Sym</th>
<th>Min</th>
<th>Typ (1)</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>MD001</td>
<td>Current into shunt regulator that produces VPOS output voltage that meets MD001A specification</td>
<td>IPOS1</td>
<td>5</td>
<td>–</td>
<td>25</td>
<td>mA</td>
<td>ENABLE pin = 5V</td>
</tr>
<tr>
<td>MD001A</td>
<td>Regulated Output Voltage Differential of VPOS to VNEG</td>
<td>VPOS</td>
<td>10.4</td>
<td>12.0</td>
<td>13.4</td>
<td>V</td>
<td>See MD001</td>
</tr>
<tr>
<td>MD002</td>
<td>VREFOUT Pin output voltage</td>
<td>VREFOUT</td>
<td>2.463</td>
<td>2.5</td>
<td>2.538</td>
<td>V</td>
<td>Load = 50 µA</td>
</tr>
<tr>
<td>MD010</td>
<td>V_GATE pin output voltage</td>
<td>V_GATE</td>
<td>VPOS - 2</td>
<td>VPOS - 1</td>
<td>VPOS</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>MD011</td>
<td>Voltage on I_SET pin</td>
<td>V_SET</td>
<td>(VREFIN/2) - 0.02</td>
<td>VREFIN/2</td>
<td>(VREFIN/2) + 0.02</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>MD012A</td>
<td>Voltage on SENSE pin to trigger current-limiting</td>
<td>VSENSE</td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>mV</td>
<td>VFB = VNEG</td>
</tr>
<tr>
<td>MD012B</td>
<td></td>
<td></td>
<td>25</td>
<td>31.0</td>
<td>40</td>
<td>mV</td>
<td>VFB = VNEG + 0.25V</td>
</tr>
<tr>
<td>MD012C</td>
<td></td>
<td></td>
<td>7</td>
<td>12</td>
<td>17</td>
<td>mV</td>
<td>VFB = VNEG + 0.5V</td>
</tr>
<tr>
<td>MD013</td>
<td>Undervoltage Threshold</td>
<td>UV_TH</td>
<td>VREFIN - 0.03</td>
<td>VREFIN</td>
<td>VREFIN + 0.03</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>MD014A</td>
<td>Overvoltage Threshold rising</td>
<td>OV_TH</td>
<td>VREFIN - 0.05</td>
<td>VREFIN</td>
<td>VREFIN + 0.05</td>
<td>V</td>
<td>VREFIN = 2.5V</td>
</tr>
<tr>
<td>MD014B</td>
<td>Overvoltage Threshold falling</td>
<td>OV_TH</td>
<td>VREFIN - 0.035</td>
<td>VREFIN</td>
<td>VREFIN - 0.02</td>
<td>V</td>
<td>VREFIN = 2.5V</td>
</tr>
<tr>
<td>MD015</td>
<td>DRAIN Pin Input Threshold Voltage</td>
<td>V_DTH</td>
<td>90</td>
<td>100</td>
<td>130</td>
<td>mV</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Data in the Typical ("Typ") column is based on characterization results at +25°C. This data is for design guidance only and is not tested.

2: Negative current is defined as current sourced by the pin.

3: All voltages are with respect to the VNEG pin voltage.
## DC Characteristics (Continued)

<table>
<thead>
<tr>
<th>Electrical Specification:</th>
<th>Unless otherwise specified, operating temperature: –40°C ( \leq T_A \leq +85°C ) (Industrial), Supply Current: ( 5 \text{ mA} \leq I_{POS} \leq 25 \text{ mA} ), ( R_{ISET} = 125 \text{ kΩ} ), ( C_{BYP} = 2 \mu\text{F} )</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Param. No.</strong></td>
<td><strong>Parameter</strong></td>
</tr>
<tr>
<td>MD020</td>
<td>DRAIN pin current</td>
</tr>
<tr>
<td>MD021</td>
<td>SENSE pin current</td>
</tr>
<tr>
<td>MD022</td>
<td>GATE pin current Pull-up</td>
</tr>
<tr>
<td>MD022A</td>
<td>Pull-down</td>
</tr>
<tr>
<td>MD022B</td>
<td>Pull-down</td>
</tr>
<tr>
<td>MD022C</td>
<td>Pull-down</td>
</tr>
<tr>
<td>MD023</td>
<td>UV(_D) pin current</td>
</tr>
<tr>
<td>MD024A</td>
<td>TIMER pin current Pull-up</td>
</tr>
<tr>
<td>MD024B</td>
<td>Pull-down</td>
</tr>
<tr>
<td>MD025</td>
<td>ISET pin current</td>
</tr>
</tbody>
</table>

**Note:**
1: Data in the Typical ("Typ") column is based on characterization results at +25°C. This data is for design guidance only and is not tested.
2: Negative current is defined as current sourced by the pin.
3: All voltages are with respect to the \( V_{\text{NEG}} \) pin voltage.
## DC Characteristics (Continued)

**Electrical Specifications:** Unless otherwise specified, operating temperature: $-40°C \leq T_A \leq +85°C$ (Industrial),
Supply Current: $5\, mA \leq I_{POS} \leq 25\, mA$, $R_{IBSET} = 125\, k\Omega$, $C_{BYP} = 2\, \mu F$.

<table>
<thead>
<tr>
<th>Param #</th>
<th>Parameter</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>MD030</td>
<td>Input Low Voltage</td>
<td>$V_{IL}$</td>
<td>$V_{NEG}$</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>$V_{NEG} \leq 0.8, V$</td>
</tr>
<tr>
<td>MD031</td>
<td>ENABLE pin</td>
<td>$V_{NEG}$</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>$V_{NEG} \leq 0.8, V$</td>
<td></td>
</tr>
<tr>
<td>MD032</td>
<td>RESTART pin</td>
<td>$V_{NEG}$</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>$V_{NEG} \leq 0.8, V$</td>
<td></td>
</tr>
<tr>
<td>MD040</td>
<td>Input High Voltage</td>
<td>$V_{IH}$</td>
<td>2.0</td>
<td>—</td>
<td>5.0</td>
<td>V</td>
<td>$V_{IH} \leq 5.0, V$</td>
</tr>
<tr>
<td>MD041</td>
<td>ENABLE pin</td>
<td>$V_{NEG}$</td>
<td>—</td>
<td>5.0</td>
<td>V</td>
<td>$V_{NEG} \leq 5.0, V$</td>
<td></td>
</tr>
<tr>
<td>MD042</td>
<td>RESTART pin</td>
<td>$V_{NEG}$</td>
<td>—</td>
<td>5.0</td>
<td>V</td>
<td>$V_{NEG} \leq 5.0, V$</td>
<td></td>
</tr>
<tr>
<td>MD050</td>
<td>Internal Resistance on UVHYS pin</td>
<td>$R_{UVHYS}$</td>
<td>500</td>
<td>1200</td>
<td>2100</td>
<td>Ω</td>
<td>$V_{UVTH} &lt; V_{REFIN}$, $I_{UVHYS} = 30, \mu A$</td>
</tr>
<tr>
<td>MD051</td>
<td>Internal Resistance on UVHYS pin</td>
<td>$R_{UVHYS}$</td>
<td>50</td>
<td>100</td>
<td>—</td>
<td>MΩ</td>
<td>$V_{UVTH} &gt; V_{REFIN}$, $I_{UVHYS} = 30, \mu A$</td>
</tr>
<tr>
<td>MD060A</td>
<td>Input Leakage Current (Notes 2, 3)</td>
<td>$I_{IL}$</td>
<td>-1</td>
<td>—</td>
<td>+1</td>
<td>μA</td>
<td>$V_{NEG} \leq V_{PIN} \leq 11, V$, Pin at high-impedance</td>
</tr>
<tr>
<td>MD060B</td>
<td>Input Leakage Current (Notes 2, 3)</td>
<td>$V_{REFIN}$, CL, SENSE, DRAINTH, ENABLE and RESTART pins</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td>μA</td>
<td>$V_{NEG} \leq V_{PIN} \leq 5, V$, Pin at hi-impedance</td>
</tr>
<tr>
<td>MD070</td>
<td>Minimum current into ENABLE pin to disable MCP18480</td>
<td>$I_{EN}$</td>
<td>—</td>
<td>10</td>
<td>30</td>
<td>μA</td>
<td>$I_{POS} = 5, mA$, ENABLE = 0.8V</td>
</tr>
<tr>
<td>MD080</td>
<td>Output Low Voltage PWRGOOD pin</td>
<td>$V_{OL}$</td>
<td>0</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
<td>$I_{OL} = 5, mA$</td>
</tr>
<tr>
<td>MD090</td>
<td>Output High Voltage PWRGOOD pin</td>
<td>$V_{OH}$</td>
<td>0.8 $V_{POS}$</td>
<td>—</td>
<td>0.96 $V_{POS}$</td>
<td>$V_{POS}$</td>
<td>$I_{OH} = 2, mA$, $7, mA \leq I_{POS} \leq 12, mA$</td>
</tr>
<tr>
<td>MD100</td>
<td>Offset Voltage at the internal comparator input that is connected to the CL pin</td>
<td>$V_{CL}$</td>
<td>-15</td>
<td>—</td>
<td>+15</td>
<td>mV</td>
<td>$V_{FB} = 0$</td>
</tr>
</tbody>
</table>

**Note:**
1: All voltages are with respect to the $V_{NEG}$ pin voltage.
2: The leakage currents on the ENABLE and RESTART pins are strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
3: Negative current is defined as coming out of the pin.
## 1.1 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created using one of the following formats:

### 1.1.1 TIMING CONDITIONS

The temperature and voltages specified in Table 1-2 apply to all timing specifications, unless otherwise noted. Figure 1-1 specifies the load conditions for the timing specifications.

### TABLE 1-1: SYMBOLOGY

<table>
<thead>
<tr>
<th>1. TppS2ppS</th>
<th>2. TppS</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>T</td>
</tr>
<tr>
<td>F</td>
<td>T</td>
</tr>
<tr>
<td>E</td>
<td>T</td>
</tr>
</tbody>
</table>

Lowercase letters (pp) indicate the device pin.

### Uppercase letters and their meanings:

<table>
<thead>
<tr>
<th>S</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>P</td>
</tr>
<tr>
<td>FR</td>
<td>R</td>
</tr>
<tr>
<td>H</td>
<td>V</td>
</tr>
<tr>
<td>I</td>
<td>Z</td>
</tr>
<tr>
<td>L</td>
<td>Hi-impedance</td>
</tr>
</tbody>
</table>

### TABLE 1-2: AC TEMPERATURE AND VOLTAGE SPECIFICATIONS

<table>
<thead>
<tr>
<th>AC CHARACTERISTICS</th>
<th>Standard Operating Conditions (unless otherwise stated)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Operating temperature: $-40^\circ C \leq T_A \leq +85^\circ C$ (industrial)</td>
</tr>
<tr>
<td></td>
<td>Operating voltage $V_{DD}$ range as described in DC spec Section 1.0.</td>
</tr>
</tbody>
</table>
FIGURE 1-1:  Load Conditions for Device Timing Specifications.
1.2 Timing Diagrams and Specifications

**FIGURE 1-2:** Startup Waveforms.

**TABLE 1-3: STARTUP TIMING REQUIREMENTS**

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Parameter Description</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>MA000</td>
<td>$U_{TH} / O_{TH}$ High ($V_{POS}$ applied) to $DRAIN_{TH}$ falling</td>
<td>$T_{UOVH2DTHF}$</td>
<td>20.2</td>
<td></td>
<td></td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>MA001A</td>
<td>$DRAIN_{TH}$ falling to $PWRGOOD$ High</td>
<td>$T_{DTHF2GATEPGH}$</td>
<td>19.3</td>
<td></td>
<td></td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>MA001B</td>
<td>$DRAIN_{TH}$ falling to $GATE$ Fast Ramp</td>
<td>$T_{DTHF2GATEFR}$</td>
<td>13.1</td>
<td></td>
<td></td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>MA002</td>
<td>GATE Fast Ramp to external FET fully enhanced</td>
<td>$T_{GATEFR2FETE}$</td>
<td>16.1</td>
<td></td>
<td></td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** Minimum and maximum specifications will be provided in future revisions of this data sheet.

Note 1: This voltage is determined by the threshold voltage of the external FET. This voltage needs to ensure the external FET is fully enhanced.
FIGURE 1-3: 

**ENABLE-to-GATE Waveforms.**

**TABLE 1-4: ENABLE-TO-GATE TIMING REQUIREMENTS**

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Parameter</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>MA010</td>
<td>ENABLE Low to GATE Low</td>
<td>$T_{ENL2GATEL}$</td>
<td>—</td>
<td>23.6</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>MA011</td>
<td>ENABLE High to GATE Fast Ramp</td>
<td>$T_{ENH2GATEFR}$</td>
<td>—</td>
<td>41</td>
<td>—</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>MA012</td>
<td>GATE Fast Ramp to GATE High</td>
<td>$T_{GATEFR2GATEH}$</td>
<td>—</td>
<td>17.8</td>
<td>—</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** This voltage is determined by the threshold voltage of the external FET. This voltage needs to ensure the external FET is fully enhanced.

**Note 1:** This voltage is determined by the threshold voltage of the external FET. This voltage needs to ensure the external FET is fully enhanced.

**Note:** Minimum and maximum specifications will be provided in future revisions of this data sheet.
FIGURE 1-4: $O_{VTH}$-to-gate Waveform.

TABLE 1-5: $O_{VTH}$-TO-GATE TIMING REQUIREMENTS

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Parameter</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>MA020</td>
<td>$O_{VTH}$ High to GATE Low</td>
<td>$T_{OVT2GATEL}$</td>
<td>—</td>
<td>58.4</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>MA021</td>
<td>$O_{VTH}$ Low to GATE Fast Ramp</td>
<td>$T_{OVL2GATEFR}$</td>
<td>—</td>
<td>40.8</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>MA022</td>
<td>GATE Fast Ramp to GATE High</td>
<td>$T_{GATEFR2GATEH}$</td>
<td>—</td>
<td>17.8</td>
<td>—</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

Note: Minimum and maximum specifications will be provided in future revisions of this data sheet.

Note 1: This voltage is determined by the threshold voltage of the external FET. This voltage needs to ensure the external FET is fully enhanced.
TABLE 1-6: UV TH-TO-GATE TIMING REQUIREMENTS

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Parameter</th>
<th>Sym</th>
<th>Min</th>
<th>Typ(^{(1)})</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>MA030</td>
<td>UV TH Low to GATE Falling Edge</td>
<td>T(_{UVL2GATEF})</td>
<td>—</td>
<td>108</td>
<td>—</td>
<td>µs</td>
<td>C(_{UVD}) = 800 nF</td>
</tr>
<tr>
<td>MA031</td>
<td>GATE High to GATE Low</td>
<td>T(_{GATEH2GATEL})</td>
<td>25.8</td>
<td>—</td>
<td>25.8</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>MA032</td>
<td>ENABLE High to GATE Fast Ramp</td>
<td>T(_{UVH2GATEFR})</td>
<td>40.4</td>
<td>—</td>
<td>40.4</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>MA033</td>
<td>GATE Fast Ramp to GATE High</td>
<td>T(_{GATEFR2GATEH})</td>
<td>58.4</td>
<td>—</td>
<td>58.4</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C, unless otherwise stated.

2: Minimum and maximum specifications will be provided in future revisions of this data sheet.

Note: This voltage is determined by the threshold voltage of the external FET. This voltage needs to ensure the external FET is fully enhanced.

FIGURE 1-5: \(U_{TH}\)-to-gate Waveform

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Figure 1-6: Sense-to-gate Waveform.

Table 1-7: Sense-to-Gate Timing Requirements

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Parameter</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>MA041</td>
<td>GATE Current Limit to GATE Off</td>
<td>$T_{GATECL2GATEO}$</td>
<td>5.5</td>
<td>—</td>
<td>—</td>
<td>ms</td>
<td>$C_{\text{TIMER}} = 0.68 \mu F$ $R_{\text{SET}} = 124 , k\Omega$</td>
</tr>
<tr>
<td>MA042</td>
<td>GATE Current Limit Recovery</td>
<td>$T_{GATECL}$</td>
<td>10.2</td>
<td>—</td>
<td>—</td>
<td>ms</td>
<td>$C_{\text{TIMER}} = 0.68 \mu F$ $R_{\text{SET}} = 124 , k\Omega$</td>
</tr>
<tr>
<td>MA043</td>
<td>SENSE High to GATE Off</td>
<td>$T_{\text{SENSEH2GATEO}}$</td>
<td>3.6</td>
<td>—</td>
<td>—</td>
<td>ms</td>
<td>—</td>
</tr>
</tbody>
</table>

Note: Minimum and maximum specifications will be provided in future revisions of this data sheet.
Figure 1-7: Current Limit Waveform.

Table 1-8: Current Limit Timing Requirements

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Parameter</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>MA050</td>
<td>External Short to Timer period start</td>
<td>T_SHORT_2_TIMERS</td>
<td>—</td>
<td>171</td>
<td>—</td>
<td>mS</td>
<td></td>
</tr>
<tr>
<td>MA051</td>
<td>Timer period</td>
<td>T_TIMER_P</td>
<td>—</td>
<td>5.8</td>
<td>—</td>
<td>sec</td>
<td>C_TIMER = 0.68 (\mu)F, R_DISCH = 1.6 M(\Omega)</td>
</tr>
<tr>
<td>MA053</td>
<td>ENABLE High to Timer period start</td>
<td>T_ENABLE_H_2_TIMERS</td>
<td>—</td>
<td>30.5</td>
<td>—</td>
<td>mS</td>
<td>C_TIMER = 0.68 (\mu)F, R_DISCH = 1.6 M(\Omega)</td>
</tr>
<tr>
<td>MA054</td>
<td>RESTART Low to Timer period start</td>
<td>T_RESTART_L_2_TIMERS</td>
<td>—</td>
<td>30.9</td>
<td>—</td>
<td>mS</td>
<td>C_TIMER = 0.68 (\mu)F, R_DISCH = 11.6 M(\Omega)</td>
</tr>
<tr>
<td>MA055</td>
<td>External Short removed to Timer off</td>
<td>T_NO_SHORT_2_TIMERS_O</td>
<td>—</td>
<td>5.8</td>
<td>—</td>
<td>sec</td>
<td>C_TIMER = 0.68 (\mu)F, R_DISCH = 1.6 M(\Omega)</td>
</tr>
</tbody>
</table>

Note 1: Minimum and maximum specifications will be provided in future revisions of this data sheet.

Note 2: This is up to one additional timer period because the external short circuit is removed asynchronously to the timer. The timer must time out before normal operation returns.
2.0 DC CHARACTERISTIC CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**FIGURE 2-1:** Supply Current ($I_{POS}$) vs. Supply Voltage ($V_{POS}$).

Data taken with the minimum following conditions:
$V_{REFIN} = 2.5V$, $I_{SET} = 10 \mu A$

**FIGURE 2-2:** Minimum Supply Current vs. Temperature.

Data taken with the minimum following conditions:
Minimum Supply Current to bring $V_{POS}$ into regulation
$V_{REFIN} = 2.5V$, $I_{SET} = 10 \mu A$
FIGURE 2-3: GATE Output High-Voltage \( (V_{POS} - V_{GATE}) \) vs. Supply Current \( (I_{POS}) \).

Data taken with the minimum following conditions:
3 mA \( \leq I_{POS} \leq 30 \) mA

\( V_{REFIN} = 2.5V, I_{SET} = 10 \) µA

**Note 1:**
- \( V_{UVTH} > V_{VREFIN} \)
- \( V_{OVTH} < V_{VREFIN} \)
- \( V_{SENSE} = V_{VNEG} \)
- \( V_{VFB} = V_{VNEG} \)
- \( V_{DRAINTH} = V_{VNEG} \)
- \( V_{OVO} = V_{VNEG} \)
- \( V_{CL} = V_{VREFIN} \)
- \( V_{ENABLE} = 5V \) (open)
- \( V_{RESTART} = V_{VNEG} \) (open)

FIGURE 2-4: GATE Output Low-Voltage \( (V_{GATE} - V_{NEG}) \) vs. Supply Current \( (I_{POS}) \).

Data taken with the minimum following conditions:
3 mA \( \leq I_{POS} \leq 30 \) mA

\( V_{REFIN} = 2.5V, I_{SET} = 10 \) µA

**Note 1:**
- \( V_{UVTH} > V_{VREFIN} \)
- \( V_{OVTH} < V_{VREFIN} \)
- \( V_{SENSE} = V_{VNEG} \)
- \( V_{VFB} = V_{VNEG} \)
- \( V_{DRAINTH} = V_{VNEG} \)
- \( V_{OVO} = V_{VNEG} \)
- \( V_{CL} = V_{VREFIN} \)
- \( V_{ENABLE} = V_{VNEG} \)
- \( V_{RESTART} = V_{VNEG} \) (open)
Data taken with the minimum following conditions:

- **IPOS** = 5 mA
  (Enables **VPOS** at its self-regulating voltage)
- **VREFIN** = 2.5V, **ISET** = 10 µA

**Note 1:**

- **VUVTH** > **VREFIN**
- **VOVTH** < **VREFIN**
- **VSENSE** = **VNNEG**
- **VFBB** = **VNNEG**
- **VDRAINTH** = **VNNEG**
- **VOVO** = **VNNEG**
- **VCL** = **VREFIN**
- **VENABLE** = 5V (open)

**FIGURE 2-5:** GATE Source (Pull-Up) Current vs. Temperature.

Data taken with the minimum following conditions:

- **IPOS** = 5 mA
  (Enables **VPOS** at its self-regulating voltage)
- **VREFIN** = 2.5V, **ISET** = 10 µA

**Note 1:**

- **VGATE** > 0.5V
- **VUVTH** > **VREFIN**
- **VOVTH** < **VREFIN**
- **VSENSE** = **VNNEG**
- **VFBB** = **VNNEG**
- **VDRAINTH** = **VNNEG**
- **VOVO** = **VNNEG**
- **VCL** = **VREFIN**
- **VENABLE** = **VNNEG** (open)

**FIGURE 2-6:** GATE Sink (Pull-Down) Current vs. Temperature.
FIGURE 2-7: GATE Source Current vs. \( I_{SET} \) Pin Current.

Data taken with the minimum following conditions:
- \(-50 \, \mu A < I_{SET} < 50 \, \mu A \) (\( I_{SET} \neq 0 \))
- \( I_{POS} = 5 \, mA \)
  (Enables \( V_{POS} \) at its self-regulating voltage)
- \( V_{REFIN} = 2.5V \)

**Note 1:**
- \( V_{GATE} > 0.5V \)
- \( V_{UVTH} > V_{VREFIN} \)
- \( V_{OVTH} < V_{VREFIN} \)
- \( V_{SENSE} = V_{VNEG} \)
- \( V_{VFB} = V_{VNEG} \)
- \( V_{DRAINTH} = V_{VNEG} \)
- \( V_{VO} = V_{VNEG} \)
- \( V_{CL} = V_{VREFIN} \)
- \( V_{ENABLE} = 5V \) (open)
- \( V_{RESTART} = V_{VNEG} \) (open)

FIGURE 2-8: PWRGOOD Output Low Voltage \( (V_{OL}) \) vs. Temperature.

Data taken with the minimum following conditions:
- \( I_{LOAD} = 1 \, mA \)
- \( I_{POS} = 5 \, mA \)
  (Enables \( V_{POS} \) at its self-regulating voltage)
- \( V_{REFIN} = 2.5V, I_{SET} = 10 \, \mu A \)

**Note 1:**
- \( V_{UVTH} > V_{VREFIN} \)
- \( V_{OVTH} < V_{VREFIN} \)
- \( V_{SENSE} = V_{VNEG} \)
- \( V_{VFB} = V_{VNEG} \)
- \( V_{DRAINTH} = V_{VNEG} \)
- \( V_{VO} = V_{VNEG} \)
- \( V_{CL} = V_{VREFIN} \)
- \( V_{ENABLE} = 5V \) (open)
- \( V_{RESTART} = V_{VNEG} \) (open)
Data taken with the minimum following conditions:

ILOAD = -1 mA
IPOS = 5 mA
(Enables VPOS at its self-regulating voltage)
VREFIN = 2.5V, ISET = 10 µA

Note 1:
VUVTH > VVREFIN
VOVTH < VVREFIN
VSENSE = VVNEG
VFB = VVNEG
VDRAIN = VVNEG
VVO = VVNEG
VCL = VVREFIN
VENABLE = 5V (open)
VRESTART = VVNEG (open)

**FIGURE 2-9:** PWRGOOD Output High-Voltage (VOH) vs. Temperature.

Data taken with the minimum following conditions:

IPOS = 5 mA
(Enables VPOS at its self-regulating voltage)
VREFIN = 2.5V, ISET = 10 µA

Note 1:
VUVTH > VVREFIN
VOVTH < VVREFIN
VSENSE = VVNEG
VFB = VVNEG
VDRAIN = VVNEG
VVO = VVNEG
VCL = VVREFIN
VENABLE = 5V (open)
VRESTART = VVNEG (open)

**FIGURE 2-10:** PWRGOOD Output High-Impedance vs. Temperature.
Data taken with the minimum following conditions:

I_{POS} = 5 \, mA  
(Enables V_{POS} at its self-regulating voltage) 
V_{REFIN} = 2.5V, I_{SET} = 10 \, \mu A

**Note 1:**

V_{UVTH} > V_{VREFIN}  
V_{OVTH} < V_{VREFIN}  
V_{SENSE} = V_{VNEG}  
V_{VFB} = V_{VNEG}  
V_{DRAIN} = V_{VNEG}  
V_{OVO} = V_{VNEG}  
V_{CL} = V_{VREFIN}  
V_{ENABLE} = 5V (open)  
V_{RESTART} = V_{VNEG} (open)

**FIGURE 2-11:** PWRGOOD Output Low-Impedance vs. Temperature.
Data taken with the minimum following conditions:
3 mA ≤ IPOS ≤ 30 mA
VREFIN = 2.5V, ISET = 10 µA

**FIGURE 2-12:** $V_{\text{REFOUT}}$ vs. Supply Current (IPOS).

Data taken with the minimum following conditions:
IPOS = 5 mA
(Enables $V_P$ at its self-regulating voltage)
VREFIN = 2.5V, Iset = 10 µA

**FIGURE 2-13:** $V_{\text{REFOUT}}$ vs. LOAD.
Data taken with the minimum following conditions:
-50 µA < I_SET < 50 µA (I_SET ≠ 0)
I_POS = 5 mA
(Enables V_POS at its self-regulating voltage)
V_REFIN = 2.5V

Note 1:
V_UVTH > V_REFIN
V_OKTH < V_REFIN
VSENSE = V_NEG
VF = V_NEG
VDRAINTH = V_NEG
VOO = V_NEG
V_CL = V_REFIN
VENABLE = 5V (open)
V_RESTART = V_NEG (open)

FIGURE 2-14: TIMER Pin Output Low Current vs. R_DISCH Current.

FIGURE 2-15: TIMER Pin Output High Current vs. I_SET Current.
Data taken with the minimum following conditions:

-50 µA < I_{SET} < 50 µA (I_{SET} ≠ 0)
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V

**Note 1:**
- V_{UVTH} < V_{VREFIN}
- V_{OVTH} < V_{VREFIN}
- V_{SENSE} = V_{VNEG}
- V_{VF} = V_{VNEG}
- V_{DRAIN\_TH} = V_{VNEG}
- V_{OVO} = V_{VNEG}
- V_{CL} = V_{VNEG}
- V_{ENABLE} = 5V (open)
- V_{RESTART} = V_{VNEG} (open)

**FIGURE 2-16:** UV_{D} Pin Current vs. I_{SET} Pin Current.

**FIGURE 2-17:** I_{SET} Pin Voltage vs. V_{REFIN} Pin Voltage.

Data taken with the minimum following conditions:

3 mA ≤ I_{POS} ≤ 30 mA
V_{REFIN} = 2.5V, I_{SET} = 10 µA
Determined by PWRGOOD signal

**Note 1:**
- V_{UVTH} > V_{VREFIN}
- V_{OVTH} < V_{VREFIN}
- V_{SENSE} = V_{VNEG}
- V_{VF} = V_{VNEG}
- V_{OVO} = V_{VNEG}
- V_{CL} = V_{VNEG}
- V_{ENABLE} = 5V (open)
- V_{RESTART} = V_{VNEG} (open)

**FIGURE 2-18:** DRAIN\_TH Threshold Voltage vs. Supply current (I_{POS}).
FIGURE 2-19: \( R_{DISCH} \) Current vs. Supply Current (\( I_{POS} \)).

Data taken with the minimum following conditions:
- \( I_{POS} = 5 \) mA
  (Enables \( V_{POS} \) at its self-regulating voltage)
- \( V_{REFIN} = 2.5 \) V, \( I_{SET} = 10 \) \( \mu \)A
- \( R_{DISCH} = 16 \) M\( \Omega \)

Note 1:
- \( V_{UVTH} > V_{VREFIN} \)
- \( V_{OVTH} < V_{VREFIN} \)
- \( V_{SENSE} = V_{VNEG} \)
- \( V_{VFB} = V_{VNEG} \)
- \( V_{DRAINTH} = V_{VNEG} \)
- \( V_{OVO} = V_{VNEG} \)
- \( V_{CL} = V_{VREFIN} \)
- \( V_{ENABLE} = 5 \) V (open)
- \( V_{RESTART} = V_{VNEG} \) (open)

FIGURE 2-20: \( R_{DISCH} \) Voltage vs. \( R_{DISCH} \) Current.

Data taken with the minimum following conditions:
- \( I_{POS} = 5 \) mA
  (Enables \( V_{POS} \) at its self-regulating voltage)
- \( V_{REFIN} = 2.5 \) V, \( I_{SET} = 10 \) \( \mu \)A
- \( I_{DISCH} \) from 100 nA to 10 \( \mu \)A (500 nA steps)

Note 1:
- \( V_{UVTH} > V_{VREFIN} \)
- \( V_{OVTH} < V_{VREFIN} \)
- \( V_{SENSE} = V_{VNEG} \)
- \( V_{VFB} = V_{VNEG} \)
- \( V_{DRAINTH} = V_{VNEG} \)
- \( V_{OVO} = V_{VNEG} \)
- \( V_{CL} = V_{VREFIN} \)
- \( V_{ENABLE} = 5 \) V (open)
- \( V_{RESTART} = V_{VNEG} \) (open)
Data taken with the minimum following conditions:

I_{POS} = 5 mA  
(Enables V_{POS} at its self-regulating voltage)

V_{REFIN} = 2.5V, I_{SET} = 10 \mu A  
Determined by GATE voltage

**Note 1:**

- \( V_{UVTH} > V_{VREFIN} \)
- \( V_{OVTH} < V_{VREFIN} \)
- \( V_{SENSE} = V_{VNEG} \)
- \( V_{VFB} = V_{VNEG} \)
- \( V_{DRAINTH} = V_{VNEG} \)
- \( V_{DVO} = V_{VNEG} \)
- \( V_{CL} = V_{VREFIN} \)
- \( V_{RESTART} = V_{VNEG} \) (open)

**FIGURE 2-21:** \( \textit{ENABLE/RESTART Pin Trip} \)  
**Point Voltage vs. Temperature.**
Data taken with the minimum following conditions:

**Note 1:**

- \( V_{UVTH} > V_{VREFIN} \)
- \( V_{OVTH} < V_{VREFIN} \)
- \( V_{SENSE} = V_{NEG}, \) I into device
- \( V_{NEG} + 100mV, \) I out of device
- \( V_{VFB} = V_{VNEG} \)
- \( V_{DRAINTH} = V_{VNEG} \)
- \( V_{OVO} = V_{VNEG} \)
- \( V_{CL} = V_{VREFIN} \)
- \( V_{ENABLE} = 5V \) (open)
- \( V_{RESTART} = V_{VNEG} \) (open)

**FIGURE 2-22:**  
**TIMER Output Sink Current vs. Temperature.**

**FIGURE 2-23:**  
**TIMER Output Source Current vs. Temperature.**
FIGURE 2-24:  CL pin Input Offset Voltage vs. Temperature.

Data taken with the minimum following conditions:

\[ I_{\text{POS}} = 5 \text{ mA} \]  
(Enables \( V_{\text{POS}} \) at its self-regulating voltage)

\[ V_{\text{REFIN}} = 2.5V, \ I_{\text{SET}} = 10 \mu A \]

**Note 1:**

\[ V_{\text{UVTH}} > V_{\text{REFIN}} \]
\[ V_{\text{OVTH}} < V_{\text{REFIN}} \]
\[ V_{\text{SENSE}} = 25mV \]
\[ V_{\text{VFB}} = V_{\text{VNEG}} \]
\[ V_{\text{DRAINTH}} = V_{\text{VNEG}} \]
\[ V_{\text{DRAINTH}} = V_{\text{VNEG}} \]
\[ V_{\text{ENABLE}} = 5V \text{ (open)} \]
\[ V_{\text{RESTAR}} = V_{\text{VNEG}} \text{ (open)} \]

FIGURE 2-25:  SENSE Pin Input Threshold vs. Temperature.

Data taken with the minimum following conditions:

\[ I_{\text{POS}} = 5 \text{ mA} \]  
(Enables \( V_{\text{POS}} \) at its self-regulating voltage)

\[ V_{\text{REFIN}} = 2.5V, \ I_{\text{SET}} = 10 \mu A \]

Use TIMER pin as indicator

**Note 1:**

\[ V_{\text{UVTH}} > V_{\text{REFIN}} \]
\[ V_{\text{OVTH}} < V_{\text{REFIN}} \]
\[ V_{\text{VFB}} = V_{\text{NEG}}, V_{\text{NEG}+250mV}, V_{\text{NEG}+500mV}, V_{\text{NEG}+1V} \]
\[ V_{\text{DRAINTH}} = V_{\text{VNEG}} \]
\[ V_{\text{DRAINTH}} = V_{\text{VNEG}} \]
\[ V_{\text{ENABLE}} = 5V \text{ (open)} \]
\[ V_{\text{RESTAR}} = V_{\text{VNEG}} \text{ (open)} \]
FIGURE 2-26:  $OV_{TH}$ Input Rising Threshold vs. OVO Voltage.

Data taken with the minimum following conditions:

$I_{POS} = 5 \text{ mA}$  
(Enables $V_{POS}$ at its self-regulating voltage)

$OVO = V_{NEG}$ to 8V

$V_{REFIN} = 2.5V$, $I_{SET} = 10 \mu A$

Use PWRGOOD pin as indicator

Note 1:

$V_{UVTH} > V_{VREFIN}$

$V_{SENSE} = V_{VNEG}$

$V_{FFB} = V_{VNEG}$

$V_{DRAINTH} = V_{VNEG}$

$V_{CL} = V_{VREFIN}$

$V_{ENABLE} = 5V$ (open)

$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-27:  $OV_{TH}$ Input Falling Threshold vs. OVO Voltage.

Data taken with the minimum following conditions:

$I_{POS} = 5 \text{ mA}$  
(Enables $V_{POS}$ at its self-regulating voltage)

$OVO = V_{NEG}$ to 8V

$V_{REFIN} = 2.5V$, $I_{SET} = 10 \mu A$

Use PWRGOOD pin as indicator

Note 1:

$V_{UVTH} > V_{VREFIN}$

$V_{SENSE} = V_{VNEG}$

$V_{FFB} = V_{VNEG}$

$V_{DRAINTH} = V_{VNEG}$

$V_{CL} = V_{VREFIN}$

$V_{ENABLE} = 5V$ (open)

$V_{RESTART} = V_{VNEG}$ (open)
Data taken with the minimum following conditions:

- \( I_{POS} = 5 \text{ mA} \)  
  (Enables \( V_{POS} \) at its self-regulating voltage)
- \( V_{REFIN} = 2.5V, I_{SET} = 10 \mu A \)

**Note 1:**
- \( V_{UVTH} < V_{VREFIN} \)
- \( V_{OVTH} < V_{VREFIN} \)
- \( V_{SENSE} = V_{VNEG} \)
- \( V_{VFB} = V_{VNEG} \)
- \( V_{DRAINTH} = V_{VNEG} \)
- \( V_{DOV} = V_{VNEG} \)
- \( V_{CL} = V_{VREFIN} \)
- \( V_{ENABLE} = 5V \) (open)
- \( V_{RESTART} = V_{VNEG} \) (open)

**FIGURE 2-28:** \( UV_D \) Current vs. Supply Current (\( I_{POS} \)).

Data taken with the minimum following conditions:

- \( I_{POS} = 5 \text{ mA} \)  
  (Enables \( V_{POS} \) at its self-regulating voltage)
- \( V_{TH} < V_{VREFIN}, \ UV_{TH} > V_{VREFIN} \)
- \( V_{REFIN} = 2.5V, I_{SET} = 10 \mu A \)

**Note 1:**
- \( V_{OVTH} < V_{VREFIN} \)
- \( V_{SENSE} = V_{VNEG} \)
- \( V_{VFB} = V_{VNEG} \)
- \( V_{DRAINTH} = V_{VNEG} \)
- \( V_{DOV} = V_{VNEG} \)
- \( V_{CL} = V_{VREFIN} \)
- \( V_{ENABLE} = 5V \) (open)
- \( V_{RESTART} = V_{VNEG} \) (open)

**FIGURE 2-29:** \( UV_{HYS} \) Pin Impedance vs. Temperature.
Data taken with the minimum following conditions:

\( I_{POS} = 5 \, \text{mA} \)
(Enables \( V_{POS} \) at its self-regulating voltage)
\( V_{REFIN} = 2.5V, \, I_{SET} = 10 \, \mu A \)
Use PWRGOOD pin as indicator

**Note 1:**

\( V_{OVTH} < V_{VREFIN} \)
\( V_{SENSE} = V_{VNEG} \)
\( V_{VFB} = V_{VNEG} \)
\( V_{DRAINTH} = V_{VNEG} \)
\( V_{OVO} = V_{VNEG} \)
\( V_{CL} = V_{VREFIN} \)
\( V_{ENABLE} = 5V \) (open)
\( V_{RESTART} = V_{VNEG} \) (open)

**FIGURE 2-30:** \( UV_{TH} \) Input Rising Threshold vs. Temperature.

Data taken with the minimum following conditions:

\( I_{POS} = 5 \, \text{mA} \)
(Enables \( V_{POS} \) at its self-regulating voltage)
\( V_{REFIN} = 2.5V, \, I_{SET} = 10 \, \mu A \)
Use PWRGOOD pin as indicator

**Note 1:**

\( V_{OVTH} < V_{VREFIN} \)
\( V_{SENSE} = V_{VNEG} \)
\( V_{VFB} = V_{VNEG} \)
\( V_{DRAINTH} = V_{VNEG} \)
\( V_{OVO} = V_{VNEG} \)
\( V_{CL} = V_{VREFIN} \)
\( V_{ENABLE} = 5V \) (open)
\( V_{RESTART} = V_{VNEG} \) (open)

**FIGURE 2-31:** \( UV_{TH} \) Input Falling Threshold vs. Temperature.
Data taken with the minimum following conditions:

- $I_{\text{POS}} = 5 \text{ mA}$
  (Enables $V_{\text{POS}}$ at its self-regulating voltage)
- $V_{\text{REFIN}} = 2.5V$, $I_{\text{SET}} = 10 \mu\text{A}$
- Use PWRGOOD pin as indicator

**Note 1:**

- $V_{\text{OVTH}} < V_{\text{REFIN}}$
- $V_{\text{SENSE}} = V_{\text{NEG}}$
- $V_{\text{VFB}} = V_{\text{NEG}}$
- $V_{\text{DRAINTH}} = V_{\text{NEG}}$
- $V_{\text{VOO}} = V_{\text{NEG}}$
- $V_{\text{CL}} = V_{\text{REFIN}}$
- $V_{\text{ENABLE}} = 5V$ (open)
- $V_{\text{RESTART}} = V_{\text{NEG}}$ (open)

**FIGURE 2-32:** $OV_{\text{TH}}$ Input Rising Threshold vs. Temperature.

Data taken with the minimum following conditions:

- $I_{\text{POS}} = 5 \text{ mA}$
  (Enables $V_{\text{POS}}$ at its self-regulating voltage)
- $V_{\text{REFIN}} = 2.5V$, $I_{\text{SET}} = 10 \mu\text{A}$
- $V_{\text{UVHYS}} = V_{\text{NEG}}$
- Use PWRGOOD pin as indicator

**Note 1:**

- $V_{\text{OVTH}} < V_{\text{REFIN}}$
- $V_{\text{SENSE}} = V_{\text{NEG}}$
- $V_{\text{VFB}} = V_{\text{NEG}}$
- $V_{\text{DRAINTH}} = V_{\text{NEG}}$
- $V_{\text{VOO}} = V_{\text{NEG}}$
- $V_{\text{CL}} = V_{\text{REFIN}}$
- $V_{\text{ENABLE}} = 5V$ (open)
- $V_{\text{RESTART}} = V_{\text{NEG}}$ (open)

**FIGURE 2-33:** $OV_{\text{TH}}$ Input Falling Threshold vs. Temperature.
### 3.0 PIN DESCRIPTIONS

#### TABLE 3-1: MCP18480 PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Direction</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;POS&lt;/sub&gt;</td>
<td>1</td>
<td>I</td>
<td>P</td>
<td>Positive supply input. Internal Shunt Regulator connected between V&lt;sub&gt;POS&lt;/sub&gt; and V&lt;sub&gt;NEG&lt;/sub&gt; limits the potential to 12V between these two pins. A series resistor must be placed on the V&lt;sub&gt;POS&lt;/sub&gt; pin to limit the current into the device.</td>
</tr>
<tr>
<td>OV&lt;sub&gt;TH&lt;/sub&gt;</td>
<td>2</td>
<td>I</td>
<td>A</td>
<td>Overvoltage protection threshold. An external resistor divider network is connected to this input pin to program the overvoltage protection threshold. The selected external resistor values for the OV&lt;sub&gt;TH&lt;/sub&gt; to system ground and OV&lt;sub&gt;TH&lt;/sub&gt; to V&lt;sub&gt;NEG&lt;/sub&gt; resistors should have currents in the 1 mA range. A typical Overvoltage threshold is -76V. Internal hysteresis in the overvoltage input comparator will allow proper operation once V&lt;sub&gt;NEG&lt;/sub&gt; falls below the selected threshold.</td>
</tr>
<tr>
<td>UV&lt;sub&gt;TH&lt;/sub&gt;</td>
<td>3</td>
<td>I</td>
<td>A</td>
<td>Undervoltage lockout threshold. An external resistor divider network is connected to this input pin to program the undervoltage lockout threshold. If the voltage on UV&lt;sub&gt;TH&lt;/sub&gt; is less than V&lt;sub&gt;NEG&lt;/sub&gt; + 2.5V, the undervoltage comparator will trip, indicating an Undervoltage condition. An external hysteresis resistor can be used to set the high-to-low (V&lt;sub&gt;THF&lt;/sub&gt;) threshold below the low-to-high (V&lt;sub&gt;THR&lt;/sub&gt;) threshold. For telecom network equipment, it is desirable to have shutdown occur at -38.5V and the startup set at -43.0V.</td>
</tr>
<tr>
<td>UV&lt;sub&gt;HYS&lt;/sub&gt;</td>
<td>4</td>
<td>I</td>
<td>A</td>
<td>Undervoltage internal comparator hysteresis. An external resistor is connected between this input to the UV&lt;sub&gt;TH&lt;/sub&gt; input pin to adjust the hysteresis of the internal Undervoltage comparator. Since it is desirable to shut down at -38.5V and restart at -43.0V in telecom switch equipment.</td>
</tr>
<tr>
<td>UV&lt;sub&gt;D&lt;/sub&gt;</td>
<td>5</td>
<td>I/O</td>
<td>A</td>
<td>Undervoltage event delay. An external capacitor is connected to this input pin to set the delay between when the UV&lt;sub&gt;TH&lt;/sub&gt; pin drops below the trip point specified by the voltage on the V&lt;sub&gt;REFIN&lt;/sub&gt; pin and when the system shutdown occurs (causing the PWRGOOD pin to be driven to an inactive level and the GATE pin to be pulled to the V&lt;sub&gt;NEG&lt;/sub&gt; pin voltage level). The UV&lt;sub&gt;D&lt;/sub&gt; pin sources a current equivalent to the I&lt;sub&gt;ISET&lt;/sub&gt; (in typical applications, the I&lt;sub&gt;ISET&lt;/sub&gt; current equals 10 µA), which charges this external capacitor while an internal comparator compares this voltage on the UV&lt;sub&gt;D&lt;/sub&gt; pin to</td>
</tr>
</tbody>
</table>

Legend: TTL = TTL compatible input  ST = Schmitt Trigger input with CMOS levels  I = Input  O = Output  P = Power  CMOS = CMOS-compatible input  A = Analog  D = Digital
### MCP18480 PIN DESCRIPTIONS (CONTINUED)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Direction</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{REFOUT}} )</td>
<td>6</td>
<td>O</td>
<td>A</td>
<td>Reference output. Internal reference output voltage (typically 2.5V). Usually tied back to the ( V_{\text{REFIN}} ) pin unless an external high-precision reference voltage is desired.</td>
</tr>
<tr>
<td>( V_{\text{REFIN}} )</td>
<td>7</td>
<td>I</td>
<td>A</td>
<td>Reference input. This pin allows a high-precision reference voltage for the following functions: - Undervoltage Comparator - Overvoltage Comparator - DRAIN Comparator - Current Limit Timer If the precision of the ( V_{\text{REFOUT}} ) output voltage is acceptable, tie the ( V_{\text{REFOUT}} ) pin to the ( V_{\text{REFIN}} ) pin.</td>
</tr>
<tr>
<td>CL</td>
<td>8</td>
<td>I</td>
<td>A</td>
<td>Current Limit. Input used to set the maximum current limit threshold allowed by the system via a resistor divider network (with the resistor ( R_{\text{CL1}} ) between the ( V_{\text{REFIN}} ) pin and the CL pin and resistor ( R_{\text{CL}} ) between the ( V_{\text{NEG}} ) pin and the CL pin). If the voltage across the sense resistor exceeds the voltage on the CL pin, it implies that there is excessive current over the allowed limit and forces the GATE pin to the ( V_{\text{NEG}} ) pin voltage level without delay.</td>
</tr>
<tr>
<td>ISET</td>
<td>9</td>
<td>I</td>
<td>A</td>
<td>Current source set. Establishes the internal ISOURCE for the following: - Undervoltage Delay - Current Limit Timer - GATE Pin Source Current An external resistor ( R_{\text{ISET}} ) from the ISET pin must be connected to either the ( V_{\text{NEG}} ) pin or the ( V_{\text{REFIN}} ) pin to set ( I_{\text{BIAS}} ), which will then establish the current sources throughout the device. The ( I_{\text{BIAS}} ) current is the same for either connection. Connecting the ( R_{\text{ISET}} ) resistor to the ( V_{\text{NEG}} ) pin will establish the PWRGOOD pin output polarity to be active-high. Connecting the ( R_{\text{ISET}} ) resistor to the ( V_{\text{REFIN}} ) pin will establish the PWRGOOD pin output polarity to be active-low.</td>
</tr>
</tbody>
</table>

Legend: TTL = TTL compatible input | ST = Schmitt Trigger input with CMOS levels |
I = Input | O = Output |
P = Power | CMOS = CMOS-compatible input |
A = Analog | D = Digital
The value of the external capacitor (CTIMER) connected to the TIMER pin sets the two time periods used during a current-limit event. These are:

- The time that the GATE pin will limit the current through the external FET
- The time that the GATE pin will disable the external FET

During current limit, a pull-up current source charges up the external capacitor. Until the voltage on the TIMER pin reaches VREFIN/2, the GATE pin is driven to maintain a reduced current flow determined by the VDS of the external FET.

While the capacitor is being discharged by the pull-down current (pull-up current is off), the GATE pin is at VNEG and the PWRGOOD pin is deasserted. When the TIMER voltage falls below approximately 100 mV, the GATE pin turns on, if the RESTART pin is low, to reset the internal fault latch. If the RESTART pin is high, the GATE pin remains off until the ENABLE pin is forced low. It is then forced high or the RESTART pin is forced low (asserted).

The PWRGOOD pin reasserts after the voltages on the DRAINTH and GATE pins meet the appropriate conditions.

The TIMER pin pull-up current is proportioned to the ISET current (approximately a multiple of 16).

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Direction</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIMER</td>
<td>10</td>
<td>I</td>
<td>A</td>
<td>Current Limit Timer.</td>
</tr>
</tbody>
</table>

The TIMER pin pull-up current is proportioned to the ISET current (approximately a multiple of 16).

VNEG 11 I P Negative supply input.
The negative voltage applied to the board by the backplane (typically the most negative voltage in the system).

RDISCH 12 I A External MOSFET activation delay.
An external resistor (RDISCH) is connected between the RDISCH pin and the VNEG pin and is used to set the delay between the deactivation and activation of the external pass MOSFET during a current-limit event. The delay is set by the values of the external capacitor (CTIMER) and the external resistor (RDISCH). The formulas are:

\[ T_{DEACT} = \frac{CTIMER \times ISET}{16} \]
\[ T_{ACT} = \frac{9.2 \times R_{DISCH} \times CTIMER}{CTIMER} \]

Legend: TTL = TTL compatible input
I = Input
P = Power
A = Analog
ST = Schmitt Trigger input with CMOS levels
O = Output
CMOS = CMOS-compatible input
D = Digital
## MCP18480

### TABLE 3-1: MCP18480 PIN DESCRIPTIONS (CONTINUED)

<table>
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<th>Pin Direction</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SENSE</td>
<td>13</td>
<td>I</td>
<td>A</td>
<td>Over-current sense. The voltage on the SENSE input pin is used to detect over-current conditions in the load connected to the external MOSFET. This pin is directly connected to the source of the MOSFET, with an external resistor (RSENSE) (typically a low resistance) connected between the source of the MOSFET and VNEG.</td>
</tr>
<tr>
<td>GATE</td>
<td>14</td>
<td>O</td>
<td>A</td>
<td>MOSFET gate driver. The GATE output pin attaches to the gate of the external MOSFET. The voltage on the GATE pin is pulled to the voltage on the VNEG pin whenever the voltage on the UV_TH pin is less than the voltage on the VREFIN pin, or the voltage on the OV_TH pin is greater than the voltage on the VREFIN pin. The GATE pin is also pulled to the voltage on the VNEG pin when the ENABLE input pin is low. When current limit is reached, the voltage on the GATE pin is adjusted to maintain a constant voltage across the RSENSE resistor while the C_TIMER capacitor starts to charge. When the voltage on C_TIMER exceeds VREFIN/2, the GATE pin is pulled to VNEG to turn off the external MOSFET. A RC network can be added from the GATE pin to the drain of the external MOSFET, along with a capacitor from the GATE pin to the VNEG pin, to control the slew rate of the GATE pin. The GATE pin pull-up current is proportioned to the ISET current.</td>
</tr>
<tr>
<td>VFB</td>
<td>15</td>
<td>I</td>
<td>A</td>
<td>External MOSFET drain monitor. The VFB input pin monitors the voltage at the drain of the external power MOSFET switch with respect to the voltage on the VNEG pin for use by the internal foldback circuitry. An external resistor divider network (RFB1 and RFB2) is attached between the drain of this external MOSFET and the VNEG pin (RFB1 is connected between the drain of the external MOSFET and the VFB pin, while RFB2 is connected between the VFB pin and the VNEG pin). This prevents high-voltage breakdown of the VFB input.</td>
</tr>
<tr>
<td>DRAIN_{TH}</td>
<td>16</td>
<td>I</td>
<td>A</td>
<td>MOSFET drain comparator threshold. This pin is used during the power-up sequence of the inserted board, and after any fault condition that <em>turns off</em> the GATE pin drive. The voltage on the pin indicates when the external FET is fully enhanced by comparing the pin voltage to an internal reference voltage (approximately 100 mV derived from the internal band gap reference). An external resistor divider network (R_{DRAIN1} and R_{DRAIN2}) is attached between the drain of this external MOSFET and the VNEG pin (R_{DRAIN1} is connected between the drain of the external MOSFET and the DRAIN_{TH} pin while R_{DRAIN2} is connected between the DRAIN_{TH} pin and the VNEG pin).</td>
</tr>
</tbody>
</table>

Legend: TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels
I = Input O = Output
P = Power CMOS = CMOS-compatible input
A = Analog D = Digital

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<table>
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</tr>
</thead>
<tbody>
<tr>
<td>OVO</td>
<td>17</td>
<td>I</td>
<td>A</td>
<td>Overvoltage detect. Typically for normal operation. This pin is tied to V\textsubscript{NEG}. This feature allows the overvoltage detection input to monitor an overvoltage condition across the power module. The voltage is sensed at the drain of the external MOSFET. The voltage across the load is internally determined based upon: • The voltage difference between system ground and the voltage on the V\textsubscript{NEG} pin • The voltage difference between the drain of the external FET and the voltage on the V\textsubscript{NEG} pin An external resistor divider network (RO\textsubscript{VO1} and RO\textsubscript{VO2}) is attached between the drain of the external MOSFET and the V\textsubscript{NEG} pin (RO\textsubscript{VO1} is connected between the drain of the external MOSFET and the OVO pin, while RO\textsubscript{VO2} is connected between the OVO pin and the V\textsubscript{NEG} pin). When the voltage across the external MOSFET (source-to-drain) equals system ground voltage (-V\textsubscript{NEG} +), the maximum desired load voltage, the GATE pin is forced to the voltage on the V\textsubscript{NEG} pin (disabling the external MOSFET). To detect Overvoltage on the board (instead of the load) directly, connect the OVO pin to the V\textsubscript{NEG} pin.</td>
</tr>
<tr>
<td>PWRGOOD</td>
<td>18</td>
<td>O</td>
<td>D</td>
<td>Power Good indicator. This state of the output is determined by four conditions. These are: • Undervoltage • Overvoltage • Current Limit • External FET is fully-enhanced (from DRAIN\textsubscript{TH} pin on power-up) PWRGOOD is a CMOS logic voltage (V\textsubscript{NEG} or V\textsubscript{NEG} +12V). PWRGOOD is active when the device has completed power-up and the system is neither in an Undervoltage or Overvoltage condition. Connecting the R\textsubscript{IS} pin to the V\textsubscript{NEG} pin configures the PWRGOOD pin to be active high. Connecting the R\textsubscript{IS} pin to the V\textsubscript{REF} pin configures the PWRGOOD pin to be active low.</td>
</tr>
<tr>
<td>ENABLE</td>
<td>19</td>
<td>I</td>
<td>TTL</td>
<td>Enable Gate driver. Used to enable the GATE pin and assert the PWRGOOD pin. The ENABLE pin is active-high and is internally pulled up to 5V. This pin is pulled low by the user to clear the current limit latch when a current-limit fault occurs with RESTART high, or to disable the GATE pin. H = Enable the GATE and PWRGOOD pins. L = Disables the GATE pin, deasserts the PWRGOOD pin and clears current limit latch. When the ENABLE pin is high, fault conditions will disable the GATE pin and deasserts the PWRGOOD pin.</td>
</tr>
</tbody>
</table>

Legend: TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels
I = Input O = Output
P = Power CMOS = CMOS-compatible input
A = Analog D = Digital
## MCP18480 PIN DESCRIPTIONS (CONTINUED)

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<th>Pin Number</th>
<th>Pin Direction</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESTART</td>
<td>20</td>
<td>I</td>
<td>TTL</td>
<td>Auto-restart enable. Enables the auto-restart feature of the device after an over-current fault. L = The internal fault latch is reset and the device attempts to restart with a frequency determined by the values of the external components $C_{\text{TIMER}}$ and $R_{\text{DISCH}}$. H = The auto-restart is disabled, allowing the GATE pin to remain at the $V_{\text{NEG}}$ pin voltage after an over-current fault. Internally pulled down to the $V_{\text{NEG}}$ pin voltage.</td>
</tr>
</tbody>
</table>

Legend: TTL = TTL compatible input
I = Input
P = Power
A = Analog
ST = Schmitt Trigger input with CMOS levels
O = Output
CMOS = CMOS-compatible input
D = Digital
4.0 APPLICATIONS INFORMATION

The MCP18480 can be programmed to have the PWRGOOD signal be either active-high or active-low via the ISET pin and the connection of the external RISET resistor (see Section 6.8.8, “Bias Block”). If the RISET resistor is connected between ISET and VNEG, the PWRGOOD output pin is an active-high signal. If the RISET resistor is connected between ISET and VREFIN, the PWRGOOD output pin is an active-low signal.

For systems using an active-low-enabled DC/DC converter module, the MCP18480 should be programmed for a high-active PWRGOOD output. Tying the RISET resistor to the VNEG pin configures the PWRGOOD to be an active-high signal. The active-high PWRGOOD switches on the external NPN and the collector of the external NPN (labeled as GOODPWR) is pulled to VNEG, enabling a low-active GOODPWR and resulting in enabling the DC/DC module.

For active-high DC/DC converter modules, the MCP18480 should be programmed for a low active PWRGOOD output. Connecting RISET to the VREFIN pin will enable an active-low PWRGOOD output. Refer to Figure 4-1 and Figure 4-2 for schematics.

Figure 4-1 shows a typical telecom application circuit where the DC/DC module is active-high. Figure 4-2 shows a typical telecom application circuit where the DC/DC module is active-low. The polarity of the MCP18480’s PWRGOOD pin (active-high or active-low) is dependant on the state of the ISET pin.

**FIGURE 4-1:** Typical Operating Circuit for Telecom Applications with Active-High power Module - foldback current limit enabled.
FIGURE 4-2: Typical operating circuit for telecom applications with Active-Low power Module - foldback current limit enabled.
The MCP18480 can typically be implemented in a backplane system in one of two methods. Figure 4-3 shows a system where the backplane integrates the MCP18480 for every slot. Figure 4-4 shows a system where the backplane does not integrate the MCP18480s and each card that will be inserted into any slot is required to integrate the MCP18480.

**FIGURE 4-3:** Backplane System Block Diagram #1.

**FIGURE 4-4:** Backplane System Block Diagram #2.
5.0 POWER-UP

5.1 \( V_{\text{POS}} \) and \( V_{\text{NEG}} \) Connection
For proper system operation, it is required that the system ground and the \( V_{\text{NEG}} \) pin have a solid connection before voltages are applied to any logic on the board.

5.2 The Board Circuitry
After the MCP18480 has “good” voltages on the \( V_{\text{POS}} \) and \( V_{\text{NEG}} \) pins, the board may have voltages applied to any of the other signals (a “good” voltage on \( V_{\text{POS}} \) indicates a “good” voltage on the system ground). The MCP18480 will start to source a small current to the external MOSFET to begin powering the board. This will turn on the MOSFET starting to power the external circuitry (load) of the board. The current from the GATE pin (into the external MOSFET) increases as the \( V_{\text{DS}} \) of the MOSFET decreases. When the \( V_{\text{DS}} \) of the MOSFET is below the voltage determined by the two resistors on the DRAIN\(_{\text{TH}}\) pin (\( R_{\text{DRAIN1}} \) and \( R_{\text{DRAIN2}} \)), and the voltage on the GATE pin is greater than 8V, the PWRGOOD pin is active.

6.0 INTERNAL SIGNAL DESCRIPTIONS

The figure on page 2 illustrates a block diagram of the MCP18480. Between the functional blocks, there are some signals that have been named. These signals are briefly explained in Section 6.1 thru Section 6.7.

6.1 Undervoltage Active
A signal that indicates (when low) that System Ground - \( V_{\text{NEG}} \) is less than the minimum voltage.

6.2 Overvoltage Active
A signal that indicates (when low) that System Ground - \( V_{\text{NEG}} \) is greater than the maximum voltage.

6.3 LATCHOFF
A signal that controls the GATE pin due to a timeout of the current-limiting timer.

6.4 Current Limit TIMER
A signal that controls the reduction of source current on the GATE pin and starts the voltage ramp of the current limit timer.

6.5 Current Limit Feedback
A voltage that is proportional to the \( V_{\text{DS}} \) of the external MOSFET to set a trip point for current-limiting.

6.6 TIMEOUT
A signal that indicates the completion of the foldback time and is used to start the latchoff time.

6.7 Circuit Breaker
A signal that immediately causes the GATE pin output to be driven to \( V_{\text{NEG}} \) upon the detection of excessive current in the external FET.
6.8 DESCRIPTION OF INTERNAL BLOCKS

The internal blocks shown in the MCP18480 Block Diagram on page 2 are discussed in Section 6.8.1 through Section 6.8.8.

### 6.8.1 UV (UNDERVOLTAGE) BLOCK

The Undervoltage lockout circuit monitors the input voltage by comparing a centertap voltage on an external resistor divider to a 2.5V reference. The centertap voltage is fed into the UV\textsubscript{TH} input pin.

If the voltage on the UV\textsubscript{TH} pin is below the internal 2.5V reference, the absolute magnitude of the supply voltage is too low for proper system operation, resulting in the external MOSFET being turned off. If the voltage on the UV\textsubscript{TH} pin is greater than \( V_{\text{NEG}} + 2.5V \), the supply voltage is above the minimal operating voltage as set by the external resistor divider network.

In telecom network applications, it is common to shut down the DC/DC converter supply when the input voltage falls below -38.5V (tolerance of ±1.0V) for greater than 100 ms. The system will not restart until the voltage exceeds -43V (tolerance of ±0.5V). This voltage difference is produced by an open-drain NMOS output (the UV\textsubscript{HYS} pin) that connects an external resistor in parallel with the lower of the two resistors in the external UV divider network until the supply ramps down to -43V. When the UV\textsubscript{TH} pin exceeds \( V_{\text{NEG}} + 2.5V \), the internal MOSFET transistor is turned off, disconnecting the external resistor connected to the UV\textsubscript{HYS} pin. The voltage at the UV\textsubscript{TH} pin increases to 2.79V. The supply voltage would have to decrease to -38.5V in order to assert the internal “Undervoltage Active” signal.

An internal 10 µA current source and an external capacitor connected to the UV\textsubscript{D} pin adjusts the delay between the input fault and the notification of this fault to the system. This is usually 100 ms for -48V telecom-type equipment. For customized adjustments, the time delay can be expressed as Equation 6-1.

\begin{equation} \label{eq:6-1} T_{\text{DELAY}} = \frac{(V_{\text{REFIN}})^2}{10\mu A} \cdot C_{UVD} \end{equation}

\( C_{UV} \) is the capacitor connected between the UV\textsubscript{D} pin and the \( V_{\text{NEG}} \) pin. A value of 1 µF would provide a delay of about 100 ms.

If the supply voltage dips below the programmed threshold, the input comparator trips the other way. The timing capacitor is released to ramp-up at the previously described rate and the Undervoltage block switches when the capacitor voltage reaches 1.25V. When the input comparator goes to a low level, the hysteresis FET is turned on and the trip point for reassertion of good \( V_{\text{NEG}} \) reverts to -43V.

While the Undervoltage Active signal is low (includes Undervoltage input filter), the GATE pin driver for the external MOSFET is disabled, the GATE pin is pulled to the voltage of the \( V_{\text{NEG}} \) pin with a 60 mA current sink and the PWRGOOD output pin is deasserted to indicate that the input voltage is out of range.

\begin{equation} \label{eq:6-2} R_{UVHYS} = \frac{R_{UV1}}{(V_{UV1} - R_{UV1} - 1)} \end{equation}

\begin{equation} \label{eq:6-3} V_{\text{REFIN}} > \frac{\left| V_{\text{NEG}} \right| \cdot R_{UV2}}{(R_{UV1} + R_{UV2})} \end{equation}

---

Note: Voltage levels discussed are with respect to external component values selected in Figure 4-1.
6.8.2 OV (OVERVOLTAGE) BLOCK

The overvoltage block behaves similarly to the undervoltage block in that it monitors an input voltage by comparing a centertap voltage on an external voltage divider (on the OVTH pin) to the VREFIN pin voltage.

If the centertap voltage is below the reference, the input voltage is not excessive. If the centertap voltage is greater than the VNEG + VREFIN pin voltages, the supply voltage is higher than the programmed acceptable maximum voltage limit. An internal flag is then activated to inform the MCP18480 that the input voltage has exceeded the preset limit.

The “Overvoltage Active” signal deasserts when the input voltage drops back below the threshold determined by the external resistors (ROV1 and ROV2).

EQUATION 6-4: OVERVOLTAGE VOLTAGE CONDITION

\[
V_{\text{REFIN}} < \frac{|V_{\text{NEG}}| \cdot R_{\text{OV2}}}{(R_{\text{OV1}} + R_{\text{OV2}})}
\]

6.8.3 FET-GOOD BLOCK

The FET-good block monitors the voltage between the drain of the external MOSFET and on the VNEG pin at power-up. It delays assertion of PWRGOOD until the drain-to-source voltage of the external FET is acceptably low and the voltage at the GATE pin is about 8V. The comparator operation is similar to Undervoltage and Overvoltage blocks.

To prevent applying excessive voltages to the gates of the FETs in the Undervoltage circuit, a resistive voltage divider is employed between ground and the VNEG pin. Similarly, the drain of the external MOSFET can be exposed to voltages at around VNEG during normal operation and as high as ground (typically 48V above VNEG).

The FET good block also monitors the GATE pin. When the GATE pin becomes >VNEG +8V and the DRAINTH pin is within its programmed range, the output of the FET good block is active.

The internal FET good signal goes high and remains active until a fault condition (Undervoltage, Overvoltage or Current Limit) is detected. Any of these conditions hold the PWRGOOD signal deasserted until the fault condition is removed and the external FET gate and drain voltages are acceptable.
6.8.4 CURRENT LIMIT BLOCK

An excessive current flowing through the external FET is sensed as a voltage across an external resistor connected between the FET’s source and $V_{NEG}$.

The drain voltage is sensed with a resistor divider network, as shown in Figure 4-1 and Figure 4-2. The voltage tap is applied to a circuit whose output is 50 mV above $V_{NEG}$ when the drain of the external FET is at $V_{NEG}$. The output is 12 mV when the $V_{FB}$ pin is $\geq V_{NEG} + 0.5V$. This output voltage is the Current Limit Feedback (CLFB) signal to the gate driver block for use in the fold-back current-limiting.

The CLFB voltage serves as the reference for a comparator whose other input monitors the voltage across the current limit sense resistor in series with the source of the external FET. When the SENSE pin exceeds the voltage on CLFB, a comparator output goes high to start the timer (see Section 6.8.5). The $V_{DS}$ dependent threshold for the current limit helps keep the FET within its safe operating area.

Another comparator in the current-limiting block watches the SENSE pin for potentially catastrophic over-current conditions, which require immediate termination of conduction in the pass MOSFET. The output of this comparator trips a comparator used in the TIMER block to skip the first part of the timeout cycle and go straight to the “off” period. In some cases, the user may want to program the system to shut off immediately if there is a short-circuit condition that exceeds a desired level. To use this feature, connect a divider between the $V_{REFIN}$ pin and the $V_{NEG}$ pin, with its center tap at the CL input pin. The circuit breaker current that would trigger this mode is given by Equation 6-5.

EQUATION 6-5: CIRCUIT BREAKER THRESHOLD

$$I_{CAT} = \frac{\left(\frac{V_{REFIN}}{R_{CL1} + R_{CL2}}\right) \cdot R_{CL2}}{R_{SENSE}}$$

If this function is not needed in a particular application, it can be disabled by connecting the CL pin to the $V_{REFIN}$ pin. Equation 6-6 shows the current of the CL pin during current-limiting.

EQUATION 6-6: CL PIN CURRENT

$$I_{CL} = \frac{V_{SENSE}}{R_{SENSE}} \quad \text{for } V_{FB} \geq 0.5V$$

$V_{SENSE} = 0.76 \times \left(0.05V - \frac{V_{DS} \cdot R_{FB2}}{R_{FB1} + R_{FB2}}\right) + 0.012V$

$for V_{FB} > 0.5V, V_{SENSE} = 0.012V$

6.8.5 TIMER BLOCK

Since the external FET can survive brief over-current episodes, it is unnecessary to turn off the FET instantly when the current rises too high (see external FET data sheet). The timer circuit uses the output of the comparator in the current-limiting block to begin charging an external capacitor with $16 \cdot I_{RISET}$ (typically 160 µA) when an over-current condition is detected. When the voltage on the capacitor ramps up to 1.25V, a comparator output goes high. This output goes to another block that tells the gate driver to turn the external FET off and deassert the PWRGOOD pin. The complementary output of the timer changes the state of a hysteresis circuit that drops the reference input of the comparator to $V_{NEG} + 100 mV (\pm 10 mV)$.

When the FET is off, the current through it drops to zero, so that the voltage across the current sense resistor also goes to zero and the current limit signal to the timer block goes away. The timer capacitor starts to discharge at a rate set by the external resistor, $R_{DISCH}$. Equation 6-7 shows the equations used to calculate the current at the TIMER pin. This current is used for other calculations.

EQUATION 6-7: TIMER PIN CURRENT CALCULATIONS

$$I_{TIMER} = 16 \cdot I_{RISET} \quad \text{Typical}$$

$$I_{TIMER} = 10 \cdot I_{RISET} \quad \text{Minimum}$$

$$I_{TIMER} = 20 \cdot I_{RISET} \quad \text{Maximum}$$

Legend: $I_{RISET}$ is the current through the external $R_{SET}$ resistor

The delay between the inception of the over-current condition and the deactivation of the FET is given by Equation 6-8.

EQUATION 6-8: OVER-CURRENT FAULT DELAY

$$T_{CLD1} = \frac{C_{TIMER}}{I_{TIMER}} \cdot 1.25$$

The time required to reset the timer and reactivate the gate driver is given by Equation 6-9.

EQUATION 6-9: OVER-CURRENT REACTIVATION DELAY

$$T_{CLD2} = 9.2 \cdot C_{TIMER} \cdot R_{DISCH}$$

As described above, the timer circuit operates as a free-running, multi-vibrator, if RESTART is low.
6.8.6 LATCH BLOCK

A current limit latch circuit determines whether, following the timeout period resulting from an over-current condition, the external FET should be latched-off until reactivated by an external signal, or be allowed to restart automatically following the timer cycle.

If the RESTART input is low, the part will restart and the gate drive to the external MOSFET will be restored automatically. If the RESTART pin is high, a current limit event will turn the FET off after the programmed delay and maintain an off condition until the ENABLE pin or RESTART pin is pulled low momentarily.

6.8.7 GATE DRIVE BLOCK

The GATE drive block sources a current equal to the voltage at CLFB divided by 1 kΩ to the gate of the external MOSFET. So the current sourced from the GATE pin is determined by the VDS of the external FET. This current, and the external capacitors around the FET, control the slew rate of the drain of the external FET, limiting the current that would otherwise have to be diverted from other boards on the backplane. In the event of a problem (Overvoltage, Undervoltage or current limit), the gate of the external FET is pulled down with 60 mA. During normal operation, the GATE pin ramps up to about 12V, sending the external FET deeply into the triode region. If the drain current becomes excessive while the drain-to-source voltage is high, the inverting input of the op amp is driven to the CLFB voltage by the current-limiting block, causing a reduction in the drive to the external FET to reduce the current through it. This foldback current-limit remains active until the voltage on CTIMER reaches VREFIN/2, after which the GATE output pin is pulled to VNEG for the duration of the timeout period, or until ENABLE is cycled low momentarily.

For applications in which it is undesirable to have the drain current track the VDS of the external pass FET in current limit, the user can tie the VFB pin to the VREF or VNEG pin. This will make the MCP18480 try to force the drain current to 12 mV/RSENSE or 50 mV/RSENSE, respectively, until the TIMER block times out. If foldback current-limiting is not desired at all, set the divider associated with the CL pin to detect the desired current in order to shut off the GATE immediately.

A voltage on the GATE pin higher than about 8V is one condition for the PWRGOOD pin to be asserted. Any fault condition that causes the GATE pin voltage to be pulled to VNEG deasserts the PWRGOOD pin. On startup, a NMOS transistor with a resistor pulling its gate up holds the GATE pin down until the MCP18480 is properly biased.

6.8.8 BIAS BLOCK

The internal voltage generation or bias block generates the biasing currents for all internal blocks. It also provides a 2.5V reference voltage that is brought out to the VREFOUT pin. This output pin is usually fed back into the VREFIN pin. However, an externally-generated 2.5V reference voltage may be directly connected to the VREFIN pin, while leaving the VREFOUT pin unconnected. A VREFIN/2 voltage is generated within the bias block, which is used as reference in the other blocks.

A internal shunt regulator limits the internal circuitry to 12V. An external current-limiting resistor in series with VPOS absorbs the excess voltage. The resulting regulated 12V source is used in the gate drive block and PWRGOOD output circuit.

The 12V source is also stepped-down to generate a 5V regulated source. Most of the other circuitry and blocks operate with the internally-generated 5V.

**EQUATION 6-10: EXTERNAL RSET CURRENT**

\[
I_{RSET} = \pm \frac{V_{REFIN}}{2RSET}
\]

Note: The direction of the current is dependant on where the external RSET resistor is connected (the ISET pin to either the VNEG pin or the VREFIN pin).

6.8.9 POWER GOOD BLOCK

The “power good” block monitors the state of the OV active, the UV active, the current limit circuitry, and output of the FET good block to generate the PWRGOOD output signal.
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

Legend:

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<th>Description</th>
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<tr>
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<td>Year code (last 2 digits of calendar year)</td>
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<tr>
<td>WW</td>
<td>Week code (week of January 1 is week '01')</td>
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<tr>
<td>NNN</td>
<td>Alphanumeric traceability code</td>
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Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard marking consists of Microchip part number, year code, week code, and traceability code.
MCP18480

20-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)

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* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MO-150
Drawing No. C04-072
APPENDIX A: REVISION HISTORY

Revision A
This is a new data sheet

Revision B
• Add device characterization information
• Enhanced functional description
APPENDIX B:  MCP18480 SCHEMATICS

This appendix contains the schematics for the MCP18480 Evaluation Board.
FIGURE B-1: Typical Operating Circuit for Telecom Applications with Active-High Power Module - Feedback Current Limit Enabled.
FIGURE B-2: Typical Operating Circuit for Telecom Applications with Active-Low Power Module - Foldback Current Limit Enabled.
FIGURE B-3: Evaluation Board Schematic (Active-Low Power Module - Foldback Current Limit Enabled).
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

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<td>Package</td>
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Device
MCP18480: -48V Hot Swap Controller
MCP18480T: -48V Hot Swap Controller (Tape and Reel)

Temperature Range I = -40°C to +85°C

Package SS = Plastic SSOP (209 mil, Body), 20-lead

Examples:

a) MCP18480-I/SS = Industrial Temp., SSOP package
b) MCP18480T-I/SS = Tape and Reel, Industrial Temp., SSOP package

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Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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