This document includes the programming specifications for the following devices:

- MCP25020
- MCP25025
- MCP25050
- MCP25055

1.0 OVERVIEW

This specification describes the requirements to program a device. Programming is accomplished through a serial interface. A serial interface reduces the number of device pins that must be controlled and eases the application requirements for the device to be programmed while in the users system. This capability increases design flexibility, and is referred to as In-Circuit Serial Programming™ (ICSP™).

1.1 Hardware Requirements

The MCP250XX requires two programmable power supplies, one for VDD (2.0V to 6.0V recommended) and one for VPP (12V to 14V). Both supplies should have a minimum resolution of 0.25V.

1.2 Programming Mode

The programming mode for the MCP250XX allows programming of user program memory and the configuration word.

### Package Types:

![Package Diagram](image-url)
2.0 MCP250XX MEMORY

The MCP250XX has two memory spaces. The first is the User EPROM Memory. This memory stores the default configuration values for the device. The second memory space is the configuration memory. This contains the values for the device oscillator and reset pin configurations.

2.1 User EPROM Memory Map

The User EPROM memory space extends from 0x00 to 0x45. Table 2-1 shows this program memory map.

This User EPROM memory is offset within the device memory map. When programming the device, an offset to the addresses in Table 2-1 is required.

Note 1: An offset of 0x10 is required to be added to the addresses shown in the User Program Memory Map (Table 2-1) when programming these locations. Therefore, there should be 16 Increment Address commands before programming the contents of the User EPROM Memory.

2: Do not program outside the specified user EPROM memory range or improper operation may occur.

2.2 Configuration Memory

Configuration memory is accessed with the Load Configuration command. Once in configuration memory, the only way to access the User EPROM Memory is to reset the device and re-enter Programming mode, as described in Section 3.1. Only the lower 3-bits should be programmed. The remaining 11-bits are reserved and should be programmed as a '1'. Programming these bits as a '1' will ensure that the factory value is not modified. When verifying this location, only verify against the lower 3-bits (the bits that were programmed).

<table>
<thead>
<tr>
<th>Address (1)</th>
<th>Location Name</th>
<th>Address (1)</th>
<th>Location Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>IOINTEN</td>
<td>23h</td>
<td>TXID0EID0</td>
</tr>
<tr>
<td>01h</td>
<td>IOINTPO</td>
<td>24h</td>
<td>TXID1SIDH</td>
</tr>
<tr>
<td>02h</td>
<td>GPLAT</td>
<td>25h</td>
<td>TXID1SIDL</td>
</tr>
<tr>
<td>03h</td>
<td>—</td>
<td>26h</td>
<td>TXID1EID8</td>
</tr>
<tr>
<td>04h</td>
<td>OPTREG1</td>
<td>27h</td>
<td>TXID1EID0</td>
</tr>
<tr>
<td>05h</td>
<td>T1CON</td>
<td>28h</td>
<td>TXID2SIDH</td>
</tr>
<tr>
<td>06h</td>
<td>T2CON</td>
<td>29h</td>
<td>TXID2SIDL</td>
</tr>
<tr>
<td>07h</td>
<td>PR1</td>
<td>2Ah</td>
<td>TXID2EID8</td>
</tr>
<tr>
<td>08h</td>
<td>PR2</td>
<td>2Bh</td>
<td>TXID2EID0</td>
</tr>
<tr>
<td>09h</td>
<td>PWM1DCH</td>
<td>2Ch</td>
<td>ADCMP3H</td>
</tr>
<tr>
<td>0Ah</td>
<td>PWM2DCH</td>
<td>2Dh</td>
<td>ADCMP3L</td>
</tr>
<tr>
<td>0 Bh</td>
<td>CNF1</td>
<td>2Eh</td>
<td>ADCMP2H</td>
</tr>
<tr>
<td>0Ch</td>
<td>CNF2</td>
<td>2Fh</td>
<td>ADCMP2L</td>
</tr>
<tr>
<td>0Dh</td>
<td>CNF3</td>
<td>30h</td>
<td>ADCMP1H</td>
</tr>
<tr>
<td>0 Eh</td>
<td>ADCON0</td>
<td>31h</td>
<td>ADCMP1L</td>
</tr>
<tr>
<td>0Fh</td>
<td>ADCON1</td>
<td>32h</td>
<td>ADCMP0H</td>
</tr>
<tr>
<td>10h</td>
<td>STCON</td>
<td>33h</td>
<td>ADCMP0L</td>
</tr>
<tr>
<td>11h</td>
<td>OPTREG2</td>
<td>34h</td>
<td>GPDDR</td>
</tr>
<tr>
<td>12h</td>
<td>—</td>
<td>35h</td>
<td>USER0</td>
</tr>
<tr>
<td>13h</td>
<td>—</td>
<td>36h</td>
<td>USER1</td>
</tr>
<tr>
<td>14h</td>
<td>RXMSIDH</td>
<td>37h</td>
<td>USER2</td>
</tr>
<tr>
<td>15h</td>
<td>RXMSIDL</td>
<td>38h</td>
<td>USER3</td>
</tr>
<tr>
<td>16h</td>
<td>RXMEID8</td>
<td>39h</td>
<td>USER4</td>
</tr>
<tr>
<td>17h</td>
<td>RXMEID0</td>
<td>3Ah</td>
<td>USER5</td>
</tr>
<tr>
<td>18h</td>
<td>RXF0SIDH</td>
<td>3Bh</td>
<td>USER6</td>
</tr>
<tr>
<td>19h</td>
<td>RXF0SIDL</td>
<td>3Ch</td>
<td>USER7</td>
</tr>
<tr>
<td>1Ah</td>
<td>RXF0EID8</td>
<td>3Dh</td>
<td>USER8</td>
</tr>
<tr>
<td>1Bh</td>
<td>RXF0EID0</td>
<td>3Eh</td>
<td>USER9</td>
</tr>
<tr>
<td>1Ch</td>
<td>RXF1SIDH</td>
<td>3Fh</td>
<td>USERA</td>
</tr>
<tr>
<td>1Dh</td>
<td>RXF1SIDL</td>
<td>40h</td>
<td>USERB</td>
</tr>
<tr>
<td>1 Eh</td>
<td>RXF1EID8</td>
<td>41h</td>
<td>USERC</td>
</tr>
<tr>
<td>1 Fh</td>
<td>RXF1EID0</td>
<td>42h</td>
<td>USERD</td>
</tr>
<tr>
<td>20h</td>
<td>TXID0SIDH</td>
<td>43h</td>
<td>USERE</td>
</tr>
<tr>
<td>21h</td>
<td>TXID0SIDL</td>
<td>44h</td>
<td>USERF</td>
</tr>
<tr>
<td>22h</td>
<td>TXID0EID8</td>
<td>45h</td>
<td>CHKSUM</td>
</tr>
</tbody>
</table>

Note 1: An offset of 0x10 is required.

2: Reserved, Program this location as 0x34FF.

3: Unimplemented, Program this location as 0x34FF.
3.0 PROGRAMMING MODE ENTRY

A specific hardware sequence is required to force the device from the normal operating mode into Programming mode. After entering into the Programming mode, the 2-wire serial interface can be used to send the commands to the MCP250XX. These commands are discussed in Section 4.0.

3.1 Programming Entry Sequence

The Programming mode is entered by raising the RST pin from \( V_{IL} \) (Parameter PD8) to \( V_{IH} \) (Parameter PD4). Then while holding the CLOCK and DATA pins (GP5 and GP4) low, raising \( V_{DD} \).

Once in this mode, the User EPROM memory and the configuration memory can be accessed (read and programmed). The interface is serial and the CLOCK pin (GP5) is a Schmitt Trigger input in this mode.

The sequence that forces the device into the Programming mode also puts all other logic into the reset state (the RST pin was initially at \( V_{IL} \)). This means that all I/O are in the reset state (High impedance inputs).

**Note 1:** Do not power any I/O pins before \( V_{DD} \) is applied.

Figure 7-2 shows the waveform for entry into Programming mode.

3.2 Programming Operation

The CLOCK pin (GP5) is used as a clock input pin. The DATA pin (GP4) is used for entering command bits and data input/output during serial communication.

To input a command, the CLOCK pin (GP5) is cycled six times. Each command bit is latched on the falling edge of the clock with the least significant bit (LSb) of the command being input first. The data on the DATA pin (GP4) is required to have a minimum setup and hold time (see Parameter P3 and Parameter P4) with respect to the falling edge of the clock. Commands that have data associated with them (read and load) are specified to have a minimum delay between the command and the data (Parameter P6).

After this delay, the clock pin is cycled 16 times with the first cycle being a start bit and the last cycle being a stop bit. The data is input/output LSb first. During a read operation the LSb will be transmitted onto the DATA pin (GP4) on the rising edge of the second cycle, and during a load operation the LSb will be latched on the falling edge of the second cycle.

All commands and data words are transmitted LSb first. The DATA pin value is latched on the falling edge of the CLOCK pin. A minimum time between the command and the data word (or another command) is required. This separation time is shown in Parameter P6 of the Electrical Specification.

The commands that are available are listed in Table 4-1. The waveforms for these commands are shown in Figure 7-3 through Figure 7-8.
4.0 PROGRAMMING COMMANDS

There are six commands that the MCP250XX will execute when in Programming mode. These commands are shown in Table 4-1. Three of the commands have data that are required. The Load commands supply data to the MCP250XX, and the Read command retrieve data from the MCP250XX.

When the device enters into Programming mode, the address pointer is pointing to 0x00. The User Program Memory has an offset of 0x10. So before starting to program a desired location in the User Program Memory Map, the Increment Address command must be executed 16 times.

<table>
<thead>
<tr>
<th>Command</th>
<th>Mapping (MSb ... LSb)</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load Configuration</td>
<td>0 0 0 0 0 0</td>
<td>0, data(14), 0</td>
</tr>
<tr>
<td>Load Data</td>
<td>0 0 0 0 1 0</td>
<td>0,1,0,1,0,0,data(8),0</td>
</tr>
<tr>
<td>Read Data</td>
<td>0 0 0 1 0 0</td>
<td>0, data(14), 0</td>
</tr>
<tr>
<td>Increment Address</td>
<td>0 0 0 1 1 0</td>
<td></td>
</tr>
<tr>
<td>Begin Programming</td>
<td>0 0 1 0 0 0</td>
<td></td>
</tr>
<tr>
<td>End Programming</td>
<td>0 0 1 1 1 0</td>
<td></td>
</tr>
</tbody>
</table>

4.1 Load Configuration

After receiving this command, the address pointer points to the Configuration memory space. To address the MCP250xx Configuration word the Increment command must be given seven times (see Figure 4-2). Then by applying 16 clock cycles to the CLOCK pin, a 14-bit “data word” will be loaded into the Transfer Latch (ready to be programmed into the configuration word, see Register 5-1). Only the lower 3-bits of the “data word” should be programmed. The remaining 11-bits of the “data word” are reserved and should be programmed as a ‘1’. Programming these bits as a ‘1’ will ensure that the factory value is not modified. When verifying this location, only verify against the lower 3-bits (the bits that were programmed).

After the Load Configuration command is supplied, the only way to have the address pointer return to pointing at the User Program Memory is to exit the Programming mode. This is accomplished by taking the voltage on the RST pin to a low level (VIL, Parameter PD8) and the re-entering into Programming mode (see Section 3.1).

Figure 7-3 shows the waveform for the Load Configuration command and Table 7-3 specifies the timing parameters that must be meet.

4.2 Load Data

After receiving this command, the chip will load in a 14-bit “data word” into the Transfer latch when 16 clock cycles are applied to the CLOCK pin.

Figure 7-4 shows the waveform for the Load Data command and Table 7-4 specifies the timing parameters that must be meet.

4.3 Read Data

After receiving this command (the first 6 bits), the device data word at the memory address currently accessed is loaded into the Transfer latch. Then as the Data is transmitted, the DATA (GP4) pin is automatically configured into an output on the second rising clock edge, and reverts back to an input (hi-impedance) after the 16th rising edge.

Figure 7-5 shows the waveform for the Read Data command and Table 7-5 specifies the timing parameters that must be meet.

This command is useful in the verify sequence of the programming algorithm. This is used to verify that if the value that was programmed at this location has been “well programmed”. That is, that the memory cell was able to retain the value previously written. A memory verification should be done at the minimum and maximum voltage that the device will experience within the application.
4.4 Increment Address

The address pointer is incremented when this command is received.

Figure 7-6 shows the waveform for the Increment Address command and Table 7-6 specifies the timing parameters that must be met.

4.5 Begin Programming

Programming of the appropriate memory (User Program Memory or Configuration Memory) will begin after this command is received and decoded. This programming pulse will continue until an End Programming command is received. Each programming pulse should meet a minimum time duration (Parameter P11 in Electrical Specification’s Table 7-7).

<table>
<thead>
<tr>
<th>Step</th>
<th>Command</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Load Command</td>
<td>Data or Configuration</td>
</tr>
<tr>
<td>2</td>
<td>Begin Programming</td>
<td>Pulse #1</td>
</tr>
<tr>
<td>3</td>
<td>End Programming</td>
<td>Wait required delay</td>
</tr>
<tr>
<td>4</td>
<td>Load Command</td>
<td>Data or Configuration</td>
</tr>
<tr>
<td>5</td>
<td>Begin Programming</td>
<td>Pulse #2</td>
</tr>
<tr>
<td>6</td>
<td>End Programming</td>
<td>Wait required delay</td>
</tr>
<tr>
<td>:</td>
<td>:</td>
<td>Repeat Load/Begin/End Programming sequence as needed</td>
</tr>
</tbody>
</table>

4.6 End Programming

After receiving this command, the chip stops programming the memory (configuration program memory or user program memory) that it was programming at the time.

Figure 7-8 shows the waveform for the End Programming command and Table 7-8 specifies the timing parameters that must be met.

4.7 Programming Algorithm Requires Variable VDD

The algorithm calls for program verification at VDDmin as well as VDDmax. Verification at VDDmin guarantees good “erase margin”. Verification at VDDmax guarantees good “program margin”.

The actual programming must be done with VDD in the VDDP range (Parameter PD1).

| VDDP | VDD range required during programming. |
| VDDV | VDD range required during verification. |
| VDDMIN | Minimum operating VDD specification for the device. |
| VDDMAX | Maximum operating VDD specification for the device. |

Programmers must verify the MCP250XX at its specified VDDMAX and VDDMIN levels. Since Microchip may introduce future versions of the MCP250XX with a broader VDD range, it is best that these levels are user selectable (defaults are ok).

Example 4-1 shows a typical command sequence that would be used in the over programming of a device.

EXAMPLE 4-1: Command Sequence

<table>
<thead>
<tr>
<th>Step</th>
<th>Command</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Load Command</td>
<td>Data or Configuration</td>
</tr>
<tr>
<td>2</td>
<td>Begin Programming</td>
<td>Pulse #1</td>
</tr>
<tr>
<td>3</td>
<td>End Programming</td>
<td>Wait required delay</td>
</tr>
<tr>
<td>4</td>
<td>Load Command</td>
<td>Data or Configuration</td>
</tr>
<tr>
<td>5</td>
<td>Begin Programming</td>
<td>Pulse #2</td>
</tr>
<tr>
<td>6</td>
<td>End Programming</td>
<td>Wait required delay</td>
</tr>
<tr>
<td>:</td>
<td>:</td>
<td>Repeat Load/Begin/End Programming sequence as needed</td>
</tr>
</tbody>
</table>

Note: Any programmer not meeting these requirements may only be classified as “prototype” or “development” programmer but not a “production” quality programmer.
FIGURE 4-1: PROGRAM FLOW CHART - MCP250XX PROGRAM MEMORY

Start

Force \( V_{PP} \) from \( V_{SS} \) to \( V_{IH} \)

Set \( V_{DD} = V_{DDP}\)

Apply 16 Increment Address Commands

\( N = 0 \)

Program Cycle

Read Data Command

Data Correct?

Yes

Apply 3N Additional Program Cycles

\( N = N + 1 \)

\( N = \# \) of Program Cycles

No

All Locations Done?

Yes

Verify all Locations @ \( V_{DD \text{ MIN.}} \)
\( V_{PP} = V_{IH} \)

Data Correct?

No

Report Programming Failure

Yes

Report Verify @ \( V_{DD \text{ MIN.}} \) Error

No

Verify all Locations @ \( V_{DD \text{ MAX.}} \)
\( V_{PP} = V_{IH} \)

Data Correct?

Yes

Done

No

Report Verify @ \( V_{DD \text{ MAX.}} \) Error

Program Cycle

Load Data Command

Begin Programming Command

Wait 100 \( \mu \)s

End Programming Command

Return

Note 1: \( V_{DDP} = V_{DD} \) range for programming (typically 4.75V - 5.25V).

2: \( V_{DD \text{ MIN.}} = \) Minimum \( V_{DD} \) for device operation.
\( V_{DD \text{ MAX.}} = \) Maximum \( V_{DD} \) for device operation.
FIGURE 4-2: PROGRAM FLOW CHART - MCP250XX CONFIGURATION WORD

![Program Flow Chart](image)

**Note 1:** $V_{DDP} = V_{DD}$ range for programming (typically 4.75V - 5.25V).

**Note 2:** $V_{DD_MN} = \text{Minimum } V_{DD}$ for device operation.

$V_{DD_MAX} = \text{Maximum } V_{DD}$ for device operation.
5.0 CONFIGURATION WORD

The MCP250XX family members have several configuration bits. These bits can be programmed (reads '0') or left unprogrammed (reads ‘1’) to select various device configurations. Register 5-1 provides an overview of configuration bits.

Only the lower 3-bits should be programmed. The remaining 11-bits are reserved and should be programmed as a '1'. Programming these bits as a '1' will ensure that the factory value is not modified.

REGISTER 5-1: CONFIGURATION REGISTER

<table>
<thead>
<tr>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 13-3  **Reserved**: Read as 'x', Program as '1'.

bit 2  **RSTEN**: Reset on GP7 Enable bit
1 = RST function is enabled on the GP7 I/O pin
0 = GP7 is a general purpose I/O pin

bit 1-0  **FOSC1**:FOSC0: Oscillator Selection bits
11 = HS oscillator
10 = Reserved
01 = XT oscillator
00 = LP oscillator

Legend:
- **R** = Readable bit
- **P** = Programmable bit
- **U** = Unimplemented bit, read as ‘0’
- **n** = Value when device is unprogrammed
- **x** = Unknown state
6.0 MEMORY VERIFICATION

The User EPROM memory and configuration word is checksummed. This enhances the validation that the correct user’s values are programmed into the device memory.

6.1 Checksum CALCULATIONS

Checksum is calculated by reading the contents of the MCP250XX User EPROM memory locations and adding the values up. The entire User EPROM memory is read (00h - 44h). Any carry bits exceeding 16-bits are ignored. Checksum computation for each member of the MCP250XX devices is shown in Table 6-1.

The checksum is calculated by summing the user memory and taking the 2s complement. The result is the truncated lower eight bits.

The Table 6-1 describes how to calculate the checksum.

<table>
<thead>
<tr>
<th>Device</th>
<th>Checksum (1)</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Unprogrammed</td>
</tr>
<tr>
<td>MCP250XX</td>
<td>[SUM(0x000:0x045)] + 1</td>
<td>0x45</td>
</tr>
<tr>
<td>MCP2502x</td>
<td>[SUM(0x000:0x045)] + 1</td>
<td>0x2C</td>
</tr>
</tbody>
</table>

Legend: SUM[a:b] = [Sum of locations a through b inclusive]

Note 1: Checksum = 2s complement of the sum of all the individual expressions, truncated to 8-bits.
        ~ = 1s complement
7.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

7.1 DC Characteristics

FIGURE 7-1: PROGRAMMING DC CHARACTERISTICS WAVEFORMS

![Programming DC Characteristics Waveforms Diagram]

TABLE 7-1: DC CHARACTERISTICS FOR PROGRAMMING MODE (PROGRAM/VERIFY)

<table>
<thead>
<tr>
<th>Parameter No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>PD1</td>
<td>VDDP</td>
<td>Supply voltage during programming</td>
<td>4.75</td>
<td>5.0</td>
<td>5.25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>PD2</td>
<td>IDD</td>
<td>Supply current (from VDD) during programming</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>PD3</td>
<td>VDDV</td>
<td>Supply voltage during verify</td>
<td>VDDmin</td>
<td>—</td>
<td>VDDmax</td>
<td>V</td>
<td>Note 1</td>
</tr>
<tr>
<td>PD4</td>
<td>VIH</td>
<td>Voltage on MCLR/VPP during programming/verify</td>
<td>12.75</td>
<td>—</td>
<td>13.25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>PD6</td>
<td>IPP</td>
<td>Programming supply current (from VPP)</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>PD8</td>
<td>VIL</td>
<td>Voltage input low level</td>
<td>DATA (GP4)</td>
<td>VSS</td>
<td>0.2 VDD</td>
<td>V</td>
<td>Schmitt Trigger input</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CLOCK (GP5)</td>
<td>VSS</td>
<td>0.2 VDD</td>
<td>V</td>
<td>Schmitt Trigger input</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RESET</td>
<td>VSS</td>
<td>0.2 VDD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>PD9</td>
<td>VIH</td>
<td>Voltage input high level</td>
<td>DATA (GP4)</td>
<td>0.8 VDD</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CLOCK (GP5)</td>
<td>0.8 VDD</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RESET</td>
<td>0.8 VDD</td>
<td>—</td>
<td>VDD</td>
<td>V</td>
</tr>
</tbody>
</table>

Note 1: Program must be verified at the minimum and maximum VDD limits of the device.

Standard Operating Conditions:
Operating Temperature: +10°C ≤ TA ≤ +40°C, unless otherwise stated, (25°C is recommended)
Operating Voltage: 4.5V ≤ VDD ≤ 5.5V, unless otherwise stated.
7.2 Timing (AC) Characteristics

**FIGURE 7-2: PROGRAMMING MODE ENTRY WAVEFORM**

![Programming Mode Entry Waveform Diagram]

**TABLE 7-2: PROGRAMMING MODE ENTRY TIMING**

<table>
<thead>
<tr>
<th>Parameter No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>TR</td>
<td>RST/VPP rise time (VSS to VHH)</td>
<td>0.15</td>
<td>—</td>
<td>1.0</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>P2</td>
<td>TF</td>
<td>RST Fall time</td>
<td>0.5</td>
<td>—</td>
<td>1.0</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>P8</td>
<td>THLD0</td>
<td>Hold time after VPP = VHH to VDD valid</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>P8A</td>
<td>T PPDP</td>
<td>Hold time after VPP = VHH to CLOCK ↑</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>P8B</td>
<td>THLD0</td>
<td>Hold time after VDD valid to CLOCK ↑</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>P9</td>
<td>TCLOCK</td>
<td>CLOCK pin Period (in Time)</td>
<td>250</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>P9A</td>
<td>FCLOCK</td>
<td>CLOCK pin Period (in Frequency)</td>
<td>—</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>P10A</td>
<td>TCLKH</td>
<td>CLOCK pin High time</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>P10B</td>
<td>TCLKL</td>
<td>CLOCK pin Low time</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Program must be verified at the minimum and maximum VDD limits of the device.
**FIGURE 7-3: LOAD CONFIGURATION COMMAND WAVEFORM**

\[
\begin{array}{cccccc}
1 & 2 & 3 & 4 & 5 & 6 \\
\hline
CLOCK & & & & & \\
DATA & 0 & 0 & 0 & 0 & 0 \\
\end{array}
\]

**TABLE 7-3: LOAD CONFIGURATION COMMAND TIMING**

<table>
<thead>
<tr>
<th>Parameter No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3</td>
<td>TSET1</td>
<td>Data in setup time before clock ↓</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>P4</td>
<td>THLD1</td>
<td>Data in hold time after clock ↓</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>P6</td>
<td>TDLY2</td>
<td>Delay between clock ↓ to clock ↑ of next command or data</td>
<td>1.0</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Program must be verified at the minimum and maximum VDD limits of the device.
### FIGURE 7-4: LOAD DATA COMMAND WAVEFORM

<table>
<thead>
<tr>
<th>VDD = VDDMIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCLR/VPP = VihH</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CLOCK</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

### TABLE 7-4: LOAD DATA COMMAND TIMING

<table>
<thead>
<tr>
<th>Parameter No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3</td>
<td>TSET1</td>
<td>Data in setup time before clock ↓</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>P4</td>
<td>THLD1</td>
<td>Data in hold time after clock ↓</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>P6</td>
<td>TDLY2</td>
<td>Delay between clock ↓ to clock ↑ of next command or data</td>
<td>1.0</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Program must be verified at the minimum and maximum VDD limits of the device.
**FIGURE 7-5: READ DATA COMMAND WAVEFORM**

![Waveform Diagram]

**TABLE 7-5: READ DATA COMMAND TIMING**

<table>
<thead>
<tr>
<th>Parameter No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3</td>
<td>TSET1</td>
<td>Data in setup time before clock ↓</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>P4</td>
<td>THLD1</td>
<td>Data in hold time after clock ↓</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>P5</td>
<td>TDLY1</td>
<td>Data input not driven to next clock input (delay required between command/data or command/command)</td>
<td>0.9</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>P6</td>
<td>TDLY2</td>
<td>Delay between clock ↓ to clock ↑ of next command or data</td>
<td>1.0</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>P7</td>
<td>TDLY3</td>
<td>Clock ↑ to data out valid (during read data)</td>
<td>—</td>
<td>—</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Program must be verified at the minimum and maximum VDD limits of the device.
FIGURE 7-6: INCREMENT ADDRESS COMMAND WAVEFORM

\[ V_{DD} = V_{DD\text{MIN}} \]

\[ \text{MCLR/VPP} = V_{IH} \]

<table>
<thead>
<tr>
<th>Parameter No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3</td>
<td>TSET1</td>
<td>Data in setup time before clock ↓</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>P4</td>
<td>THLD1</td>
<td>Data in hold time after clock ↓</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>P6</td>
<td>TDLY2</td>
<td>Delay between clock ↓ to clock ↑ of next command or data</td>
<td>1.0</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Program must be verified at the minimum and maximum \( V_{DD} \) limits of the device.
FIGURE 7-7: BEGIN PROGRAMMING COMMAND WAVEFORM

VDD = VDDMIN
MCLR/VPP = VIHH
CLOCK
DATA

P11 End Programming Command

TABLE 7-7: BEGIN PROGRAMMING COMMAND TIMING

<table>
<thead>
<tr>
<th>Parameter No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3</td>
<td>TSET1</td>
<td>Data in setup time before clock ↓</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>P4</td>
<td>THLD1</td>
<td>Data in hold time after clock ↓</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>P11</td>
<td></td>
<td>Programming Pulse Width</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>User Memory</td>
<td>90</td>
<td>100</td>
<td>110</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Configuration Memory</td>
<td>90</td>
<td>100</td>
<td>110</td>
<td>µs</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Program must be verified at the minimum and maximum VDD limits of the device.
FIGURE 7-8: END PROGRAMMING COMMAND WAVEFORM

TABLE 7-8: END PROGRAMMING COMMAND TIMING

<table>
<thead>
<tr>
<th>Parameter No.</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3</td>
<td>TSET1</td>
<td>Data in setup time before clock ↓</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>P4</td>
<td>THLD1</td>
<td>Data in hold time after clock ↓</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>P6</td>
<td>TDLY2</td>
<td>Delay between clock ↓ to clock ↑ of next command or data</td>
<td>1.0</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>P11</td>
<td></td>
<td>Programming Pulse Width (1) User Memory</td>
<td>90</td>
<td>100</td>
<td>110</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Configuration Memory</td>
<td>90</td>
<td>100</td>
<td>110</td>
<td>µs</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Only required if the previous command was the Begin Programming Command.

2: Program must be verified at the minimum and maximum VDD limits of the device.
Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip’s products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, FilterLab, KEELog, MPLAB, PIC, PICmicro, PICMASTER, PICSTART, PRO MATE, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

dsPIC, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microD, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, MXDEV, PICC, PICDEM, PICDEM.net, rPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2001, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.
WORLDWIDE SALES AND SERVICE

AMERICAS
Corporate Office
2335 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Rocky Mountain
2335 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-564-0034 Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Dayton
Two Prestige Place, Suite 130
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit
Tri-Area Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo
2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1988 Fax: 949-263-1338

New York
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC
Australia
Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Beihai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-6766200 Fax: 86-28-6766599

China - Fuzhou
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Rm. 531, North Building
Fujian Foreign Trade Center Hotel
73 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7557563 Fax: 86-591-7557572

China - Shanghai
Microchip Technology Consulting (Shanghai) Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen
Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renninan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

Hong Kong
Microchip Technology Hong Kong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India
Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O’Shaughnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinjyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan
Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE
Denmark
Microchip Technology Nordic ApS
Regus Business Centre
Laatrup høj 1-3
Ballajoer DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Microchip Technology SARL
Parc d’Activite du Moulins de Massy
43 Rue du Saule Trappu
Batiment A 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144-0 Fax: 49-89-627-144-44

Italy
Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom
Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

© 2001 Microchip Technology Inc.