### Synchronous Buck Features

- **Input Voltage**: 4.5V to 40V (operating), 48V (non-operating)
- **Output Voltage**: 0.3V to 16V
  - 0.1% typical output voltage accuracy
  - Greater than 16V requires external divider
- **Switching Frequency**: 100 kHz to 1.6 MHz
- **Shutdown Quiescent Current**: 50 µA Typical
- **High-Drive**:
  - +5V Gate Drive
  - 2A Source Current
  - 2A Sink Current
- **Low-Drive**:
  - +5V Gate Drive
  - 2A Source Current
  - 4A Sink Current
- **Emulated Average Current Mode Control**
- **Differential Remote Output Sense**
- **Multi-Phase Systems**:
  - Master or Slave
  - Frequency Synchronized
  - Common Current Sense Signal
- **Multiple Output Systems**:
  - Master or Slave
  - Frequency Synchronized
- **AEC-Q100 Qualified**
- **Configureable Parameters**:
  - Overcurrent Limit
  - Input Undervoltage Lockout
  - Input Overvoltage
  - Output Overvoltage
  - Output Undervoltage
  - Internal Analog Compensation
  - Soft Start Profile
  - Synchronous Driver Dead Time
  - Switching Frequency
- **Thermal Shutdown**

### Microcontroller Features

- **Precision 8 MHz Internal Oscillator Block**:
  - Factory Calibrated
- **Interrupt Capable**
  - Firmware
  - Interrupt-on-Change Pins
- **Only 35 Instructions to Learn**
- **4096 Words On-Chip Program Memory**
- **High Endurance Flash**:
  - 100,000 Write Flash Endurance
  - Flash Retention: >40 years
- **Watchdog Timer (WDT) with Independent Oscillator for Reliable Operation**
- **Programmable Code Protection**
- **In-Circuit Debug (ICD) via Two Pins (MCP19123)**
- **In-Circuit Serial Programming™ (ICSP™) via Two Pins**
- **12 I/O Pins and One Input-Only Pin (MCP19122)**
  - 3 Open Drain Pins
  - 2 Weak Current Source Pins
- **16 I/O Pins and One Input-Only Pin (MCP19123)**
  - 3 Open Drain Pins
  - 2 Weak Current Source Pins
- **Analog-to-Digital Converter (ADC)**:
  - 10-bit Resolution
  - 24 Internal Channels
  - 8 External Channels
- **Timer0**: 8-bit Timer/Counter with 8-bit Prescaler
- **Enhanced Timer1**:
  - 16-bit Timer/Counter with Prescaler
  - 2 Selectable Clock Sources
  - External Gate Input Mode
- **Timer2**: 8-Bit Timer/Counter with Prescaler
  - 8-bit Period Register
- **Capture, Compare Module**
- **\(^2\text{C}^\text{TM} \text{Communication}**:
  - 7-bit Address Masking
  - 2 Dedicated Address Registers
  - SMBus/PMBus™ Compatibility
Pin Diagram – 24-Pin 4X4 QFN (MCP19122)
# TABLE 1: 24-PIN QFN (MCP19122) SUMMARY

<table>
<thead>
<tr>
<th>I/O</th>
<th>24-Pin QFN</th>
<th>ANSEL</th>
<th>A/D</th>
<th>Timers</th>
<th>MSSP</th>
<th>Interrupt</th>
<th>Pull-up</th>
<th>Basic</th>
<th>Additional</th>
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<tbody>
<tr>
<td>GPA0</td>
<td>1</td>
<td>Y</td>
<td>AN0</td>
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<td>—</td>
<td>IOC</td>
<td>Y</td>
<td>—</td>
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<tr>
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<td>IOC</td>
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<td>AN2</td>
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<td>IOC</td>
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<td>—</td>
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<td>IOC</td>
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<td>—</td>
<td>Weak Current Source</td>
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<tr>
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<td>—</td>
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<tr>
<td>GPA5</td>
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<td>—</td>
<td>IOC (4)</td>
<td>Y (5)</td>
<td>MCLR</td>
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<td>GPA6</td>
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<td>ICSPDAT</td>
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<td>SCL</td>
<td>IOC</td>
<td>N</td>
<td>ICSPCLK</td>
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<td>SDA</td>
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<td>—</td>
</tr>
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<td>—</td>
<td>IOC</td>
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<td>—</td>
<td>IOC</td>
<td>Y</td>
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</tr>
<tr>
<td>V&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>19</td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Device Input Voltage</td>
</tr>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
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<td>—</td>
<td>—</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>Internal Regulator Output</td>
</tr>
<tr>
<td>GND</td>
<td>9</td>
<td>N</td>
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<td>—</td>
<td>GND</td>
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</tr>
<tr>
<td>P&lt;sub&gt;GND&lt;/sub&gt;</td>
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</tr>
<tr>
<td>LDRV</td>
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</tr>
<tr>
<td>PHASE</td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Switch Node</td>
</tr>
<tr>
<td>BOOT</td>
<td>18</td>
<td>N</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
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<td>Floating Bootstrap Supply</td>
</tr>
<tr>
<td>+V&lt;sub&gt;SEN&lt;/sub&gt;</td>
<td>11</td>
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<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Output Voltage Differential Sense</td>
</tr>
<tr>
<td>−V&lt;sub&gt;SEN&lt;/sub&gt;</td>
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<td>—</td>
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<td>—</td>
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<td>—</td>
<td>Output Voltage Differential Sense</td>
</tr>
<tr>
<td>ISP</td>
<td>13</td>
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<td>—</td>
<td>—</td>
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<td>—</td>
<td>—</td>
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<td>Current Sense Input</td>
</tr>
<tr>
<td>ISN</td>
<td>12</td>
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<td>—</td>
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<td>—</td>
<td>—</td>
<td>Current Sense Input</td>
</tr>
<tr>
<td>EP</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Exposed Pad</td>
</tr>
</tbody>
</table>

**Note**

1: The Analog Debug Output is selected when the BUFFCON<BNCHEN> bit is set.
2: Selected when device is functioning as multiple output master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.
3: Selected when device is functioning as multi-phase master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.
4: The IOC is disabled when MCLR is enabled.
5: Weak pull-up always enabled when MCLR is enabled, otherwise the pull-up is under user control.
Pin Diagram – 28-Pin 5X5 QFN (MCP19123)
# TABLE 2: 28-PIN QFN (MCP19123) SUMMARY

<table>
<thead>
<tr>
<th>I/O</th>
<th>28-Pin QFN</th>
<th>ANSEL</th>
<th>A/D</th>
<th>Timers</th>
<th>MSSP</th>
<th>Interrupt</th>
<th>Pull-up</th>
<th>Basic</th>
<th>Additional</th>
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<tr>
<td>GPA0</td>
<td>1</td>
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<td>AN0</td>
<td>—</td>
<td>—</td>
<td>IOC</td>
<td>Y</td>
<td>—</td>
<td>Analog Debug Output (1)</td>
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<tr>
<td>GPA1</td>
<td>2</td>
<td>Y</td>
<td>AN1</td>
<td>—</td>
<td>—</td>
<td>IOC</td>
<td>Y</td>
<td>—</td>
<td>Sync Signal In/Out (2, 3)</td>
</tr>
<tr>
<td>GPA2</td>
<td>3</td>
<td>Y</td>
<td>AN2</td>
<td>T0CKI</td>
<td>—</td>
<td>IOC</td>
<td>Y</td>
<td>—</td>
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<tr>
<td>GPA3</td>
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<td>Exposed Pad</td>
</tr>
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</table>

**Note**
1: The Analog Debug Output is selected when the BUFFCON<BNCHEN> bit is set.
2: Selected when device is functioning as multiple output master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.
3: Selected when device is functioning as multi-phase master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.
4: The IOC is disabled when MCLR is enabled.
5: Weak pull-up always enabled when MCLR is enabled, otherwise the pull-up is under user control.
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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

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1.0 DEVICE OVERVIEW

The MCP19122/3 is a stand-alone mixed signal synchronous buck pulse-width modulated (PWM) current mode controller that features an integrated microcontroller core, high-endurance flash memory, communication and configurable analog circuitry. It features integrated synchronous drivers, bootstrap device, internal linear regulator and 4k words of nonvolatile memory. The devices are capable of efficiently converting 4.5V-40V to 0.3V-16V.

Since the MCP19122/3 uses traditional analog control circuitry to regulate the output of the DC/DC converter, the integration of the PIC® microcontroller mid-range core is used to provide complete customization of device operating parameters, start-up and shut-down profiles, protection levels and fault handling procedures.

After initial device configuration using Microchip’s MPLAB® X Integrated Development Environment (IDE) software, PMBus commands or I²C can be used by a host to communicate with, or modify, the operation of the MCP19122/3.

**FIGURE 1-1: TYPICAL APPLICATION CIRCUIT**
Note 1: Not implemented on the MCP19122.
## 2.0 PIN DESCRIPTION

The MCP19122/3 family of devices features pins that have multiple functions associated with each pin. Table 2-1 provides a description of the different functions. See Section 2.1 “Detailed Pin Description” for more detailed information.

### TABLE 2-1: MCP19122/3 PINOUT DESCRIPTION

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
<th>Input Type</th>
<th>Output Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPA0/AN0/ANALOG_TEST</td>
<td>GPA0</td>
<td>TTL</td>
<td>CMOS</td>
<td>General purpose I/O</td>
</tr>
<tr>
<td>AN0</td>
<td>AN</td>
<td>—</td>
<td>—</td>
<td>A/D Channel 0 input.</td>
</tr>
<tr>
<td>ANALOG_TEST</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Internal analog signal multiplexer output (1)</td>
</tr>
<tr>
<td>GPA1/AN1/SYC_SIGNAL</td>
<td>GPA1</td>
<td>TTL</td>
<td>CMOS</td>
<td>General purpose I/O</td>
</tr>
<tr>
<td>AN1</td>
<td>AN</td>
<td>—</td>
<td>—</td>
<td>A/D Channel 1 input</td>
</tr>
<tr>
<td>SYC_SIGNAL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Switching clock synchronization signal input and output (2,3)</td>
</tr>
<tr>
<td>GPA2/AN2/T0CKI/INT</td>
<td>GPA2</td>
<td>TTL</td>
<td>CMOS</td>
<td>General purpose I/O</td>
</tr>
<tr>
<td>AN2</td>
<td>AN</td>
<td>—</td>
<td>—</td>
<td>A/D Channel 2 input</td>
</tr>
<tr>
<td>T0CKI</td>
<td>ST</td>
<td>—</td>
<td>—</td>
<td>Timer0 clock input</td>
</tr>
<tr>
<td>INT</td>
<td>ST</td>
<td>—</td>
<td>—</td>
<td>External interrupt</td>
</tr>
<tr>
<td>GPA3/AN3/T1G1</td>
<td>GPA3</td>
<td>TTL</td>
<td>CMOS</td>
<td>General purpose I/O</td>
</tr>
<tr>
<td>AN3</td>
<td>AN</td>
<td>—</td>
<td>—</td>
<td>A/D Channel 3 input</td>
</tr>
<tr>
<td>T1G1</td>
<td>ST</td>
<td>—</td>
<td>—</td>
<td>Timer1 gate input 1</td>
</tr>
<tr>
<td>GPA4</td>
<td>GPA4</td>
<td>TTL</td>
<td>OD</td>
<td>General purpose I/O</td>
</tr>
<tr>
<td>GPA5/MCLR</td>
<td>GPA5</td>
<td>TTL</td>
<td>—</td>
<td>General purpose input only</td>
</tr>
<tr>
<td>MCLR</td>
<td>ST</td>
<td>—</td>
<td>—</td>
<td>Master Clear with internal pull-up</td>
</tr>
<tr>
<td>GPA6/CCD1(4)/ICSPDAT(5)</td>
<td>GPA6</td>
<td>ST</td>
<td>CMOS</td>
<td>General purpose I/O</td>
</tr>
<tr>
<td>CCD1</td>
<td>ST</td>
<td>CMOS</td>
<td>Capture/Compare input 1 (4)</td>
<td></td>
</tr>
<tr>
<td>ICSPDAT</td>
<td>CMOS</td>
<td>—</td>
<td>—</td>
<td>Serial Programming Data I/O (5)</td>
</tr>
<tr>
<td>GPA7/SCL/ICSPCLK(5)</td>
<td>GPA7</td>
<td>ST</td>
<td>OD</td>
<td>General purpose open drain I/O</td>
</tr>
<tr>
<td>SCL</td>
<td>ST</td>
<td>—</td>
<td>—</td>
<td>I²C clock</td>
</tr>
<tr>
<td>ICSPCLK</td>
<td>ST</td>
<td>—</td>
<td>—</td>
<td>Serial Programming Clock (5)</td>
</tr>
<tr>
<td>GPB0/SDA</td>
<td>GPB0</td>
<td>TTL</td>
<td>OD</td>
<td>General purpose I/O</td>
</tr>
<tr>
<td>SDA</td>
<td>I²C</td>
<td>OD</td>
<td>—</td>
<td>I²C data input/output</td>
</tr>
<tr>
<td>GPB1/AN4/CON_SIGNAL</td>
<td>GPB1</td>
<td>TTL</td>
<td>CMOS</td>
<td>General purpose I/O</td>
</tr>
<tr>
<td>AN4</td>
<td>AN</td>
<td>—</td>
<td>—</td>
<td>A/D Channel 4 input</td>
</tr>
<tr>
<td>CON_SIGNAL</td>
<td>—</td>
<td>—</td>
<td>Current sense output or current reference input (3)</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- AN = Analog input or output
- CMOS = CMOS compatible input or output
- OD = Open Drain
- TTL = TTL compatible input
- ST = Schmitt Trigger input with CMOS levels
- I²C = Schmitt Trigger input with I²C

**Note:**
1. Analog Test is selected when the BUFFCON<BNCHEN> bit is set.
2. Selected when device is functioning as multiple output master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.
3. Selected when device is functioning as multi-phase master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.
4. Feature only available on the MCP19123.
5. Feature only available on the MCP19122.
<table>
<thead>
<tr>
<th>Name</th>
<th>Function Type</th>
<th>Input Type</th>
<th>Output Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPB2/AN5/T1G2</td>
<td>GPB2</td>
<td>TTL</td>
<td>CMOS</td>
<td>General purpose I/O</td>
</tr>
<tr>
<td></td>
<td>AN5</td>
<td>AN</td>
<td>—</td>
<td>A/D Channel 5 input</td>
</tr>
<tr>
<td></td>
<td>T1G2</td>
<td>ST</td>
<td>—</td>
<td>Timer1 gate input 2</td>
</tr>
<tr>
<td>GPB3/CLOCK</td>
<td>GPB3</td>
<td>TTL</td>
<td>CMOS</td>
<td>General purpose I/O</td>
</tr>
<tr>
<td></td>
<td>CLOCK</td>
<td>—</td>
<td>—</td>
<td>Clock signal input/output (2,3)</td>
</tr>
<tr>
<td>GPB4/AN6/ICSPDAT</td>
<td>GPB4</td>
<td>TTL</td>
<td>CMOS</td>
<td>General purpose I/O (4)</td>
</tr>
<tr>
<td>ICDDAT</td>
<td>AN6</td>
<td>AN</td>
<td>—</td>
<td>A/D Channel 6 input (4)</td>
</tr>
<tr>
<td></td>
<td>ICSPDAT</td>
<td>ST</td>
<td>—</td>
<td>Serial Programming Data I/O (4)</td>
</tr>
<tr>
<td></td>
<td>ICDDAT</td>
<td>ST</td>
<td>—</td>
<td>In-circuit debug data (4)</td>
</tr>
<tr>
<td>GPB5/AN7/ICSPCLK</td>
<td>GPB5</td>
<td>TTL</td>
<td>CMOS</td>
<td>General purpose I/O (4)</td>
</tr>
<tr>
<td>ICCLK</td>
<td>AN7</td>
<td>AN</td>
<td>—</td>
<td>A/D Channel 7 input (4)</td>
</tr>
<tr>
<td></td>
<td>ISCPCLK</td>
<td>ST</td>
<td>—</td>
<td>Serial Programming Clock (4)</td>
</tr>
<tr>
<td></td>
<td>ICCLK</td>
<td>ST</td>
<td>—</td>
<td>In-circuit debug clock (4)</td>
</tr>
<tr>
<td>GPB6/CCD2</td>
<td>GPB6</td>
<td>TTL</td>
<td>CMOS</td>
<td>General purpose I/O</td>
</tr>
<tr>
<td></td>
<td>CCD2</td>
<td>ST</td>
<td>CMOS</td>
<td>Capture/Compare input (2,4)</td>
</tr>
<tr>
<td>GPB7/ VADC</td>
<td>GPB7</td>
<td>TTL</td>
<td>CMOS</td>
<td>General purpose I/O</td>
</tr>
<tr>
<td></td>
<td>VADC</td>
<td>AN</td>
<td>—</td>
<td>External voltage reference for A/D (4)</td>
</tr>
<tr>
<td>V_IN</td>
<td>V_IN</td>
<td>—</td>
<td>—</td>
<td>Device input supply voltage</td>
</tr>
<tr>
<td>V_DD</td>
<td>V_DD</td>
<td>—</td>
<td>—</td>
<td>Internal +5V LDO output pin</td>
</tr>
<tr>
<td>GND</td>
<td>GND</td>
<td>—</td>
<td>—</td>
<td>Small signal quiet ground</td>
</tr>
<tr>
<td>P_GND</td>
<td>P_GND</td>
<td>—</td>
<td>—</td>
<td>Large signal power ground</td>
</tr>
<tr>
<td>LDRV</td>
<td>LDRV</td>
<td>—</td>
<td>—</td>
<td>High-current drive signal connected to the gate of the low-side MOSFET</td>
</tr>
<tr>
<td>HDRV</td>
<td>HDRV</td>
<td>—</td>
<td>—</td>
<td>Floating high-current drive signal connected to the gate of the high-side MOSFET</td>
</tr>
<tr>
<td>PHASE</td>
<td>PHASE</td>
<td>—</td>
<td>—</td>
<td>Synchronous buck switch node connection</td>
</tr>
<tr>
<td>BOOT</td>
<td>BOOT</td>
<td>—</td>
<td>—</td>
<td>Floating bootstrap supply</td>
</tr>
<tr>
<td>+VSEN</td>
<td>+VSEN</td>
<td>—</td>
<td>—</td>
<td>Positive input of the output voltage sense differential amplifier</td>
</tr>
<tr>
<td>−VSEN</td>
<td>−VSEN</td>
<td>—</td>
<td>—</td>
<td>Negative input of the output voltage sense differential amplifier</td>
</tr>
<tr>
<td>ISP</td>
<td>ISP</td>
<td>—</td>
<td>—</td>
<td>Current sense input</td>
</tr>
<tr>
<td>ISN</td>
<td>ISN</td>
<td>—</td>
<td>—</td>
<td>Current sense input</td>
</tr>
<tr>
<td>EP</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>Exposed Thermal Pad</td>
</tr>
</tbody>
</table>

**Legend:**
- AN = Analog input or output  
- CMOS = CMOS compatible input or output  
- TTL = TTL compatible input  
- ST = Schmitt Trigger input with CMOS levels  
- OD = Open Drain  
- I2C = Schmitt Trigger input with I2C

**Note:**
1: Analog Test is selected when the BUFFCON<BNCHEN> bit is set.
2: Selected when device is functioning as multiple output master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.
3: Selected when device is functioning as multi-phase master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.
4: Feature only available on the MCP19123.
5: Feature only available on the MCP19122.
2.1 Detailed Pin Description

2.1.1 GPA0 PIN
GPA0 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available. AN0 is an input to the A/D. To configure this pin to be read by the A/D on channel 0, bits TRISA0 and ANSA0 must be set.

When the BUFFCON<BNCHEN> bit is set, this pin is configured as the ANALOG_TEST function. It is a buffered output of the internal analog and digital signal multiplexer. Analog signals present on this pin are controlled by the ADCON0 register; see Register 19-1. Digital signals present on this pin are controlled by the BUFFCON register; see Register 7-1.

2.1.2 GPA1 PIN
GPA1 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available. AN1 is an input to the A/D. To configure this pin to be read by the A/D on channel 1, bits TRISA1 and ANSA1 must be set.

When the MCP19122/3 is configured as a multiple output or multi-phase MASTER or SLAVE, this pin is configured to be the switching frequency synchronization input or output, SYN_SIGNAL. See Section 3.12 “System Configuration Control” for more information.

2.1.3 GPA2 PIN
GPA2 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak current source and interrupt-on-change are also available. AN2 is an input to the A/D. To configure this pin to be read by the A/D on channel 2, bits TRISA2 and ANSA2 must be set.

When bit T0CS is set, the T0CKI function is enabled. See Section 21.0 “Timer0 Module” for more information.

GPA2 can also be configured as an external interrupt by setting of the INTE bit. See Section 13.0.1 “GPA2/ INT Interrupt” for more information.

2.1.4 GPA3 PIN
GPA3 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak current source and interrupt-on-change are also available. AN3 is an input to the A/D. To configure this pin to be read by the A/D on channel 3, bits TRISA3 and ANSA3 must be set.

T1G1 is an input to the TIMER1 gate. To configure this pin to be an external source to the TIMER1 gate circuitry, see Section 22.0 “Timer1 Module With Gate Control”.

2.1.5 GPA4 PIN
GPA4 is a true open drain general purpose pin whose data direction is controlled in TRISGPA. There is no internal connection between this pin and device VDD, making this pin ideal to be used as an SMBus Alert pin. This pin does not have a weak pull-up, but interrupt-on-change is available.

2.1.6 GPA5 PIN
GPA5 is a general purpose TTL input-only pin. An internal weak pull-up and interrupt-on-change are also available.

For programming purposes, this pin is to be connected to the MCLR pin of the serial programmer. See Section 29.0 “In-Circuit Serial Programming™ (ICSP™)” for more information.

2.1.7 GPA6 PIN
GPA6 is a general purpose CMOS input/output pin whose data direction is controlled in TRISGPA. An interrupt-on-change is also available.

On the MCP19122, the ISCPDAT is the primary serial programming data input function. This is used in conjunction with ICSPCLK to serial program the device. This pin function is only implemented on the MCP19122.

On the MCP19123, this pin can be configured as an input to the CCD module. For more information refer to Section 24.0 “Dual Capture/Compare (CCD) Module”.

2.1.8 GPA7 PIN
GPA7 is a true open drain general purpose pin whose data direction is controlled in TRISGPA. There is no internal connection between this pin and device VDD. This pin does not have a weak pull-up, but interrupt-on-change is available.

When the MCP19122/3 is configured for I2C communication (see Section 27.2 “I2C Mode Overview”), GPA7 functions as the I2C clock, SCL. GPA7 functions as the I2C clock, SCL. On the MCP19122, the ISCPCLK is the serial programming clock function. This is used in conjunction with ISCPDAT to serial program the device. This pin function is only implemented on the MCP19122.
2.1.9 GPB0 PIN

GPB0 is a true open drain general purpose pin whose data direction is controlled in TRISGPB. There is no internal connection between this pin and device VDD. This pin does not have a weak pull-up, but interrupt-on-change is available.

When the MCP19122/3 is configured for I2C communication (see Section 27.2 “I2C Mode Overview”), GPB0 functions as the I2C clock, SDA.

2.1.10 GPB1 PIN

GPB1 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN4 is an input to the A/D. To configure this pin to be read by the A/D on channel 4, bits TRISB1 and ANSB1 must be set.

When the MCP19122/3 is configured as a multi-phase MASTER or SLAVE, this pin is configured to be the sensed current input or output signal. On a device configured to be a MASTER, this is an output signal of the sensed current that is to be shared with the SLAVE devices. On a device configured as a SLAVE, this is an input signal used to as a current regulation point. See Section 3.12 “System Configuration Control”, for more information.

2.1.11 GPB2 PIN

GPB2 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN5 is an input to the A/D. To configure this pin to be read by the A/D on channel 5, bits TRISB2 and ANSB2 must be set.

T1G2 is an input to the TIMER1 gate. To configure this pin to be an external source to the TIMER1 gate circuitry, see Section 22.0 “Timer1 Module With Gate Control”.

2.1.12 GPB3 PIN

GPB3 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

When the MCP19122/3 is configured as a multiple output or multi-phase Master or Slave, this pin is configured to be the switching frequency clock input or output. See Section 3.12 “System Configuration Control”.

2.1.13 GPB4 PIN

This pin and associated functions are only available on the MCP19123 device.

GPB4 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN6 is an input to the A/D. To configure this pin to be read by the A/D on channel 6, bits TRISB4 and ANSB4 must be set.

On the MCP19123, the ISCPDAT is the primary serial programming data input function. This is used in conjunction with ICSPCLK to serial program the device.

The ICDDAT is the in-circuit debug data function. This pin function is only implemented on the MCP19123. See Section 29.2 “In-Circuit Debugger”.

2.1.14 GBP5 PIN

This pin and associated functions is only available on the MCP19123 device.

GBP5 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN7 is an input to the A/D. To configure this pin to be read by the A/D on channel 7, bits TRISB5 and ANSB5 must be set.

On the MCP19123, the ISCPCLK is the primary serial programming clock function. This is used in conjunction with ISCPDAT to serial program the device.

The ICDDLK is the in-circuit debug clock function. This pin function is only implemented on the MCP19123. See Section 29.2 “In-Circuit Debugger”.

2.1.15 GPB6 PIN

This pin and associated functions is only available on the MCP19123 device.

GPB6 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

CCD2 is an input to the CCD module. For more information refer to Section 24.0 “Dual Capture/Compare (CCD) Module”.

2.1.16 GPB7 PIN

This pin and associated functions is only available on the MCP19123 device.

GPB7 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

VADC is an external A/D reference voltage input. See Section 19.0 “Analog-to-Digital Converter (ADC) Module”.

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2.1.17 **V\textsubscript{IN}** PIN
Device input power connection pin. It is recommended that capacitance be placed between this pin and the GND pin of the device.

2.1.18 **V\textsubscript{DD}** PIN
The output of the internal +5.0V regulator is connected to this pin. It is recommended that a 1.0 µF bypass capacitor be connected between this pin and the GND pin of the device. The bypass capacitor should be placed physically close to the device.

2.1.19 **GND** PIN
GND is the small signal ground connection pin. This pin should be connected to the exposed pad, on the bottom of the package.

2.1.20 **P\textsubscript{GND}** PIN
Connect all large signal level ground returns to P\textsubscript{GND}. These large-signal level ground traces should have a small loop area and minimal length to prevent coupling of switching noise to sensitive traces.

2.1.21 **LDRV** PIN
The gate of the low-side or rectifying MOSFET is connected to LDRV. The PCB trace connecting LDRV to the gate must be of minimal length and appropriate width to handle the high peak drive currents and fast voltage transitions.

2.1.22 **HDRV** PIN
The gate of the high-side MOSFET is connected to HDRV. This is a floating driver referenced to PHASE. The PCB trace connecting HDRV to the gate must be of minimal length and appropriate width to handle the high peak drive current and fast voltage transitions.

2.1.23 **PHASE** PIN
The PHASE pin provides the return path for the high-side gate driver. The source of the high-side MOSFET, drain of the low-side MOSFET and the inductor are connected to this pin.

2.1.24 **BOOT** PIN
The BOOT pin is the floating bootstrap supply pin for the high-side gate driver. A capacitor is connected between this pin and the PHASE pin to provide the necessary charge to turn on the high-side MOSFET.

2.1.25 **+V\textsubscript{SEN}** PIN
The non-inverting input of the unity gain amplifier used for output voltage remote sensing is connected to the +V\textsubscript{SEN} pin.

2.1.26 **-V\textsubscript{SEN}** PIN
The inverting input of the unity gain amplifier used for output voltage remote sensing is connected to the –V\textsubscript{SEN} pin.

2.1.27 **ISP** PIN
The non-inverting input of the current sense amplifier is connected to the ISP pin.

2.1.28 **ISN** PIN
The inverting input of the current sense amplifier is connected to the ISN pin.

2.1.29 **EXPOSED PAD (EP)**
There is no internal connection to the Exposed Thermal Pad. The EP should be connected to the GND pin and to the GND PCB plane to aid in the removal of the heat.
3.0 FUNCTIONAL DESCRIPTION

3.1 Internal Supplies

The operating input voltage of the MCP19122/3 ranges from 4.5V to 40V. There are two internal Low Dropout (LDO) voltage regulators. A 5V LDO (VDD) is used to power the internal microcontroller, the internal gate driver circuitry and provide a 5V output for external use. It is recommended that a 1 µF ceramic capacitor be placed between the VDD pin and the PGND pin.

The MODECON<VDDEN> bit controls the state of the 5V VDD LDO when the SLEEP command is issued to the MCP19122/3. See Section 3.12.3 “VDD LDO Control” for more information.

The gate drive current required to drive the external power MOSFETs must be added to the MCP19122/3 quiescent current IQ(max). This total current must be less than the maximum current, I DD-OUT, available from VDD that is specified in Section 4.0 “Electrical Characteristics”.

A second 4V LDO (AVDD) is used to power the internal analog circuitry. The AVDD is not available externally. AVDD is calibrated to 4.096V and is the default ADC reference voltage.

EQUATION 3-1: TOTAL REGULATOR CURRENT

\[ I_{DD-OUT} > (I_Q + I_{DRIVE} + I_{EXT}) \]

Where:
- I DD-OUT is the total current available from VDD
- I Q is the device quiescent current
- I DRIVE is the current required to drive the external MOSFETs
- I EXT is the amount of current used to power additional external circuitry.

EQUATION 3-2: GATE DRIVE CURRENT

\[ I_{DRIVE} = (Q_{gHIGH} + Q_{gLOW}) \times F_{SW} \]

Where:
- I DRIVE is the current required to drive the external MOSFETs
- Q gHIGH is the total gate charge of the high-side MOSFET
- Q gLOW is the total gate charge of the low-side MOSFET
- F SW is the switching frequency

3.2 Switching Frequency

The switching frequency is configurable over the range of 100 kHz to 1.6 MHz. The Timer2 module is used to generate the HDRV/LDRV switching frequency. Refer to Section 26.0, Enhanced PWM Module for more information. Example 3-1 shows how to configure the MCP19122/3 for a switching frequency of 300 kHz.

**EXAMPLE 3-1: CONFIGURING F SW**

<table>
<thead>
<tr>
<th>BANKSEL</th>
<th>T2CON</th>
<th>CLRF T2CON ;Turn off Timer2</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLRF</td>
<td>TMR2  ;Initialize module</td>
<td></td>
</tr>
<tr>
<td>MOV LW</td>
<td>0x19 ;Fsw=300 kHz</td>
<td></td>
</tr>
<tr>
<td>MOV LW</td>
<td>0x0A ;Max duty cycle=40%</td>
<td></td>
</tr>
<tr>
<td>MOV W</td>
<td>PR2</td>
<td></td>
</tr>
<tr>
<td>MOV LW</td>
<td>0x00 ;No phase shift</td>
<td></td>
</tr>
<tr>
<td>MOV W</td>
<td>PWMPHL</td>
<td></td>
</tr>
<tr>
<td>MOV W</td>
<td>PWMP HH</td>
<td></td>
</tr>
<tr>
<td>MOV LW</td>
<td>0x04 ;Turn on Timer2</td>
<td></td>
</tr>
<tr>
<td>MOV W</td>
<td>T2CON</td>
<td></td>
</tr>
</tbody>
</table>
3.3 Input Voltage Monitoring

The input voltage to the MCP19122/3 is monitored to determine an input undervoltage or an input overvoltage. It can also be measured by the ADC and reported as telemetry data.

3.3.1 INPUT UNDERVOLTAGE LOCKOUT

The VINUVLO register contains the digital value that sets the input under voltage lockout. When the input voltage on the VIN pin to the MCP19122/3 is below this programmed level, the PIR2<UVLOIF> status flag will be set. This bit is automatically cleared when the MCP19122/3 VIN voltage rises above this programmed level. The VINUVLO shall operate on a rising or falling input voltage. Hysteresis shall exist between the rising threshold that clears the flag and the failing threshold that sets the flag.

A hardware under voltage lockout path can be enabled by setting the VINCON<UVLOEN> bit. When this bit is set and the voltage on the VIN pin is below the threshold set by the VINUVLO register, hardware will keep the high-side and low-side MOSFET drivers off. Once the voltage on the VIN pin is greater than the threshold set by the VINUVLO register, the high-side and low-side MOSFET drivers are enabled.

To function properly, the VIN under voltage lockout setting must be lower than the VIN over voltage lockout setting. The state of the VINUVLO and VINOVL registers are unknown at power-up. Therefore if only the VIN under voltage lockout is desired, the VIN over voltage lockout threshold still must be set in the VINOVL register.

Note: The UVLOIF interrupt flag bit is set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register.

Note: The UVLOIF interrupt flag bit is set when an interrupt condition occurs regardless of the state of the VINCON<UVLOEN> bit.

REGISTER 3-1: VINUVLO: INPUT UNDER VOLTAGE LOCKOUT CONTROL REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>UVLO3</td>
<td>UVLO2</td>
<td>UVLO1</td>
<td>UVLO0</td>
</tr>
</tbody>
</table>

bit 7-

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

bit 7-4  Unimplemented: Read as ‘0’

bit 3-0  UVLO<3:0>: Under Voltage Lockout Configuration bits
0000 = 4.0V
0001 = 6.0V
0010 = 8.0V
0011 = 10.0V
0100 = 12.0V
0101 = 14.0V
0110 = 16.0V
0111 = 18.0V
1000 = 20.0V
1001 = 22.0V
1010 = 24.0V
1011 = 26.0V
1100 = 28.0V
1101 = 30.0V
1110 = 32.0V
1111 = 34.0V
3.3.2 INPUT OVER VOLTAGE LOCKOUT

The VINOVLO register contains the digital value that sets the input over voltage lockout. When the input voltage on the VIN pin to the MCP19122/3 is above this programmed level, the PIR2<OVLOIF> status flag will be set. This bit is automatically cleared when the MCP19122/3 VIN voltage falls below this programmed level. The VINOVLO shall operate on a rising or falling input voltage. Hysteresis shall exist between the rising threshold that sets the flag and the failing threshold that clears the flag.

A hardware over voltage lockout path can be enabled by setting the VINCON<OVLOEN> bit. When this bit is set and the voltage on the VIN pin is above the threshold set by the VINOVLO register, hardware will keep the high-side and low-side MOSFET drivers off. Once the voltage on the VIN pin is lower than the threshold set by the VINOVLO register, the high-side and low-side MOSFET drivers are enabled.

To function properly, the VIN overvoltage lockout setting must be lower than the VIN undervoltage lockout setting. The state of the VINUVLO and VINOVLO registers are unknown at power-up. Therefore if only the VIN overvoltage lockout is desired, the VIN undervoltage lockout threshold still must be set in the VINUVLO register.

Note: The OVLOIF interrupt flag bit is set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register.

Note: The OVLOIF interrupt flag bit is set when an interrupt condition occurs regardless of the state of the VINCON<OVLOEN> bit.

REGISTER 3-2: VINOVLO: INPUT OVERVOLTAGE LOCKOUT CONTROL REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

bit 7-4  Unimplemented: Read as ‘0’
bit 3-0  OVLO<3:0>: Overvoltage Lockout Configuration bits

- 0000 = 12.0V
- 0001 = 14.0V
- 0010 = 16.0V
- 0011 = 18.0V
- 0100 = 20.0V
- 0101 = 22.0V
- 0110 = 24.0V
- 0111 = 26.0V
- 1000 = 28.0V
- 1001 = 30.0V
- 1010 = 32.0V
- 1011 = 34.0V
- 1100 = 36.0V
- 1101 = 38.0V
- 1110 = 40.0V
- 1111 = 42.0V
3.3.3 INPUT UNDER/OVERVOLTAGE CONTROL REGISTER

The VINCON register is the comparator control register for both the input undervoltage lockout and input over-voltage lockout. It contains the enable bits, the polarity edge detection bits and the status output bits for both protection circuits. The interrupt flags <UVLOIF> and <OVLOIF> in the PIR2 register are independent of the enable <UVLOEN> and <OVLOEN> bits in the VINCON register. The <UVLOOUT> undervoltage lockout status output bit in the VINCON register indicates if an UVLO event has occurred. The <OVLOOUT> overvoltage lockout status output bit in the VINCON register indicates if an OVLO event has occurred.

When the input voltage on the V\textsubscript{IN} pin to the MCP19122/3 is below the threshold programmed by the VINUVLO register and the <UVLOEN> bit is set, both the HDRV and LDRV gate drivers are disabled.

When the input voltage on the V\textsubscript{IN} pin to the MCP19122/3 is above the threshold programmed by the VINOVLO register and the <OVLOEN> bit is set, both the HDRV and LDRV gate drivers are disabled.

## REGISTER 3-3: VINCON: INPUT VOLTAGE UVLO AND OVLO CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>UVLOEN</td>
<td>UVLOOUT</td>
<td>UVLOINTP</td>
<td>UVLOINTN</td>
<td>OVLOEN</td>
<td>OVLOOUT</td>
<td>OVLOINTP</td>
<td>OVLOINTN</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- ‘-n’ = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**bit 7**

- **UVLOEN**: UVLO Comparator Module Logic Enable bit
  - 1 = UVLO Comparator Module Logic enabled
  - 0 = UVLO Comparator Module Logic disabled

**bit 6**

- **UVLOOUT**: Undervoltage Lock Out Status bit
  - 1 = UVLO event has occurred
  - 0 = UVLO event has not occurred

**bit 5**

- **UVLOINTP**: UVLO Comparator Interrupt-on-Positive Going Edge Enable bit
  - 1 = UVLOIF will be set upon a positive going edge of the UVLO
  - 0 = No UVLOIF will be set upon a positive going edge of the UVLO

**bit 4**

- **UVLOINTN**: UVLO Comparator Interrupt on Negative Going Edge Enable bit
  - 1 = UVLOIF will be set upon a negative going edge of the UVLO
  - 0 = No UVLOIF will be set upon a negative going edge of the UVLO

**bit 3**

- **OVLOEN**: OVLO Comparator Module Logic Enable bit
  - 1 = OVLO Comparator Module Logic enabled
  - 0 = OVLO Comparator Module Logic disabled

**bit 2**

- **OVLOOUT**: Overvoltage Lock Out Status bit
  - 1 = OVLO event has occurred
  - 0 = OVLO event has not occurred

**bit 1**

- **OVLOINTP**: OVLO Comparator Interrupt on Positive Going Edge Enable bit
  - 1 = OVLOIF will be set upon a positive going edge of the OVLO
  - 0 = No OVLOIF will be set upon a positive going edge of the OVLO

**bit 0**

- **OVLOINTN**: OVLO Comparator Interrupt on Negative Going Edge Enable bit
  - 1 = OVLOIF will be set upon a negative going edge of the OVLO
  - 0 = No OVLOIF will be set upon a negative going edge of the OVLO
3.4 Output Overcurrent

The MCP19122/3 features a cycle-by-cycle peak current limit. By monitoring the OCIF interrupt flag, custom over current fault handling can be implemented.

To detect an output overcurrent, the MCP19122/3 senses the voltage drop across the high-side MOSFET while it is conducting. Leading-edge blanking is incorporated to mask the overcurrent measurement for a given amount of time. This helps prevent false overcurrent readings.

When an output overcurrent is sensed, the OCIF flag is set and the high-side drive signal is immediately terminated. Without any custom overcurrent handling implemented, the high-side drive signal will be asserted high at the beginning of the next clock cycle. If the overcurrent condition still exists, the high-drive signal will again be terminated.

The OCIF interrupt flag must be cleared in software. It can only be cleared once a switching cycle without an overcurrent condition has occurred.

Register OCCON contains the bits used to configure both the output overcurrent limit and the amount of leading edge blanking (see Register 3-4).

The OCCON<OCEN> bit must be set to enable the input overcurrent circuitry.

**Note:** The OCIF interrupt flag bit is set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register.
### REGISTER 3-4: OCCON: OUTPUT OVERCURRENT CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>OCEN</td>
<td>OCLEB1</td>
<td>OCLEB0</td>
<td>OOC4</td>
<td>OOC3</td>
<td>OOC2</td>
<td>OOC1</td>
<td>OOC0</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

- **bit 7**
  - **OCEN**: Output Overcurrent Control bit
    - 1 = Output Overcurrent comparator is enabled
    - 0 = Output Overcurrent comparator is disabled

- **bit 6-5**
  - **OCLEB<1:0>**: Leading Edge Blanking
    - 00 = 110 ns blanking
    - 01 = 200 ns blanking
    - 10 = 380 ns blanking
    - 11 = 740 ns blanking

- **bit 4-0**
  - **OOC<4:0>**: Output Overcurrent Configuration bits
    - 00000 = 91 mV drop
    - 00001 = 112 mV drop
    - 00010 = 134 mV drop
    - 00011 = 155 mV drop
    - 00100 = 177 mV drop
    - 00101 = 198 mV drop
    - 00110 = 220 mV drop
    - 00111 = 241 mV drop
    - 01000 = 263 mV drop
    - 01001 = 284 mV drop
    - 01010 = 306 mV drop
    - 01011 = 327 mV drop
    - 01100 = 350 mV drop
    - 01101 = 370 mV drop
    - 01110 = 392 mV drop
    - 01111 = 413 mV drop
    - 10000 = 435 mV drop
    - 10001 = 456 mV drop
    - 10010 = 478 mV drop
    - 10011 = 500 mV drop
    - 10100 = 521 mV drop
    - 10101 = 542 mV drop
    - 10110 = 585 mV drop
    - 10111 = 607 mV drop
    - 11000 = 628 mV drop
    - 11001 = 650 mV drop
    - 11010 = 671 mV drop
    - 11011 = 693 mV drop
    - 11100 = 714 mV drop
    - 11101 = 736 mV drop
    - 11110 = 757 mV drop
    - 11111 = 757 mV drop
3.5 Current Sensing

The system output current can be sensed by using either a low value resistor placed in series with the output or for applications that require the highest possible efficiency the series resistance (DCR) of the inductor. For applications that use DCR sensing, a resistor in series with a capacitor are placed around the inductor, as shown in Figure 3-1. If the value of \( R_S \) and \( C_S \) are chosen so the RC time constant matches the inductor time constant, the voltage appearing across \( C_S \) will equal the voltage across the DCR and therefore the current flowing through the inductor. Equation 3-3 can be used to select \( R_S \) and \( C_S \).

**FIGURE 3-1: INDUCTOR CURRENT SENSE FILTER**

![Figure 3-1 Diagram](image)

**EQUATION 3-3: CALCULATING FILTER VALUES**

\[
\frac{L}{DCR} = (R_S \times C_S)
\]

Where:
- \( L \) is the inductance value of the output inductor
- \( DCR \) is the series resistance of the output inductor
- \( R_S \) is the current sense filter resistor
- \( C_S \) is the current sense filter capacitor

3.5.1 CURRENT SENSE GAIN

The entire current sense path has a fixed gain of 32. Additional gain or attenuation can be added. The amount added is controlled by the CSGSCON register, Register 3-5. The gain added to this current sense signal does not change the +6 dB of current sense gain added before being read by the A/D.

3.5.2 INDUCTOR OR SENSE RESISTOR SELECTION

The DCR of the inductor or the value of the sense resistor are to be selected so the output of the internal current sense amplifier output does not exceed 3.0V at full load current. The internal current sense amplifier has a fixed gain of 32. See Equation 3-4.

**EQUATION 3-4: SENSE ELEMENT RESISTANCE**

\[
R_{\text{SENSE}} = \frac{AMP_{\text{VOUT}}}{AMP_{\text{GAIN}} \times I_{\text{MAX}}}
\]

Where:
- \( R_{\text{SENSE}} \) is the resistance of the sense element
- \( AMP_{\text{VOUT}} \) is the maximum output voltage of the current sense amplifier
- \( AMP_{\text{GAIN}} \) is the fixed gain of the current sense amplifier
- \( I_{\text{MAX}} \) is the maximum application load current

3.5.3 MEASURING SYSTEM LOAD CURRENT

The system load current can be measured by the internal ADC. Before being measured by the ADC, the sampled current is gained by a fixed +6 dB. It is recommended that multiple ADC readings of the sampled current be taken and averaged together to provide a more uniform measurement.
**REGISTER 3-5: CSGSCON: CURRENT SENSE GAIN CONTROL REGISTER**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CSGS4</td>
<td>CSGS3</td>
<td>CSGS2</td>
<td>CSGS1</td>
<td>CSGS0</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **x** = Bit is unknown

*bit 7-5 Unimplemented: Read as ‘0’*

*bit 4-0 CSGS<4:0>: Current Sense Gain Setting bits*

<table>
<thead>
<tr>
<th>Setting</th>
<th>Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>000000</td>
<td>-3.0 dB</td>
</tr>
<tr>
<td>000010</td>
<td>-2.6 dB</td>
</tr>
<tr>
<td>000011</td>
<td>-2.4 dB</td>
</tr>
<tr>
<td>000100</td>
<td>-2.2 dB</td>
</tr>
<tr>
<td>000101</td>
<td>-2.0 dB</td>
</tr>
<tr>
<td>000110</td>
<td>-1.8 dB</td>
</tr>
<tr>
<td>000111</td>
<td>-1.6 dB</td>
</tr>
<tr>
<td>001000</td>
<td>-1.4 dB</td>
</tr>
<tr>
<td>001001</td>
<td>-1.2 dB</td>
</tr>
<tr>
<td>001010</td>
<td>-1.0 dB</td>
</tr>
<tr>
<td>001011</td>
<td>-0.8 dB</td>
</tr>
<tr>
<td>001100</td>
<td>-0.6 dB</td>
</tr>
<tr>
<td>001101</td>
<td>-0.4 dB</td>
</tr>
<tr>
<td>001110</td>
<td>-0.2 dB</td>
</tr>
<tr>
<td>001111</td>
<td>0.0 dB</td>
</tr>
<tr>
<td>010000</td>
<td>0.2 dB</td>
</tr>
<tr>
<td>010001</td>
<td>0.4 dB</td>
</tr>
<tr>
<td>010010</td>
<td>0.6 dB</td>
</tr>
<tr>
<td>010011</td>
<td>0.8 dB</td>
</tr>
<tr>
<td>010100</td>
<td>1.0 dB</td>
</tr>
<tr>
<td>010101</td>
<td>1.2 dB</td>
</tr>
<tr>
<td>010110</td>
<td>1.4 dB</td>
</tr>
<tr>
<td>010111</td>
<td>1.6 dB</td>
</tr>
<tr>
<td>011000</td>
<td>1.8 dB</td>
</tr>
<tr>
<td>011001</td>
<td>2.0 dB</td>
</tr>
<tr>
<td>011010</td>
<td>2.2 dB</td>
</tr>
<tr>
<td>011011</td>
<td>2.4 dB</td>
</tr>
<tr>
<td>011100</td>
<td>2.6 dB</td>
</tr>
<tr>
<td>011101</td>
<td>2.8 dB</td>
</tr>
<tr>
<td>011110</td>
<td>3.0 dB</td>
</tr>
<tr>
<td>011111</td>
<td>3.2 dB</td>
</tr>
</tbody>
</table>
3.6 Control Parameters

3.6.1 COMPENSATION SETTING

The MCP19122/3 is an emulated current mode controller with integrated compensation. The desired response of the overall loop can be tuned by proper placement of the compensation zero frequency and gain. The CMPZCON register, Register 3-6, is used to adjust the compensation zero frequency and gain. Figure 3-2 shows a simplified drawing of the internal compensation with and the adjustable gain differential amplifier.

REGISTER 3-6: CMPZCON: COMPENSATION SETTING CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMPZF3</td>
<td>CMPZF2</td>
<td>CMPZF1</td>
<td>CMPZF0</td>
<td>CMPZG3</td>
<td>CMPZG2</td>
<td>CMPZG1</td>
<td>CMPZG0</td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 6</td>
<td>bit 5</td>
<td>bit 4</td>
<td>bit 3</td>
<td>bit 2</td>
<td>bit 1</td>
<td>bit 0</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 7-4 **CMPZF<3:0>:** Compensation Zero Frequency Setting bits
- 0000 = 1500 Hz
- 0001 = 1850 Hz
- 0010 = 2300 Hz
- 0011 = 2840 Hz
- 0100 = 3460 Hz
- 0101 = 4300 Hz
- 0110 = 5300 Hz
- 0111 = 6630 Hz
- 1000 = 8380 Hz
- 1001 = 9950 Hz
- 1010 = 12200 Hz
- 1011 = 14400 Hz
- 1100 = 18700 Hz
- 1101 = 23000 Hz
- 1110 = 28400 Hz
- 1111 = 35300 Hz

bit 3-0 **CMPZG<3:0>:** Compensation Gain Setting bits
- 0000 = 30.13 dB
- 0001 = 27.73 dB
- 0010 = 24.66 dB
- 0011 = 22.41 dB
- 0100 = 20.08 dB
- 0101 = 17.78 dB
- 0110 = 15.42 dB
- 0111 = 13.06 dB
- 1000 = 10.75 dB
- 1001 = 8.30 dB
- 1010 = 6.02 dB
- 1011 = 3.52 dB
- 1100 = 1.21 dB
- 1101 = −1.41 dB
- 1110 = −3.74 dB
- 1111 = −6.02 dB
3.6.2 SLOPE COMPENSATION RAMP

The difference between the average inductor current and the DC value of the sampled inductor current can cause instability for certain operating conditions. This instability occurs when the inductor ripple current does not return to its initial value by the start of the next switching cycle. Adding slope compensation ramp to the current sense signal prevents this oscillation. The amount of slope added is controlled by the RAMPCON register, Register 3-7.

**Note 1:** To enable the slope compensation circuitry, the RAMPCON<RAMPEN> bit must be cleared.

**REGISTER 3-7: RAMPCON: COMPENSATION RAMP CONTROL REGISTER**

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMPEN</td>
<td>—</td>
<td>—</td>
<td>RMP4</td>
<td>RMP3</td>
<td>RMP2</td>
<td>RMP1</td>
<td>RMP0</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- -n = Value at POR
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown

**bit 7** **RMPEN:** Compensation Ramp Disable bit

- 1 = Compensation ramp is disabled
- 0 = Compensation ramp is enabled

**bit 6-5** **Unimplemented:** Read as '0'

**bit 4-0** **RMP<4:0>:** Compensation Ramp Configuration bits

\[ RMP<4 : 0> = \left(\frac{dV}{dt} \times 200/V_{IN}\right) \]

Where \(dV/dt\) is in V/\(\mu\)s
3.7 Determining System Output Voltage

3.7.1 REFERENCE VOLTAGE CONFIGURATION

The control system reference voltage is determined by the setting contained in the 10-bit \( V_{\text{REF}} \) DAC. The system reference is adjustable in 2 mV typical increments. The configuring of this DAC is accomplished by the settings contained in the VOUTH and VOUTL registers. See Equation 3-5 for more information.

**Note 1:** To enable the slope compensation circuitry, the RAMPCON<RAMPEN> bit must be cleared.

See Section 4.0, Electrical Characteristics for more information regarding the DAC specification.

**REGISTER 3-8: VOUTL: OUTPUT VOLTAGE SET POINT LSB CONTROL REGISTER**

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOUT7</td>
<td>VOUT6</td>
<td>VOUT5</td>
<td>VOUT4</td>
<td>VOUT3</td>
<td>VOUT2</td>
<td>VOUT1</td>
<td>VOUT0</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 7-0 \( \text{VOUT}<7:0> \): Output Voltage Set Point LSB Configuration bits

**REGISTER 3-9: VOUTH: OUTPUT VOLTAGE SET POINT MSB CONTROL REGISTER**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>VOUT9</td>
<td>VOUT8</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 7-2 Unimplemented: Read as ‘0’

bit 1-0 \( \text{OVOUT}<9:8> \): Output Voltage Set Point MSB Configuration bits
3.7.2 DIFFERENTIAL AMPLIFIER GAIN CONTROL

The MCP19122/3 contains a low offset programmable gain differential amplifier used for remote sensing of the output voltage. Connect the +VSEN and –VSEN pins directly at the load for better load regulation. The +VSEN and –VSEN are the positive and negative inputs, respectively, of the programmable gain differential amplifier.

The programmable gain settings are controlled by the DAGCON register, Register 3-10.

EQUATION 3-5: SYSTEM OUTPUT VOLTAGE

\[ V_{REFDAC} = \frac{V_{OUT}}{DAG \times DACSTEP} \]

Where:
- \( V_{REFDAC} \) is the concatenated decimal value of VOUTH and VOUTL
- \( DAG \) is the programmable gain of the differential amplifier.
- \( DACSTEP \) is the volts/step of the reference voltage DAC, typically 2 mV/step
- \( V_{OUT} \) is the desired output voltage

Note 1: If the hexadecimal \( V_{REFDAC} \) value calculated is larger than 10-bits, the programmable gain differential amplifier gain must be adjusted.

REGISTER 3-10: DAGCON: DIFFERENTIAL AMPLIFIER GAIN CONTROL REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>DAG2</td>
<td>DAG1</td>
<td>DAG0</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- ’n’ = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 7-3 Unimplemented: Read as ‘0’

bit 2-0 DAG<2:0>: Differential Amplifier Gain control bit

000 = Gain of 1
001 = Gain of 1/2
010 = Gain of 1/4
011 = Gain of 1/8
100 = Gain of 2
101 = Gain of 4
110 = Gain of 8
111 = Gain of 1
3.8 System Output Voltage Protection

The MCP19122/3 provides the option for hardware and/or software protection for a system output under voltage as well as a system output over voltage.

3.8.1 OUTPUT UNDERSHOT

The output voltage is monitored and compared to an adjustable undervoltage (UV) reference. When the output voltage is below the UV reference the PIR2<UVIF> flag is set. If the hardware UV accelerator response circuitry (see Register 3-14) is enabled, the high-side MOSFET is turned on until the maximum programmed duty cycle is reached. Then the low-side MOSFET is turned on for the remainder of the switching period.

Once the output voltage is above the UV reference the MCP19122/3 returns to normal operation. The UVIF flag must be cleared in software.

The output undervoltage reference is controlled by the VOTUVLO register, Register 3-11. A fixed voltage is subtracted from the adjustable system output voltage reference.

**Note 1:** The system output voltage reference is determined by the setting in the VOUTH and VOUTL registers.

**Note 2:** The UVIF interrupt flag bit is set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INT-CON register.

**REGISTER 3-11: VOTUVLO: OUTPUT UNDER VOLTAGE DETECT LEVEL CONTROL REGISTER**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>OUV3</td>
<td>OUV2</td>
<td>OUV1</td>
<td>OUV0</td>
</tr>
</tbody>
</table>

**Legend:**

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'

-\(n\) = Value at POR  
\('1\)' = Bit is set  
\('0\)' = Bit is cleared  
x = Bit is unknown

**bit 7-4** Unimplemented: Read as '0'

**bit 3-0** **OUV<3:0>: Output Under Voltage Detect Level Configuration bits**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>(V_{\text{REF}} - 50 \text{ mV})</td>
</tr>
<tr>
<td>0001</td>
<td>(V_{\text{REF}} - 80 \text{ mV})</td>
</tr>
<tr>
<td>0010</td>
<td>(V_{\text{REF}} - 110 \text{ mV})</td>
</tr>
<tr>
<td>0011</td>
<td>(V_{\text{REF}} - 140 \text{ mV})</td>
</tr>
<tr>
<td>0100</td>
<td>(V_{\text{REF}} - 170 \text{ mV})</td>
</tr>
<tr>
<td>0101</td>
<td>(V_{\text{REF}} - 200 \text{ mV})</td>
</tr>
<tr>
<td>0110</td>
<td>(V_{\text{REF}} - 230 \text{ mV})</td>
</tr>
<tr>
<td>0111</td>
<td>(V_{\text{REF}} - 260 \text{ mV})</td>
</tr>
<tr>
<td>1000</td>
<td>(V_{\text{REF}} - 290 \text{ mV})</td>
</tr>
<tr>
<td>1001</td>
<td>(V_{\text{REF}} - 320 \text{ mV})</td>
</tr>
<tr>
<td>1010</td>
<td>(V_{\text{REF}} - 350 \text{ mV})</td>
</tr>
<tr>
<td>1011</td>
<td>(V_{\text{REF}} - 380 \text{ mV})</td>
</tr>
<tr>
<td>1100</td>
<td>(V_{\text{REF}} - 410 \text{ mV})</td>
</tr>
<tr>
<td>1101</td>
<td>(V_{\text{REF}} - 440 \text{ mV})</td>
</tr>
<tr>
<td>1110</td>
<td>(V_{\text{REF}} - 470 \text{ mV})</td>
</tr>
<tr>
<td>1111</td>
<td>(V_{\text{REF}} - 500 \text{ mV})</td>
</tr>
</tbody>
</table>
3.8.2 OUTPUT OVER VOLTAGE

The output voltage is monitored and compared to an adjustable over voltage (OV) reference. When the output voltage is above OV reference the PIR2<OVIF> flag is set. If the hardware OV accelerator response circuitry, see Register 3-14, is enabled the high-side and low-side MOSFETs are turned off until the output voltage fails below the output over voltage reference. Once the output voltage is below the OV reference the MCP19122/3 returns to normal operation. The OVIF flag must be cleared in software.

The output under voltage reference is controlled by the VOTOVLO register, Register 3-12. A fixed voltage is added to the adjustable system output voltage reference.

Note 1: The system output voltage reference is determined by the setting in the VOUTH and VOUTL registers.

2: The OVIF interrupt flag bit is set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register.

REGISTER 3-12: VOTOVLO: OUTPUT OVER VOLTAGE DETECT LEVEL CONTROL REGISTER

<table>
<thead>
<tr>
<th>bit 7-4</th>
<th>bit 3-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>R/W-x</td>
<td>R/W-x</td>
</tr>
<tr>
<td>R/W-x</td>
<td>R/W-x</td>
</tr>
<tr>
<td>Unimplemented: Read as ‘0’</td>
<td></td>
</tr>
</tbody>
</table>

bit 3-0

OOV<3:0>: Output Over Voltage Detect Level Configuration bits

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>VREF + 50 mV</td>
</tr>
<tr>
<td>0001</td>
<td>VREF + 80 mV</td>
</tr>
<tr>
<td>0010</td>
<td>VREF + 110 mV</td>
</tr>
<tr>
<td>0011</td>
<td>VREF + 140 mV</td>
</tr>
<tr>
<td>0100</td>
<td>VREF + 170 mV</td>
</tr>
<tr>
<td>0101</td>
<td>VREF + 200 mV</td>
</tr>
<tr>
<td>0110</td>
<td>VREF + 230 mV</td>
</tr>
<tr>
<td>0111</td>
<td>VREF + 260 mV</td>
</tr>
<tr>
<td>1000</td>
<td>VREF + 290 mV</td>
</tr>
<tr>
<td>1001</td>
<td>VREF + 320 mV</td>
</tr>
<tr>
<td>1010</td>
<td>VREF + 350 mV</td>
</tr>
<tr>
<td>1011</td>
<td>VREF + 380 mV</td>
</tr>
<tr>
<td>1100</td>
<td>VREF + 410 mV</td>
</tr>
<tr>
<td>1101</td>
<td>VREF + 440 mV</td>
</tr>
<tr>
<td>1110</td>
<td>VREF + 470 mV</td>
</tr>
<tr>
<td>1111</td>
<td>VREF + 500 mV</td>
</tr>
</tbody>
</table>
3.9 Internal Synchronous Driver

The internal synchronous driver is capable of driving two N-Channel MOSFETs in a synchronous rectified buck converter topology. The gate of the floating MOSFET is connected to the HDRV pin. The source of this MOSFET is connected to the PHASE pin. This pin is capable of sourcing and sinking 2A of peak current.

The MOSFET connected to the LDRV pin is not floating. The low-side MOSFET gate is connected to the LDRV pin and the source of this MOSFET is connected to P_{GND}. This pin is capable of sourcing a peak current of 2A. The peak sink current is 4A. This helps keep the low-side MOSFET off when the high-side MOSFET is turning on.

3.9.1 MOSFET DRIVER DEAD TIME

The MOSFET driver dead time is defined as the time between one drive signal going low and the complimentary drive signal going high. Refer to Figure 3-3. The MCP19122/3 has the capability to adjust both the high-side and low-side driver dead time independently. The adjustment of the driver dead time is controlled by the DEADCON register.

Note 1: The DEADCON register controls the amount of dead time added to the HDRV or LDRV signal.

3.9.2 MOSFET DRIVER CONTROL

The MCP19122/3 has the ability to independently disable high-side or low-side driver circuitry. This control of the HDRV or LDRV signal is accomplished by setting or clearing the HIDIS or LODIS bits in the PE1 register. When either driver is disabled, the output signal is set low. The default power-on or reset state is to have the high-side and low-side drivers disabled.

3.10 High-Side MOSFET Driver Supply

A floating voltage is required by the high-side driver. An external bootstrap capacitor connected between the BOOT and PHASE pins supplies this gate drive voltage. This capacitor is charged by internally connecting the BOOT pin to V_{DD} when the PHASE pin is low.

The selection of the bootstrap capacitor is based upon the total charge of the high-side power MOSFET and the allowable droop in the voltage applied to the gate of the high-side power MOSFET.

EQUATION 3-6: BOOTSTRAP CAPACITOR

\[ C_{BOOT} = \frac{Q_{G(Total)}}{\Delta V_{DROOP}} \]

Where:
- \( Q_{G(Total)} \) = High-side MOSFET Total Gate Charge (C)
- \( V_{DROOP} \) = Allowable Gate Drive Voltage Droop (V)
## MCP19122/3

### REGISTER 3-13: DEADCON: DRIVER DEAD TIME CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>HDLY3</td>
<td>HDLY2</td>
<td>HDLY1</td>
<td>HDLY0</td>
<td>LDLY3</td>
<td>LDLY2</td>
<td>LDLY1</td>
<td>LDLY0</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**bit 7-4**

HDLY<3:0>: High-Side Dead Time Configuration bits

<table>
<thead>
<tr>
<th>Code</th>
<th>Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>14 ns</td>
</tr>
<tr>
<td>0001</td>
<td>18 ns</td>
</tr>
<tr>
<td>0010</td>
<td>22 ns</td>
</tr>
<tr>
<td>0011</td>
<td>26 ns</td>
</tr>
<tr>
<td>0100</td>
<td>30 ns</td>
</tr>
<tr>
<td>0101</td>
<td>34 ns</td>
</tr>
<tr>
<td>0110</td>
<td>38 ns</td>
</tr>
<tr>
<td>0111</td>
<td>42 ns</td>
</tr>
<tr>
<td>1000</td>
<td>46 ns</td>
</tr>
<tr>
<td>1001</td>
<td>50 ns</td>
</tr>
<tr>
<td>1010</td>
<td>54 ns</td>
</tr>
<tr>
<td>1011</td>
<td>58 ns</td>
</tr>
<tr>
<td>1100</td>
<td>62 ns</td>
</tr>
<tr>
<td>1101</td>
<td>66 ns</td>
</tr>
<tr>
<td>1110</td>
<td>70 ns</td>
</tr>
<tr>
<td>1111</td>
<td>74 ns</td>
</tr>
</tbody>
</table>

**bit 3-0**

LDLY<3:0>: Low-Side Dead Time Configuration bits

<table>
<thead>
<tr>
<th>Code</th>
<th>Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>-4 ns</td>
</tr>
<tr>
<td>0001</td>
<td>0 ns</td>
</tr>
<tr>
<td>0010</td>
<td>4 ns</td>
</tr>
<tr>
<td>0011</td>
<td>8 ns</td>
</tr>
<tr>
<td>0100</td>
<td>12 ns</td>
</tr>
<tr>
<td>0101</td>
<td>16 ns</td>
</tr>
<tr>
<td>0110</td>
<td>20 ns</td>
</tr>
<tr>
<td>0111</td>
<td>24 ns</td>
</tr>
<tr>
<td>1000</td>
<td>28 ns</td>
</tr>
<tr>
<td>1001</td>
<td>32 ns</td>
</tr>
<tr>
<td>1010</td>
<td>36 ns</td>
</tr>
<tr>
<td>1011</td>
<td>40 ns</td>
</tr>
<tr>
<td>1100</td>
<td>44 ns</td>
</tr>
<tr>
<td>1101</td>
<td>48 ns</td>
</tr>
<tr>
<td>1110</td>
<td>52 ns</td>
</tr>
<tr>
<td>1111</td>
<td>56 ns</td>
</tr>
</tbody>
</table>
3.11 Analog Peripheral Control

The MCP19122/3 has various analog peripherals. These peripherals can be configured to allow customizable operation. Refer to Register 3-14 more information.

3.11.1 DIODE EMULATION MODE

The MCP19122/3 can operate in either diode emulation or synchronous rectification mode. When operating in diode emulation mode, the LDRV signal is terminated when the voltage across the low-side MOSFET is approximately 0V. This provides better light load efficiency by preventing reverse current from flowing through the inductor. Both the HDRV and LDRV signals are low until the beginning of the next switching cycle. At that time, the HDRV signal is asserted high, turning on the high-side MOSFET.

The PE1<DECON> bit controls the diode emulation operating mode of the MCP19122/3.

3.11.2 HIGH-SIDE DRIVER CONTROL

The high-side driver is enabled by clearing the PE1<HIDIS> bit. Setting this bit disables the high-side driver.

Note: The HIDIS bit is reset to ‘1’ so the high-side driver is in a known state after reset. This bit must be cleared by software for normal operation.

3.11.3 LOW-SIDE DRIVE CONTROL

The low-side driver is enabled by clearing the PE1<LODIS> bit. Setting this bit disables the low-side driver.

Note: The LODIS bit is reset to ‘1’ so the low-side driver is in a known state after reset. This bit must be cleared by software for normal operation.

3.11.4 OUTPUT UNDERTENSION ACCELERATOR

The MCP19122/3 has additional control circuitry to allow it to respond quickly to an output undervoltage condition. The enabling of this circuitry is handled by the PE1<UVTEE> bit. When this bit is set, the MCP19122/3 will respond to an output undervoltage condition by turning off the high-side and low-side MOSFETs until the output voltage is below the output undervoltage threshold set by the OUVCON register. The undervoltage reference is controlled by the VOTUVO register, Register 3-11.

3.11.5 OUTPUT OVER VOLTAGE ACCELERATOR

The MCP19122/3 has additional control circuitry to allow it to respond quickly to an output overvoltage condition. The enabling of this circuitry is handled by the PE1<OVTEE> bit. When this bit is set, the MCP19122/3 will respond to an output overvoltage condition by turning off the high-side and low-side MOSFETs until the output voltage is below the output overvoltage threshold set by the OOVCON register. The overvoltage reference is controlled by the VOTOVLO register, Register 3-12.

3.11.6 RELATIVE EFFICIENCY RAMP MEASUREMENT CONTROL

The PE1<SPAN> bit determines what portion of the Relative Efficiency Measurement timing ramp is connected to A/D channel 0x08h. When the PE1<MEASEN> bit is low and the PE1<SPAN> bit is low, the RELEFF channel of the A/D (channel 0x08h) will measure the valley of the relative efficiency timing ramp. When the PE1<MEASEN> is low and the PE1<SPAN> bit is hit, the RELEFF channel of the A/D will measure the peak of the relative efficiency timing ramp.
## REGISTER 3-14: PE1: ANALOG PERIPHERAL ENABLE 1 CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td><strong>DECON</strong></td>
<td><strong>TOPO</strong></td>
<td><strong>HIDIS</strong></td>
<td><strong>LODIS</strong></td>
<td><strong>MEASEN</strong></td>
<td><strong>SPAN</strong></td>
<td><strong>UVTEE</strong></td>
<td><strong>OVTEE</strong></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**bit 7 DECON (Diode Emulation Mode bit):**
- 1 = Diode emulation mode enabled
- 0 = Synchronous rectification mode enabled

**bit 6 TOPO (Topology selection control bit):**
- 1 = Boost topology is enabled
- 0 = Buck topology is enabled

**bit 5 HIDIS (High-side driver control bit):**
- 1 = High-side driver is disabled
- 0 = High-side driver is enabled

**bit 4 LODIS (Low-side driver control bit):**
- 1 = Low-side driver is disabled
- 0 = Low-side driver is enabled

**bit 3 MEASEN (Relative efficiency measurement control bit):**
- 1 = Initiate relative efficiency measurement
- 0 = Relative efficiency measurement not in progress

**bit 2 SPAN (Relative efficiency ramp measurement control bit):**
- 1 = A/D channel 0x08h measures the peak of the RELEFF signal
- 0 = A/D channel 0x08h measures the valley of the RELEFF signal

**bit 1 UVTEE (Output Undervoltage Accelerator Enable bit):**
- 1 = Output undervoltage accelerator is enabled
- 0 = Output undervoltage accelerator is disabled

**bit 0 OVTEE (Output Overvoltage Accelerator Enable bit):**
- 1 = Output overvoltage accelerator is enabled
- 0 = Output overvoltage accelerator is disabled
3.12 System Configuration Control

The MCP19122/3 is capable of operating in a variety of different configurations. The MODECON register controls the system configuration of the MCP19122/3.

3.12.1 ERROR AMPLIFIER CLAMP

The internal error amplifier is a rail-to-rail amplifier. However, the output of the error amplifier can be clamped to an adjustable level. The MODECON<EACLMP> is the error amplifier clamp control bit. Setting this bit enables the error amplifier clamp. The bit is cleared on a reset making the error amplifier clamp disabled by default.

The error amplifier clamp source is controlled by the MODECON<CLMPSEL> bit. When this bit is set, the voltage present on GPA3 will set the error amplifier clamp voltage.

The clamp voltage can also be determined by a combination of the GPA3 pin voltage and the sampled output current. This is achieved by clearing the MODECON<CLMPSEL> bit.

**Note:** The GPA3 pin can be configured as a weak current source by setting the WPUGPA<WCS1> bit. See Register 17-3.

3.12.2 INTERNAL PEDESTAL VOLTAGE

To improve accuracy at low voltages, a pedestal voltage is implemented throughout the analog control loop. This voltage is typically 500 mV and can be enabled or disabled by the MODECON<VGNDEN> bit. This pedestal voltage is enabled on any reset. The VGNDEN bit must be cleared to disable the pedestal.

When the MCP19122/3 is disabled, the system output voltage may float up. If the pedestal voltage is also disabled under this condition, the output voltage will not float up. It is recommended that the pedestal voltage always be enabled while operating the MCP19122/3. Operating with the pedestal voltage disabled may cause the MCP19122/3 to not meet all of the electrical specifications contained in the specification table. See Section 4.0 “Electrical Characteristics”.

3.12.3 VDD LDO CONTROL

The VDDEN bit controls the state of the internal 5V VDD LDO when the SLEEP command is issued to the microcontroller core. If the VDDEN bit is set and the SLEEP command is issued the 5V VDD LDO will remain operational and capable of supporting a load.

When the SLEEP command is issued and the VDDEN bit is clear, the 5V VDD LDO will be commanded to a low current consumption state. The voltage will drop to approximately 3V and will not be able to supply any external current.

3.12.4 VOLTAGE/CURRENT SOURCE

The system output voltage or load current can be controlled by the MCP19122/3. The MODECON<CNSG> is the control system configuration bit. When the CNSG bit is cleared, the MCP19122/3 functions as a voltage source. The system output voltage is regulated by comparing the sensed voltage to the adjustable reference voltage.

When the CNSG bit is set, the MCP19122/3 is configured to control the system output current. The output current is regulated by adjusting the high-side duty cycle according to the amount of error that exists between the sampled load current and the adjustable reference.

3.12.5 MULTIPLE OUTPUT SYSTEM CONFIGURATION

The MCP19122/3 is capable of being configured as a Master or Slave in a multiple output system. The device configuration is set by the MODECON<MSC2:0> bits.

3.12.5.1 Multiple Output System Master

When configured as a Master, the GPA1 pin is automatically set to output the switching frequency synchronization signal. The frequency of this synchronization signal sets the converters switching frequency. The GPB3 pin is automatically set to output the system clock signal frequency of 8 MHz.

3.12.5.2 Multiple Output System Slave

There are two different multiple output Slave configurations. The first configuration, MSC<2:0> = 010, requires the Slave to receive a switching frequency synchronization signal and system clock signal from a Master device. For this configuration GPA1 and GPB3 are automatically set as an input. The switching frequency synchronization signal from the Master is connected to the GPA1 pin. Phase shift from this synchronization signal can be applied. See Equation 26-2. The 8 MHz system clock from the Master is connected to the GPB3 pin. This multiple output Slave mode results in less switching waveform frequency jitter when compared to the Master’s switching waveforms.

The second multiple output system Slave configuration, MSC<2:0> = 110, requires the Slave to only receive a switching frequency synchronization signal from the Master. GPA1 is automatically set as an input and the switching frequency synchronization signal from the Master is connected to this pin. Phase shift
from the synchronization signal can be applied. See Equation 26-2. No system clock is required in this mode.

### 3.12.6 MULTI-PHASE SYSTEM

The MCP19122/3 is capable of being configured as a Master or Slave in a multi-phase system. The MODECON<MSC2:0> bits determine the device configuration.

#### 3.12.6.1 Multi-phase System Master

When configured as a Master, the GPA1 pin is automatically set to output the switching frequency synchronization signal. The frequency of this synchronization signal sets the converters switching frequency. The GPB3 pin is automatically set to output the system clock signal frequency of 8 MHz. The GPB1 pin is automatically set to output the sampled current sense signal.

#### 3.12.6.2 Multi-phase System Slave

When configured as a Slave, GPA1 is set to be the switching frequency synchronization signal input pin. The Master’s switching frequency synchronization signal is to be connected to this pin. Phase shift from the synchronization signal can be applied. See Register 26-2.

To ensure proper synchronization between the Master and Slave, GPB3 of the Slave is set to be the system clock input pin. Both the Master and Slave GPB3 pins must be connected together.

To properly balance the system output current between the phases, all devices need to regulate to the same current. On the Slave devices, GPB1 is set to be the current sense input signal from the Master. Both the Master and Slave GPB1 pins must be connected together. The MODECON<CNSG> must also be set to a '1' so the Slave device is set to control the system output current.

**Note 1:** The TMR2 register should be initialized to 0 to allow proper synchronization.

**Note 2:** The PWMPHL and PWMPHH register control the amount of phase shift applied.
### REGISTER 3-15: MODECON: SYSTEM CONFIGURATION CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLMPSEL</td>
<td>VGNDEN</td>
<td>VDDEN</td>
<td>CNSG</td>
<td>EACLMP</td>
<td>MSC2</td>
<td>MSC1</td>
<td>MSC0</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

#### Bit Descriptions:
- **bit 7**: CLMPSEL: Error Amplifier Clamp Configuration bit
  - 1 = EA Clamp current set by GPA3 pin voltage
  - 0 = EA Clamp current set by GPA3 pin voltage and average output current
- **bit 6**: VGNDEN: Virtual Ground Control bit
  - 1 = Virtual Ground is enabled
  - 0 = Virtual Ground is disabled
- **bit 5**: VDDEN: VDD LDO control bit
  - 0 = VDD LDO is disabled when SLEEP command issued
  - 1 = VDD LDO remains enabled when SLEEP command issued
- **bit 4**: CNSG: Control Signal configuration bit
  - 0 = Device set to control system output voltage
  - 1 = Device set to control system output current
- **bit 3**: EACLMP: Error Amplifier Clamp control bit
  - 1 = Error amplifier output clamp enabled
  - 0 = Error amplifier output clamp disabled
- **bit 2-0**: MSC<2:0>: System configuration control bit
  - 000 = Device set as a stand alone unit
  - 001 = Device set as multiple output Master (GPB3: clock signal out, GPA1: synchronization signal out)
  - 010 = Device set as multiple output Slave (GPB3: clock signal in, GPA1: synchronization signal in)
  - 011 = Device set as multi-phase Master (GPB3: clock signal out, GPA1: synchronization signal out, GPB1: demand out)
  - 100 = Device set as multi-phase Slave (GPB3: clock signal in, GPA1: synchronization signal in, GPB1: demand in)
  - 101 = Device set as multiple output Master (GPA1: synchronization signal out)
  - 110 = Device set as multiple output Slave (GPA1: synchronization signal in)
  - 111 = Unimplemented
3.13  Miscellaneous Features

3.13.1  OVERTEMPERATURE
The MCP19122/3 features a hardware overtemperature shutdown protection typically set at +160°C. No firmware fault-handling procedure is required to shutdown the MCP19122/3 for an over temperature condition.

3.13.2  DEVICE ADDRESSING
The communication address of the MCP19122/3 is stored in the SSPADD register. This value can be loaded when the device firmware is programmed or configured by external components. By reading a voltage on a GPIO with the ADC, a device specific address can be stored into the SSPADD register.

The MCP19122/3 contains a second address register, SSPADD2. This is a 7-bit address that can be used as the SMBus alert address when PMBus communication is used. See Section 27.0, Master Synchronous Serial Port (MSSP) Module for more information.

3.13.3  DEVICE ENABLE
A GPIO pin can be configured to be a device enable pin. By configuring the pin as an input, the PORT register or the interrupt on change (IOC) can be used to enable the device. Example 3-2 shows how to configure a GPIO as an enable pin by testing the PORT register.

EXAMPLE 3-2: CONFIGURING GPA3 AS DEVICE ENABLE

```
BANKSEL TRISGPA
BSF TRISGPA, 3 ; Set GPA3 as input
BANKSEL ANSELA
BCF ANSELA, 3 ; Set GPA3 as digital input
;
;
WAIT_ENABLE:
BANKSEL PORTGPA
BTFSS PORTGPA, 3 ; Test GPA3 to see if pulled high
; A high on GPA3 indicated device to be enabled
GOTO WAIT_ENABLE ; Stay in loop waiting for device enable
BANKSEL ATSTCON
BSF ATSTCON, 0 ; Enable the device by enabling drivers
;
;
; Insert additional user code here
```

3.13.4  OUTPUT POWER GOOD
The output voltage measured between the +VSEN and −VSEN pins can be monitored by the internal ADC. In firmware, when this ADC reading matches a user-defined power good value, a GPIO can be toggled to indicate the system output voltage is within a specified range. Delays, hysteresis and time out values can all be configured in firmware.

3.13.5  OUTPUT VOLTAGE SOFT-START
During start-up, soft start of the output voltage is accomplished in firmware. By using one of the internal timers and incrementing the OVCCON or OVFCON register on a timer overflow, very long soft start times can be achieved.

3.13.6  OUTPUT VOLTAGE TRACKING
The MCP19122/3 can be configured to track another voltage signal at start-up or shutdown. The ADC is configured to read a GPIO that has the desired tracking voltage applied to it. The firmware then handles the tracking of the internal output voltage reference to this ADC reading.
4.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN} - V_{GND} )</td>
<td>(-0.3) to +43V</td>
</tr>
<tr>
<td>( V_{IN} - V_{GND} ) (non-switching)</td>
<td>(-0.3) to +48V</td>
</tr>
<tr>
<td>( V_{BOOT} - V_{IN} )</td>
<td>(-0.3) to (+V_{D MAX}V)</td>
</tr>
<tr>
<td>( V_{PHASE} ) (continuous)</td>
<td>(GND - 0.3) to (+V_{IN}V)</td>
</tr>
<tr>
<td>( V_{PHASE} ) (transient &lt; 100 ns)</td>
<td>(GND - 5.0) to (+V_{IN}V)</td>
</tr>
<tr>
<td>( V_{DD} ) internally generated</td>
<td>(+5V \pm 8%)</td>
</tr>
<tr>
<td>( V_{HDRV}, HDRV ) Pin</td>
<td>(+V_{PHASE} - 0.3V) to (V_{BOOT} + 0.3V)</td>
</tr>
<tr>
<td>( V_{LDRV}, LDRV ) Pin</td>
<td>((V_{GND} - 0.3V)) to ((V_{DD} + 0.3V))</td>
</tr>
<tr>
<td>Voltage on MCLR with respect to GND</td>
<td>(-0.3) to +13.5V</td>
</tr>
<tr>
<td>(+V_{SEN}, ISP, ISN) pins</td>
<td>((V_{GND} - 0.3V)) to +16V</td>
</tr>
<tr>
<td>Maximum Voltage: any other pin</td>
<td>(+V_{GND} - 0.3V) to (+V_{DD} + 0.3V)</td>
</tr>
<tr>
<td>Maximum output current sunk by any single I/O pin</td>
<td>25 mA</td>
</tr>
<tr>
<td>Maximum output current sourced by any single I/O pin</td>
<td>25 mA</td>
</tr>
<tr>
<td>Maximum current sunk by all GPIO</td>
<td>65 mA</td>
</tr>
<tr>
<td>Maximum current sourced by all GPIO</td>
<td>45 mA</td>
</tr>
<tr>
<td>ESD protection on all pins (HBM)</td>
<td>1.0 kV</td>
</tr>
<tr>
<td>ESD protection on all pins (MM)</td>
<td>200 V</td>
</tr>
</tbody>
</table>

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
### ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Unless otherwise noted, $V_{IN} = 12\, \text{V}$, $F_{SW} = 300\, \text{kHz}$, $T_A = +25^\circ\text{C}$. **Boldface** specifications apply over the $T_A$ range of $-40^\circ\text{C}$ to $+125^\circ\text{C}$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>$V_{IN}$</td>
<td>4.5</td>
<td>—</td>
<td>40</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Quiescent Current</td>
<td>$I_Q$</td>
<td>—</td>
<td>5</td>
<td>10</td>
<td>mA</td>
<td>Not Switching, $V_{SEN} &gt; V_{REF}$, $\text{MODECON}&lt;\text{VGNDEN}&gt; = 0$</td>
</tr>
<tr>
<td>Input Shutdown Current</td>
<td>$I_{SHDN}$</td>
<td>—</td>
<td>50</td>
<td>150</td>
<td>µA</td>
<td>SLEEP Command, $V_{DD}$ disabled</td>
</tr>
<tr>
<td>Internal Regulator $V_{DD}$</td>
<td>$V_{DD}$</td>
<td>4.6</td>
<td>5.0</td>
<td>5.4</td>
<td>V</td>
<td>$V_{IN} = 6, \text{V}$ to $40, \text{V}$</td>
</tr>
<tr>
<td>Maximum external $V_{DD}$ output current</td>
<td>$I_{DD-OUT}$</td>
<td>35</td>
<td>—</td>
<td>—</td>
<td>mA</td>
<td>$V_{IN} = 6, \text{V}$ to $40, \text{V}$</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>$\Delta V_{DD-OUT}/(V_{DD-OUT}\cdot\Delta V_{IN})$</td>
<td>—</td>
<td>0.1</td>
<td>0.45</td>
<td>%/V</td>
<td>$(V_{DD-OUT} \pm 1.0,\text{V}) \leq V_{IN} \geq 40,\text{V}$ Note 2</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>$\Delta V_{DD-OUT}/V_{DD-OUT}$</td>
<td>$-0.5$</td>
<td>±0.1</td>
<td>$+0.5$</td>
<td>%</td>
<td>$I_{DD-OUT} = 1,\text{mA}$ to $20,\text{mA}$ Note 2</td>
</tr>
<tr>
<td>Output Short Circuit Current</td>
<td>$I_{DD-OUT_SC}$</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>mA</td>
<td>$V_{IN} = (V_{DD-OUT} + 1.0,\text{V})$ Note 2</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_{IN} \cdot V_{DD-OUT}$</td>
<td>—</td>
<td>0.5</td>
<td>1</td>
<td>V</td>
<td>$I_{DD-OUT} = 35,\text{mA}$, $V_{IN} = V_{DD-OUT} \pm 1.0,\text{V}$ Note 2</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>$PSRR_{LDO}$</td>
<td>—</td>
<td>60</td>
<td>—</td>
<td>dB</td>
<td>$f \leq 1000,\text{Hz}$, $I_{DD-OUT} = 36,\text{mA}$, $C_{IN} = 0,\mu\text{F}$, $C_{DD-OUT} = 1,\mu\text{F}$</td>
</tr>
<tr>
<td>Band Gap</td>
<td>$BG$</td>
<td>1.205</td>
<td>1.230</td>
<td>1.254</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Internal Regulator $AV_{DD}$</td>
<td>$AV_{DD}$</td>
<td>3.97</td>
<td>4.096</td>
<td>4.23</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Overcurrent</td>
<td>$OC_{MIN}$</td>
<td>90</td>
<td>—</td>
<td>755</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Overcurrent Step Size</td>
<td>$OC_{STEP_SIZE}$</td>
<td>15</td>
<td>21</td>
<td>25</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Adjustable Leading Edge Blanking Time</td>
<td>$LEB$</td>
<td>90</td>
<td>110</td>
<td>135</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>150</td>
<td>200</td>
<td>250</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>250</td>
<td>380</td>
<td>480</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>500</td>
<td>740</td>
<td>950</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Current Sense Fixed Gain</td>
<td>$I_{SENSE_GAIN}$</td>
<td>30</td>
<td>32</td>
<td>34</td>
<td>V/V</td>
<td></td>
</tr>
<tr>
<td>Current Sense Amplifier Offset</td>
<td>$I_{SENSE_OFFSET}$</td>
<td>$-10$</td>
<td>0</td>
<td>10</td>
<td>mV</td>
<td>Fixed gain removed</td>
</tr>
</tbody>
</table>

**Note:**
1. These parameters are characterized but not production tested.
2. $V_{DD-OUT}$ is the voltage present at the $V_{DD}$ pin. $V_{DD}$ is the internally generated bias voltage.
3. This is the voltage measured between the PHASE pin and GND. When measured voltage is between 2.5 mV and +2.5 mV, the LOWDR signal is to be pulled low.
4. This is the total source current for all GPIO pins combined. Individually each pin can source a maximum of 15 mA.
5. System output voltage tolerance specified when $1.024\,\text{V} \leq V_{REF} \leq 2.046\,\text{V}$.
### ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Unless otherwise noted, $V_{IN} = 12\,\text{V}$, $F_{SW} = 300\,\text{kHz}$, $T_A = +25\,\text{C}$. **Boldface** specifications apply over the $T_A$ range of $-40\,\text{C}$ to $+125\,\text{C}$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pedestal Voltage</td>
<td>$V_{PEDESTAL}$</td>
<td>—</td>
<td>500</td>
<td>—</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Voltage Reference</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Adjustable $V_{OUT}$ Range</td>
<td>$V_{OUT_RANGE}$</td>
<td>0.5</td>
<td>—</td>
<td>16</td>
<td>V</td>
<td>$V_{OUT}$ range with no external voltage divider</td>
</tr>
<tr>
<td>Reference Voltage Step Size</td>
<td>$V_{REF_STEP}$</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>mV</td>
<td>Differential amplifier gain setting of 1/8, 1/4, 1/2, 1 and 2 Note 5</td>
</tr>
<tr>
<td>System Output Voltage Tolerance</td>
<td>$V_{TOL}$</td>
<td>—3%</td>
<td>—</td>
<td>+3%</td>
<td></td>
<td>Differential amplifier gain setting of 4 Note 5</td>
</tr>
<tr>
<td>System Output Voltage Tolerance</td>
<td>$V_{TOL}$</td>
<td>—5%</td>
<td>—</td>
<td>+5%</td>
<td></td>
<td>Differential amplifier gain setting of 8 Note 5</td>
</tr>
<tr>
<td>System Output Voltage Tolerance</td>
<td>$V_{TOL}$</td>
<td>—6.5%</td>
<td>—</td>
<td>+6.5%</td>
<td></td>
<td>Differential amplifier gain setting of 8 Note 5</td>
</tr>
<tr>
<td>Output Over Voltage Reference</td>
<td>$O_{VSTEP}$</td>
<td>27</td>
<td>31</td>
<td>35</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Output Under Voltage DAC</td>
<td>$U_{VSTEP}$</td>
<td>27</td>
<td>31</td>
<td>35</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Remote Sense Differential Amplifier</td>
<td>$R_{IN}$</td>
<td>—</td>
<td>12</td>
<td>—</td>
<td>kOhm</td>
<td></td>
</tr>
<tr>
<td>Common Mode Voltage Range</td>
<td>$V_{CMR}$</td>
<td>—0.5</td>
<td>—</td>
<td>+0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Differential Feedback Voltage Range</td>
<td>$V_{DIFF}$</td>
<td>0</td>
<td>16</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Oscillator/PWM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal Oscillator Frequency</td>
<td>$F_{OSC}$</td>
<td>7.60</td>
<td>8.00</td>
<td>8.40</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>$F_{SW}$</td>
<td>—</td>
<td>$F_{OSC}/N$</td>
<td>—</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Switching Frequency Range Select</td>
<td>N</td>
<td>4</td>
<td>80</td>
<td>—</td>
<td>$F_{SW} = 100,\text{kHz}$ to $2,\text{MHz}$</td>
<td></td>
</tr>
<tr>
<td>Maximum Duty Cycle</td>
<td>—</td>
<td>—</td>
<td>$(N-1)/N$</td>
<td>—</td>
<td>%/100</td>
<td></td>
</tr>
<tr>
<td>Dead Time Adjustment</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LDRV Dead Time Adjustable Range</td>
<td>$D_{T_RANGE_L}$</td>
<td>-4</td>
<td>—</td>
<td>56</td>
<td>ns</td>
<td>Labeled LDLY in Figure 3-3</td>
</tr>
<tr>
<td>HDRV Dead Time Adjustable Range</td>
<td>$D_{T_RANGE_H}$</td>
<td>14</td>
<td>—</td>
<td>74</td>
<td>ns</td>
<td>Labeled HDLY in Figure 3-3</td>
</tr>
<tr>
<td>Dead Time Step Size</td>
<td>$D_{STEP}$</td>
<td>—</td>
<td>4</td>
<td>—</td>
<td>ns</td>
<td>For both HDLY and LDLY</td>
</tr>
<tr>
<td>HDRV Output Driver</td>
<td>$R_{HDRV_SCR}$</td>
<td>—</td>
<td>1.4</td>
<td>2.7</td>
<td>$\Omega$</td>
<td>Measured at $100,\text{mA}$</td>
</tr>
</tbody>
</table>

**Note 1:** These parameters are characterized but not production tested.

2: $V_{DD-OUT}$ is the voltage present at the $V_{DD}$ pin. $V_{DD}$ is the internally generated bias voltage.

3: This is the voltage measured between the PHASE pin and GND. When measured voltage is between 2.5 mV and +2.5 mV, the LOWDR signal is to be pulled low.

4: This is the total source current for all GPIO pins combined. Individually each pin can source a maximum of 15 mA.

5: System output voltage tolerance specified when $1.024V \leq V_{REF} \leq 2.046V$. 
ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $V_{IN} = 12\,\text{V}$, $F_{SW} = 300\,\text{kHz}$, $T_A = +25^\circ\text{C}$. Boldface specifications apply over the $T_A$ range of $-40^\circ\text{C}$ to $+125^\circ\text{C}$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>HDRV Sink Resistance</td>
<td>$R_{HDRV-SINK}$</td>
<td>—</td>
<td>1.2</td>
<td>2.5</td>
<td>$\Omega$</td>
<td>Measured at 100mA</td>
</tr>
<tr>
<td>HDRV Source Current</td>
<td>$I_{HDRV-SCR}$</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>$A$</td>
<td>Note 1</td>
</tr>
<tr>
<td>HDRV Sink Current</td>
<td>$I_{HDRV-SINK}$</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>$A$</td>
<td>Note 1</td>
</tr>
<tr>
<td>HDRV Minimum On Time</td>
<td>$t_{MIN}$</td>
<td>75</td>
<td>95</td>
<td>—</td>
<td>ns</td>
<td>Note 1</td>
</tr>
<tr>
<td>LDRV Source Resistance</td>
<td>$R_{LDRV-SCR}$</td>
<td>—</td>
<td>1.8</td>
<td>3.2</td>
<td>$\Omega$</td>
<td>Measured at 100mA</td>
</tr>
<tr>
<td>LDRV Sink Resistance</td>
<td>$R_{LDRV-SINK}$</td>
<td>—</td>
<td>0.6</td>
<td>2</td>
<td>$\Omega$</td>
<td>Measured at 100mA</td>
</tr>
<tr>
<td>LDRV Source Current</td>
<td>$I_{LDRV-SCR}$</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>$A$</td>
<td>Note 1</td>
</tr>
<tr>
<td>LDRV Sink Current</td>
<td>$I_{LDRV-SINK}$</td>
<td>—</td>
<td>4</td>
<td>—</td>
<td>$A$</td>
<td>Note 1</td>
</tr>
<tr>
<td>LDRV Minimum On Time</td>
<td>$t_{MIN}$</td>
<td>—</td>
<td>167</td>
<td>—</td>
<td>ns</td>
<td>Note 1</td>
</tr>
<tr>
<td>Bootstrap Blocking Device</td>
<td>$R_{BL}$$\text{ock}$</td>
<td>20</td>
<td>40</td>
<td>—</td>
<td>$\Omega$</td>
<td>Note 1</td>
</tr>
<tr>
<td>GPIO Pins</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPIO Weak Current Source</td>
<td>—</td>
<td>—</td>
<td>45</td>
<td>55</td>
<td>$\mu\text{A}$</td>
<td>Selected current source on GPA2, GPA3.</td>
</tr>
<tr>
<td>Maximum GPIO Sink Current</td>
<td>$I_{SINK_GPIO}$</td>
<td>—</td>
<td>—</td>
<td>35</td>
<td>mA</td>
<td>Note 1, Note 4</td>
</tr>
<tr>
<td>Maximum GPIO Source Current</td>
<td>$I_{SOURCE_GPIO}$</td>
<td>—</td>
<td>—</td>
<td>35</td>
<td>mA</td>
<td>Note 1, Note 4</td>
</tr>
<tr>
<td>GPIO Weak Pull-up Current</td>
<td>$I_{PULL-UP_GPIO}$</td>
<td>50</td>
<td>250</td>
<td>400</td>
<td>$\mu\text{A}$</td>
<td>$V_{DD} = 5,\text{V}$</td>
</tr>
<tr>
<td>GPIO Input Leakage Current</td>
<td>$I_{PULL-UP_GPIO}$</td>
<td>—</td>
<td>±0.1</td>
<td>±1</td>
<td>$\mu\text{A}$</td>
<td>Negative current is defined as current sourced by the pin. $T_A = +90^\circ\text{C}$</td>
</tr>
<tr>
<td>GPIO Input Low Voltage</td>
<td>$V_{IL}$</td>
<td>GND</td>
<td>—</td>
<td>0.8</td>
<td>$V$</td>
<td>I/O Port with TTL buffer $V_{DD} = 5,\text{V}, T_A = +90^\circ\text{C}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GND</td>
<td>—</td>
<td>0.2$V_{DD}$</td>
<td>I/O Port with Schmitt Trigger buffer, $V_{DD} = 5,\text{V}, T_A = +90^\circ\text{C}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>GND</td>
<td>—</td>
<td>0.2$V_{DD}$</td>
<td>MCLR, $T_A = +90^\circ\text{C}$</td>
<td></td>
</tr>
<tr>
<td>GPIO Input High Voltage</td>
<td>$V_{IH}$</td>
<td>2.0</td>
<td>$V_{DD}$</td>
<td>—</td>
<td>$V$</td>
<td>I/O Port with TTL buffer $V_{DD} = 5,\text{V}, T_A = +90^\circ\text{C}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.8$V_{DD}$</td>
<td>—</td>
<td>$V_{DD}$</td>
<td>$V$</td>
<td>I/O Port with Schmitt Trigger buffer, $V_{DD} = 5,\text{V}, T_A = +90^\circ\text{C}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.8$V_{DD}$</td>
<td>—</td>
<td>$V_{DD}$</td>
<td>$V$</td>
<td>MCLR, $T_A = +90^\circ\text{C}$</td>
</tr>
<tr>
<td>Thermal Shutdown</td>
<td>$T_{SHD}$</td>
<td>—</td>
<td>160</td>
<td>—</td>
<td>$^\circ\text{C}$</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: These parameters are characterized but not production tested.
2: $V_{DD-OUT}$ is the voltage present at the $V_{DD}$ pin. $V_{DD}$ is the internally generated bias voltage.
3: This is the voltage measured between the PHASE pin and GND. When measured voltage is between 2.5 mV and +2.5 mV, the LOWDR signal is to be pulled low.
4: This is the total source current for all GPIO pins combined. Individually each pin can source a maximum of 15 mA.
5: System output voltage tolerance specified when $1.024\,\text{V} \leq V_{REF} \leq 2.046\,\text{V}$.
ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, \( V_{IN} = 12\, \text{V} \), \( F_{SW} = 300\, \text{kHz} \), \( T_A = +25^\circ \text{C} \). Boldface specifications apply over the \( T_A \) range of \(-40^\circ \text{C} \) to \(+125^\circ \text{C} \).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Shutdown Hysteresis</td>
<td>( T_{SHD_HYS} )</td>
<td>—</td>
<td>20</td>
<td>—</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** These parameters are characterized but not production tested.

**Note 2:** \( V_{DD-OUT} \) is the voltage present at the \( V_{DD} \) pin. \( V_{DD} \) is the internally generated bias voltage.

**Note 3:** This is the voltage measured between the PHASE pin and GND. When measured voltage is between 2.5 mV and +2.5 mV, the LOWDR signal is to be pulled low.

**Note 4:** This is the total source current for all GPIO pins combined. Individually each pin can source a maximum of 15 mA.

**Note 5:** System output voltage tolerance specified when \( 1.024\, \text{V} \leq V_{REF} \leq 2.046\, \text{V} \).

THERMAL SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
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<tbody>
<tr>
<td>Temperature Ranges</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Specified Temperature Range</td>
<td>( T_A )</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>( T_A )</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>( T_J )</td>
<td>—</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>( T_A )</td>
<td>-65</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
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</table>

**Thermal Package Resistances**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, 24L-QFN 4x4</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>42</td>
<td>—</td>
<td>°C/W</td>
<td>Note 1</td>
</tr>
<tr>
<td>Thermal Resistance, 28L-QFN 5x5</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>35.3</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** The parameter is determined using a High K 2S2P 4-layer board as described in JESD51-7, as well as JESD 51-5 for packages with exposed pads.
5.0 DIGITAL ELECTRICAL CHARACTERISTICS

5.1 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS
3. Tcc:st
4. Ts

<table>
<thead>
<tr>
<th>T</th>
<th>Frequency</th>
<th>T</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>Frequency</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Lowercase letters (pp) and their meanings:

<table>
<thead>
<tr>
<th>pp</th>
<th>cc</th>
<th>CCP1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ck</td>
<td>CLKOUT</td>
</tr>
<tr>
<td></td>
<td>cs</td>
<td>CS</td>
</tr>
<tr>
<td></td>
<td>di</td>
<td>SDI</td>
</tr>
<tr>
<td></td>
<td>do</td>
<td>SDO</td>
</tr>
<tr>
<td></td>
<td>dt</td>
<td>Data in</td>
</tr>
<tr>
<td></td>
<td>io</td>
<td>I/O port</td>
</tr>
<tr>
<td></td>
<td>mc</td>
<td>MCLR</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>pp</th>
<th>osc</th>
<th>OSC1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>rd</td>
<td>RD</td>
</tr>
<tr>
<td></td>
<td>rw</td>
<td>RD or WR</td>
</tr>
<tr>
<td></td>
<td>sc</td>
<td>SCK</td>
</tr>
<tr>
<td></td>
<td>ss</td>
<td>SS</td>
</tr>
<tr>
<td></td>
<td>t0</td>
<td>T0CKI</td>
</tr>
<tr>
<td></td>
<td>t1</td>
<td>T1CKI</td>
</tr>
<tr>
<td></td>
<td>wr</td>
<td>WR</td>
</tr>
</tbody>
</table>

Uppercase letters and their meanings:

<table>
<thead>
<tr>
<th>S</th>
<th>F</th>
<th>Fall</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>H</td>
<td>High</td>
</tr>
<tr>
<td></td>
<td>I</td>
<td>Invalid (high-impedance)</td>
</tr>
<tr>
<td></td>
<td>L</td>
<td>Low</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>i2c only</th>
<th>AA</th>
<th>output access</th>
<th>High</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>BUF</td>
<td>Bus free</td>
<td>Low</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tcc:st</th>
<th>(i2c specifications only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HD</td>
<td>Hold</td>
</tr>
<tr>
<td>ST</td>
<td>DATA input hold</td>
</tr>
<tr>
<td></td>
<td>START condition</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SU</th>
<th>Setup</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAT</td>
<td>DATA input hold</td>
</tr>
<tr>
<td>STA</td>
<td>START condition</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>STA</th>
<th>STOP condition</th>
</tr>
</thead>
</table>

FIGURE 5-1: LOAD CONDITIONS

Load Condition 1

- Pin
- $R_L = 464\Omega$
- $C_L = 50\,\text{pF}$ for all GPIO pins

Load Condition 2

- Pin
- $V_{SS}$
5.2 AC Characteristics: MCP19122/3

FIGURE 5-2: EXTERNAL CLOCK TIMING

![External Clock Timing Diagram]

TABLE 5-1: EXTERNAL CLOCK TIMING REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ. †</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>F_{OSC}</td>
<td>Oscillator Frequency(^{(1)})</td>
<td>— 8</td>
<td>— 8</td>
<td>— 8</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>T_{OSC}</td>
<td>Oscillator Period(^{(1)})</td>
<td>— 250</td>
<td>— 250</td>
<td>— 250</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>T_{CY}</td>
<td>Instruction Cycle Time(^{(4)})</td>
<td>— 1000</td>
<td>— 1000</td>
<td>— 1000</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at V_{IN} = 1.2 V (V_{DD} = 5 V), +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1**: Instruction cycle period (T_{CY}) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code.

FIGURE 5-3: I/O TIMING

![I/O Timing Diagram]
TABLE 5-2: I/O TIMING REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ. †</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>17</td>
<td>TosH2ioV</td>
<td>OSC1↑ (Q1 cycle) to Port out valid</td>
<td>—</td>
<td>50</td>
<td>70*</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>TosH2iol</td>
<td>OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)</td>
<td>50</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>TioV2osH</td>
<td>Port input valid to OSC1↑ (I/O in setup time)</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>TioR</td>
<td>Port output rise time</td>
<td>—</td>
<td>32</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>TioF</td>
<td>Port output fall time</td>
<td>—</td>
<td>15</td>
<td>30</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>22*</td>
<td>Tinp</td>
<td>INT pin high or low time</td>
<td>25</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>23*</td>
<td>Trbp</td>
<td>GPIO Interrupt-on-change new input level time</td>
<td>T_DY</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at V_IN = 1.2 V (V_DD = 5 V), +25°C unless otherwise stated.

FIGURE 5-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING
FIGURE 5-5: BROWN-OUT RESERT TIMING AND CHARACTERISTICS

TABLE 5-3: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, AND POWER-UP TIMER REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ.†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>T_{MCL}</td>
<td>MCLR Pulse Width (low)</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td>V_{DD} = 5V, –40°C to +85°C</td>
</tr>
<tr>
<td>31</td>
<td>T_{WDT}</td>
<td>Watchdog Timer Time-out Period (No Prescaler)</td>
<td>7</td>
<td>18</td>
<td>33</td>
<td>ms</td>
<td>V_{DD} = 5V, –40°C to +85°C</td>
</tr>
<tr>
<td>32</td>
<td>T_{OST}</td>
<td>Oscillation Start-up Timer Period</td>
<td>—</td>
<td>1024T_{OSC}</td>
<td>—</td>
<td>—</td>
<td>T_{OSC} = OSC1 period</td>
</tr>
<tr>
<td>33*</td>
<td>T_{PWRT}</td>
<td>Power-up Timer Period (4 x T_{WDT})</td>
<td>28</td>
<td>72</td>
<td>132</td>
<td>ms</td>
<td>V_{DD} = 5V, –40°C to +85°C</td>
</tr>
<tr>
<td>34</td>
<td>T_{IOZ}</td>
<td>I/O high-impedance from MCLR Low or Watchdog Timer Reset</td>
<td>—</td>
<td>—</td>
<td>2.0</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>*</td>
<td>V_{POR}</td>
<td>Power-on Reset Voltage</td>
<td>—</td>
<td>2.13</td>
<td>—</td>
<td>V</td>
<td>V_{DD} Rising</td>
</tr>
<tr>
<td>*</td>
<td>V_{POR,HYS}</td>
<td>Power-on Reset Voltage Hysteresis</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>*</td>
<td>V_{BOR}</td>
<td>Brown-out Reset voltage</td>
<td>—</td>
<td>2.7</td>
<td>—</td>
<td>V</td>
<td>V_{DD} Falling</td>
</tr>
<tr>
<td>*</td>
<td>B_{VHY}</td>
<td>Brown-out Hysteresis</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>T_{BCR}</td>
<td>Brown-out Reset pulse width</td>
<td>100*</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td>V_{DD} ≤ V_{BOR} (D005)</td>
</tr>
<tr>
<td>48</td>
<td>T_{CKEZ-TMR}</td>
<td>Delay from clock edge to timer increment</td>
<td>2T_{OSC}</td>
<td>—</td>
<td>7T_{OSC}</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ.” column is at V_{IN} = 12V (V_{DD} = 5V), +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
TABLE 5-4: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ.†</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>40*</td>
<td>T0H</td>
<td>T0CKI High Pulse Width</td>
<td>No Prescaler</td>
<td>0.5TCY + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>41*</td>
<td>T0L</td>
<td>T0CKI Low Pulse Width</td>
<td>No Prescaler</td>
<td>0.5TCY + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>42*</td>
<td>T0P</td>
<td>T0CKI Period</td>
<td>Greater of:</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>N = prescale value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 or TCY + 40</td>
<td></td>
<td></td>
<td></td>
<td>(2, 4, ..., 256)</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in "Typ" column is at VIN = 12V (VD = 5V), +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note:
Refer to Figure 5-1 for load conditions.
## TABLE 5-5: MCP19122/3 A/D CONVERTER (ADC) CHARACTERISTICS:

### Standard Operating Conditions (unless otherwise stated)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ. †</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD01</td>
<td>N_R</td>
<td>Resolution</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>bit</td>
<td></td>
</tr>
<tr>
<td>AD02</td>
<td>E_IL</td>
<td>Integral Error</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td>Lsb</td>
<td>VREF_ADC=AVDD VREF_ADC=VDD</td>
</tr>
<tr>
<td>AD03</td>
<td>E_DL</td>
<td>Differential Error</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td>Lsb</td>
<td>No missing codes to 10 bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VREF_ADC=AVDD VREF_ADC=VDD</td>
</tr>
<tr>
<td>AD04</td>
<td>E_OFF</td>
<td>Offset Error</td>
<td>—</td>
<td>+3.0</td>
<td>+7.0</td>
<td>Lsb</td>
<td>VREF_ADC=AVDD VREF_ADC=VDD</td>
</tr>
<tr>
<td>AD07</td>
<td>E_GN</td>
<td>Gain Error</td>
<td>—</td>
<td>±2</td>
<td>±6</td>
<td>Lsb</td>
<td>VREF_ADC=AVDD VREF_ADC=VDD</td>
</tr>
<tr>
<td>AD07*</td>
<td>V_AIN</td>
<td>Full-Scale Range</td>
<td>GND</td>
<td>AVDD</td>
<td>—</td>
<td></td>
<td>AVDD Selected as ADC Reference</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>GND</td>
<td>VDD</td>
<td>—</td>
<td></td>
<td>VDD Selected as ADC Reference</td>
</tr>
<tr>
<td>AD08</td>
<td>Z_AIN</td>
<td>Recommended Impedance of Analog Voltage Source</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>kΩ</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in 'Typ' column is at VIN = 1.2 V (AVDD = 4.096V), +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Total Absolute Error includes integral, differential, offset and gain errors.

**Note 2:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

**Note 3:** When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module. To minimize Sleep current the ADC Reference must be set to the (default) AVDD.
### TABLE 5-6: MCP19122/3 A/D CONVERSION REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Min.</th>
<th>Typ. †</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD130*</td>
<td>T(_{AD})</td>
<td>A/D Clock Period</td>
<td>1.6</td>
<td>—</td>
<td>9.0</td>
<td>µs</td>
<td>T(_{OSC})-based</td>
</tr>
<tr>
<td>AD131</td>
<td>T(_{CNV})</td>
<td>A/D Internal RC Oscillator Period</td>
<td>1.6</td>
<td>4.0</td>
<td>6.0</td>
<td>µs</td>
<td>ADCS&lt;1:0&gt; = 11 (ADRC mode)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Conversion Time (not including Acquisition Time)(^{(1)})</td>
<td>—</td>
<td>11</td>
<td>—</td>
<td>T(_{AD})</td>
<td>Set GO/DONE bit to new data in A/D Result register</td>
</tr>
<tr>
<td>AD132*</td>
<td>T(_{ACQ})</td>
<td>Acquisition Time</td>
<td>—</td>
<td>11.5</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>AD133*</td>
<td>T(_{AMP})</td>
<td>Amplifier Settling Time</td>
<td>—</td>
<td>—</td>
<td>5</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>AD134</td>
<td>T(_{GO})</td>
<td>Q4 to A/D Clock Start</td>
<td>—</td>
<td>T(_{OSC}/2)</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in ‘Typ’ column is at \(V_{IN} = 12V (V_{DD} = 5V)\), +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** ADRESH and ADRESL registers may be read on the following TCY cycle.

### FIGURE 5-8: A/D CONVERSION TIMING

Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.
6.0 TYPICAL PERFORMANCE CURVES.

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.
FIGURE 6-7: HDRV RDS-ON VS. TEMPERATURE

FIGURE 6-8: LDRV RDS-ON VS. TEMPERATURE

FIGURE 6-9: OSCILLATOR FREQUENCY VS. TEMPERATURE

FIGURE 6-10: CURRENT SENSE GAIN VS. TEMPERATURE

FIGURE 6-11: GPA2/3 SOURCE CURRENT VS. TEMPERATURE
7.0 TEST MUX CONTROL

To allow for easier system design and bench testing, the MCP19122/3 feature a multiplexer used to output various internal analog and digital signals. These signals can be measured on the GPA0 pin through a unity gain buffer. The configuration control of the GPA0 pin is found in the BUFFCON register.

When the BUFFCON<BNCHEN> bit is set, the analog multiplexer output is connected to the GPA0 pin and the CHS<4:0> bits of the ADCON0 register determine which internal analog signal can be measured on the GPA0 pin. Refer to the ADCON0 register (Register 19-1) for analog signals that can be view on GPA0 while BNCHEN is set.

When the BUFFCON<DIGOEN> bit is set, the digital multiplexer output is connected to the GPA0 pin. The DSEL<4:0> bits of the BUFFCON register determine which internal digital signal can be measured on the GPA0 pin.

If a conflict exist where both the BNCHEN and DIGOEN bits are set, the DIGOEN bit takes priority.

When measuring signals with the unity gain buffer, the buffer offset must be added to the measured signal. The factory measured buffer offset can be read from memory location 2087h. Refer to Section 10.1.1 “Reading Program Memory as Data” for more information.

REGISTER 7-1: BUFFCON: TEST MUX CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BNCHEN</td>
<td>DIGOEN</td>
<td>—</td>
<td>DSEL4</td>
<td>DSEL3</td>
<td>DSEL2</td>
<td>DSEL1</td>
<td>DSEL0</td>
</tr>
</tbody>
</table>

Legend:

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 7  BNCHEN: GPA0 analog multiplexer configuration control bit
       1 = GPA0 is configured to be analog multiplexer output
       0 = GPA0 is configured for normal operation

bit 6  DIGOEN: GPA0 digital multiplexer configuration control bit
       1 = GPA0 is configured to be digital multiplexer output
       0 = GPA0 is configured for normal operation

bit 5  Unimplemented: Read as ‘0’

bit 4-0  DSEL<4:0>: Multiplexer output control bit
       00000 = 50% period signal
       00001 = System clock
       00010 = Inductor current SAMPLE signal
       00011 = OV Comparator Output
       00100 = UV Comparator Output
       00101 = OVLO Comparator Output
       00110 = UVLO Comparator Output
       00111 = OC Comparator Output
       01000 = high_on signal
       01001 = Low-side on signal before the delay block
       01010 = T2_EQ_PR2 Signal
       01011 = PWM_OUT Signal
       01100 = Clock Select / Switchover Waveform
       01101 = DEM Comparator Output
       01111 = DEM Blanking Time
       10000 = Output of PWM Comparator
       10001 = SWFRQ Signal
       10010 = T2_EQ_PR2 Signal
       10011 = PWM_OUT Signal
       10100 = Clock Select / Switchover Waveform
       10101 = DEM Comparator Output
       10111 = DEM Blanking Time
       10111 = Auto Zero Time Or’ed Signal
8.0 RELATIVE EFFICIENCY MEASUREMENT

With a constant input voltage, output voltage and load current, any change in the high-side MOSFET on-time represents a change in the system efficiency. The MCP19122/3 is capable of measuring the on-time of the high-side MOSFET. Therefore, the relative efficiency of the system can be measured and optimized by changing the system parameters’ driver dead time, such as switching frequency.

8.1 Relative Efficiency Measurement Procedure

To measure the relative efficiency, the RELEFF register, PE1<MEASEN> bit, and the ADC RELEFF input are used. The following steps outlines the measurement process:

1. Clear the PE1<MEASEN> bit.
2. Set the PE1<SPAN> bit.
3. With the ADC, read the RELEFF channel and store this reading as the High.
4. Clear the PE1<SPAN> bit.
5. With the ADC, read the RELEFF channel and store this reading as the Low.
6. Set the PE1<MEASEN> bit to initiate a measurement cycle.
7. Monitor the RELEFF<MSDONE> bit. When set, it indicates the measurement is complete.
8. When the measurement is complete, use the ADC to read the RELEFF channel. This value becomes the Fractional variable in Equation 10 1. This reading should be accomplished within 50ms of the RELEFF<MSDONE> bit is set.
9. Read the value of the RE<6:0> bits in the RELEFF register and store the reading as Whole.
10. Clear the PE1<MEASEN> bit.
11. The relative efficiency is then calculated by the following equation:

\[
\text{EQUATION 8-1:} \quad \text{Duty Cycle} = \frac{\text{Whole} + \left(\frac{\text{Fractional} - \text{Low}}{\text{High} - \text{Low}}\right)}{(PR2 + 1)}
\]

Where:

- **Whole** = Value obtained in Step 9 of the measurement procedure
- **Fractional** = Value obtained in Step 8 of the measurement procedure
- **High** = Value obtained in Step 3 of the measurement procedure
- **Low** = Value obtained in Step 5 of the measurement procedure

**Note 1:** The RELEFF<MSDONE> bit is set and cleared automatically.

REGISTER 8-1: RELEFF: RELATIVE EFFICIENCY MEASUREMENT REGISTER

<table>
<thead>
<tr>
<th>R-0</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSDONE</td>
<td>RE6</td>
<td>RE5</td>
<td>RE4</td>
<td>RE3</td>
<td>RE2</td>
<td>RE1</td>
<td>RE0</td>
</tr>
</tbody>
</table>

**Legend:**

<table>
<thead>
<tr>
<th>R = Readable bit</th>
<th>W = Writable bit</th>
<th>U = Unimplemented bit, read as ‘0’</th>
</tr>
</thead>
<tbody>
<tr>
<td>-n = Value at POR</td>
<td>‘1’ = Bit is set</td>
<td>‘0’ = Bit is cleared</td>
</tr>
</tbody>
</table>

**bit 7**  
**MSDONE:** Relative efficiency measurement done bit  
1 = Relative efficiency measurement is complete  
0 = Relative efficiency measurement is not complete

**bit 6-0**  
**RE<6:0>**: Whole clock counts for relative efficiency measurement result
9.0 DEVICE CALIBRATION

Read-only memory locations 2080h through 208Fh contain factory calibration data. Refer to Section 20.0 “Flash Program Memory Control” for information on how to read from these memory locations.

9.1 Calibration Word 1

The TTA<3:0> bits at memory location 2080h calibrate the over temperature shutdown threshold point. Firmware must read these values and write them to the TTACAL register for proper calibration.

The FCAL<6:0> bits at memory location 2080h set the internal oscillator calibration. Firmware must read these values and write them to the OSCCAL register for proper calibration.

REGISTER 9-1: CALWD1: CALIBRATION WORD 1 REGISTER

<table>
<thead>
<tr>
<th></th>
<th>U-0</th>
<th>U-0</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 13</td>
<td>—</td>
<td>—</td>
<td>TTA3</td>
<td>TTA2</td>
<td>TTA1</td>
<td>TTA0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  P = Programmable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

bit 13-12 Unimplemented: Read as ‘0’
bit 11-8 TTA<3:0>: Overtemperature shutdown calibration bits.
bit 7 Unimplemented: Read as ‘0’
bit 6-0 FCAL<6:0>: Internal oscillator calibration bits
9.2 Calibration Word 2

The BGT<3:0> bits at memory location 2081h calibrate the internal band gap over temperature. Firmware must read these values and write them to the BGTCAL register for proper calibration.

The BGR<5:0> bits at memory location 2081h calibrate the internal band gap. Firmware must read these values and write them to the BGRCAL register for proper calibration.

REGISTER 9-2: CALWD2: CALIBRATION WORD 2 REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>BGT3</td>
<td>BGT2</td>
<td>BGT1</td>
<td>BGT0</td>
</tr>
</tbody>
</table>

bit 13 - bit 8

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>BGR5</td>
<td>BGR4</td>
<td>BGR3</td>
<td>BGR2</td>
<td>BGR1</td>
<td>BGR0</td>
</tr>
</tbody>
</table>

bit 7 - bit 0

Legend:
R = Readable bit
P = Programmable bit
U = Unimplemented bit, read as '0'
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown

bit 13-12 Unimplemented: Read as ‘0’
bit 11-8 BGT<3:0>: Internal band gap temperature calibration bits.
bit 7-6 Unimplemented: Read as ‘0’
bit 5-0 BGR<5:0>: Internal band gap calibration bits.
9.3 Calibration Word 3

The AVDD<3:0> bits at memory location 2082h calibrate the internal 4.096V bias voltage. Firmware must read these values and write them to the AVDDCAL register for proper calibration.

The VOUR<4:0> bits at memory location 2082h calibrate the output overvoltage and undervoltage reference. Firmware must read these values and write them to the VOURCAL register for proper calibration.

REGISTER 9-3: CALWD3: CALIBRATION WORD 3 REGISTER

Legend:
- R = Readable bit
- P = Programmable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 13-12 Unimplemented: Read as '0'
bit 11-8 AVDD<3:0>: Internal 4V bias voltage calibration bits.
bit 7-5 Unimplemented: Read as ‘0’
bit 4-0 VOUR<4:0>: Output overvoltage and undervoltage reference calibration bits.
9.4 Calibration Word 4

The DOV<5:0> bits at memory location 2083h set the offset calibration for the output voltage remote sense differential amplifier. Firmware must read these values and write them to the DOVCAL register for proper calibration.

The VEAO<4:0> bits at memory location 2083h calibrate the offset of the error amplifier. Firmware must read these values and write them to the VEAOCAL register for proper calibration.

REGISTER 9-4: CALWD4: CALIBRATION WORD 4 REGISTER

<table>
<thead>
<tr>
<th>bit 13</th>
<th>bit 8</th>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>R/P-1</td>
<td>R/P-1</td>
<td>R/P-1</td>
</tr>
<tr>
<td>—</td>
<td>DOV4</td>
<td>DOV3</td>
<td>DOV2</td>
</tr>
<tr>
<td></td>
<td>DOV1</td>
<td>DOV0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 13</th>
<th>bit 8</th>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/P-1</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>VEA04</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VEA03</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VEA02</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VEA01</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VEA00</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- P = Programmable bit
- U = Unimplemented bit, read as '0'
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown

- bit 13: Unimplemented: Read as '0'
- bit 12-8: DOV<4:0>: Output voltage remote sense differential amplifier offset calibration bits
- bit 7-5: Unimplemented: Read as '0'
- bit 4-0: VEAO<4:0>: Error amplifier offset voltage calibration bits
### 9.5 Calibration Word 5

The VREF<4:0> bits at memory location 2084h calibrate the reference to the DAC that sets the output voltage reference. Firmware must read these values and write them to the VREFCAL register for proper calibration.

The VRFS<4:0> bits at memory location 2084h calibrate the full scale range of reference to the DAC that sets the output voltage reference. Firmware must read these values and write them to the VRFSCAL register for proper calibration. The VRFS<4:0> bits are to be loaded in to the VRFSCAL register when the DAG-CON = 0x00h or 0x07h.

### REGISTER 9-5: CALWD5: CALIBRATION WORD 5 REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>VREF4</td>
<td>VREF3</td>
<td>VREF2</td>
<td>VREF1</td>
</tr>
<tr>
<td>bit 13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>VRFS4</td>
<td>VRFS3</td>
<td>VRFS2</td>
<td>VRFS1</td>
<td>VRFS0</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **P** = Programmable bit
- **U** = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

- **bit 13** Unimplemented: Read as ‘0’
- **bit 12-8** VREF<4:0>: Output voltage reference DAC calibration bits
- **bit 7-5** Unimplemented: Read as ‘0’
- **bit 4-0** VRFS<4:0>: Output voltage reference DAC full scale range calibration bits
9.6 Calibration Word 6

The RAMP<4:0> bits at memory location 2085h calibrate the span of the slope compensation ramp. Firmware must read these values and write them to the RAMPCAL register for proper calibration.

The CSR<4:0> bits at memory location 2085h are used to calibrate the gain of the current sense amplifier. Firmware must read these values and write them to the CSRCAL register for proper calibration.

REGISTER 9-6: CALWD6: CALIBRATION WORD 6 REGISTER

<table>
<thead>
<tr>
<th>bit 13</th>
<th>U-0</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>—</td>
<td>RAMP4</td>
<td>RAMP3</td>
<td>RAMP2</td>
<td>RAMP1</td>
<td>RAMP0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7</th>
<th>U-0</th>
<th>U-0</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>—</td>
<td>—</td>
<td>CSR4</td>
<td>CSR3</td>
<td>CSR2</td>
<td>CSR1</td>
<td>CSR0</td>
<td></td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit  P = Programmable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

- bit 13 Unimplemented: Read as ‘0’
- bit 12-8 RAMP<4:0>: Slope compensation ramp span calibration bits
- bit 7-5 Unimplemented: Read as ‘0’
- bit 4-0 CSR<4:0>: Current sense amplifier gain calibration bits
9.7 Calibration Word 7

Calibration Word 7 at memory location 2086h contains the offset calibration for the output overvoltage and undervoltage comparators.

The OVCO<3:0> bits contain the output overvoltage comparator offset voltage calibration.

The UVCO<3:0> bits contain the output undervoltage comparator offset voltage calibration.

Firmware must read these values and write them to the OVUVCAL register for proper operation.

**REGISTER 9-7: CALWD7: CALIBRATION WORD 7 REGISTER**

<table>
<thead>
<tr>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>UVO3</td>
<td>UVO2</td>
<td>UVO1</td>
<td>UVO0</td>
<td>OVO3</td>
<td>OVO2</td>
<td>OVO1</td>
<td>OVO0</td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 7</td>
<td>bit 7</td>
<td>bit 7</td>
<td>bit 7</td>
<td>bit 7</td>
<td>bit 7</td>
<td>bit 7</td>
</tr>
</tbody>
</table>

**Legend:**

R = Readable bit  
P = Programmable bit  
U = Unimplemented bit, read as ‘0’  
‘1’ = Bit is set  
‘0’ = Bit is cleared  
x = Bit is unknown

- bit 13-8 Unimplemented: Read as ‘0’
- bit 7-4 UVCO<3:0>: Output Undervoltage Comparator Offset calibration bits
- bit 3-0 OVCO<3:0>: Output Overvoltage Comparator Offset calibration bits
### 9.8 Calibration Word 8

The DEMOV<4:0> bits at memory location 2087h contain the diode emulation mode comparator offset voltage. Firmware must read these values and write them to the DEMCAL register for proper operation.

**REGISTER 9-8: CALWD8: CALIBRATION WORD 8 REGISTER**

<table>
<thead>
<tr>
<th>bit 13</th>
<th>bit 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
</tr>
</tbody>
</table>

**Legend:**

- R = Readable bit
- P = Programmable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown

- bit 13-5: **Unimplemented**: Read as '0'
- bit 4-0: **DEMOV<4:0>**: Diode Emulation Mode Comparator Offset Voltage calibration bits
9.9 Calibration Word 9

The HCSOV<4:0> bits at memory location 2088h contain the calibration values for the offset voltage on the high-side current sense amplifier. Firmware must read these values and write them to the HCSOVCAL register for proper operation.

REGISTER 9-9: CALWD9: CALIBRATION WORD 9 REGISTER

| bit 13-7 | Unimplemented: Read as '0' |
| bit 6-0  | HCSOV<6:0>: High-side Current Amplifier Offset Voltage calibration bits |

Legend:
R = Readable bit  P = Programmable bit  U = Unimplemented bit, read as '0'
-n = Value at POR       ‘1’ = Bit is set       ‘0’ = Bit is cleared       x = Bit is unknown

<table>
<thead>
<tr>
<th>U-0</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>HCSOV6</td>
<td>HCSOV5</td>
<td>HCSOV4</td>
<td>HCSOV3</td>
<td>HCSOV2</td>
<td>HCSOV1</td>
<td>HCSOV0</td>
</tr>
</tbody>
</table>

bit 7

—

bit 8
9.10 Calibration Word 10

The TANA<7:0> bits at memory location 2089h contain the ADC reading from the internal temperature sensor when the silicon temperature is at +25°C.

This 10-bit reading can be used to calculate the silicon die temperature. See Section 25.0 "Internal Temperature Indicator Module" for more details.

REGISTER 9-10: CALWD10: CALIBRATION WORD 10 REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TANA9</td>
<td>TANA8</td>
<td>bit 8</td>
</tr>
<tr>
<td>bit 13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>TANA7</td>
<td>TANA6</td>
<td>TANA5</td>
<td>TANA4</td>
<td>TANA3</td>
<td>TANA2</td>
<td>TANA1</td>
<td>TANA0</td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  P = Programmable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

bit 13-8  Unimplemented: Read as ‘0’
bit 7-0  TANA<9:0>: ADC internal temperature sensor at +25°C calibration bits
9.11 Calibration Word 11

The BUFF<7:0> bits at memory location 208Ah represent the offset voltage of the unity gain buffer in units of millivolts. This is an 8-bit two’s complement number. The MSB is the sign bit. If the MSB is set to 1, the resulting number is negative.

**REGISTER 9-11: CALWD11: CALIBRATION WORD 11 REGISTER**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **P** = Programmable bit
- **U** = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

- **bit 13-8** Unimplemented: Read as ‘0’
- **bit 7-0** BUFF<7:0>: Unity gain buffer offset voltage calibration bits
### 9.12 Calibration Word 12

The ADCCAL<13:0> bits at memory location 208Bh contain the calibration bits for the A/D converter. Calibration Word 12 contains the factory measurement of the full scale ADC reference. The value represents the number of A/D converter counts per volt.

**REGISTER 9-12: CALWD12: CALIBRATION WORD 12 REGISTER**

<table>
<thead>
<tr>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADCC13</td>
<td>ADCC12</td>
<td>ADCC11</td>
<td>ADCC10</td>
<td>ADCC9</td>
<td>ADCC8</td>
<td>ADCC7</td>
<td>ADCC6</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 13</th>
<th>bit 8</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **P** = Programmable bit
- **U** = Unimplemented bit, read as '0'
- **-n** = Value at POR
- **'1'** = Bit is set
- **'0'** = Bit is cleared
- **x** = Bit is unknown

<table>
<thead>
<tr>
<th>bit 13-5</th>
<th><strong>ADCC&lt;13:5&gt;</strong>: Whole number of A/D converter counts</th>
</tr>
</thead>
<tbody>
<tr>
<td>111111111 = 511</td>
<td></td>
</tr>
<tr>
<td>•</td>
<td></td>
</tr>
<tr>
<td>•</td>
<td></td>
</tr>
<tr>
<td>•</td>
<td></td>
</tr>
<tr>
<td>000000000 = 0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 4-0</th>
<th><strong>ADCC&lt;4:0&gt;</strong>: Fraction number of A/D converter counts</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111 = 0.96875</td>
<td></td>
</tr>
<tr>
<td>•</td>
<td></td>
</tr>
<tr>
<td>•</td>
<td></td>
</tr>
<tr>
<td>0001 = 0.03125</td>
<td></td>
</tr>
<tr>
<td>0000 = 0</td>
<td></td>
</tr>
</tbody>
</table>
9.13 Calibration Word 13

Calibration Word 13 at memory location 208Ch contain
the offset of the A/D converter. This calibration word
can be used to calibrate signals read by the A/D
converter.

REGISTER 9-13: CALWD13: CALIBRATION WORD 13 REGISTER

<table>
<thead>
<tr>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADCO13</td>
<td>ADCO12</td>
<td>ADCO11</td>
<td>ADCO10</td>
<td>ADCO9</td>
<td>ADCO8</td>
</tr>
<tr>
<td>bit 13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R/P-1</td>
<td>R/P-1</td>
<td>R/P-1</td>
<td>R/P-1</td>
<td>R/P-1</td>
<td>R/P-1</td>
</tr>
<tr>
<td>ADCO7</td>
<td>ADCO6</td>
<td>ADCO5</td>
<td>ADCO4</td>
<td>ADCO3</td>
<td>ADCO2</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  P = Programmable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

bit 13-0 ADCO<13:0>: A/D converter offset

9.14 Calibration Words 14-16

Memory locations 208Dh to 208Fh contain reference voltage span adjustment (VRFSCAL) calibration
values to be used with different settings of the differential amplifier gain. The appropriate VRFSCAL
value must be used to achieve the system output voltage tolerance specification listed in the Section
“Electrical characteristics”.

REGISTER 9-14: CALWD14: CALIBRATION WORD 14 REGISTER

<table>
<thead>
<tr>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>VRS144</td>
<td>VRS143</td>
<td>VRS142</td>
<td>VRS141</td>
<td>VRS140</td>
</tr>
<tr>
<td>bit 13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R/P-1</td>
<td>R/P-1</td>
<td>R/P-1</td>
<td>R/P-1</td>
<td>R/P-1</td>
<td>R/P-1</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>VRS184</td>
<td>VRS183</td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  P = Programmable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

bit 13 Unimplemented: Read as ‘0’
bit 12-8 VRS14<4:0>: VRFSCAL calibration with Differential Amplifier gain of 1/4 (DAGCON = 0x02h)
bit 7-5 Unimplemented: Read as ‘0’
bit 4-0 VRS18<4:0>: VRFSCAL calibration with Differential Amplifier gain of 1/8 (DAGCON = 0x03h)
9.14.2 CALIBRATION WORD 15

The VSR12<4:0> bits in CALWD 15 at memory location 208Eh are to be loaded into the VRFSCAL register when the DAGCON = 0x01h. The VRS2<4:0> bits of CALWD15 are to be loaded into the VRSFCAL register when the DAGCON = 0x04h.

REGISTER 9-15: CALWD15: CALIBRATION WORD 15 REGISTER

<table>
<thead>
<tr>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VRS24</td>
<td>VRS23</td>
<td>VRS22</td>
<td>VRS21</td>
<td>VRS20</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- U = Unimplemented bit, read as '0'
- P = Programmable bit
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown

bit 13 Unimplemented: Read as '0'
bit 12-8 VRS2<4:0>: VRFSCAL calibration with Differential Amplifier gain of 2 (DAGCON = 0x04h)
bit 7-5 Unimplemented: Read as '0'
bit 4-0 VRS12<4:0>: VRFSCAL calibration with Differential Amplifier gain of 1/2 (DAGCON = 0x01h)
9.14.3 CALIBRATION WORD 16

The VSR4<4:0> bits in CALWD 16 at memory location 208Fh are to be loaded into the VRFSCAL register when the DAGCON = 0x05h. The VRS8<4:0> bits of CALWD16 are to be loaded into the VRSFCAL register when the DAGCON = 0x06h.

REGISTER 9-16: CALW16: CALIBRATION WORD 16 REGISTER

<table>
<thead>
<tr>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>VRS84</td>
<td>VRS83</td>
<td>VRS82</td>
<td>VRS81</td>
<td>VRS80</td>
<td></td>
</tr>
<tr>
<td>bit 13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit 8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
<th>R/P-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>VRS44</td>
<td>VRS43</td>
<td>VRS42</td>
<td>VRS84</td>
<td>VRS40</td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- R = Readable bit
- P = Programmable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 13: Unimplemented: Read as ‘0’
bit 12-8: VRS8<4:0>: VRFSCAL calibration with Differential Amplifier gain of 8 (DAGCON = 0x06h)
bit 7-5: Unimplemented: Read as ‘0’
bit 4-0: VRS4<4:0>: VRFSCAL calibration with Differential Amplifier gain of 4 (DAGCON = 0x05h)
10.0 MEMORY ORGANIZATION

There are two types of memory in the MCP19122/3:

- Program Memory
- Data Memory
  - Special Function Registers (SFRs)
  - General-Purpose RAM

10.1 Program Memory Organization

The MCP19122/3 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 4K x 14 (0000h-0FFFh) is physically implemented. Addressing a location above this boundary will cause a wrap-around within the first 4K x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 10-1). The width of the program memory bus (instruction word) is 14-bits. Since all instructions are a single word, the MCP19122/3 has space for 4K of instructions.

![Program Memory Map](image-url)
10.1.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set a Files Select Register (FSR) to point to the program memory.

10.1.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 10-1.

**EXAMPLE 10-1: RETLW INSTRUCTION**

```
constants
    ADDWF_PCL
    RETLW DATA0 ;Index0 data
    RETLW DATA1 ;Index1 data
    RETLW DATA2
    RETLW DATA3

my_function
    ;... LOTS OF CODE...
    MOVLW DATA_INDEX
    CALL constants
    ;... THE CONSTANT IS IN W
```

10.2 Data Memory Organization

The data memory (see Table 10-1) is partitioned into four banks, which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-7Fh in Bank 0, A0h-EFh in Bank 1 and 120h-16Fh in Bank 2 are General Purpose Registers, implemented as static RAM. All other RAM is unimplemented and returns '0' when read. The RP<1:0> bits of the STATUS register are the bank select bits.

To move values from one register to another register, the value must pass through the W register. This means that for all register-to-register moves, two instruction cycles are required.

The entire data memory can be accessed either directly or indirectly. Direct addressing may require the use of the RP<1:0> bits. Indirect addressing uses the Indirect REgister Pointer (IRP) bit in the STATUS register for access to the Bank0/Bank1 or the Bank2/Bank3 areas of data memory.

10.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 64 x 8 in the MCP19122/3. Each register is accessed, either directly or indirectly, through the FSR (refer to Section 10.5 “Indirect Addressing, INDF and FSR Registers”).

10.2.2 CORE REGISTERS

The core registers contain the registers that directly affect the basic operation. The core registers can be addressed from any bank. These registers are listed in Table 10-1. For detailed information refer to Table 10-2.

**TABLE 10-1: CORE REGISTERS**

<table>
<thead>
<tr>
<th>Addresses</th>
<th>BANKx</th>
</tr>
</thead>
<tbody>
<tr>
<td>x00h, x02h, x03h, x0Ah</td>
<td>INDF</td>
</tr>
<tr>
<td>x80h, x82h, x83h, x8Ah</td>
<td>PCL</td>
</tr>
<tr>
<td>x100h, x102h, x103h, x10Ah</td>
<td>STATUS</td>
</tr>
<tr>
<td>x180h, x182h, x183h, x18Ah</td>
<td>FSR</td>
</tr>
<tr>
<td>x180h, x182h, x183h, x18Ah</td>
<td>PCLATH</td>
</tr>
<tr>
<td>x180h, x182h, x183h, x18Ah</td>
<td>INTCON</td>
</tr>
</tbody>
</table>

10.2.3 STATUS REGISTER

The STATUS register, shown in Register 10-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (RAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as '000u uuu' (where u = unchanged).

Therefore, it is recommended that only BCF, BSF, SWAPF and MOVF instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see the Section 28.0 “Instruction Set Summary”.

**Note 1:** The C and DC bits operate as Borrow and Digit Borrow out bits, respectively, in subtraction.
10.2.4 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 10-2). These registers are static RAM.

The special registers can be classified into two sets:

- core
- peripheral

The Special Function Registers associated with the microcontroller core are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

REGISTER 10-1: STATUS: STATUS REGISTER

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R-1</th>
<th>R-1</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRP</td>
<td>RP1</td>
<td>RP0</td>
<td>TO</td>
<td>PD</td>
<td>Z</td>
<td>DC(1)</td>
<td>C(1)</td>
</tr>
</tbody>
</table>

Legend:

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 7  
IRP: Register Bank Select bit (used for Indirect addressing)
1 = Bank 2 & 3 (100h - 1FFh)
0 = Bank 0 & 1 (00h - FFh)

bit 6-5  
RP<1:0>: Register Bank Select bits (used for Direct addressing)
00 = Bank 0 (00h - 7Fh)
01 = Bank 1 (80h - FFh)
10 = Bank 2 (100h - 17Fh)
11 = Bank 3 (180h - 1FFh)

bit 4  
TO: Time-out bit
1 = After power-up, CLRWDT instruction or SLEEP instruction
0 = A WDT time-out occurred

bit 3  
PD: Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2  
Z: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1  
DC: Digit Carry/Digit Borrow bit(1) (ADDWF, ADDLW, SUBLW, SUBWF instructions)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0  
C: Carry/Borrow bit(1) (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For Borrow, the polarity is reversed. A subtraction is executed by adding the two’s complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high-order or low-order bit of the source register.
# 10.3 DATA MEMORY

## TABLE 10-2: MCP19122/3 DATA MEMORY MAP

<table>
<thead>
<tr>
<th>File Address</th>
<th>File Address</th>
<th>File Address</th>
<th>File Address</th>
<th>File Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Indirect addr. (1)</td>
<td>Indirect addr. (1)</td>
<td>Indirect addr. (1)</td>
<td>Indirect addr. (1)</td>
<td>Indirect addr. (1)</td>
</tr>
<tr>
<td>00h</td>
<td>01h</td>
<td>02h</td>
<td>03h</td>
<td>04h</td>
</tr>
<tr>
<td>TMR0</td>
<td>OPTION_REG</td>
<td>PCL</td>
<td>STATUS</td>
<td>FSR</td>
</tr>
<tr>
<td>05h</td>
<td>06h</td>
<td>07h</td>
<td>08h</td>
<td>09h</td>
</tr>
<tr>
<td>PORTGPA</td>
<td>PORTGPB</td>
<td>PIR1</td>
<td>PIR2</td>
<td>PCON</td>
</tr>
<tr>
<td>0Ah</td>
<td>0Bh</td>
<td>0Ch</td>
<td>0Dh</td>
<td>0Eh</td>
</tr>
<tr>
<td>PCLATH</td>
<td>INTC</td>
<td>TMR1L</td>
<td>TMR1H</td>
<td>T1CON</td>
</tr>
<tr>
<td>0Fh</td>
<td>10h</td>
<td>11h</td>
<td>12h</td>
<td>13h</td>
</tr>
<tr>
<td>T2CON</td>
<td>PR2</td>
<td>T1GCON</td>
<td>PWMPH</td>
<td>PWMPH</td>
</tr>
<tr>
<td>14h</td>
<td>15h</td>
<td>16h</td>
<td>17h</td>
<td>18h</td>
</tr>
<tr>
<td>PWMRH</td>
<td>PWMRH</td>
<td>PWMRH</td>
<td>PWMRH</td>
<td>PWMRH</td>
</tr>
<tr>
<td>19h</td>
<td>1Ah</td>
<td>1Bh</td>
<td>1Ch</td>
<td>1Dh</td>
</tr>
<tr>
<td>ADCON0</td>
<td>ADCON1</td>
<td>General Purpose Register</td>
<td>General Purpose Register</td>
<td>General Purpose Register</td>
</tr>
<tr>
<td>1Eh</td>
<td>1Fh</td>
<td>20h</td>
<td>21h</td>
<td>22h</td>
</tr>
<tr>
<td>7Fh</td>
<td>Accesses Bank 0</td>
<td>6Fh</td>
<td>Accesses Bank 0</td>
<td>6Fh</td>
</tr>
<tr>
<td>8Fh</td>
<td>96 Bytes</td>
<td>97h</td>
<td>98h</td>
<td>99h</td>
</tr>
<tr>
<td>Bank 0</td>
<td>Bank 1</td>
<td>Bank 2</td>
<td>Bank 3</td>
<td></td>
</tr>
</tbody>
</table>

- Unimplemented data memory locations, read as ‘0’.
- Not a physical register.
- Only accessible when DBGEN = 0 and ICKBUG<INBUG> = 1.
- Only in MCP19123 and DSTEMP.
### TABLE 10-3: MCP19122/3 SPECIAL REGISTERS SUMMARY BANK 0

<table>
<thead>
<tr>
<th>Addr.</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR Reset</th>
<th>Value on all other resets(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>INDF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxxx xxxxx</td>
<td>xxxxx xxxxx</td>
</tr>
<tr>
<td>01h</td>
<td>TMR0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxxx xxxxx</td>
<td>xxxxx xxxxx</td>
</tr>
<tr>
<td>02h</td>
<td>PCL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>uuuuuu</td>
<td>uuuuuu</td>
</tr>
<tr>
<td>03h</td>
<td>STATUS</td>
<td>IRP</td>
<td>RP1</td>
<td>RP0</td>
<td>TO</td>
<td>PD</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
<td>0001 1xxx</td>
<td>000g quuuu</td>
</tr>
<tr>
<td>04h</td>
<td>FSR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxxx xxxxx</td>
<td>uuuuuu</td>
</tr>
<tr>
<td>05h</td>
<td>PORTGA</td>
<td>GPA7</td>
<td>GPA6</td>
<td>GPA5</td>
<td>GPA4</td>
<td>GPA3</td>
<td>GPA2</td>
<td>GPA1</td>
<td>GPA0</td>
<td>xxxxx xxxxx</td>
<td>uuuuuu</td>
</tr>
<tr>
<td>06h</td>
<td>PORTGB</td>
<td>GPB7</td>
<td>GPB6</td>
<td>GPB5</td>
<td>GPB4</td>
<td>GPB3</td>
<td>GPB2</td>
<td>GPB1</td>
<td>GPB0</td>
<td>xxxxx xxxxx</td>
<td>uuuuuu</td>
</tr>
<tr>
<td>07h</td>
<td>PIR1</td>
<td>TMR1GIF</td>
<td>ADIF</td>
<td>BCLIF</td>
<td>SSPIF</td>
<td>CC2IF</td>
<td>CC1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>08h</td>
<td>PIR2</td>
<td>UVIF</td>
<td>OTIF</td>
<td>OCIF</td>
<td>OVF</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0000 --00</td>
<td>0000 --00</td>
</tr>
<tr>
<td>09h</td>
<td>PCON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>0Ah</td>
<td>PCLATH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>0Ch</td>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>TOIE</td>
<td>INTE</td>
<td>T0IF</td>
<td>INTF</td>
<td>IOCF</td>
<td>—</td>
<td>0000 000x</td>
<td>0000 0000</td>
</tr>
<tr>
<td>0Dh</td>
<td>T1CON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>0Eh</td>
<td>T2CON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>12h</td>
<td>T1GCON</td>
<td>TMR1GE</td>
<td>T1GPOL</td>
<td>T1GTM</td>
<td>T1GSPM</td>
<td>T1GGO/DONE</td>
<td>T1GVAL</td>
<td>T1GSS1</td>
<td>T1GSS0</td>
<td>0000 0x00</td>
<td>1111 1111</td>
</tr>
<tr>
<td>13h</td>
<td>PWMPHL</td>
<td>SLAVE Phase Shift Register</td>
<td>xxxxx xxxxx</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
</tr>
<tr>
<td>14h</td>
<td>PWMPHH</td>
<td>SLAVE Phase Shift Register</td>
<td>xxxxx xxxxx</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
</tr>
<tr>
<td>15h</td>
<td>PWMRL</td>
<td>PWM Register Low Byte</td>
<td>xxxxx xxxxx</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
</tr>
<tr>
<td>16h</td>
<td>PWMRH</td>
<td>PWM Register High Byte</td>
<td>xxxxx xxxxx</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
</tr>
<tr>
<td>17h</td>
<td>CC1RL</td>
<td>Capture1/Compare1 Register 1 x Low Byte (LSB)</td>
<td>xxxxx xxxxx</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
</tr>
<tr>
<td>18h</td>
<td>CC1RH</td>
<td>Capture1/Compare1 Register 1 x High Byte (MSB)</td>
<td>xxxxx xxxxx</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
</tr>
<tr>
<td>19h</td>
<td>CC2RL</td>
<td>Capture2/Compare2 Register 2 x Low Byte (LSB)</td>
<td>xxxxx xxxxx</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
</tr>
<tr>
<td>1Ah</td>
<td>CC2RH</td>
<td>Capture2/Compare2 Register 2 x High Byte (MSB)</td>
<td>xxxxx xxxxx</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
</tr>
<tr>
<td>1Bh</td>
<td>CCDCON</td>
<td>CC2M3</td>
<td>CC2M2</td>
<td>CC2M1</td>
<td>CC2M0</td>
<td>CC1M3</td>
<td>CC1M2</td>
<td>CC1M1</td>
<td>CC1M0</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>1Ch</td>
<td>ADRESL</td>
<td>Least significant 8 bits of the right-shifted result(3)</td>
<td>xxxxx xxxxx</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
<td>uuuuuu</td>
</tr>
<tr>
<td>1Dh</td>
<td>ADRESH</td>
<td>Most significant 2 bits of right-shifted result(3)</td>
<td>--- ----</td>
<td>xx uu uu</td>
<td>uu uu uu</td>
<td>uu uu uu</td>
<td>uu uu uu</td>
<td>uu uu uu</td>
<td>uu uu uu</td>
<td>uu uu uu</td>
<td>uu uu uu</td>
</tr>
<tr>
<td>1Eh</td>
<td>ADCON0</td>
<td>CHS5</td>
<td>CHS4</td>
<td>CHS3</td>
<td>CHS2</td>
<td>CHS1</td>
<td>CHS0</td>
<td>GO/DONE</td>
<td>ADON</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>1Fh</td>
<td>ADCON1</td>
<td>—</td>
<td>ADCS2</td>
<td>ADCS1</td>
<td>ADCS0</td>
<td>—</td>
<td>ADFM</td>
<td>VCFG1</td>
<td>VCFG0</td>
<td>--000 --000</td>
<td>--000 --000</td>
</tr>
</tbody>
</table>

**Legend:**
- — = Unimplemented locations read as '0'; u = unchanged, x = unknown, q = value depends on condition shaded = unimplemented

**Note:**
1. Other (non-power-up) resets include MCLR Reset and Watchdog Timer Reset during normal operation.
2. MCLR and WDT reset does not affect the previous value data latch. The IOCF bit will be cleared upon reset but will set again if the mismatch exists.
3. Results of ADC reading maybe left- or right-shifted. Results shown here are for right-shifted results.
TABLE 10-4: MCP19122/3 SPECIAL REGISTERS SUMMARY BANK 1

<table>
<thead>
<tr>
<th>Addr.</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR Reset</th>
<th>Values on all other resets(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bank 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80h</td>
<td>INDF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxxx xxxx</td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>81h</td>
<td>OPTION_REG</td>
<td>RAPU</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
<td>1111 1111</td>
<td>1111 1111</td>
</tr>
<tr>
<td>82h</td>
<td>PCL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>83h</td>
<td>STATUS</td>
<td>IRP</td>
<td>RP1</td>
<td>RP0</td>
<td>T0</td>
<td>T0</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
<td>0001 1xxx</td>
<td>000q quuu</td>
</tr>
<tr>
<td>84h</td>
<td>FSR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xxxxx xxxx</td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>85h</td>
<td>TRISGPA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td>1111 1111</td>
<td>1111 1111</td>
</tr>
<tr>
<td>86h</td>
<td>TRISGPB</td>
<td>TRISB7</td>
<td>TRISB6</td>
<td>TRISB5</td>
<td>TRISB4</td>
<td>TRISB3</td>
<td>TRISB2</td>
<td>TRISB1</td>
<td>TRISB0</td>
<td>1111 1111</td>
<td>1111 1111</td>
</tr>
<tr>
<td>87h</td>
<td>PIE1</td>
<td>TMR1IE</td>
<td>ADIE</td>
<td>BCLIE</td>
<td>SSPIE</td>
<td>CC2IE</td>
<td>CC1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>88h</td>
<td>PIE2</td>
<td>UVIE</td>
<td>OTIE</td>
<td>OCIE</td>
<td>Ovie</td>
<td>—</td>
<td>—</td>
<td>OVLOIE</td>
<td>UVLOIE</td>
<td>0000 --00</td>
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<td>OOC3</td>
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<td>OOC1</td>
<td>OOC0</td>
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<td>RE5</td>
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<td>RE3</td>
<td>RE2</td>
<td>RE1</td>
<td>RE0</td>
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<td>000 xxxxxx</td>
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</tbody>
</table>

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note:
1: Other (non power-up) resets include MCLR Reset and Watchdog Timer Reset during normal operation.
2: GPA5 pull-up is enabled when pin is configured as MCLR in Configuration Word.
3: MCLR and WDT Reset does not affect the previous value data latch. The IOCF bit will be cleared upon reset but will set again if the mismatch exists.
### TABLE 10-5: MCP19122/3 SPECIAL REGISTERS SUMMARY BANK 2

<table>
<thead>
<tr>
<th>Addr.</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR Reset</th>
<th>Value on all other resets(1)</th>
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<td>PEIE</td>
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<td>HCSOV0</td>
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<td>--xxx xxxx</td>
<td>--uu uuuu</td>
</tr>
</tbody>
</table>

**Legend:**  
- --- Unimplemented locations read as 0.  
- u = unchanged, x = unknown, q = value depends on condition shaded = unimplemented  

**Note 1:** Other (non-power-up) resets include MCLR Reset and Watchdog Timer Reset during normal operation.  

**Note 2:** MCLR and WDT reset does not affect the previous value data latch. The IOCF bit will be cleared upon reset but will set again if the mismatch exists.
# TABLE 10-6: PIC18FXXXX SPECIAL REGISTERS SUMMARY BANK 3

<table>
<thead>
<tr>
<th>Addr.</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR Reset</th>
<th>Values on all other resets(1)</th>
</tr>
</thead>
<tbody>
<tr>
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<td>xxxx xxxx</td>
<td>uuuu uuuu</td>
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<td>RAPU</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
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<td>T0</td>
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<td>IOCB4</td>
<td>IOCB3</td>
<td>IOCB2</td>
<td>IOCB1</td>
<td>IOCB0</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>187h</td>
<td>ANSELA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ANSA3</td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
<td>—</td>
<td>1111 1111</td>
<td>1111 1111</td>
</tr>
<tr>
<td>188h</td>
<td>ANSLEB</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ANSB5</td>
<td>ANSB4</td>
<td>—</td>
<td>ANSB2</td>
<td>ANSB1</td>
<td>—</td>
<td>1111 1111</td>
</tr>
<tr>
<td>189h</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>18Ah</td>
<td>PCLATH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>18Bh</td>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>TOIF</td>
<td>IOCE</td>
<td>INF</td>
<td>NOF</td>
<td>0000 000x</td>
<td>0000 000u</td>
</tr>
<tr>
<td>18ch</td>
<td>PORTICD(4)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>18dh</td>
<td>TRISICD(4)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>18eh</td>
<td>ICKBUG(4)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0--</td>
<td>0--</td>
</tr>
<tr>
<td>18fh</td>
<td>BIGBUG(4)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0--</td>
<td>0--</td>
</tr>
<tr>
<td>190h</td>
<td>PMCON1</td>
<td>—</td>
<td>CALSEL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WREN</td>
<td>WR</td>
<td>RD</td>
<td>0--</td>
</tr>
<tr>
<td>191h</td>
<td>PMCON2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>192h</td>
<td>PMADRL</td>
<td>PMADRL7</td>
<td>PMADRL6</td>
<td>PMADRL5</td>
<td>PMADRL4</td>
<td>PMADRL3</td>
<td>PMADRL2</td>
<td>PMADRL1</td>
<td>PMADRL0</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>193h</td>
<td>PMADRH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>194h</td>
<td>PMDATL</td>
<td>PMDATL7</td>
<td>PMDATL6</td>
<td>PMDATL5</td>
<td>PMDATL4</td>
<td>PMDATL3</td>
<td>PMDATL2</td>
<td>PMDATL1</td>
<td>PMDATL0</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>195h</td>
<td>PMDATH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>196h</td>
<td>TTACAL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>197h</td>
<td>OSCCAL</td>
<td>—</td>
<td>FACL6</td>
<td>FCAL5</td>
<td>FCAL4</td>
<td>FCAL3</td>
<td>FCAL2</td>
<td>FCAL1</td>
<td>FCAL0</td>
<td>—xxx</td>
<td>—uuu</td>
</tr>
<tr>
<td>198h</td>
<td>BGTCAL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>199h</td>
<td>BGRCAL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>19Ah</td>
<td>AVDDCAL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>19Bh</td>
<td>VOURCAL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>19Ch</td>
<td>DOVCAL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>19Dh</td>
<td>VEAOCAL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>19 Eh</td>
<td>BUFFCON</td>
<td>BNCHE</td>
<td>DIG0EN</td>
<td>—</td>
<td>DSEL4</td>
<td>DSEL3</td>
<td>DSEL2</td>
<td>DSEL1</td>
<td>DSEL0</td>
<td>00-0 0000</td>
<td>00-0 0000</td>
</tr>
</tbody>
</table>

## Legend
- **—** = Unimplemented locations read as '0'
- **u** = unchanged
- **x** = unknown
- **q** = value depends on condition
- **shaded** = unimplemented

## Note
1: Other (non power-up) resets include MCLR Reset and Watchdog Timer Reset during normal operation.
2: GPA5 pull-up is enabled when pin is configured as MCLR in Configuration Word.
3: MCLR and WDT Reset does not affect the previous value data latch. The IOCF bit will be cleared upon reset but will set again if the mismatch exists.
4: Only accessible when DBGEN = 0 and ICKBUG<INBUG> = 1.
10.3.0.1 OPTION Register

The OPTION register is a readable and writable register, which contains various control bits to configure:

- Timer0/WDT prescaler
- External GPA2/INT interrupt
- Timer0
- Weak pull-ups on PORTGPA and PORTGPB

**REGISTER 10-2: OPTION_REG: OPTION REGISTER**

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAPU(1)</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **-n** = Value at POR
- **‘1’ = Bit is set**
- **‘0’ = Bit is cleared**
- **x = Bit is unknown**

**bit 7**

**RAPU:** Port GPx Pull-up Enable bit

- **1** = Port GPx pull-ups are disabled
- **0** = Port GPx pull-ups are enabled

**bit 6**

**INTEDG:** Interrupt Edge Select bit

- **0** = Interrupt on rising edge of INT pin
- **1** = Interrupt on falling edge of INT pin

**bit 5**

**T0CS:** TMR0 Clock Source Select bit

- **1** = Transition on T0CKI pin
- **0** = Internal instruction cycle clock

**bit 4**

**T0SE:** TMR0 Source Edge Select bit

- **1** = Increment on high-to-low transition on T0CKI pin
- **0** = Increment on low-to-high transition on T0CKI pin

**bit 3**

**PSA:** Prescaler Assignment bit

- **1** = Prescaler is assigned to WDT
- **0** = Prescaler is assigned to the Timer0 module

**bit 2-0**

**PS<2:0>:** Prescaler Rate Select bits

<table>
<thead>
<tr>
<th>Bit Value</th>
<th>TMRO Rate</th>
<th>WDT Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>1: 2</td>
<td>1: 1</td>
</tr>
<tr>
<td>001</td>
<td>1: 4</td>
<td>1: 2</td>
</tr>
<tr>
<td>010</td>
<td>1: 8</td>
<td>1: 4</td>
</tr>
<tr>
<td>011</td>
<td>1: 16</td>
<td>1: 8</td>
</tr>
<tr>
<td>100</td>
<td>1: 32</td>
<td>1: 16</td>
</tr>
<tr>
<td>101</td>
<td>1: 64</td>
<td>1: 32</td>
</tr>
<tr>
<td>110</td>
<td>1: 128</td>
<td>1: 64</td>
</tr>
<tr>
<td>111</td>
<td>1: 256</td>
<td>1: 128</td>
</tr>
</tbody>
</table>

**Note 1:** Individual WPUx bit must also be enabled.
10.4 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 10-2 shows the two situations for loading the PC. The upper example in Figure 10-2 shows how the PC is loaded on a write to PCL (PCLATH<4:0> -> PCH). The lower example in Figure 10-2 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> -> PCH).

FIGURE 10-2: LOADING OF PC IN DIFFERENT SITUATIONS

<table>
<thead>
<tr>
<th>Instruction with Destination</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC&lt;12:8&gt;</td>
</tr>
<tr>
<td>PCH&lt;7:0&gt;</td>
</tr>
<tr>
<td>ALU Result</td>
</tr>
<tr>
<td>5</td>
</tr>
<tr>
<td>PCLATH&lt;4:0&gt;</td>
</tr>
<tr>
<td>8</td>
</tr>
<tr>
<td>PCL</td>
</tr>
<tr>
<td>12 8 7 0</td>
</tr>
<tr>
<td>GOTO, CALL</td>
</tr>
<tr>
<td>Opcode &lt;10:0&gt;</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>PCLATH&lt;4:3&gt;</td>
</tr>
<tr>
<td>11</td>
</tr>
</tbody>
</table>

10.4.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<12:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire content of the program counter to be changed by writing the desired upper 5 bits to the PCLATH register. When the lower 8 bits are written to the PCL register, all 13 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

10.4.2 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). Care should be exercised when jumping into a look-up table or program branch table (computed GOTO) by modifying the PCL register. Assuming that PCLATH is set to the table start address, if the table length is greater than 255 instructions or if the lower 8 bits of the memory address rolls over from 0xFFh to 0X00h in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and the table location within the table.

For more information, refer to Application Note AN556 – “Implementing a Table Read” (DS00556).

10.4.3 COMPUTED FUNCTION CALLS

A computed function CALL allows programs to maintain tables of functions and provide another way to execute state machines or look-up tables. When performing a table read using a computed function CALL, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block).

If using the CALL instruction, the PCH<2:0> and PCL registers are loaded with the operand of the CALL instruction. PCH<4:3> is loaded with PCLATH<4:3>.

10.4.4 STACK

The MCP19122/3 has an 8-level x 13-bit wide hardware stack (refer to Figure 10-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFI instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no Status bits to indicate Stack Overflow or Stack Underflow conditions.
2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFI instructions or the vectoring to an interrupt address.

10.5 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing. Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register directly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR and the IRP bit of the STATUS register, as shown in Figure 10-3.

A simple program to clear RAM location 40h-7Fh using indirect addressing is shown in Example 10-2.
EXAMPLE 10-2: INDIRECT ADDRESSING

MOVLW 0x40 ;initialize pointer
MOVWF FSR ;to RAM
NEXT CLRF INDF ;clear INDF register
INCF FSR ;inc pointer
BTFSS FSR,7 ;all done?
GOTO NEXT ;no clear next
CONTINUE ;yes continue

FIGURE 10-3: DIRECT/INDIRECT ADDRESSING

For memory map detail, see Figure 10-2.
11.0 SPECIAL FEATURES OF THE CPU

The MCP19122/3 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving features and offer code protection.

These features are:
- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator selection
- Sleep
- Code protection
- ID Locations
- In-Circuit Serial Programming

The Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, is designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can use the Power-up Timer to provide at least a 72 ms Reset. With these functions-on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-Down mode. The user can wake-up from Sleep through:
- External Reset
- Watchdog Timer Wake-up
- An interrupt

11.1 Configuration Bits

The Configuration bits can be programmed (read as ‘0’), or left unprogrammed (read as ‘1’) to select various device configurations as shown in Register 11-1. These bits are mapped in program memory location 2007h.

Note: Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See “Memory Programming Specification” (DS41561) for more information.
# REGISTER 11-1: CONFIGURATION WORD REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value 1</th>
<th>Value 0</th>
<th>Value n</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>DEBUG</td>
<td>—</td>
<td>—</td>
<td>BOREN</td>
</tr>
<tr>
<td>12</td>
<td>Unimplemented: Read as ‘1’.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11-10</td>
<td>WRT&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>9</td>
<td>Unimplemented: Read as ‘1’.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>BOREN</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>7</td>
<td>Unimplemented: Read as ‘1’.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>CP</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>5</td>
<td>MCLRE</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>4</td>
<td>PWRTE</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>3</td>
<td>WDTE</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>2-0</td>
<td>Unimplemented: Read as ‘1’.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Legend:
- **R** = Readable bit
- **P** = Programmable bit
- **U** = Unimplemented bit, read as ‘1’
- ‘0’ = Bit is cleared
- ‘1’ = Bit is set
- ‘-n’ = Value when blank or after Bulk Erase

### Notes:
1. Enabling Brown-out Reset does not automatically enable Power-up Timer.
2. The Configuration bit is managed automatically by the device development tools. The user should not attempt to manually write this bit location. However, the user should ensure that this location has been programmed to a ‘1’ and the device checksum is correct for proper operation of production software.
11.2 Code Protection

Code protection allows the device to be protected from unauthorized access. Internal access to the program memory is unaffected by any code protection setting.

11.2.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the CP bit in the Configuration Word. When CP = 0, external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Writing the program memory is dependent upon the write protection setting.

11.3 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as boot loader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in the Configuration Word define the size of the program memory block that is protected.

11.4 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable during Program/Verify mode. Only the Least Significant 7 bits of the ID locations are reported when using MPLAB Integrated Development Environment (IDE).
12.0 RESETS

The reset logic is used to place the MCP19122/3 into a known state. The source of the reset can be determined by using the device status bits.

There are multiple ways to reset this device:

- Power-on Reset (POR)
- WDT Reset during normal operation
- WDT Reset during Sleep
- MCLR Reset during normal operation
- MCLR Reset during Sleep
- Brown-out Reset (BOR)

To allow VDD to stabilize, an optional power-up timer can be enabled to extend the Reset time after a POR event.

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a “Reset state” on:

- Power-on Reset
- MCLR Reset
- MCLR Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

WDT wake-up does not cause register resets in the same manner as a WDT Reset since wake-up is viewed as the resumption of normal operation. TO and PD bits are set or cleared differently in different Reset situations, as indicated in Table 12-1. Software can use these bits to determine the nature of the Reset. See Table 12-2 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 12-1.

The MCLR Reset path has a noise filter to detect and ignore small pulses. See Section 5.0, Digital Electrical Characteristics for pulse-width specifications.

Note 1: Refer to the Configuration Word register (Register 11-1).
### 12.1 Power-on Reset (POR)

The on-chip POR circuit holds the chip in Reset until \( V_{DD} \) has reached a high enough level for proper operation. To take advantage of the POR, simply connect the MCLR pin through a resistor to \( V_{DD} \). This will eliminate external RC components usually needed to create Power-on Reset. If the BOR is enabled, the maximum rise time specification does not apply. The BOR circuitry will keep the device in Reset until \( V_{DD} \) reaches \( V_{BOR} \) (see Section 12.3 “Brown-out Reset (BOR)”).

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure proper operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

### 12.2 MCLR

MCP19122/3 has a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive MCLR pin low.

Voltages applied to the MCLR pin that exceed its specification can result in both MCLR Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the MCLR pin no longer be tied directly to \( V_{DD} \). The use of an RC network, as shown in Figure 12-2, is suggested.

An internal MCLR option is enabled by clearing the MCLRE bit in the Configuration Word register. When MCLRE = 0, the Reset signal to the chip is generated internally. When the MCLRE = 1, the MCLR pin becomes an external Reset input. In this mode, the MCLR pin has a weak pull-up to \( V_{DD} \).

### TABLE 12-1: TIME-OUT IN VARIOUS SITUATIONS

<table>
<thead>
<tr>
<th>Oscillator Configuration</th>
<th>Power-up: PWRTE = 0</th>
<th>Power-up: PWRTE = 1</th>
<th>Brown-out Reset: PWRTE = 0</th>
<th>Brown-out Reset: PWRTE = 1</th>
<th>Wake-up from Sleep</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTOSC</td>
<td>TpWRT</td>
<td>—</td>
<td>TpWRT</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

### TABLE 12-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE

<table>
<thead>
<tr>
<th>POR</th>
<th>BOR</th>
<th>TO</th>
<th>PD</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>x</td>
<td>1</td>
<td>1</td>
<td>Power-on Reset</td>
</tr>
<tr>
<td>u</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Brown-out Reset</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>0</td>
<td>u</td>
<td>WDT Reset</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>0</td>
<td>0</td>
<td>WDT Wake-up</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>MCLR Reset during normal operation</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>1</td>
<td>0</td>
<td>MCLR Reset during Sleep</td>
</tr>
</tbody>
</table>

Legend:  
\( u \) = unchanged,  \( x \) = unknown

### FIGURE 12-2: RECOMMENDED MCLR CIRCUIT

![MCLR Circuit Diagram](image-url)
12.3 Brown-out Reset (BOR)

The BOREN bit in the Configuration Word register enables or disables the BOR mode. See Register 11-1 for the Configuration Word definition.

A brown-out occurs when VDD falls below VBOR for greater than 100 µs minimum. On a Reset (Power-On, Brown-Out, Watchdog Timer, etc.), the chip will remain in Reset until VDD rises above VBOR (refer to Figure 12-3). If enabled, the Power-up Timer will be invoked by the Reset and will keep the chip in Reset an additional 72 ms. During power-up, it is recommended that the BOR configuration bit is enabled, holding the MCU in Reset (OSC turned off and no code execution) until VDD exceeds the VBOR threshold. Users have the option of adding an additional 72 ms delay by clearing the PWRTE bit. At this time, the VDD voltage level is high enough to operate the MCU functions only; all other device functionality is not operational. This is independent of the value of VIN, which is typically VDD + VDROPOUT. During power-down with BOR enabled, the MCU operation will be held in Reset when VDD falls below the VBOR threshold. With BOR disabled or while operating in Sleep mode, the POR will hold the part in Reset when VDD falls below the VPOR threshold.

A brown-out occurs when VIN falls below VBOR for greater than parameter TBOR. The brown-out condition will reset the device. This will occur regardless of VIN slew rate. A Brown-out Reset may not occur if VIN falls below VBOR for less than parameter TBOR.

If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will execute a 72 ms Reset.

Note: The Power-up Timer is enabled by the PWRTE bit in the Configuration Word register.

If VIN falls below VBOR for less than parameter TBOR, the device will reset.

FIGURE 12-3: BROWN-OUT SITUATIONS

Note 1: 72 ms delay only if PWRTE bit is programmed to ‘0’.
12.4 Power-up Timer (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time-out on power-up only, from POR Reset. The Power-up Timer operates from an internal RC oscillator. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the V_{DD} to rise to an acceptable level. A Configuration bit (PWRTE), can disable (if set) or enable (if cleared or programmed) the Power-up Timer.

The Power-up Timer delay will vary from chip to chip due to:
- V_{DD} variation
- Temperature variation
- Process variation

The Power-Up Timer optionally delays device execution after a POR event. This timer is typically used to allow V_{DD} to stabilize before allowing the device to start running.

The Power-up Timer is controlled by the PWRTE bit of the Configuration Word.

12.5 Watchdog Timer (WDT) Reset

The Watchdog Timer generates a Reset if the firmware does not issue a \texttt{CLRWDT} instruction within the time-out period. The TO and PD bits in the STATUS register are changed to indicate the WDT Reset. See Section 15.0, Watchdog Timer (WDT) for more information.

12.6 Start-up Sequence

Upon the release of a POR, the following must occur before the device will begin executing:
- Power-up Timer runs to completion (if enabled)
- Oscillator start-up timer runs to completion
- MCLR must be released (if enabled)

The total time-out will vary based on PWRTE bit status. For example, with PWRTE bit erased (PWRT disabled), there will be no time-out at all. Figures 12-4, 12-5 and 12-6 depict time-out sequences.

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs will expire. Then, bringing MCLR high will begin execution immediately (see Figure 12-5). This is useful for testing purposes or to synchronize more than one MCP19122/3 device operating in parallel.

12.6.1 POWER CONTROL (PCON) REGISTER

The Power Control register PCON (address 8Eh) has two Status bits to indicate what type of Reset occurred last.

Note: Voltage spikes below V_{SS} at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 \Omega should be used when applying a “low” level to the MCLR pin, rather than pulling this pin directly to V_{SS}.

FIGURE 12-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED MCLR): CASE 1

\begin{center}
\begin{tikzpicture}
\begin{scope}[every node/.style={midway,above}]
\draw (0,0) -- (0,2) node {V_{DD}};
\draw (0,1) -- (0,1.5) node {MCLR};
\draw (0,0.5) -- (0,1) node {Internal POR};
\draw (0,0.2) -- (0,0.5) node {PWRT Time-out};
\draw (0,0) -- (0,0.2) node {OST Time-out};
\draw (0,0) -- (0,0) node {Internal Reset};
\end{scope}
\draw (1,0) -- (1,1.5) node {T_{PWRT}};
\draw (1,0) -- (1,0) node {T_{IOSCST}};
\end{tikzpicture}
\end{center}
FIGURE 12-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED MCLR): CASE 2

VDD
MCLR
Internal POR
PWRT Time-out
OST Time-out
Internal Reset

TPWRT

FIGURE 12-6: TIME-OUT SEQUENCE ON POWER-UP (MCLR WITH VDD)

VDD
MCLR
Internal POR
PWRT Time-out
OST Time-out
Internal Reset

TPWRT

TIOSCST
12.7  Determining the Cause of a Reset

Upon any Reset, multiple bits in the STATUS and PCON register are updated to indicate the cause of the Reset. Table 12-3 and Table 12-4 show the Reset conditions of these registers.

### Table 12-3: Reset Status Bits and Their Significance

<table>
<thead>
<tr>
<th>POR</th>
<th>BOR</th>
<th>TO</th>
<th>PD</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>x</td>
<td>1</td>
<td>1</td>
<td>Power-on Reset</td>
</tr>
<tr>
<td>u</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Brown-out Reset</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>0</td>
<td>u</td>
<td>WDT Reset</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>0</td>
<td>0</td>
<td>WDT Wake-up from Sleep</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>1</td>
<td>0</td>
<td>Interrupt Wake-up from Sleep</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>MCLR Reset during normal operation</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>1</td>
<td>0</td>
<td>MCLR Reset during Sleep</td>
</tr>
<tr>
<td>0</td>
<td>u</td>
<td>0</td>
<td>x</td>
<td>Not allowed. TO is set on POR</td>
</tr>
<tr>
<td>0</td>
<td>u</td>
<td>x</td>
<td>0</td>
<td>Not allowed. PD is set on POR</td>
</tr>
</tbody>
</table>

### Table 12-4: Reset Condition for Special Registers (Note 2)

<table>
<thead>
<tr>
<th>Condition</th>
<th>Program Counter</th>
<th>STATUS Register</th>
<th>PCON Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-on Reset</td>
<td>0000h</td>
<td>0001 1xxxx</td>
<td>---- --0u</td>
</tr>
<tr>
<td>Brown-out Reset</td>
<td>000</td>
<td>0001 1xxx</td>
<td>---- --u0</td>
</tr>
<tr>
<td>MCLR Reset during normal operation</td>
<td>0000h</td>
<td>000u uuuu</td>
<td>---- --uu</td>
</tr>
<tr>
<td>MCLR Reset during Sleep</td>
<td>0000h</td>
<td>0001 0uuu</td>
<td>---- --uu</td>
</tr>
<tr>
<td>WDT Reset</td>
<td>0000h</td>
<td>0000 uuuu</td>
<td>---- --uu</td>
</tr>
<tr>
<td>WDT Wake-up from Sleep</td>
<td>PC + 1</td>
<td>uuu0 0uuu</td>
<td>---- --uu</td>
</tr>
<tr>
<td>Interrupt Wake-up from Sleep</td>
<td>PC + 1(1)</td>
<td>uuu1 0uuu</td>
<td>---- --uu</td>
</tr>
</tbody>
</table>

Legend:  
- u = unchanged,  
- x = unknown,  
- = unimplemented bit, reads as ’0’.

Note 1: When the wake-up is due to an interrupt and Global Enable bit (GIE) is set, the return address is pushed on the stack and PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

2: If a Status bit is not implemented, that bit will be read as ‘0’.
12.8 Power Control (PCON) Register

The Power Control (PCON) register contains flag bits to differentiate between:

- Power-on Reset (POR)
- Over Temperature (OT)
- Brown-out Reset (BOR)

**REGISTER 12-1: PCON: POWER CONTROL REGISTER**

| bit 7-2 | Unimplemented: Read as '0' |
| bit 1   | POR: Power-on Reset Status bit |
|        | 1 = No Power-on Reset occurred |
|        | 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs) |
| bit 0   | Unimplemented: Read as '0' |

**TABLE 12-5: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS**

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>POR</td>
<td>BOR</td>
</tr>
<tr>
<td>STATUS</td>
<td>IPR</td>
<td>RP1</td>
<td>RP0</td>
<td>TO</td>
<td>PD</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
<td>77</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented bit, reads as '0'. Shaded cells are not used by Resets.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.
13.0 INTERRUPTS

The MCP19122/3 has multiple sources of interrupt:

• External Interrupt (INT pin)
• Interrupt-on-Change (IOC) Interrupts
• Timer0 Overflow Interrupt
• Timer1 Overflow Interrupt
• Timer1 Gate Interrupt
• Timer2 Match Interrupt
• ADC Interrupt
• SSP
• BCL
• Input Undervoltage Interrupt
• Input Overvoltage Interrupt
• System Output Overvoltage Interrupt
• System Output Undervoltage Interrupt
• System Output Overcurrent Interrupt
• Overtemperature
• CC1
• CC2

The Interrupt Control register (INTCON) and Peripheral Interrupt Request Registers (PIRx) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

The Global Interrupt Enable bit, GIE of the INTCON register, enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register and PIEx registers. GIE is cleared on Reset.

When an interrupt is serviced, the following actions occur automatically:

• The GIE is cleared to disable any further interrupt.
• The return address is pushed onto the stack.
• The PC is loaded with 0004h.

The Return from Interrupt instruction, RETFIE, exits the interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

• INT Pin Interrupt
• Interrupt-on-Change (IOC) Interrupts
• Timer0 Overflow Interrupt

The peripheral interrupt flags are contained in the PIR1 and PIR2 registers. The corresponding interrupt enable bit is contained in the PIE1 and PIE2 registers.

For external interrupt events, such as the INT pin or PORTGPx change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 13-2). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

Note 1: Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

2: When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on Timer1, Timer2, comparators, ADC, CCD modules, refer to the respective peripheral section.

13.0.1 GPA2/INT INTERRUPT

The external interrupt on the GPA2/INT pin is edge-triggered; either on the rising edge if the INTEDG bit of the OPTION register is set, or the falling edge, if the INTEDG bit is clear. When a valid edge appears on the GPA2/INT pin, the INTF bit of the INTCON register is set. This interrupt can be disabled by clearing the INTE control bit of the INTCON register. The INTF bit must be cleared by software in the Interrupt Service Routine before re-enabling this interrupt. The GPA2/INT interrupt can wake-up the processor from Sleep, if the INTE bit was set prior to going into Sleep. See Section 14.0 “Power-Down Mode (Sleep)” for details on Sleep.

Note: The ANSELx register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read ‘0’ and cannot generate an interrupt.
13.0.2 TIMER0 INTERRUPT
An overflow (FFh → 00h) in the TMR0 register will set the T0IF bit of the INTCON register. The interrupt can be enabled/disabled by setting/clearing T0IE bit of the INTCON register. See Section 21.0 “Timer0 Module” for operation of the Timer0 module.

13.0.3 PORTGPX INTERRUPT-ON-CHANGE
An input change on PORTGPx sets the IOCIF bit of the INTCON register. The interrupt can be enabled/disabled by setting/clearing the IOCIE bit of the INTCON register. Plus, individual pins can be configured through the IOC register.

Note: If a change on the I/O pin should occur when any PORTGPx operation is being executed, then the IOCIF interrupt flag may not get set.
13.1 Interrupt Control Registers

13.1.1 INTCON REGISTER

The INTCON register is a readable and writable register, that contains the various enable and flag bits for the TMR0 register overflow, interrupt-on-change and external INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

---

**FIGURE 13-2: INT PIN INTERRUPT TIMING**

<table>
<thead>
<tr>
<th>PC</th>
<th>Inst (PC)</th>
<th>Inst (PC + 1)</th>
<th>—</th>
<th>Inst (0004h)</th>
<th>Inst (0005h)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction Fetched</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Instruction Executed</td>
<td>Inst (PC – 1)</td>
<td>Inst (PC)</td>
<td>Dummy Cycle</td>
<td>Dummy Cycle</td>
<td>Inst (0004h)</td>
</tr>
</tbody>
</table>

**INSTRUCTION FLOW**

- **Q1** | **Q2** | **Q3** | **Q4** | **Q1** | **Q2** | **Q3** | **Q4** | **Q1** | **Q2** | **Q3** | **Q4** | **Q1** | **Q2** | **Q3** | **Q4** |

**INTF flag**

Note 1: INTF flag is sampled here (every Q1).
Note 2: Asynchronous interrupt latency = 3-4 T\_CY. Synchronous latency = 3 T\_CY, where T\_CY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
Note 3: CLKOUT is available only in INTOSC and RC Oscillator modes.
Note 4: For minimum width of INT pulse, refer to AC specifications in Section 5.0, Digital Electrical Characteristics.
Note 5: INTF is enabled to be set any time during the Q4-Q1 cycles.
REGISTER 13-1: INTCON: INTERRUPT CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Legend</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td><strong>GIE</strong>:</td>
<td>Global Interrupt Enable bit</td>
</tr>
<tr>
<td></td>
<td>R = Readable bit</td>
<td>1 = Enables all unmasked interrupts</td>
</tr>
<tr>
<td></td>
<td>W = Writable bit</td>
<td>0 = Disables all interrupts</td>
</tr>
<tr>
<td>6</td>
<td><strong>PEIE</strong>:</td>
<td>Peripheral Interrupt Enable bit</td>
</tr>
<tr>
<td></td>
<td>R = Readable bit</td>
<td>1 = Enables all unmasked peripheral interrupts</td>
</tr>
<tr>
<td></td>
<td>W = Writable bit</td>
<td>0 = Disables all peripheral interrupts</td>
</tr>
<tr>
<td>5</td>
<td><strong>T0IE</strong>:</td>
<td>TMR0 Overflow Interrupt Enable bit</td>
</tr>
<tr>
<td></td>
<td>R = Readable bit</td>
<td>1 = Enables the TMR0 interrupt</td>
</tr>
<tr>
<td></td>
<td>W = Writable bit</td>
<td>0 = Disables the TMR0 interrupt</td>
</tr>
<tr>
<td>4</td>
<td><strong>INTE</strong>:</td>
<td>INT External Interrupt Enable bit</td>
</tr>
<tr>
<td></td>
<td>R = Readable bit</td>
<td>1 = Enables the INT external interrupt</td>
</tr>
<tr>
<td></td>
<td>W = Writable bit</td>
<td>0 = Disables the INT external interrupt</td>
</tr>
<tr>
<td>3</td>
<td><strong>IOCE</strong>:</td>
<td>Interrupt-on-Change Enable bit</td>
</tr>
<tr>
<td></td>
<td>R = Readable bit</td>
<td>1 = Enables the interrupt-on-change</td>
</tr>
<tr>
<td></td>
<td>W = Writable bit</td>
<td>0 = Disables the interrupt-on-change</td>
</tr>
<tr>
<td>2</td>
<td><strong>T0IF</strong>:</td>
<td>TMR0 Overflow Interrupt Flag bit</td>
</tr>
<tr>
<td></td>
<td>R = Readable bit</td>
<td>1 = TMR0 register has overflowed (must be cleared in software)</td>
</tr>
<tr>
<td></td>
<td>W = Writable bit</td>
<td>0 = TMR0 register did not overflow</td>
</tr>
<tr>
<td>1</td>
<td><strong>INTF</strong>:</td>
<td>External Interrupt Flag bit</td>
</tr>
<tr>
<td></td>
<td>R = Readable bit</td>
<td>1 = The external interrupt occurred (must be cleared in software)</td>
</tr>
<tr>
<td></td>
<td>W = Writable bit</td>
<td>0 = The external interrupt did not occur</td>
</tr>
<tr>
<td>0</td>
<td><strong>IOCF</strong>:</td>
<td>Interrupt-on-Change Interrupt Flag bit</td>
</tr>
<tr>
<td></td>
<td>R = Readable bit</td>
<td>1 = When at least one of the interrupt-on-change pins changed state</td>
</tr>
<tr>
<td></td>
<td>W = Writable bit</td>
<td>0 = None of the interrupt-on-change pins have changed state</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**Note 1:** IOC register must also be enabled.

**Note 2:** T0IF bit is set when TMR0 rolls over. TMR0 is unchanged on Reset and should be initialized before clearing T0IF bit.
13.1.1.1 PIE1 Register

The PIE1 register contains the Peripheral Interrupt Enable bits, as shown in Register 13-1.

Note 1: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

### REGISTER 13-1: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMR1GIE</td>
<td>ADIE</td>
</tr>
<tr>
<td>BCLIE</td>
<td>SSPIE</td>
</tr>
<tr>
<td>CC2IE</td>
<td>CC1IE</td>
</tr>
<tr>
<td>TMR2IE</td>
<td>TMR1IE</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

- **bit 7** TMR1GIE: Timer1 Gate Interrupt Enable bit
  - 1 = Enables the Timer1 gate interrupt
  - 0 = Disables the Timer1 gate interrupt
- **bit 6** ADIE: ADC Interrupt Enable bit
  - 1 = Enables the ADC interrupt
  - 0 = Disables the ADC interrupt
- **bit 5** BCLIE: MSSP Bus Collision Interrupt Enable bit
  - 1 = Enables the MSSP Bus Collision Interrupt
  - 0 = Disables the MSSP Bus Collision Interrupt
- **bit 4** SSPIE: Synchronous Serial Port (MSSP) Interrupt Enable bit
  - 1 = Enables the MSSP interrupt
  - 0 = Disables the MSSP interrupt
- **bit 3** CC2IE: Capture2/Compare2 Interrupt Enable bit
  - 1 = Enables the Capture2/Compare2 interrupt
  - 0 = Disables the Capture2/Compare2 interrupt
- **bit 2** CC1IE: Capture1/Compare1 Interrupt Enable bit
  - 1 = Enables the Capture1/Compare1 interrupt
  - 0 = Disables the Capture1/Compare1 interrupt
- **bit 1** TMR2IE: Timer2 Interrupt Enable
  - 1 = Enables the Timer2 interrupt
  - 0 = Disables the Timer2 interrupt
- **bit 2** TMR1IE: Timer1 Interrupt Enable
  - 1 = Enables the Timer1 interrupt
  - 0 = Disables the Timer1 interrupt
13.1.1.2 PIE2 Register

The PIE2 register contains the Peripheral Interrupt Enable bits, as shown in Register 13-2.

Note 1: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

### REGISTER 13-2: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3-2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>UVIE</td>
<td>OTIE</td>
<td>OCIE</td>
<td>OVIE</td>
<td>—</td>
<td>—</td>
<td>OVLOIE</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>UVLOIE</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **-n** = Value at POR
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **x** = Bit is unknown

- **bit 7 UVIE**: Output Undervoltage Interrupt enable bit
  - 1 = Enables the UV interrupt
  - 0 = Disables the UV interrupt

- **bit 6 OTIE**: Overtemperature Interrupt enable bit
  - 1 = Enables over temperature interrupt
  - 0 = Disables over temperature interrupt

- **bit 5 OCIE**: Output Overcurrent Interrupt enable bit
  - 1 = Enables the OC interrupt
  - 0 = Disables the OC interrupt

- **bit 4 OVIE**: Output Overvoltage Interrupt enable bit
  - 1 = Enables the OV interrupt
  - 0 = Disables the OV interrupt

- **bit 3-2 Unimplemented**: Read as '0'

- **bit 1 OVLOIE**: $V_{IN}$ Overvoltage Lock Out Interrupt Enable bit
  - 1 = Enables the $V_{IN}$ OVLO interrupt
  - 0 = Disables the $V_{IN}$ OVLO interrupt

- **bit 0 UVLOIE**: $V_{IN}$ Undervoltage Lock Out Interrupt Enable bit
  - 1 = Enables the $V_{IN}$ UVLO interrupt
  - 0 = Disables the $V_{IN}$ UVLO interrupt
13.1.1.3 PIR1 Register

The PIR1 register contains the Peripheral Interrupt Flag bits, as shown in Register 13-3.

**Note 1:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

**REGISTER 13-3: PIR1: PERIPHERAL INTERRUPT FLAG REGISTER 1**

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMR1GIF</td>
<td>ADIF</td>
</tr>
<tr>
<td>BCLIF</td>
<td>SSPIF</td>
</tr>
<tr>
<td>CC2IF</td>
<td>CC1IE</td>
</tr>
<tr>
<td>TMR2IF</td>
<td>TMR1IF</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown

- **bit 7 TMR1GIF:** Timer1 Gate Interrupt Flag bit
  - 1 = Interrupt is pending
  - 0 = Interrupt is not pending
- **bit 6 ADIF:** ADC Interrupt Flag bit
  - 1 = ADC conversion complete
  - 0 = ADC conversion has not completed or has not been started
- **bit 5 BCLIF:** MSSP Bus Collision Interrupt Flag bit
  - 1 = Interrupt is pending
  - 0 = Interrupt is not pending
- **bit 4 SSPIF:** Synchronous Serial Port (MSSP) Interrupt Flag bit
  - 1 = Interrupt is pending
  - 0 = Interrupt is not pending
- **bit 3 CC2IF:** Capture2/Compare2 Interrupt Flag bit
  - 1 = Capture or Compare has occurred
  - 0 = Capture or Compare has not occurred
- **bit 2 CC1IF:** Capture2/Compare2 Interrupt Flag bit
  - 1 = Capture or Compare has occurred
  - 0 = Capture or Compare has not occurred
- **bit 1 TMR2IF:** Timer2 to PR2 Match Interrupt Flag
  - 1 = Timer2 to PR2 match occurred (must be cleared in software)
  - 0 = Timer2 to PR2 match did not occur
- **bit 0 TMR1IF:** Timer1 Interrupt Flag
  - 1 = Timer1 rolled over (must be cleared in software)
  - 0 = Timer1 has not rolled over
13.1.1.4 PIR2 Register

The PIR2 register contains the Peripheral Interrupt Flag bits, as shown in Register 13-4.

**Note 1:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

### REGISTER 13-4: PIR2: PERIPHERAL INTERRUPT FLAG REGISTER 2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Legend</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>UVIF</td>
<td>Output Undervoltage error interrupt flag bit</td>
</tr>
<tr>
<td>6</td>
<td>OTIF</td>
<td>Overtemperature interrupt flag bit</td>
</tr>
<tr>
<td>5</td>
<td>OCIF</td>
<td>Output over current error interrupt flag bit</td>
</tr>
<tr>
<td>4</td>
<td>OVIF</td>
<td>Output overvoltage error interrupt flag bit</td>
</tr>
<tr>
<td>3-2</td>
<td>Unimplemented</td>
<td>Read as '0'</td>
</tr>
<tr>
<td>1</td>
<td>OVLOIF</td>
<td>VIN Overvoltage Lock Interrupt Flag bit</td>
</tr>
<tr>
<td>0</td>
<td>UVLOIF</td>
<td>VIN Undervoltage Lock Out Interrupt Flag bit</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **-n** = Value at POR
- '1' = Bit is set
- '0' = Bit is cleared
- **x** = Bit is unknown

- **bit 7**: **UVIF**: Output Undervoltage error interrupt flag bit
  - 1 = Output undervoltage error has occurred
  - 0 = Output undervoltage error has not occurred

- **bit 6**: **OTIF**: Overtemperature interrupt flag bit
  - 1 = Overtemperature error has occurred
  - 0 = Overtemperature error has not occurred

- **bit 5**: **OCIF**: Output over current error interrupt flag bit
  - 1 = Output overcurrent error has occurred
  - 0 = Output overcurrent error has not occurred

- **bit 4**: **OVIF**: Output overvoltage error interrupt flag bit
  - 1 = Output overvoltage error has occurred
  - 0 = Output overvoltage error has not occurred

- **bit 3-2**: Unimplemented: Read as '0'

- **bit 1**: **OVLOIF**: VIN Overvoltage Lock Interrupt Flag bit
  - With OVLOINTP bit set
  - 1 = A $V_{IN}$ NOT overvoltage to $V_{IN}$ overvoltage edge has been detected
  - 0 = A $V_{IN}$ NOT overvoltage to $V_{IN}$ overvoltage edge has NOT been detected

  - With OVLOINTN bit set
  - 1 = A $V_{IN}$ overvoltage to $V_{IN}$ NOT overvoltage edge has been detected
  - 0 = A $V_{IN}$ overvoltage to $V_{IN}$ NOT overvoltage edge has NOT been detected

- **bit 0**: **UVLOIF**: VIN Undervoltage Lock Out Interrupt Flag bit
  - With UVLOINTP bit set
  - 1 = A $V_{IN}$ NOT undervoltage to $V_{IN}$ undervoltage edge has been detected
  - 0 = A $V_{IN}$ NOT undervoltage to $V_{IN}$ undervoltage edge has NOT been detected

  - With UVLOINTN bit set
  - 1 = A $V_{IN}$ undervoltage to $V_{IN}$ NOT undervoltage edge has been detected
  - 0 = A $V_{IN}$ undervoltage to $V_{IN}$ NOT undervoltage edge has NOT been detected
13.2 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Temporary holding registers W_TEMP and STATUS_TEMP should be placed in the last 16 bytes of GPR. These 16 locations are common to all banks and do not require banking. This makes context save and restore operations simpler. The code shown in Example 13-1 can be used to:

- Store the W register
- Store the STATUS register
- Execute the ISR code
- Restore the Status (and Bank Select Bit register)
- Restore the W register

Note: The MCP19122/3 device does not require saving the PCLATH. However, if computed GOTOs are used in both the ISR and the main code, the PCLATH must be saved and restored in the ISR.

**TABLE 13-5: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS**

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>IOCE</td>
<td>T0IF</td>
<td>INTF</td>
<td>IOCF</td>
<td>102</td>
</tr>
<tr>
<td>OPTION_REG</td>
<td>RAPU</td>
<td>INTEDG</td>
<td>T0CE</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
<td>83</td>
</tr>
<tr>
<td>PIE1</td>
<td>—</td>
<td>ADIE</td>
<td>BCLIE</td>
<td>SSPIE</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>103</td>
</tr>
<tr>
<td>PIE2</td>
<td>UVIE</td>
<td>—</td>
<td>OCIE</td>
<td>OVIE</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>VINV</td>
<td>104</td>
</tr>
<tr>
<td>PIR1</td>
<td>—</td>
<td>ADIF</td>
<td>BCLIF</td>
<td>SSPIF</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TMR1IF</td>
<td>105</td>
</tr>
<tr>
<td>PIR2</td>
<td>UVIF</td>
<td>—</td>
<td>OCIF</td>
<td>OVF</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>VINIF</td>
<td>106</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented locations read as ‘0’. Shaded cells are not used by Interrupts.

**EXAMPLE 13-1: SAVING STATUS AND W REGISTERS IN RAM**

```assembly
MOVWF W_TEMP ;Copy W to TEMP register
SWAPF STATUS,W ;Swap status to be saved into W
;Swaps are used because they do not affect the status bits
MOVWF STATUS_TEMP ;Save status to bank zero STATUS_TEMP register
 ;
 ;(ISR)
 ;(sets bank to original state)
SWAPF STATUS_TEMP,W ;Swap STATUS_TEMP register into W
MOVWF STATUS ;Move W into STATUS register
SWAPF W_TEMP,F ;Swap W_TEMP
SWAPF W_TEMP,W ;Swap W_TEMP into W
```
14.0 POWER-DOWN MODE (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction.

Upon entering SLEEP, the following conditions exist:

- WDT will be cleared but keeps running, if enabled for operation during SLEEP.
- PD bit of the STATUS register is cleared.
- TO bit of the STATUS register is set.
- CPU clock is disabled.
- The ADC is inoperable due to the absence of the 4V LDO power (AVDD) while the ADC reference is set to AVDD. To minimize sleep current the ADC reference must be set to the default AVDD.
- I/O Ports maintain the status they had before SLEEP was executed (driving high, low or high-impedance).
- Resets other than WDT and BOR are not affected by SLEEP mode.
- Analog circuitry power (AVDD) is removed during SLEEP.

Refer to individual chapters for more details on peripheral operation during SLEEP.

To minimize current consumption, the following conditions should be considered:

- I/O pins should not be floating.
- External circuitry sinking current from I/O pins.
- Internal circuitry sourcing current from I/O pins.
- Current draw from pins with internal weak pull-ups.
- Modules using Timer1 oscillator.
- ADC reference must be set to default condition (AVDD).
- I/O pins that are high-impedance inputs should be pulled to VDD or GND externally to avoid switching currents caused by floating inputs.

If the VDDEN bit is set, the SLEEP instruction removes power from the analog circuitry. AVDD is shut down to minimize current draw in SLEEP Mode and to achieve the 50µA typical shutdown current. Shutdown current specifications can only be met with no current draw from external loads. The 5V VDD voltage drops to 2.5V-3.0V and is only capable of supplying >1mA in SLEEP Mode. If more than 1mA of current are drawn from pins with internal weak pull-ups, the WDT is cleared when the device wakes up from SLEEP, regardless of the source of the wake-up.

14.0.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

1. External Reset input on MCLR pin, if enabled.
2. POR Reset.
3. Watchdog Timer, if enabled.
4. Any external interrupt.
5. Interrupts by peripherals capable of running during SLEEP (see individual peripheral for more information).

The first two events will cause a device reset. The last three events are considered a continuation of program execution. To determine whether a device reset or wake-up event occurred, refer to Section 12.7 “Determining the Cause of a Reset”

The following peripheral interrupts can wake the device from SLEEP:

- Interrupt-on-change
- External interrupt from INT pin

When the SLEEP instruction is being executed, the next instruction (PC + 1) is prefetched. For the device to wake up through an interrupt event, the corresponding interrupt enable bit must be enabled. Wake-up will occur regardless of the state of the GIE bit. If the GIE bit is disabled, the device continues execution at the instruction after the SLEEP instruction, the device will then call the Interrupt Service Routine. In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

The WDT is cleared when the device wakes up from SLEEP, regardless of the source of the wake-up.

14.0.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs before the execution of the SLEEP instruction:
  - SLEEP instruction will execute as a NOP.
  - WDT and WDT prescaler will not be cleared.
  - TO bit in the STATUS register will not be set.
  - PD bit in the STATUS register will not be cleared.

- If the interrupt occurs during or after the execution of a SLEEP instruction:
  - SLEEP instruction will be completely executed
  - Device will immediately wake up from SLEEP
  - WDT and WDT prescaler will be cleared
  - TO bit in STATUS register will be set
  - PD bit in the STATUS register will be cleared
Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flags bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the PD bit. If the PD bit is set, the SLEEP instruction was executed as a NOP.

**FIGURE 14-1: WAKE-UP FROM SLEEP THROUGH INTERRUPT**

**TABLE 14-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE**

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>IOCE</td>
<td>T0IF</td>
<td>INTF</td>
<td>IOCF</td>
<td>102</td>
</tr>
<tr>
<td>IOCA</td>
<td>IOCA7</td>
<td>IOCA6</td>
<td>IOCA5</td>
<td>—</td>
<td>IOCA3</td>
<td>IOCA2</td>
<td>IOCA1</td>
<td>IOCA0</td>
<td>130</td>
</tr>
<tr>
<td>IOCB</td>
<td>IOCB7</td>
<td>IOCB6</td>
<td>IOCB5</td>
<td>IOCB4</td>
<td>—</td>
<td>—</td>
<td>IOCB1</td>
<td>IOCB0</td>
<td>130</td>
</tr>
<tr>
<td>PIE1</td>
<td>TXIE</td>
<td>RCIE</td>
<td>BCLIE</td>
<td>SSPIE</td>
<td>CC2IE</td>
<td>CC1IE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>103</td>
</tr>
<tr>
<td>PIE2</td>
<td>CDSIE</td>
<td>ADIE</td>
<td>—</td>
<td>OTIE</td>
<td>Ovie</td>
<td>DRUVIE</td>
<td>OVLOIE</td>
<td>UVLOIE</td>
<td>104</td>
</tr>
<tr>
<td>PIR1</td>
<td>TXIF</td>
<td>RCIF</td>
<td>BCLIF</td>
<td>SSPIF</td>
<td>CC2IF</td>
<td>CC1IF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>105</td>
</tr>
<tr>
<td>PIR2</td>
<td>CDSIF</td>
<td>ADIF</td>
<td>—</td>
<td>OTIF</td>
<td>OVIIF</td>
<td>DRUVIF</td>
<td>OVLOIF</td>
<td>UVLOIF</td>
<td>106</td>
</tr>
<tr>
<td>STATUS</td>
<td>IRP</td>
<td>RP1</td>
<td>RP0</td>
<td>T0</td>
<td>PD</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
<td>77</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented, read as ‘0’. Shaded cells are not used in Power-down mode.
15.0 WATCHDOG TIMER (WDT)

The Watchdog Timer is a free-running timer, using the on-chip RC oscillator as its clock source. The WDT is enabled by setting the WDTE bit of the Configuration Word (default setting). When WDTE is set, the on-chip RC oscillator will always be enabled to provide a clock source to the WDT module.

15.1 Watchdog Timer (WDT) Operation

During normal operation, a WDT time-out generates a device Reset. If the device is in Sleep mode, a WDT time-out causes the device to wake-up and continue with normal operation; this is known as a WDT wake-up. The WDT can be permanently disabled by clearing the WDTE configuration bit.

The postscaler assignment is fully under software control and can be changed during program execution.

15.2 WDT Period

The WDT has a nominal time-out period of 18 ms (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device Reset.

The TO bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

15.3 WDT Programming Considerations

It should also be taken in account that under worst-case conditions (i.e., VDD = Min., Temperature = Max., Max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

FIGURE 15-1: WATCHDOG TIMER WITH SHARED PRESCALE BLOCK DIAGRAM

- **Note 1:** T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION_REG register.
- **2:** WDTE bit is in the Configuration Word register.
### TABLE 15-1: WDT STATUS

<table>
<thead>
<tr>
<th>Conditions</th>
<th>WDT</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDTE = 0</td>
<td></td>
</tr>
<tr>
<td>CLRWDT Command</td>
<td></td>
</tr>
<tr>
<td>Exit Sleep</td>
<td></td>
</tr>
<tr>
<td>SLEEP Command</td>
<td>Cleared</td>
</tr>
</tbody>
</table>

### TABLE 15-2: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPTION_REG</td>
<td>RAPU</td>
<td>INTEDG</td>
<td>T0CE</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
<td>83</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented locations read as ‘0’. Shaded cells are not used by Watchdog Timer.

### TABLE 15-3: SUMMARY OF CONFIGURATION WORD ASSOCIATED WITH WATCHDOG TIMER

<table>
<thead>
<tr>
<th>Name</th>
<th>Bits</th>
<th>Bit -7</th>
<th>Bit -6</th>
<th>Bit 13/5</th>
<th>Bit 12/4</th>
<th>Bit 11/3</th>
<th>Bit 10/2</th>
<th>Bit 9/1</th>
<th>Bit 8/0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG</td>
<td>13:8</td>
<td>—</td>
<td>—</td>
<td>DBGEN</td>
<td>WRT1</td>
<td>WRT0</td>
<td>BOREN</td>
<td></td>
<td>88</td>
<td></td>
</tr>
<tr>
<td>CONFIG</td>
<td>7:0</td>
<td>—</td>
<td>CP</td>
<td>MCLRE</td>
<td>PWRTF</td>
<td>WDTE</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

Legend: — = unimplemented locations read as ‘0’. Shaded cells are not used by Watchdog Timer.
16.0 OSCILLATOR MODES

The MCP19122/3 has one oscillator configuration, which is an 8 MHz internal oscillator.

16.1 Internal Oscillator (INTOSC)

The Internal Oscillator module provides a system clock source of 8 MHz. The frequency of the internal oscillator can be trimmed with a calibration value in the OSCTUNE register.

16.2 Oscillator Calibration

The 8 MHz internal oscillator is factory calibrated. The factory calibration values reside in the read-only Calibration Word 1 register. These values must be read from the Calibration Word 1 register and stored in the OSCCAL register. Refer to Section 20.0 “Flash Program Memory Control” for the procedure on reading from program memory.

Note 1: The FCAL<6:0> bits from the Calibration Word 1 register must be written into the OSCCAL register to calibrate the internal oscillator.

16.3 Frequency Tuning in User Mode

In addition to the factory calibration, the base frequency can be tuned in the user’s application. This frequency tuning capability allows the user to deviate from the factory calibrated frequency. The user can tune the frequency by writing to the OSCTUNE register (see Register 16-1).

REGISTER 16-1: OSCTUNE: – OSCILLATOR TUNING REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TUN4</td>
<td>TUN3</td>
<td>TUN2</td>
<td>TUN1</td>
<td>TUN0</td>
</tr>
</tbody>
</table>

bit 7-5 Unimplemented: Read as ’0’

bit 4-0 TUN<4:0>: Frequency Tuning bits

- 01111 = Maximum frequency
- 01110 = 
- 
- 00001 = Center frequency. Oscillator Module is running at the calibrated frequency.
- 11111 = 
- 
- 10000 = Minimum frequency
16.3.1 OSCILLATOR DELAY UPON POWER-UP, WAKE-UP AND BASE FREQUENCY CHANGE

In applications where the OSCTUNE register is used to shift the frequency of the internal oscillator, the user should not expect the frequency of the internal oscillator to stabilize immediately. In this case, the frequency may shift gradually toward the new value. The time for this frequency shift is less than eight cycles of the base frequency.

On power-up, the device is held in reset by the power-up time, if the power-up timer is enabled. Following a wake-up from Sleep mode or POR, an internal delay of \(~10\ \mu s\) is invoked to allow the memory bias to stabilize before program execution can begin.

### TABLE 16-1: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSCTUNE</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TUN4</td>
<td>TUN3</td>
<td>TUN2</td>
<td>TUN1</td>
<td>TUN0</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented locations read as '0'. Shaded cells are not used by clock sources.

### TABLE 16-2: SUMMARY OF CALIBRATION WORD ASSOCIATED WITH CLOCK SOURCES

<table>
<thead>
<tr>
<th>Name</th>
<th>Bits</th>
<th>Bit -/7</th>
<th>Bit -/6</th>
<th>Bit 13/5</th>
<th>Bit 12/4</th>
<th>Bit 11/3</th>
<th>Bit 10/2</th>
<th>Bit 9/1</th>
<th>Bit 8/0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>CALWD1</td>
<td>13:8</td>
<td>—</td>
<td>—</td>
<td>BGR5</td>
<td>BGR4</td>
<td>BGR3</td>
<td>BGR2</td>
<td>BGR1</td>
<td>BGR0</td>
<td>61</td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td>—</td>
<td>FCAL6</td>
<td>FCAL5</td>
<td>FCAL4</td>
<td>FCAL3</td>
<td>FCAL2</td>
<td>FCAL1</td>
<td>FCAL0</td>
<td></td>
</tr>
</tbody>
</table>

Legend: — = unimplemented locations read as '0'. Shaded cells are not used by clock sources.
17.0 I/O PORTS

In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Each port has two registers for its operation. These registers are:
- TRISGPx registers (data direction register)
- PORTGPx registers (reads the levels on the pins of the device)

Some ports may have one or more of the following additional registers. These registers are:
- ANSELx (analog select)
- WPUx (weak pull-up)

Ports with analog functions also have an ANSELx register, which can disable the digital input and save power. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 17-1.

FIGURE 17-1: GENERIC I/O PORTGFX OPERATION

17.1 PORTGPA and TRISGPA Registers

PORTGPA is an 8-bit wide, bidirectional port consisting of five CMOS I/O, two open drain I/O, and one open drain input-only pin. The corresponding data direction register is TRISGPA (Register 17-2). Setting a TRISGPA bit (\( = 1 \)) will make the corresponding PORTGPA pin an input (i.e., disable the output driver). Clearing a TRISGPA bit (\( = 0 \)) will make the corresponding PORTGPA pin an output (i.e., enables output driver). The exception is GPA5, which is input only and its TRISGPA bit will always read as '1'. Example 17-1 shows how to initialize an I/O port.

Reading the PORTGPA register (Register 17-1) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations.

The TRISGPA register (Register 17-2) controls the PORTGPA pin output drivers, even when they are being used as analog inputs. The user must ensure the bits in the TRISGPA register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'. If the pin is configured for a digital output (either port or alternate function), the TRISGPA bit must be cleared in order for the pin to drive the signal, and a read will reflect the state of the pin.

17.1.1 INTERRUPT-ON-CHANGE

Each PORTGPA pin is individually configurable as an interrupt-on-change pin. Control bits IOCA<7:0> enable or disable the interrupt function for each pin. The interrupt-on-change feature is disabled on a Power-on Reset. Reference Section 18.0 “Interrupt-On-Change” for more information.

17.1.2 WEAK PULL-UPS

PORTGPA<1:0> and PORTGPA5 have an internal weak pull-up. PORTGPA<7:6> are special ports for the SSP module and do not have weak pull-ups. PORTGPA<3:2> are special current source ports and do not have weak pull-ups. PORTGPA4 is a true open drain pin and does not have a weak pull-up. Individual control bits can enable or disable the internal weak pull-ups (see Register 17-3). The weak pull-up is automatically turned off when the port pin is configured as an output or on a Power-on Reset setting the Rapu bit of the OPTION register. The weak pull-up on GPA5 is enabled when configured as MCLR pin by setting bit 5 of the Configuration Word or when controlled by software.

17.1.3 WEAK CURRENT SOURCE

PORTGPA<3:2> are capable of being configured as weak current sources. Setting WPUGPA<3:2> to 0 allows each pin to source 50 μA (typical). By connecting GPA2 or GPA3 to ground with a resistor The voltage on the pin can be read with the A/V to determine device I2C/PMBus address. The value of the resistor to ground shall be 3 kΩ to 50 kΩ.

EXAMPLE 17-1: INITIALIZING PORTA

; This code example illustrates ; initializing the PORTGPA register. The ; other ports are initialized in the same ; manner.

BANKSEL PORTGPA;
CLRF PORTGPA;Init PORTA
BANKSEL ANSELA;
CLRF ANSELA;digital I/O
BANKSEL TRISGPA;
MOVLW B'00011111';Set GPA<4:0> as
;inputs
MOVWF TRISGPA;and set GPA<7:6> as
;outputs
The current source on GPA3 also functions as the Error Amplifier clamp control source.

17.1.4 ANSELA REGISTER
The ANSELA register (Register 17-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allows analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on the digital output functions. A pin with TRISGPA clear and ANSELA set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note: The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSELA bits must be initialized to '0' by user software.

17.1.5 PORTGPA FUNCTIONS AND OUTPUT PRIORITIES
Each PORTGPA pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 17-1. For additional information, refer to the appropriate section in this data sheet.

PORTGPA pins GPA7 and GPA4 are true open-drain pins with no connection back to VDD.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority. Analog input functions, such as ADC, are not shown in the priority lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELA registers. Digital output functions may control the pin when it is in Analog mode with the priority shown in Table 17-1.
## TABLE 17-1: PORTGPA FUNCTIONS

<table>
<thead>
<tr>
<th>Pad Name</th>
<th>Function</th>
<th>I/O</th>
<th>Type &amp; Priority(1)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>GPA0</strong></td>
<td>The GPA0 pad has basic port, peripheral and test mode features. The test mode outputs of the ALT_ICSPDAT and ANALOG_TEST take priority over the port data. The TRISGPA bit is overridden when configured as ALT_ICSPDAT or analog test output. The pad is an output only when configured so by the user. Enabling the AN0 input disables the input buffers and forces PORTGPA&lt;0&gt; to read ‘0’.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPA0</td>
<td>OUT</td>
<td>CMOS-4</td>
<td>PORTGPA&lt;0&gt; data output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN</td>
<td>TTL</td>
<td>PORTGPA&lt;0&gt; data input</td>
<td></td>
</tr>
<tr>
<td>AN0</td>
<td>IN</td>
<td>ANA</td>
<td>Channel 0 A/D input</td>
<td></td>
</tr>
<tr>
<td>ANALOG_TEST</td>
<td>OUT</td>
<td>ANA-3</td>
<td>Analog test mode output</td>
<td></td>
</tr>
<tr>
<td><strong>GPA1</strong></td>
<td>The GPA1 pad has basic port, peripheral and test mode features. The pad is an output only when configured so by the user. Enabling the AN1 input disables the input buffers and forces PORTGPA&lt;1&gt; to read ‘0’.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPA1</td>
<td>OUT</td>
<td>CMOS-2</td>
<td>PORTGPA&lt;1&gt; data output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN</td>
<td>TTL</td>
<td>PORTGPA&lt;1&gt; data input</td>
<td></td>
</tr>
<tr>
<td>AN1</td>
<td>IN</td>
<td>ANA</td>
<td>Channel 1 A/D input</td>
<td></td>
</tr>
<tr>
<td>SYNC_SIGNAL</td>
<td>IN</td>
<td>ST</td>
<td>Synchronization signal input</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OUT</td>
<td>CMOS-1</td>
<td>Synchronization signal output</td>
<td></td>
</tr>
<tr>
<td><strong>GPA2</strong></td>
<td>The GPA2 pad has basic port, peripheral and test mode features. The pad is an output only when configured so by the user. Enabling the AN2 input disables the input buffers and forces PORTGPA&lt;2&gt; to read ‘0’.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPA2</td>
<td>OUT</td>
<td>CMOS-1</td>
<td>PORTGPA&lt;2&gt; data output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN</td>
<td>ST</td>
<td>PORTGPA&lt;2&gt; data input</td>
<td></td>
</tr>
<tr>
<td>AN2</td>
<td>IN</td>
<td>ANA</td>
<td>Channel 2 A/D input</td>
<td></td>
</tr>
<tr>
<td>T0CKI</td>
<td>IN</td>
<td>ST</td>
<td>Timer 0 input</td>
<td></td>
</tr>
<tr>
<td>INT</td>
<td>IN</td>
<td>ST</td>
<td>External interrupt input</td>
<td></td>
</tr>
<tr>
<td><strong>GPA3</strong></td>
<td>The GPA3 pad has basic port, peripheral and test mode features. The pad is an output only when configured so by the user. Enabling the AN3 input disables the input buffers and forces PORTGPA&lt;3&gt; to read ‘0’.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPA3</td>
<td>OUT</td>
<td>CMOS-1</td>
<td>PORTGPA&lt;3&gt; data output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN</td>
<td>ST</td>
<td>PORTGPA&lt;3&gt; data input</td>
<td></td>
</tr>
<tr>
<td>AN3</td>
<td>IN</td>
<td>ANA</td>
<td>Channel 3 A/D input</td>
<td></td>
</tr>
<tr>
<td>T1G1</td>
<td>IN</td>
<td>ST</td>
<td>Input 1 to Timer1 gate</td>
<td></td>
</tr>
<tr>
<td><strong>GPA4</strong></td>
<td>The GPA4 pad is a high voltage port. The TRISGPA bit is always set.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPA4</td>
<td>OUT</td>
<td>OD</td>
<td>PORTGPA&lt;4&gt; open drain data output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN</td>
<td>TTL</td>
<td>PORTGPA&lt;4&gt; open drain data input</td>
<td></td>
</tr>
<tr>
<td><strong>GPA5</strong></td>
<td>The GPA5 pad is an input-only high voltage port. The TRISGPA bit is always set.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPA5</td>
<td>IN</td>
<td>TTL</td>
<td>PORTGPA&lt;5&gt; open drain data input</td>
<td></td>
</tr>
<tr>
<td>MCLR</td>
<td>IN</td>
<td>ST</td>
<td>MCLR input</td>
<td></td>
</tr>
<tr>
<td>TEST</td>
<td>IN</td>
<td>HV</td>
<td>ICSP and test mode entry high voltage pin</td>
<td></td>
</tr>
</tbody>
</table>

Legend: OUT - Output, IN - Input, ANA - Analog Signal, DIG - Digital Output, OD - Open Drain Output, ST - Schmitt Buffer Input, TTL - TTL Buffer Input, XTAL - Crystal connection, HV - High Voltage

Note 1: Output priority number determines the precedence of data into the MUX when multiple outputs are available at the same time (1 - highest priority). This number affects drive data, but not drive enable. Items with same priority number are mutually exclusive.

2: Pad module signal connections reflect only the module input signals. Output connections are addressed in the corresponding consumer module.
### TABLE 17-1: PORTGPA FUNCTIONS (CONTINUED)

<table>
<thead>
<tr>
<th>Pad Name</th>
<th>Function</th>
<th>I/O</th>
<th>Type &amp; Priority(1)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPA6</td>
<td>OUT</td>
<td>CMOS-3</td>
<td>PORTGPA&lt;6&gt; data output</td>
<td></td>
</tr>
<tr>
<td>GPA6</td>
<td>IN</td>
<td>ST</td>
<td>PORTGPA&lt;6&gt; data input</td>
<td></td>
</tr>
<tr>
<td>ICSPDAT</td>
<td>OUT</td>
<td>CMOS-1</td>
<td>ICSP Data output (MCP19122 Only)</td>
<td></td>
</tr>
<tr>
<td>ICSPDAT</td>
<td>IN</td>
<td>ST</td>
<td>ICSP Data input (MCP19122 Only)</td>
<td></td>
</tr>
<tr>
<td>CCD1</td>
<td>OUT</td>
<td>CMOS-2</td>
<td>CCD1 output</td>
<td></td>
</tr>
<tr>
<td>CCD1</td>
<td>IN</td>
<td>ST</td>
<td>CCD1 input</td>
<td></td>
</tr>
<tr>
<td>GPA7</td>
<td>OUT</td>
<td>OD-2</td>
<td>PORTGPA&lt;7&gt; open drain</td>
<td></td>
</tr>
<tr>
<td>GPA7</td>
<td>IN</td>
<td>ST</td>
<td>PORTGPA&lt;7&gt; data input</td>
<td></td>
</tr>
<tr>
<td>SCL</td>
<td>IN</td>
<td>I2C</td>
<td>I2C slave mode clock input with selectable I2C or SMBus input levels</td>
<td></td>
</tr>
<tr>
<td>ICSPCLK</td>
<td>OUT</td>
<td>OD-1</td>
<td>I2C master mode clock output</td>
<td></td>
</tr>
<tr>
<td>ICSPCLK</td>
<td>IN</td>
<td>ST</td>
<td>ICSPCK input (MCP19122 Only)</td>
<td></td>
</tr>
</tbody>
</table>

Legend: OUT - Output, IN - Input, ANA - Analog Signal, DIG - Digital Output, OD - Open Drain Output, ST - Schmitt Buffer Input, TTL - TTL Buffer Input, XTAL - Crystal connection, HV - High Voltage

**Note 1:** Output priority number determines the precedence of data into the MUX when multiple outputs are available at the same time (1 - highest priority). This number affects drive data, but not drive enable. Items with same priority number are mutually exclusive.

**Note 2:** Pad module signal connections reflect only the module input signals. Output connections are addressed in the corresponding consumer module.
### REGISTER 17-1: PORTGPA: PORTGPA REGISTER

<table>
<thead>
<tr>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>R/W-x</th>
<th>GPA7</th>
<th>GPA6</th>
<th>GPA5</th>
<th>GPA4</th>
<th>GPA3</th>
<th>GPA2</th>
<th>GPA1</th>
<th>GPA0</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>bit 7</th>
<th>GPA7</th>
<th>General Purpose Open Drain I/O pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 6</td>
<td>GPA6</td>
<td>General Purpose I/O pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Port pin is &gt; VIH</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Port pin is &lt; VIL</td>
</tr>
<tr>
<td></td>
<td>GPA5/MCLR: General Purpose Open Drain Input pin</td>
<td></td>
</tr>
<tr>
<td>bit 5</td>
<td>GPA4</td>
<td>General Purpose Open Drain I/O pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GPA&lt;3:0&gt;: General Purpose I/O pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Port pin is &gt; VIH</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Port pin is &lt; VIL</td>
</tr>
</tbody>
</table>

### REGISTER 17-2: TRISGPA: PORTGPA TRI-STATE REGISTER

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>TRISA7</th>
<th>TRISA6</th>
<th>TRISA5</th>
<th>TRISA4</th>
<th>TRISA3</th>
<th>TRISA2</th>
<th>TRISA1</th>
<th>TRISA0</th>
</tr>
</thead>
</table>

| bit 7-6 | TRISA<7:6>: PORTGPA Tri-State Control bit |
|         | 1 = PORTGPA pin configured as an input (tri-stated) |
|         | 0 = PORTGPA pin configured as an output |
| bit 5   | TRISA5: GPA5 Port Tri-State Control bit |
|         | This bit is always ‘1’ as GPA5 is an input only |
| bit 4-0 | TRISA<4:0>: PORTGPA Tri-State Control bit |
|         | 1 = PORTGPA pin configured as an input (tri-stated) |
|         | 0 = PORTGPA pin configured as an output |

---

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### REGISTER 17-3: WPUGPA: WEAK PULL-UP PORTGPA REGISTER

<p>| | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>R/W-1</td>
<td>U-0</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
<tr>
<td>----</td>
<td>----</td>
<td>------</td>
<td>---</td>
<td>------</td>
<td>------</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td>——</td>
<td>——</td>
<td>WPUA5</td>
<td>——</td>
<td>WCS1</td>
<td>WCS0</td>
<td>WPUA1</td>
<td>WPUA0</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- *x* = Bit is unknown

- **bit 7-6** Unimplemented: Read as ‘0’
- **bit 5** **WPUA5**: Weak Pull-up Register bit
  - 1 = Pull-up enabled
  - 0 = Pull-up disabled
- **bit 4** Unimplemented: Read as ‘0’
- **bit 3-2** **WCS<1:0>**: Weak Current Source bit
  - 1 = Pull-up enabled
  - 0 = Pull-up disabled
- **bit 1-0** **WPUA<1:0>**: Weak Pull-up Register bit
  - 1 = Pull-up enabled
  - 0 = Pull-up disabled

**Note 1:** The weak pull-up device is enabled only when the global RAPU bit is enabled, the pin is in input mode (TRISGPA = 1), and the individual WPUA bit is enabled (WPUA = 1), and the pin is not configured as an analog input.

**Note 2:** GPA5 weak pull-up is also enabled when the pin is configured as MCLR in Configuration word.

**Note 3:** GPA2 and GPA3 weak current sources are not dependant on the global RAPU.

### REGISTER 17-4: ANSELA: ANALOG SELECT PORTGPA REGISTER

<p>| | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
<tr>
<td>----</td>
<td>----</td>
<td>----</td>
<td>------</td>
<td>------</td>
<td>------</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td>——</td>
<td>——</td>
<td>——</td>
<td>ANSA3</td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- *x* = Bit is unknown

- **bit 7-4** Unimplemented: Read as ‘0’
- **bit 3-0** **ANSA<3:0>**: Analog Select PORTGPA Register bit
  - 1 = Analog input. Pin is assigned as analog input.\(^{[1]}\)
  - 0 = Digital I/O. Pin is assigned to port or special function.

**Note 1:** Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.
### Table 17-2: Summary of Registers Associated with PORTGPA

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSELA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ANSA3</td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
</tr>
<tr>
<td>OPTION_REG</td>
<td>RAPU</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
<td>83</td>
</tr>
<tr>
<td>IOCA</td>
<td>IOCA7</td>
<td>IOCA6</td>
<td>IOCA5</td>
<td>IOCA4</td>
<td>IOCA3</td>
<td>IOCA2</td>
<td>IOCA1</td>
<td>IOCA0</td>
<td>130</td>
</tr>
<tr>
<td>PORTGPA</td>
<td>GPA7</td>
<td>GPA6</td>
<td>GPA5</td>
<td>GPA4</td>
<td>GPA3</td>
<td>GPA2</td>
<td>GPA1</td>
<td>GPA0</td>
<td>119</td>
</tr>
<tr>
<td>TRISGPA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td>119</td>
</tr>
<tr>
<td>WPUGPA</td>
<td>—</td>
<td>—</td>
<td>WPUA5</td>
<td>—</td>
<td>WCS1</td>
<td>WCS0</td>
<td>WPUA1</td>
<td>WPUA0</td>
<td>120</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented locations read as ‘0’. Shaded cells are not used by PORTGPA.
17.2 PORTGPB and TRISGPB Registers

PORTGPB is an 8-bit wide, bidirectional port consisting of seven general purpose I/O ports. The corresponding data direction register is TRISGPB (Register 17-6). Setting a TRISGPB bit (= 1) will make the corresponding PORTGPB pin an input (i.e., disable the output driver). Clearing a TRISGPB bit (= 0) will make the corresponding PORTGPB pin an output (i.e., enable the output driver). Example 17-1 shows how to initialize an I/O port.

Some pins for PORTGPB are multiplexed with an alternate function for the peripheral, or a clock function. In general, when a peripheral or clock function is enabled, that pin may not be used as a general purpose I/O pin.

Reading the PORTGPB register (Register 17-5) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations.

The TRISGPB register (Register 17-6) controls the PORTGPB pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISGPB register are maintained set when using them as analog inputs. I/O pins configured as analog input always read ‘0’. If the pin is configured for a digital output (either port or alternate function), the TRISGPB bit must be cleared in order for the pin to drive the signal and a read will reflect the state of the pin.

17.2.1 INTERRUPT-ON-CHANGE

Each PORTGPB pin is individually configurable as an interrupt-on-change pin. Control bits IOCB<7:4> and IOCB<2:0> enable or disable the interrupt function for each pin. The interrupt-on-change feature is disabled on a Power-on Reset. Reference Section 18.0 “Interrupt-On-Change” for more information.

17.2.2 WEAK PULL-UPS

Each of the PORTGPB pins, except GPB0, has an individually configurable internal weak pull-up. Control bits WPUB<7:4> and WPUB<2:1> enable or disable each pull-up (see Register 17-7). Each weak pull-up is automatically turned off when the port pin is configured as an output. All pull-ups are disabled on a Power-on Reset by the RAPU bit of the OPTION register.

17.2.3 ANSELB REGISTER

The ANSELB register (Register 17-8) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELB bit high will cause all digital reads on the pin to be read as ‘0’ and allows analog functions on the pin to operate correctly.

The state of the ANSELB bits has no effect on the digital output functions. A pin with TRISGPB clear and ANSELB set will still operate as a digital output, but the

Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note: The ANSELB bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSELB bits must be initialized to ‘0’ by the user’s software.

17.2.4 PORTGPB FUNCTIONS AND OUTPUT PRIORITIES

Each PORTGPB pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 17-3. For additional information, refer to the appropriate section in this data sheet.

PORTGPB pin GPB0 is a true open drain pin with no connection back to VDD.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority. Analog input functions, such as ADC, and some digital input functions are not included in the list below. These inputs are active when the I/O pin is set for Analog mode using the ANSELB registers. Digital output functions may control the pin when it is in Analog mode, with the priority shown in Table 17-3.
### TABLE 17-3: PORTGPB FUNCTIONS (2)

<table>
<thead>
<tr>
<th>Pad Name</th>
<th>Function</th>
<th>I/O</th>
<th>Type &amp; Priority (1)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>GPB0</strong></td>
<td>The GPB0 pad has basic port, peripheral and test mode features. The pad is an output only when configured so by the user.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>GPB0</strong></td>
<td>OUT</td>
<td>OD-2</td>
<td>PORTGPB&lt;0&gt; data output, open drain</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN</td>
<td>TTL</td>
<td>PORTGPB&lt;0&gt; data input, open drain</td>
<td></td>
</tr>
<tr>
<td><strong>SDA</strong></td>
<td>IN</td>
<td>I2C</td>
<td>I2C slave mode data input with selectable I2C or SMBus input levels</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OUT</td>
<td>OD-1</td>
<td>I2C master mode data open drain output</td>
<td></td>
</tr>
<tr>
<td><strong>GPB1</strong></td>
<td>The GPB1 pad has basic port, peripheral and test mode features. The pad is an output only when configured by the user. Enabling the AN4 input disables the input buffers and forces PORTGPB&lt;1&gt; to read ‘0’.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>GPB1</strong></td>
<td>OUT</td>
<td>CMOS-2</td>
<td>PORTGPB&lt;1&gt; data output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN</td>
<td>TTL</td>
<td>PORTGPB&lt;1&gt; data input</td>
<td></td>
</tr>
<tr>
<td><strong>AN4</strong></td>
<td>IN</td>
<td>ANA</td>
<td>Channel 4 A/D input</td>
<td></td>
</tr>
<tr>
<td><strong>CON_SIGNAL</strong></td>
<td>IN</td>
<td>ANA</td>
<td>Slave mode Current Reference input</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OUT</td>
<td>ANA-1</td>
<td>Master mode Current Sense output</td>
<td></td>
</tr>
<tr>
<td><strong>GPB2</strong></td>
<td>The GPB2 pad has basic port and peripheral features. The pad is an output only when so configured by the user. Enabling the AN5 input disables the input buffers and forces PORTGPB&lt;2&gt; to read ‘0’.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>GPB2</strong></td>
<td>OUT</td>
<td>CMOS</td>
<td>PORTGPB&lt;2&gt; data output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN</td>
<td>TTL</td>
<td>PORTGPB&lt;2&gt; data input</td>
<td></td>
</tr>
<tr>
<td><strong>AN5</strong></td>
<td>IN</td>
<td>ANA</td>
<td>Channel 5 A/D input</td>
<td></td>
</tr>
<tr>
<td><strong>T1G2</strong></td>
<td>IN</td>
<td>ST</td>
<td>Input 2 to TIMER1 gate</td>
<td></td>
</tr>
<tr>
<td><strong>GPB3</strong></td>
<td>The GPB3 pad has basic port and peripheral features. The pad is an output only when so configured by the user.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>GPB3</strong></td>
<td>OUT</td>
<td>CMOS-2</td>
<td>PORTGPB&lt;3&gt; data output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN</td>
<td>TTL</td>
<td>PORTGPA&lt;3&gt; data input</td>
<td></td>
</tr>
<tr>
<td><strong>CLOCK</strong></td>
<td>OUT</td>
<td>CMOS</td>
<td>Oscillator output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN</td>
<td>ST</td>
<td>Oscillator input</td>
<td></td>
</tr>
<tr>
<td><strong>GPB4</strong></td>
<td>The GPB4 pad has basic port, peripheral and test mode features. The test mode outputs of ICSPDAT take priority over the port data. The TRISGPB bit is overridden to ‘0’ when configured as ICSPDAT. The pad is an output only when configured so by the user. Enabling the AN6 input disables the input buffers and forces PORTGPB&lt;4&gt; to read ‘0’. This pin is only available on the MCP19123.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>GPB4</strong></td>
<td>OUT</td>
<td>CMOS-3</td>
<td>PORTGPB&lt;4&gt; data output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN</td>
<td>TTL</td>
<td>PORTGPB&lt;4&gt; data input</td>
<td></td>
</tr>
<tr>
<td><strong>AN6</strong></td>
<td>IN</td>
<td>ANA</td>
<td>Channel 6 A/D input</td>
<td></td>
</tr>
<tr>
<td><strong>ICSPDAT</strong></td>
<td>OUT</td>
<td>CMOS-2</td>
<td>Serial programming data output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN</td>
<td>ST</td>
<td>Serial programming data input</td>
<td></td>
</tr>
<tr>
<td><strong>ICDDAT</strong></td>
<td>OUT</td>
<td>CMOS-1</td>
<td>In-Circuit debug data output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN</td>
<td>ST</td>
<td>In-Circuit debug data input</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **OUT** - Output, **IN** - Input, **ANA** - Analog Signal, **DIG** - Digital Output, **OD** - Open Drain Output, **ST** - Schmitt Buffer Input, **TTL** - TTL Buffer Input, **XTAL** - Crystal connection, **HV** - High Voltage

**Note 1:** Output priority number determines the precedence of data into the MUX when multiple outputs are available at the same time (1 - highest priority). This number affects drive data, but not drive enable. Items with same priority number are mutually exclusive.

**Note 2:** Pad module signal connections reflect only the module input signals. Output connections are addressed in the corresponding consumer module.
## Pad Name | Function | I/O Type | Priority (1) | Description
--- | --- | --- | --- | ---
**GPB5** | The GPB5 pad has basic port and peripheral features. The pad is an output only when configured so by the user. This pin is only available on the MCP19123. | OUT | CMOS | PORTGPB<5> data output
IN | TTL | PORTGPB<5> data input
**AN7** | IN | ANA | Channel 7 A/D input
**ICSPCLK** | IN | ST | Serial programming clock input
**ICDCLK** | IN | ST | In-Circuit debugger clock input

**GPB6** | The GPB6 pad has basic port and peripheral features. The pad is an output only when so configured by the user. This pin is only available on the MCP19123. | OUT | CMOS-2 | PORTGPB<6> data output
IN | TTL | PORTGPB<6> data input
**CCD2** | OUT | CMOS-1 | CCD2 output
IN | ST | CCD2 input

**GPB7** | The GPB7 pad has basic port and peripheral features. The pad is an output only when so configured by the user. This pin is only available on the MCP19123. | OUT | CMOS-1 | PORTGPB<7> data output
IN | TTL | PORTGPB<7> data input
**VDAC** | IN | ANA | External ADC reference

Legend: OUT - Output, IN - Input, ANA - Analog Signal, DIG - Digital Output, OD - Open Drain Output, ST - Schmitt Buffer Input, TTL - TTL Buffer Input, XTAL - Crystal connection, HV - High Voltage

**Note 1:** Output priority number determines the precedence of data into the MUX when multiple outputs are available at the same time (1 - highest priority). This number affects drive data, but not drive enable. Items with same priority number are mutually exclusive.

**Note 2:** Pad module signal connections reflect only the module input signals. Output connections are addressed in the corresponding consumer module.
**REGISTER 17-5: PORTGPB: PORTGPB REGISTER**

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>GPB&lt;7:0&gt;: General Purpose I/O Pin bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 = Port pin is &gt; VIH</td>
</tr>
<tr>
<td></td>
<td>0 = Port pin is &lt; VIL</td>
</tr>
</tbody>
</table>

**Note 1:** Not implemented on MCP19122.

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>TRISB&lt;7:0&gt;: PORTGPB Tri-State Control bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 = PORTGPB pin configured as an input (tri-stated)</td>
</tr>
<tr>
<td></td>
<td>0 = PORTGPB pin configured as an output</td>
</tr>
</tbody>
</table>

**Legend:**
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set   ‘0’ = Bit is cleared  x = Bit is unknown

---

**REGISTER 17-6: TRISGPB: PORTGPB TRI-STATE REGISTER**

<table>
<thead>
<tr>
<th>Bit 7-0</th>
<th>TRISB&lt;7:0&gt;: PORTGPB Tri-State Control bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 = PORTGPB pin configured as an input (tri-stated)</td>
</tr>
<tr>
<td></td>
<td>0 = PORTGPB pin configured as an output</td>
</tr>
</tbody>
</table>

**Legend:**
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set   ‘0’ = Bit is cleared  x = Bit is unknown
REGISTER 17-7: WPUGPB: WEAK PULL-UP PORTGPB REGISTER

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>WPUB7(2)</td>
<td>WPUB6(2)</td>
<td>WPUB5(2)</td>
<td>WPUB4(2)</td>
<td>WPUB3</td>
<td>WPUB2</td>
<td>WPUB1</td>
<td>—</td>
</tr>
</tbody>
</table>

bit 7

Legend:
R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’

-n = Value at POR  
‘1’ = Bit is set  
‘0’ = Bit is cleared  
x = Bit is unknown

bit 7-3  
WPUB<7:3>: Weak Pull-up Register bit

1 = Pull-up enabled
0 = Pull-up disabled

bit 2-1  
WPUB<2:1>: Weak Pull-up Register bit

1 = Pull-up enabled
0 = Pull-up disabled

bit 0  
Unimplemented: Read as ‘0’

Note 1: The weak pull-up device is enabled only when the global RAPU bit is enabled, the pin is in Input mode (TRISGPA = 1), the individual WPUB bit is enabled (WPUB = 1), and the pin is not configured as an analog input.

REGISTER 17-8: ANSELB: ANALOG SELECT PORTGPB REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>U-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>ANSB5(2)</td>
<td>ANSB4(2)</td>
<td>—</td>
<td>ANSB2</td>
<td>ANSB1</td>
<td>—</td>
</tr>
</tbody>
</table>

bit 7

Legend:
R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’

-n = Value at POR  
‘1’ = Bit is set  
‘0’ = Bit is cleared  
x = Bit is unknown

bit 7-6  
Unimplemented: Read as ‘0’

bit 5-4  
ANSB<5:4>: Analog Select PORTGPB Register bit

1 = Analog input. Pin is assigned as analog input(1)
0 = Digital I/O. Pin is assigned to port or special function.

bit 3  
Unimplemented: Read as ‘0’

bit 2-1  
ANSB<2:1>: Analog Select PORTGPB Register bit

1 = Analog input. Pin is assigned as analog input(1)
0 = Digital I/O. Pin is assigned to port or special function.

bit 0  
Unimplemented: Read as ‘0’

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

2: Not implemented on MCP19122.
### TABLE 17-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTGPB

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSELB</td>
<td>—</td>
<td>—</td>
<td>ANSB5</td>
<td>ANSB4</td>
<td>—</td>
<td>ANSB2</td>
<td>ANSB1</td>
<td>—</td>
<td>126</td>
</tr>
<tr>
<td>OPTION_REG</td>
<td>RAPU</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
<td>83</td>
</tr>
<tr>
<td>IOC8</td>
<td>IOCB7</td>
<td>IOCB6</td>
<td>IOCB5</td>
<td>IOCB4</td>
<td>IOCB3</td>
<td>IOCB2</td>
<td>IOCB1</td>
<td>IOCB0</td>
<td>130</td>
</tr>
<tr>
<td>PORTGPB</td>
<td>GPB7</td>
<td>GPB6</td>
<td>GPB5</td>
<td>GPB4</td>
<td>GPB3</td>
<td>GPB2</td>
<td>GPB1</td>
<td>GPB0</td>
<td>125</td>
</tr>
<tr>
<td>TRISGPB</td>
<td>TRISB7</td>
<td>TRISB6</td>
<td>TRISB5</td>
<td>TRISB4</td>
<td>TRISB3</td>
<td>TRISB2</td>
<td>TRISB1</td>
<td>TRISB0</td>
<td>125</td>
</tr>
<tr>
<td>WPUGPB</td>
<td>WPUB7</td>
<td>WPUB6</td>
<td>WPUB5</td>
<td>WPUB4</td>
<td>WPUB3</td>
<td>WPUB2</td>
<td>WPUB1</td>
<td>—</td>
<td>126</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented locations read as ‘0’. Shaded cells are not used by PORTGPB.
18.0 INTERRUPT-ON-CHANGE

Each PORTGPA and PORTGPB pin is individually configurable as an interrupt-on-change pin. Control bits IOCA and IOCB enable or disable the interrupt function for each pin. Refer to Register 18-1 and Register 18-2. The interrupt-on-change is disabled on a Power-on Reset.

The interrupt-on-change on GPA5 is disabled when configured as MCLR pin in the Configuration Word.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTGPA or PORTGPB. The mismatched outputs of the last read of all the PORTGPA and PORTGPB pins are OR'ed together to set the Interrupt-on-Change Interrupt Flag bit (IOCF) in the INTCON register.

18.1 Enabling the Module

To allow individual port pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

18.2 Individual Pin Configuration

To enable a pin to detect an interrupt-on-change, the associated IOCAx or IOCBx bit of the IOCA or IOCB register is set.

18.3 Clearing Interrupt Flags

The user, in the Interrupt Service Routine, clears the interrupt by:

a) Any read of PORTGPA or PORTGPB AND Clear flag bit IOCF. This will end the mismatch condition;

OR

b) Any write of PORTGPA or PORTGPB AND Clear flag bit IOCF will end the mismatch condition.

A mismatch condition will continue to set flag bit IOCF. Reading PORTGPA or PORTGPB will end the mismatch condition and allow flag bit IOCF to be cleared. The latch holding the last read value is not affected by a MCLR Reset. After this Reset, the IOCF flag will continue to be set if a mismatch is present.

Note: If a change on the I/O pin should occur when any PORTGPA or PORTGPB operation is being executed, then the IOCF interrupt flag may not get set.

18.4 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCE bit is set.
18.5 Interrupt-On-Change Registers

REGISTER 18-1: IOCA: INTERRUPT-ON-CHANGE PORTGPA REGISTER

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOCA7</td>
<td>IOCA6</td>
<td>IOCA5</td>
<td>IOCA4</td>
<td>IOCA3</td>
<td>IOCA2</td>
<td>IOCA1</td>
<td>IOCA0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
-n = Value at POR  '1' = Bit is set  '0' = Bit is cleared  x = Bit is unknown

bit 7-6  \(\text{IOCA<7:6>}:\) Interrupt-on-Change PORTGPA Register bits.
1 = Interrupt-on-change enabled on the pin
0 = Interrupt-on-change disabled on the pin

bit 5  \(\text{IOCA<5>}:\) Interrupt-on-Change PORTGPA Register bits\(^{(1)}\).
1 = Interrupt-on-change enabled on the pin
0 = Interrupt-on-change disabled on the pin

bit 4-0  \(\text{IOCA<4:0>}:\) Interrupt-on-Change PORTGPA Register bits.
1 = Interrupt-on-change enabled on the pin
0 = Interrupt-on-change disabled on the pin

Note 1: The Interrupt-on-change on GPA5 is disabled if GPA5 is configured as MCLR.

REGISTER 18-2: IOCB: INTERRUPT-ON-CHANGE PORTGPB REGISTER

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOCB7(^{(1)})</td>
<td>IOCB6(^{(1)})</td>
<td>IOCB5(^{(1)})</td>
<td>IOCB4(^{(1)})</td>
<td>IOCB3</td>
<td>IOCB2</td>
<td>IOCB1</td>
<td>IOCB0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
-n = Value at POR  '1' = Bit is set  '0' = Bit is cleared  x = Bit is unknown

bit 7-0  \(\text{IOCB<7:0>}:\) Interrupt-on-Change PORTGPB Register bits.
1 = Interrupt-on-change enabled on the pin
0 = Interrupt-on-change disabled on the pin

Note 1: Not implemented on MCP19122.
### TABLE 18-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPT-ON-CHANGE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSELA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ANSA3</td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
<td>120</td>
</tr>
<tr>
<td>ANSELB</td>
<td>—</td>
<td>—</td>
<td>ANSB5</td>
<td>ANSB4</td>
<td>—</td>
<td>ANSB2</td>
<td>ANSB1</td>
<td>—</td>
<td>126</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>IOCE</td>
<td>T0IF</td>
<td>INTF</td>
<td>IOCF</td>
<td>102</td>
</tr>
<tr>
<td>IOCA</td>
<td>IOCA7</td>
<td>IOCA6</td>
<td>IOCA5</td>
<td>IOCA4</td>
<td>IOCA3</td>
<td>IOCA2</td>
<td>IOCA1</td>
<td>IOCA0</td>
<td>130</td>
</tr>
<tr>
<td>IOCB</td>
<td>IOCB7</td>
<td>IOCB6</td>
<td>IOCB5</td>
<td>IOCB4</td>
<td>IOCB3</td>
<td>IOCB2</td>
<td>IOCB1</td>
<td>IOCB0</td>
<td>130</td>
</tr>
<tr>
<td>TRISGPA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td>119</td>
</tr>
<tr>
<td>TRISGPB</td>
<td>TRISB7</td>
<td>TRISB6</td>
<td>TRISB5</td>
<td>TRISB4</td>
<td>TRISB3</td>
<td>TRISB2</td>
<td>TRISB1</td>
<td>TRISB0</td>
<td>125</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented locations read as ‘0’. Shaded cells are not used by interrupt-on-change.
19.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESH:ADRESL register pair). Figure 19-1 shows the block diagram of the ADC.

On the MCP19122/3 devices the 4.096V AVDD or 5V VDD can be used for the ADC reference. On the MCP19123 device an external reference can be used by selecting the ADREF pin as the ADC voltage reference source. The ADCON1<ACFG> bit controls the ADC reference source.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

Note: Once VIN is greater than AVDD + VDROPOUT, AVDD is in regulation, allowing A/D readings to be accurate. Once VIN is greater than VDD + VDROPOUT, VDD is in regulation. Setting the ADC reference to VDD allows accurate ratiometric measurements.
FIGURE 19-1: ADC BLOCK DIAGRAM
19.1 ADC Configuration

When configuring and using the ADC, the following functions must be considered:
• Port configuration
• Channel selection
• ADC conversion clock source
• Interrupt control
• Result formatting

19.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. Refer to Section 17.0 “I/O Ports” for more information.

19.1.2 CHANNEL SELECTION

There are up to 30 channel selections available on the MCP19122 and 32 channel selections available on the MCP19123. See Figure 19-1 and Register 19-1 for channel information.

The CHS<4:0> bits of the ADCON0 register determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to Section 19.2 “ADC Operation” for more information.

19.1.3 ADC CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ADCON1 register. There are five possible clock options:
• F OSC/8
• F OSC/16
• F OSC/32
• F OSC/64
• F RC (clock derived from internal oscillator with a divisor of 16)

The time to complete one bit conversion is defined as TAD. One full 10-bit conversion requires 11 TAD periods as shown in Figure 19-2.

For a correct conversion, the appropriate TAD specification must be met. Refer to the A/D conversion requirements in Section 5.0 “Digital Electrical Characteristics” for more information. Table 19-1 gives examples of appropriate ADC clock selections.

Note: Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

Note: Unless using the F RC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

TABLE 19-1: ADC CLOCK PERIOD (TAD) VS. DEVICE OPERATING FREQUENCIES

<table>
<thead>
<tr>
<th>ADC Clock Period (TAD)</th>
<th>Device Frequency (F OSC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC Clock Source</td>
<td>ADCS&lt;2:0&gt;</td>
</tr>
<tr>
<td>F OSC/8</td>
<td>001</td>
</tr>
<tr>
<td>F OSC/16</td>
<td>101</td>
</tr>
<tr>
<td>F OSC/32</td>
<td>010</td>
</tr>
<tr>
<td>F OSC/64</td>
<td>110</td>
</tr>
<tr>
<td>F RC</td>
<td>x11</td>
</tr>
</tbody>
</table>

Legend: Shaded cells are outside of recommended range.

Note 1: The F RC source has a typical TAD time of 4 µs for V DD > 3.0V.
2: These values violate the minimum required TAD time.
3: For faster conversion times, the selection of another clock source is recommended.
4: The F RC clock source is only recommended if the conversion will be performed during Sleep.
19.1.4 INTERRUPTS
The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC Interrupt Flag is the ADIF bit in the PIR1 register. The ADC Interrupt Enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

Note 1: The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.

This interrupt can be generated while the device is operating, or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the GIE and PEIE bits of the INTCON register must be disabled. If the GIE and PEIE bits of the INTCON register are enabled, execution will switch to the Interrupt Service Routine.

19.1.5 RESULT FORMATTING
The 10-bit A/D conversion result can be supplied in two formats, left justified or right justified. The ADFM bit of the ADCON0 register controls the output format. Figure 19-3 shows the output format.
19.2 ADC Operation

19.2.1 STARTING A CONVERSION
To enable the ADC module, the ADON bit of the ADCON0 register must be set to a ‘1’. Setting the GO/DONE bit of the ADCON0 register to a ‘1’ will start the Analog-to-Digital conversion.

Note: The GO/DONE bit should not be set in the same instruction that turns on the ADC. Refer to Section 19.2.4 “A/D Conversion Procedure”.

19.2.2 COMPLETION OF A CONVERSION
When the conversion is complete, the ADC module will:
• Clear the GO/DONE bit
• Set the ADIF Interrupt Flag bit
• Update the ADRESH:ADRESL registers with new conversion result

19.2.3 TERMINATING A CONVERSION
If a conversion must be terminated before completion, the GO/DONE bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete Analog-to-Digital conversion sample. Instead, the ADRESH:ADRESL register pair will retain the value of the previous conversion. Additionally, a two TAD delay is required before another acquisition can be initiated. Following the delay, an input acquisition is automatically started on the selected channel.

Note: A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

19.2.4 A/D CONVERSION PROCEDURE
This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
   • Disable pin output driver (Refer to the TRIS register)
   • Configure pin as analog (Refer to the ANSEL register)

2. Configure the ADC module:
   • Select ADC conversion clock
   • Select ADC input channel
   • Turn on ADC module

3. Configure ADC interrupt (optional):
   • Clear ADC interrupt flag
   • Enable ADC interrupt
   • Enable peripheral interrupt
   • Enable global interrupt(1)

4. Wait the required acquisition time(2).
5. Start conversion by setting the GO/DONE bit.
6. Wait for ADC conversion to complete by one of the following:
   • Polling the GO/DONE bit
   • Waiting for the ADC interrupt (interrupts enabled)

7. Read ADC Result.
8. Clear the ADC interrupt flag (required if interrupt is enabled).

Note 1: The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

2: Refer to Section 19.4 “A/D Acquisition Requirements”.

EXAMPLE 19-1: A/D CONVERSION

;This code block configures the ADC for polling, Frc clock and AN0 input.
;Conversion start & polling for completion are included.
BANKSEL ADCON1
MOVLW B'01110000' ;Frc clock
MOVWF ADCON1
BANKSEL TRISGPA
BSF TRISGPA,0 ;Set GPA0 to input
BANKSEL ANSELA
BSF ANSELA,0 ;Set GPA0 to analog
BANKSEL ADCON0
MOVLW B'01000001' ;Select channel AN0
MOVWF ADCON0 ;Turn ADC On
CALL SampleTime ;Acquisition delay
BSF ADCON0,1 ;Start conversion
BTFSC ADCON0,1 ;Is conversion done?
GOTO §-1 ;No, test again
BANKSEL ADRESH
MOVF ADRESH,W ;Read upper 2 bits
MOVWF RESULTHI ;Store in GPR space
BANKSEL ADRESL
MOVF ADRESL,W ;Read lower 8 bits
MOVWF RESULTLO ;Store in GPR space

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MCP19122/3
## 19.3 ADC Register Definitions

### REGISTER 19-1: ADCON0: A/D CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHS5</td>
<td>CHS4</td>
<td>CHS3</td>
<td>CHS2</td>
<td>CHS1</td>
<td>CHS0</td>
<td>GO/DONE</td>
<td>ADON</td>
</tr>
</tbody>
</table>

### Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
  - ‘1’ = Bit is set
  - ‘0’ = Bit is cleared
  - x = Bit is unknown

### Bit 7-2

**CHS<5:0>: Analog Channel Select bits**

- 000000 = GPA0
- 000001 = GPA1
- 000010 = GPA2
- 000011 = GPA3
- 000100 = GPB1
- 000101 = GPB2
- 000110 = GPB4\(^{(1)}\)
- 000111 = GPB5\(^{(1)}\)
- 001000 = RELEFF (see Section 3.11.6 “Relative Efficiency Ramp Measurement Control”)
- 001001 = Ratio of input voltage (\(V_{IN}/16\))
- 001010 = Output voltage measured after differential amplifier
- 001011 = \(V_{REF\_REG}\)
- 001100 = Error amplifier output
- 001101 = Average current after Sample & Hold and gain trim
- 001110 = \(I_{SENSE}\) signal after gain and slope compensation signal
- 001111 = Average output current with +6dB gain added
- 010000 = Internal temperature sensor
- 010001 = Band gap voltage reference
- 010010 = \(V_{REF\_REP}\): Center of the two \(V_{OUT}\) floating references
- 010100 = Output under voltage comparator reference
- 010101 = Input under voltage comparator reference
- 010110 = Input over voltage comparator reference
- 010111 = Over current reference
- 011000 = Master’s current sense signal input (measured on Slave unit)
- 011001 = \(V_{BG\_REP}\): DAC reference voltage amplifier output
- 011010 = GPA3 Buffered
- 011100 = Internal virtual ground (~500mV)
- 011101 = RAWS after Sample & Hold and added gain, but before slope is added
- 011110 = E/A output after the clamp, input to the PWM comparator
- 011110 = Raw \(I_{SENSE}\) (input to Sample & Hold)
- 011111 = Error Amplifier clamp reference level shifted by 500mV

\* 111111 = Unimplemented

### Bit 1

**GO/DONE: A/D Conversion Status bit**

- 1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
- 0 = A/D conversion completed/not in progress

### Bit 0

**ADON: ADC Enable bit**

- 1 = ADC is enabled
- 0 = ADC is disabled and consumes no operating current

**Note 1:** Not implemented on MCP19122.
### REGISTER 19-2: ADCON1: A/D CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6-4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>ADCS&lt;2:0&gt;</td>
<td>-</td>
<td>ADFM</td>
<td>VCFG&lt;1:0&gt;</td>
</tr>
<tr>
<td>Unimplemented: Read as ‘0’</td>
<td>A/D Conversion Clock Select bits</td>
<td>Unimplemented: Read as ‘0’</td>
<td>A/D Result Format Select</td>
<td>A/D Voltage Reference bit</td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 6-4</td>
<td>bit 3</td>
<td>bit 2</td>
<td>bit 1-0</td>
</tr>
<tr>
<td>Unimplemented: Read as ‘0’</td>
<td>ADCS&lt;2:0&gt;</td>
<td>Unimplemented: Read as ‘0’</td>
<td>ADFM: A/D Result Format Select</td>
<td>VCFG&lt;1:0&gt;</td>
</tr>
<tr>
<td>-</td>
<td>000 = Reserved</td>
<td>-</td>
<td>1 = Right justified</td>
<td>11 = ADREF pin</td>
</tr>
<tr>
<td>-</td>
<td>001 = FOSC/8</td>
<td>-</td>
<td>0 = Left justified</td>
<td>10 = ADREF pin</td>
</tr>
<tr>
<td>-</td>
<td>010 = FOSC/32</td>
<td>-</td>
<td></td>
<td>01 = Internal Vdd Reference</td>
</tr>
<tr>
<td>-</td>
<td>x11 = FRC (clock derived from internal oscillator with a divisor of 16)</td>
<td>-</td>
<td></td>
<td>00 = Internal A/D Reference</td>
</tr>
<tr>
<td>-</td>
<td>100 = Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>-</td>
<td>101 = FOSC/16</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>-</td>
<td>110 = FOSC/64</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **P** = Programmable bit
- **U** = Unimplemented bit, read as ‘0’
- -\(n\) = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- \(x\) = Bit is unknown
**REGISTER 19-3: ADRESH: ADC RESULT REGISTER HIGH (ADRESH)**

<table>
<thead>
<tr>
<th></th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R-x</th>
<th>R-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7-2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ADRES9</td>
<td>ADRES8</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

bit 7-2  
**Unimplemented**: Read as ‘0’

bit 1-0  
**ADRES<9:8>: Most Significant A/D Results**

**Note 1**: Only for ADFM = 1.

**REGISTER 19-4: ADRESL: ADC RESULT REGISTER LOW (ADRESL)**

<table>
<thead>
<tr>
<th></th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
<th>R-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7-0</td>
<td>ADRES7</td>
<td>ADRES6</td>
<td>ADRES5</td>
<td>ADRES4</td>
<td>ADRES3</td>
<td>ADRES2</td>
<td>ADRES1</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

bit 7-0  
**ADRES<7:0>: Least Significant A/D results**

**Note 1**: Only for ADFM = 1.
19.4 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor \( C_{\text{HOLD}} \) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 19-4. The source impedance \( R_S \) and the internal sampling switch \( R_{SS} \) impedance directly affect the time required to charge the capacitor \( C_{\text{HOLD}} \). The sampling switch \( R_{SS} \) impedance varies over the device voltage \( V_{DD} \), refer to Figure 19-4.

The maximum recommended impedance for analog sources is 10 kΩ. As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 19-1 may be used. This equation assumes that 1/2 LSB error is used (1,024 steps for the ADC). The 1/2 LSB error is the maximum error allowed for the ADC to meet its specified resolution.

### EQUATION 19-1: ACQUISITION TIME EXAMPLE

**Assumptions:**
- Temperature = +50°C and external impedance of 10 kΩ 5.0V \( V_{DD} \)
- \( T_{ACQ} = \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \)
- \( T_{ACQ} = T_{AMP} + T_C + T_{COFF} \)
- \( = 2 \mu s + T_C + [(\text{Temperature} - 25^\circ\text{C})(0.05 \mu s/\circ\text{C})] \)

The value for \( T_C \) can be approximated with the following equations:

\[
V_{\text{APPLIED}} \left(1 - \frac{1}{\left(2^n + 1\right)}\right) = V_{\text{CHOLD}} \quad ;[1] \quad V_{\text{CHOLD}} \text{ charged to within 1/2 lsb}
\]

\[
V_{\text{APPLIED}} \left(1 - e^{-\frac{T_C}{R_C}}\right) = V_{\text{CHOLD}} \quad ;[2] \quad V_{\text{CHOLD}} \text{ charge response to } V_{\text{APPLIED}}
\]

\[
V_{\text{APPLIED}} \left(1 - e^{-\frac{T_C}{R_C}}\right) = V_{\text{APPLIED}} \left(1 - \frac{1}{\left(2^n + 1\right)}\right) \quad ;\text{combining [1] and [2]}
\]

**Note:** Where \( n = \text{number of bits of the ADC} \).

Solving for \( T_C \):

\[
T_C = -C_{\text{HOLD}}(R_{IC} + R_{SS} + R_S) \ln(1/2047)
\]

\[
= -10 \text{pF}(1 \text{kΩ} + 7 \text{kΩ} + 10 \text{kΩ}) \ln(0.0004885)
\]

\[
= 1.37 \mu s
\]

Therefore:

\[
T_{ACQ} = 2 \mu s + 1.37 \mu s + [(50^\circ\text{C} - 25^\circ\text{C})(0.05 \mu s/\circ\text{C})]
\]

\[
= 4.67 \mu s
\]

**Note 1:** The charge holding capacitor \( C_{\text{HOLD}} \) is not discharged after each conversion.

**Note 2:** The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.
FIGURE 19-4: ANALOG INPUT MODEL

Legend:
- \( C_{\text{HOLD}} \): Sample/hold capacitance
- \( C_{\text{PIN}} \): Input capacitance
- \( I_{\text{LEAKAGE}} \): Leakage current at the pin due to various junctions
- \( R_{\text{IC}} \): Interconnect resistance
- \( R_{\text{SS}} \): Resistance of sampling switch
- \( \text{SS} \): Sampling switch
- \( V_T \): Threshold voltage
- \( V_I \): Input pin

Note 1: Refer to Section 5.0 “Digital Electrical Characteristics”.

FIGURE 19-5: ADC TRANSFER FUNCTION

Legend:
- \( 0.5 \text{ LSB} \): Half scale transition
- \( 1.5 \text{ LSB} \): Full scale transition
- \( V_{\text{REF}^-} \): Reference negative
- \( V_{\text{REF}^+} \): Reference positive
- \( V_T \): Threshold voltage
- \( V_{\text{DD}} \): Supply voltage
- \( R_{\text{SS}} \): Sampling switch resistance
- \( V_{\text{SS}} \): Ground
- \( V_{\text{OUT}} \): ADC output code

Legend:
- \( 0 \text{ to } 7 \): Codes for zero scale
- \( 8 \text{ to } F \): Codes for one scale
- \( 10 \text{ to } 15 \): Codes for full scale
### TABLE 19-2: SUMMARY OF REGISTERS ASSOCIATED WITH ADC

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADCON0</td>
<td>—</td>
<td>CHS4</td>
<td>CHS3</td>
<td>CHS2</td>
<td>CHS1</td>
<td>CHS0</td>
<td>GO/DONE</td>
<td>ADON</td>
<td>138</td>
</tr>
<tr>
<td>ADCON1</td>
<td>—</td>
<td>ADCS2</td>
<td>ADCS1</td>
<td>ADCS0</td>
<td>—</td>
<td>ADFM</td>
<td>VCFG1</td>
<td>VCFG0</td>
<td>139</td>
</tr>
<tr>
<td>ADRESH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>139</td>
</tr>
<tr>
<td>ADCONL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ADRES9</td>
<td>ADRES8</td>
<td>140</td>
</tr>
<tr>
<td>ADRESH</td>
<td>ADRES7</td>
<td>ADRES6</td>
<td>ADRES5</td>
<td>ADRES4</td>
<td>ADRES3</td>
<td>ADRES2</td>
<td>ADRES1</td>
<td>ADRES0</td>
<td>140</td>
</tr>
<tr>
<td>ANSELA</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ANSA3</td>
<td>ANSA2</td>
<td>ANSA1</td>
<td>ANSA0</td>
</tr>
<tr>
<td>ANSELB</td>
<td>—</td>
<td>—</td>
<td>ANSB5</td>
<td>ANSB4</td>
<td>—</td>
<td>ANSB2</td>
<td>ANSB1</td>
<td>—</td>
<td>126</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>IOCE</td>
<td>T0IF</td>
<td>INTF</td>
<td>IOCF</td>
<td>102</td>
</tr>
<tr>
<td>PIE1</td>
<td>—</td>
<td>ADIE</td>
<td>BCLIE</td>
<td>SSPIE</td>
<td>—</td>
<td>—</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>103</td>
</tr>
<tr>
<td>PIR1</td>
<td>—</td>
<td>ADIF</td>
<td>BCLIF</td>
<td>SSPIF</td>
<td>—</td>
<td>—</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>105</td>
</tr>
<tr>
<td>TRISGPA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td>119</td>
</tr>
<tr>
<td>TRISGPB</td>
<td>TRISB7</td>
<td>TRISB6</td>
<td>TRISB5</td>
<td>TRISB4</td>
<td>—</td>
<td>TRISB2</td>
<td>TRISB1</td>
<td>TRISB0</td>
<td>125</td>
</tr>
</tbody>
</table>

**Legend:** — = unimplemented read as "0". Shaded cells are not used for ADC module.
20.0  FLASH PROGRAM MEMORY CONTROL

The Flash program memory is readable and writable during normal operation (full \( V_{IN} \) range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers (see Registers 20-1 to 20-5). There are six SFRs used to read and write this memory:

- PMCON1
- PMCON2
- PMDATL
- PMDATH
- PMADRL
- PMADR

When interfacing the program memory block, the PMDATL and PMDATH registers form a two-byte word, which holds the 14-bit data for read/write, and the PMADRL and PMADR registers form a two-byte word, which holds the 13-bit address of the FLASH location being accessed. These devices have 4K words of program Flash with an address range from 0000h to 0FFFh.

The program memory allows single-word read and a by four word write. A four-word write automatically erases the row of the location and writes the new data (erase before write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the voltage range of the device for byte or word operations.

When the device is code protected, the CPU may continue to read and write the Flash program memory. Depending on the settings of the Flash Program Memory Enable (WRT<1:0>) bits, the device may or may not be able to write certain blocks of the program memory, however, reads of the program memory are allowed.

When the Flash Program Memory Code Protection (CP) bit is enabled, the program memory is code protected, and the device programmer (ICSP) cannot access data or program memory.

20.1  PMADR and PMADRL Registers

The PMADR and PMADRL registers can address up to a maximum of 4K words of program memory.

When selecting a program address value, the Most Significant Byte (MSB) of the address is written to the PMADR register and the Least Significant Byte (LSB) is written to the PMADRL register.

20.2  PMCON1 and PMCON2 Registers

PMCON1 is the control register for the data program memory accesses.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear.

The CALSEL bit allows the user to read locations in test memory in case there are calibration bits stored in the calibration word locations that need to be transferred to SFR trim registers. The CALSEL bit is only for reads, and if a write operation is attempted with CALSEL = 1, no write will occur.

PMCON2 is not a physical register. Reading PMCON2 will read all ’0’s. The PMCON2 register is used exclusively in the flash memory write sequence.
## 20.3 Flash Program Memory

### Control Registers

**REGISTER 20-1: PMDATL: PROGRAM MEMORY DATA LOW BYTE REGISTER**

<table>
<thead>
<tr>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **PMDATL<7:0>**

  **Legend:**
  - **R** = Readable bit
  - **W** = Writable bit
  - **U** = Unimplemented bit, read as ‘0’
  - **-n** = Value at POR
  - ‘1’ = Bit is set
  - ‘0’ = Bit is cleared
  - **x** = Bit is unknown

  **bit 7-0**
  - **PMDATL<7:0>: 8 Least Significant Data bits Read from Program Memory**

**REGISTER 20-2: PMADRL: PROGRAM MEMORY ADDRESS LOW BYTE REGISTER**

<table>
<thead>
<tr>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **PMADRL<7:0>**

  **Legend:**
  - **R** = Readable bit
  - **W** = Writable bit
  - **U** = Unimplemented bit, read as ‘0’
  - **-n** = Value at POR
  - ‘1’ = Bit is set
  - ‘0’ = Bit is cleared
  - **x** = Bit is unknown

  **bit 7-0**
  - **PMADRL<7:0>: 8 Least Significant Address bits for Program Memory Read/Write Operation**

**REGISTER 20-3: PMDATH: PROGRAM MEMORY DATA HIGH BYTE REGISTER**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **PMDATH<5:0>**

  **Legend:**
  - **R** = Readable bit
  - **W** = Writable bit
  - **U** = Unimplemented bit, read as ‘0’
  - **-n** = Value at POR
  - ‘1’ = Bit is set
  - ‘0’ = Bit is cleared
  - **x** = Bit is unknown

  **bit 7-6**
  - **Unimplemented: Read as ‘0’**

  **bit 5-0**
  - **PMDATH<5:0>: 6 Most Significant Data bits Read from Program Memory**
## REGISTER 20-4: PMADRH: PROGRAM MEMORY ADDRESS HIGH BYTE REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PMADRH&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

- **bit 7-4 Unimplemented:** Read as ‘0’
- **bit 3-0 PMADRH<3:0>:** Specifies the 4 Most Significant Address bits or High bits for Program Memory Reads.

## REGISTER 20-5: PMCON1: PROGRAM MEMORY CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/S-0</th>
<th>R/S-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CALSEL</td>
<td></td>
<td></td>
<td></td>
<td>WREN</td>
<td>WR</td>
<td>RD</td>
</tr>
</tbody>
</table>

**Legend:**
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

- **bit 7 Unimplemented:** Read as ‘0’
- **bit 6 CALSEL:** Program Memory calibration space select bit
  - 1 = Select test memory area for reads only, for loading calibration (excluding Configuration Word and Device ID)
  - 0 = Select user area for reads
- **bit 5-3 Unimplemented:** Read as ‘0’
- **bit 2 WREN:** Program Memory Write Enable bit
  - 1 = Allows write cycles
  - 0 = Inhibits write to the Flash Program Memory
- **bit 1 WR:** Write Control bit
  - 1 = Initiates a write cycle to program memory. (The bit is cleared by hardware when write is complete. The WR bit can only be set (not cleared) in software.)
  - 0 = Write cycle to the Flash memory is complete
- **bit 0 RD:** Read Control bit
  - 1 = Initiates a program memory read. (The read takes one cycle. The RD is cleared in hardware; the RD bit can only be set (not cleared) in software.)
  - 0 = Does not initiate a Flash memory read
20.3.1 READING THE FLASH PROGRAM MEMORY

To read a program memory location, the user must write two bytes of the address to the PMADRL and PMADRH registers, and then set control bit RD (PMCON1<0>). Once the read control bit is set, the program memory Flash controller will use the second instruction cycle after to read the data. This causes the second instruction immediately following the “BSF PMCON1,RD” instruction to be ignored. The data is available, in the very next cycle, in the PMDATL and PMDATH registers; it can be read as two bytes in the following instructions. PMDATL and PMDATH registers will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 20-1: FLASH PROGRAM READ

```
BANKSELPM_ADR; Change STATUS bits RP1:0 to select bank with PMADR
MOVLWMS_PROG_PM_ADDR;
MOVWFPMADR; MS Byte of Program Address to read
MOVLWLS_PROG_PM_ADDR;
MOVWFPMADR; LS Byte of Program Address to read
BANKSELPMCON1; Bank to containing PMCON1
BSF PMCON1, RD; EE Read

NOP ; First instruction after BSF PMCON1,RD executes normally

NOP ; Any instructions here are ignored as program memory is read in second cycle after BSF PMCON1,RD

BANKSELPMDATL; Bank to containing PMADRL
MOVFPMADTL, W; W = LS Byte of Program PMDATL
MOVFPMADTL, W; W = MS Byte of Program PMDATL
```

FIGURE 20-1: FLASH PROGRAM MEMORY READ CYCLE EXECUTION – NORMAL MODE

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash ADDR</td>
<td>PC</td>
<td>PC + 1</td>
<td>PMADRH,PMADR</td>
<td>PC + 3</td>
<td>PC + 4</td>
<td>PC + 5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flash DATA</td>
<td>INSTR (PC)</td>
<td>INSTR (PC + 1)</td>
<td>PMDATH,PMDATL</td>
<td>INSTR (PC + 3)</td>
<td>INSTR (PC + 4)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RD bit</td>
<td>Executed here</td>
<td>Executed here</td>
<td>BSF PMCON1,RD</td>
<td>Executed here</td>
<td>NOP</td>
<td>Executed here</td>
<td>NOP</td>
<td>INSTR (PC + 3)</td>
<td>Executed here</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| PMDA
| |
| PMDATL |
| Register |
| EERHLT |
20.3.2 WRITING TO THE FLASH PROGRAM MEMORY

A word of the Flash program memory may only be written to if the word is in an unprotected segment of memory, as defined in Section 11.1 “Configuration Bits” (bits WRT1:WRT0).

Flash program memory must be written in four-word blocks. See Figures 20-2 and 20-3 for more details. A block consists of four words with sequential addresses, with a lower boundary defined by an address, where PMADRL<1:0> = 00. All block writes to program memory are done as 16-word erase by four-word write operations. The write operation is edge-aligned and cannot occur across boundaries.

To write program data, the WREN bit must be set and the data must first be loaded into the buffer registers (see Figure 20-2). This is accomplished by first writing the destination address to PMADRL and PMADRH, and then writing the data to PMDATL and PMDATH. After the address and data have been set, then the following sequence of events must be executed:

1. Write 55h, then AAh, to PMCON2 (Flash programming sequence).
2. Set the WR control bit of the PMCON1 register.

All four buffer register locations should be written to with correct data. If less than four words are being written to in the block of four words, then a read from the program memory location(s) not being written to must be performed. This takes the data from the program memory location(s) not being written and loads it into the PMDATL and PMDATH registers. Then the sequence of events to transfer data to the buffer registers must be executed.

To transfer data from the buffer registers to the program memory, the PMADRL and PMADRH must point to the last location in the four-word block (PMADRL<1:0> = 11). Then the following sequence of events must be executed:

1. Write 55h, then AAh, to PMCON2 (Flash programming sequence).
2. Set control bit WR of the PMCON1 register to begin the write operation.

The user must follow the same specific sequence to initiate the write for each word in the program block, writing each program word in sequence (000, 001, 010, 011). When the write is performed on the last word (PMADRL<1:0> = 11), a block of 16 words is automatically erased and the content of the four-word buffer registers are written into the program memory.

After the “BSF PMCON1,WR” instruction, the processor requires two cycles to set up the erase/write operation. The user must place two NOP instructions after the WR bit is set. Since data is being written to buffer registers, the writing of the first three words of the block appears to occur immediately. The processor will halt internal operation for the typical 2ms to write to the memory only when the PMADRL<3:0> = xx11. The halt time will be 4ms typical if the part is also erasing which only occurs if the PMADRL<3:0> = 0011.

Refer to Figure 20-2 for a block diagram of the buffer registers and the control signals for test mode.

20.3.3 PROTECTION AGAINST SPURIOUS WRITE

There are conditions when the device should not write to the program memory. To protect against spurious writes, various mechanisms have been built in. On power-up, WREN is cleared. Also, the Power-up Timer (72 ms duration) prevents program memory writes.

The write initiate sequence, and the WREN bit, help prevent an accidental write during a power glitch or software malfunction.

20.3.4 OPERATION DURING CODE PROTECT

When the device is code protected, the CPU is able to read and write unscrambled data to the program memory. The test mode access is disabled.

20.3.5 OPERATION DURING WRITE PROTECT

When the program memory is write protected, the CPU can read and execute from the program memory. The portions of program memory that are write protected can not be modified by the CPU using the PMCON registers. The write protection has no effect in ICSP mode.

Note: The write protect bits are used to protect the users' program from modification by the user's code. They have no effect when programming is performed by ICSP. The code-protect bits, when programmed for code protection, will prevent the program memory from being written via the ICSP interface.

The user must follow the same specific sequence to initiate the write for each word in the program block, writing each program word in sequence (000, 001, 010, 011). When the write is performed on the last word (PMADRL<1:0> = 11), a block of 16 words is automatically erased and the content of the four-word buffer registers are written into the program memory.

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Note: The write protect bits are used to protect the users' program from modification by the user's code. They have no effect when programming is performed by ICSP. The code-protect bits, when programmed for code protection, will prevent the program memory from being written via the ICSP interface.
**FIGURE 20-2: BLOCK WRITES TO 4K FLASH PROGRAM MEMORY**

If at new row sixteen words of Flash are erased, then four buffers are transferred to Flash automatically after this word is written.

**FIGURE 20-3: FLASH PROGRAM MEMORY LONG WRITE CYCLE EXECUTION**

- Processor halted
- EE Write Time
- NOP
- INSTR (PC + 2)
21.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:
- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (shared with Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Interrupt on overflow

Figure 21-1 is a block diagram of the Timer0 module.

FIGURE 21-1: BLOCK DIAGRAM OF THE TIMER0

21.1 Timer0 Operation

The Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

21.1.1 8-BIT TIMER MODE

The Timer0 module will increment every instruction cycle, if used without a prescaler. 8-Bit Timer mode is selected by clearing the T0CS bit of the OPTION_REG register.

When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note: The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written.

21.1.2 8-BIT COUNTER MODE

In 8-Bit Counter mode, the Timer0 module will increment on every rising or falling edge of the T0CKI pin. The incrementing edge is determined by the T0SE bit of the OPTION_REG register.

8-Bit Counter mode using the T0CKI pin is selected by setting the T0CS bit in the OPTION_REG register to '1'.

21.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A single software programmable prescaler is available for use with either Timer0 or the Watchdog Timer (WDT), but not both simultaneously. The prescaler assignment is controlled by the PSA bit of the OPTION_REG register. To assign the prescaler to Timer0, the PSA bit must be cleared to '0'.

There are 8 prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION_REG register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be disabled by setting the PSA bit of the OPTION_REG register.

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the prescaler.
21.1.4 SWITCHING PRESCALER BETWEEN TIMER0 AND WDT MODULES

The prescaler is shared between the Timer0 and the WDT. As a result of having the prescaler assigned to either Timer0 or the WDT, it is possible to generate an unintended device Reset when switching prescaler values. When changing the prescaler assignment from Timer0 to the WDT module, the instruction sequence shown in Example 21-1 must be executed.

**EXAMPLE 21-1: CHANGING PRESCALER (TIMER0 → WDT)**

```assembly
BANKSELTMR0 ;
CLRWD ;Clear WDT
CLRFTMR0 ;Clear TRM0 and ;prescaler
BANKSELOPTION_REG;
BSF OPTION_REG,PSA;Select WDT
CLRWD ;
;MOVLRW11110000;Mask prescaler
ANDWF OPTION_REG,W;bits
IORLRW00000101;Set WDT prescaler
MOVWF OPTION_REG;to 1:32
```

When changing the prescaler assignment from the WDT to the Timer0 module, the following instruction sequence must be executed (see Example 21-2).

**EXAMPLE 21-2: CHANGING PRESCALER (WDT → TIMER0)**

```assembly
CLRWD ;Clear WDT and ;prescaler
BANKSELOPTON_REG ;
MOVL b'11110000' ;Mask TRM0 select and
ANDWF OPTION_REG,W ;prescaler bits
IORL b'00000011' ;Set prescale to 1:16
MOVF OPTION_REG ;
```

21.1.5 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The TOIF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The TOIF bit can only be cleared in software. The Timer0 interrupt enable is the T0IE bit of the INTCON register.

**Note:** The Timer0 interrupt cannot wake the processor from Sleep since the timer is frozen during Sleep.

21.1.6 USING TIMER0 WITH AN EXTERNAL CLOCK

When Timer0 is in Counter mode, the synchronization of the T0CKI input and the Timer0 register is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, the high and low periods of the external clock source must meet the timing requirements as shown in Section 5.0 “Digital Electrical Characteristics”.

21.1.7 OPERATION DURING SLEEP

Timer0 cannot operate while the processor is in Sleep mode. The contents of the TMR0 register will remain unchanged while the processor is in Sleep mode.

### TABLE 21-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>IOIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>IOCIF</td>
<td>102</td>
</tr>
<tr>
<td>OPTION_REG</td>
<td>RAUP</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
<td>83</td>
</tr>
<tr>
<td>TMR0</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISO</td>
<td>151*</td>
</tr>
<tr>
<td>TRISGPA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>TRISA4</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISO</td>
<td>119</td>
</tr>
</tbody>
</table>

**Legend:** — = Unimplemented locations, read as ‘0’. Shaded cells are not used by the Timer0 module.

*Page provides register information.*
22.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer with the following features:
- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Two selectable internal clock sources
- 2-bit prescaler
- Synchronous or asynchronous operation
- Multiple Timer1 gate (count enable) sources

• Interrupt on overflow
• Time base for the Capture/Compare function
• Special Event Trigger (with CCD)
• Selectable Gate Source Polarity
• Gate Toggle mode
• Gate Single-pulse mode
• Gate Value Status
• Gate Event Interrupt

Figure 22-1 is a block diagram of the Timer1 module.

Note 1: Timer1 register increments on rising edge.
22.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing timer, which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the timer. The module is a timer and increments on every instruction cycle.

Timer1 is enabled by configuring the TMR1ON and TMR1GE bits in the T1CON and T1GCON registers, respectively. Table 22-1 displays the Timer1 enable selections.

**TABLE 22-1: TIMER1 ENABLE SELECTIONS**

<table>
<thead>
<tr>
<th>TMR1ON</th>
<th>TMR1GE</th>
<th>Timer1 Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Off</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Off</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Always On</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Externally Enabled</td>
</tr>
</tbody>
</table>

22.2 Clock Source Selection

The TMR1CS bit of the T1CON register is used to select the clock source for Timer1. Table 22-2 displays the clock source selections.

**TABLE 22-2: CLOCK SOURCE SELECTIONS**

<table>
<thead>
<tr>
<th>TMR1CS</th>
<th>Clock Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>8 MHz System Clock (Fosc)</td>
</tr>
<tr>
<td>0</td>
<td>2 MHz Instruction Clock (Fosc/4)</td>
</tr>
</tbody>
</table>

22.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, the TMR1H:TMR1L register pair will increment on multiples of Fosc or Fosc/4 as determined by the Timer1 prescaler.

As an example, when the FOSC internal clock source is selected, the TIMER1 register value will increment by four counts every instruction clock cycle.

**Note:** In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge (see Figure 22-2) after any one or more of the following conditions:

- Timer1 enabled after POR Reset
- Write to TMR1H or TMR1L
- Timer1 is disabled
- Timer1 is disabled (TMR1ON = 0) when T1CKI is high then Timer1 is enabled (TMR1ON=1) when T1CKI is low.
22.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

22.4 Timer1 Gate

Timer1 can be configured to increment freely or the incrementing can be enabled and disabled using Timer1 gate circuitry. This is also referred to as Timer1 gate increment enable. Timer1 gate can also be driven by multiple selectable sources.

22.4.1 TIMER1 GATE INCREMENT ENABLE

The Timer1 gate is enabled by setting the TMR1GE bit of the T1GCON register. The polarity of the Timer1 gate is configured using the T1GPOL bit of the T1GCON register.

When Timer1 Gate (T1Gx) input is active, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 gate input is inactive, no incrementing will occur and Timer1 will hold the current count. See Figure 22-3 for timing details.

<table>
<thead>
<tr>
<th>T1GCLK</th>
<th>T1GCLK</th>
<th>T1Gx</th>
<th>Timer1 Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>↑</td>
<td>0</td>
<td>0</td>
<td>Increments</td>
</tr>
<tr>
<td>↑</td>
<td>0</td>
<td>1</td>
<td>Holds Count</td>
</tr>
<tr>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>Holds Count</td>
</tr>
<tr>
<td>↑</td>
<td>1</td>
<td>1</td>
<td>Increments</td>
</tr>
</tbody>
</table>

22.4.2 TIMER1 GATE SOURCE SELECTION

The Timer1 gate source can be selected from one of three different sources. Source selection is controlled by the T1GSS bits of the T1GCON register. The polarity for each available source is also selectable. Polarity selection is controlled by the T1GPO bit of the T1GCON register.

<table>
<thead>
<tr>
<th>T1GSS</th>
<th>Timer1 Gate Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>Output of UV Comparator</td>
</tr>
<tr>
<td>10</td>
<td>Timer1 Gate Pin T1G2</td>
</tr>
<tr>
<td>01</td>
<td>Overflow of Timer0 (TMR0 increments from FFh to 00h)</td>
</tr>
<tr>
<td>00</td>
<td>Timer1 Gate Pin T1G1</td>
</tr>
</tbody>
</table>

22.4.2.1 T1G1 Pin Gate Operation

The GPBA3/T1G1 pin is one source for Timer1 gate control. It can be used to supply an external source to the Timer1 gate circuitry.

22.4.2.2 Timer0 Overflow Gate Operation

When Timer0 increments from FFh to 00h, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 gate circuitry.

22.4.2.3 T1G2 Pin Gate Operation

The GPB2/T1G2 pin is one source for the Timer1 gate control. It can be used to supply an external source to the Timer1 gate circuitry.

22.4.2.4 UV Comparator Output

The output of the output under voltage comparator is one source for the Timer1 gate control. A low-to-high transition of the comparator output shall stop TIMER1.

22.4.3 TIMER1 GATE TOGGLE MODE

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal, as opposed to the duration of a single level pulse.

The Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. See Figure 22-4 for timing details.

Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When the T1GTM bit is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

Note: Enabling Toggle mode at the same time as changing the gate polarity may result in indeterminate operation.

22.4.4 TIMER1 GATE SINGLE-PULSE MODE

When Timer1 Gate Single-Pulse mode is enabled, it is possible to capture a single pulse gate event. Timer1 Gate Single-Pulse mode is first enabled by setting the T1GSPM bit in the T1GCON register. Next, the T1GGO/DONE bit in the T1GCON register must be set. The Timer1 will be fully enabled on the next incrementing edge. On the next trailing edge of the
In Compare mode, an event is triggered when the value CCxRH:CCxRL register pair matches the value in the TMR1H:TMR1L register pair. This event can be a Special Event Trigger.

For more information, see Section 24.0, Dual Capture/Compare (CCD) Module.

### 22.7 CCD Special Event Trigger

When the CCD is configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The CCD module may still be configured to generate a CCD interrupt.

In this mode of operation, the CCxRH:CCxRL register pair becomes the period register for Timer1.

Timer1 should be clocked by FOSC/4 to utilize the Special Event Trigger.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the CCD, the write will take precedence.

For more information, see Section 24.2.3, Special Event Trigger.

---

Note: The TMR1H:TMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.
FIGURE 22-2: TIMER1 INCREMENTING EDGE

Note 1: Arrows indicate counter increments.

FIGURE 22-3: TIMER1 GATE COUNT ENABLE MODE
FIGURE 22-4: TIMER1 GATE TOGGLE MODE

- **TMR1GE**
- **T1GPOL**
- **T1GTM**
- **T1G_IN**
- **T1CLK**
- **T1GVAL**
- **TIMER1**

FIGURE 22-5: TIMER1 GATE SINGLE-PULSE MODE

- **TMR1GE**
- **T1GPOL**
- **T1GSPM**
- **T1GGO/DONE**
  - Set by software
  - Cleared by hardware on falling edge of T1GVAL
- **T1G_IN**
- **T1CLK**
- **T1GVAL**
- **TIMER1**
- **TMR1GIF**
  - Cleared by software
  - Set by hardware on falling edge of T1GVAL
  - Cleared by software
FIGURE 22-6: TIMER1 GATE SINGLE-PULSE AND TOGGLE COMBINED MODE

<table>
<thead>
<tr>
<th>TMR1GE</th>
<th>Set by software</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1GPOLO</td>
<td>Cleared by hardware on falling edge of T1GVAL</td>
</tr>
<tr>
<td>T1GSPM</td>
<td>Counting enabled on rising edge of T1G</td>
</tr>
<tr>
<td>T1GTMO</td>
<td>Cleared by software</td>
</tr>
</tbody>
</table>

![Diagram of Timer1 GATE Single-Pulse and Toggle Combined Mode]

- **T1G_IN**: Input signal
- **T1CLK**: Clock signal
- **T1GVAL**: Value signal
- **TIMER1**: Timer value (N, N+1, N+2, N+3, N+4)
- **TMR1GIF**: Interrupt flag

Set by hardware on falling edge of T1GVAL
Cleared by software
### 22.8 Timer1 Control Registers

**REGISTER 22-1: T1CON: TIMER1 CONTROL REGISTER**

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5-4</th>
<th>Bit 3-2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>—</td>
<td>T1CKPS&lt;1:0&gt;</td>
<td>—</td>
<td>—</td>
<td>TMR1CS</td>
<td>TMR1ON</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

- **bit 7-6** Unimplemented: Read as ‘0’
- **bit 5-4** T1CKPS<1:0>: Timer1 Input Clock Prescale Select bits
  - 11 = 1:8 Prescale value
  - 10 = 1:4 Prescale value
  - 01 = 1:2 Prescale value
  - 00 = 1:1 Prescale value
- **bit 3-2** Unimplemented: Read as ‘0’
- **bit 1** TMR1CS: Timer1 Clock Source Select bits
  - 1 = Timer1 clock source is 8 MHz system clock (Fosc)
  - 0 = Timer1 clock source is 2 MHz instruction clock (Fosc/4)
- **bit 0** TMR1ON: Timer1 On bit
  - 1 = Enables Timer1
  - 0 = Stops Timer1
  - Clears Timer1 gate flip-flop
**REGISTER 22-2: T1GCON: TIMER1 GATE CONTROL REGISTER**

<table>
<thead>
<tr>
<th></th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R-x</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMR1GE</td>
<td>T1GPOL</td>
<td>T1GTM</td>
<td>T1GSPM</td>
<td>T1GGO/DONE</td>
<td>T1GVAL</td>
<td>T1GSS&lt;1:0&gt;</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**bit 7**  
**TMR1GE:** Timer1 Gate Enable bit
- If TMR1ON = 0:
  - This bit is ignored
- If TMR1ON = 1:
  - 1 = Timer1 incrementing is controlled by the Timer1 gate function
  - 0 = Timer1 increments regardless of Timer1 gate function

**bit 6**  
**T1GPOL:** Timer1 Gate Polarity bit
- 1 = Timer1 gate is active-high (Timer1 counts when gate is high)
- 0 = Timer1 gate is active-low (Timer1 counts when gate is low)

**bit 5**  
**T1GTM:** Timer1 Gate Toggle mode bit
- 1 = Timer1 Gate Toggle mode is enabled.
- 0 = Timer1 Gate Toggle mode is disabled and toggle flip-flop is cleared
- Timer1 gate flip-flop toggles on every rising edge.

**bit 4**  
**T1GSPM:** Timer1 Gate Single Pulse mode bit
- 1 = Timer1 Gate Single-Pulse mode is enabled and is controlling Timer1 gate
- 0 = Timer1 Gate Single-Pulse mode is disabled

**bit 3**  
**T1GGO/DONE:** Timer1 Gate Single-Pulse Acquisition Status bit
- 1 = Timer1 gate single-pulse acquisition is ready, waiting for an edge
- 0 = Timer1 gate single-pulse acquisition has completed or has not been started
- This bit is automatically cleared when T1GSPM is cleared.

**bit 2**  
**T1GVAL:** Timer1 Gate Current State bit
- Indicates the current state of the Timer1 gate that could be provided to TMR1H:TMR1L.
- Unaffected by Timer1 Gate Enable (TMR1GE).

**bit 1-0**  
**T1GSS<1:0>:** Timer1 Gate Source Select bits
- 11 = UV Comparator Output
- 10 = Timer1 gate pin T1G2
- 01 = Timer0 overflow output
- 00 = Timer1 gate pin T1G1
23.0 TIMER2 MODULE

The Timer2 module is an 8-bit timer with the following features:

- 8-bit timer register (TMR2)
- 8-bit period register (PR2)
- Interrupt on TMR2 match with PR2
- Software programmable prescaler (1:1, 1:4, 1:16)

See Figure 23-1 for a block diagram of Timer2.

23.1 Timer2 Operation

The clock input to the Timer2 module is the system clock (Fosc). The clock is fed into the Timer2 prescaler, which has prescale options of 1:1, 1:4 or 1:16. The output of the prescaler is then used to increment the TMR2 register.

The values of TMR2 and PR2 are constantly compared to determine when they match. TMR2 will increment from 00h until it matches the value in PR2. When a match occurs, TMR2 is reset to 00h on the next increment cycle.

The match output of the Timer2/PR2 comparator is used to set the TMR2IF interrupt flag bit in the PIR1 register.

The TMR2 and PR2 registers are both fully readable and writable. On any Reset, the TMR2 register is set to 00h and the PR2 register is set to FFh.

Timer2 is turned on by setting the TMR2ON bit in the T2CON register to a '1'. Timer2 is turned off by clearing the TMR2ON bit to a '0'.

The Timer2 prescaler is controlled by the T2CKPS bits in the T2CON register. The prescaler counter are cleared when:

- A write to TMR2 occurs.
- A write to T2CON occurs.
- Any device Reset occurs (Power-on Reset, MCLR Reset, Watchdog Timer Reset, or Brown-out Reset).

**Note:** TMR2 is not cleared when T2CON is written.
23.2 Timer2 Control Register

**REGISTER 23-1: T2CON: TIMER2 CONTROL REGISTER**

<table>
<thead>
<tr>
<th>Bit 7-3</th>
<th>Bit 2</th>
<th>Bit 1-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unimplemented: Read as '0'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMR2ON: Timer2 On bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 = Timer2 is on</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = Timer2 is off</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T2CKPS&lt;1:0&gt;: Timer2 Clock Prescale Select bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td>00 = Prescaler is 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>01 = Prescaler is 4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 = Prescaler is 8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11 = Prescaler is 16</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**TABLE 23-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2**

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>IOCE</td>
<td>T0IF</td>
<td>INTF</td>
<td>IOCF</td>
<td>102</td>
</tr>
<tr>
<td>PIE1</td>
<td>—</td>
<td>ADIE</td>
<td>BCLIIE</td>
<td>SSPIE</td>
<td>—</td>
<td>—</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>103</td>
</tr>
<tr>
<td>PIR1</td>
<td>—</td>
<td>ADIF</td>
<td>BCLIF</td>
<td>SSPIF</td>
<td>—</td>
<td>—</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>105</td>
</tr>
<tr>
<td>PR2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>163*</td>
</tr>
<tr>
<td>T2CON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TMR2ON</td>
<td>T2CKPS1</td>
<td>T2CKPS0</td>
</tr>
<tr>
<td>TMR2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>163*</td>
</tr>
</tbody>
</table>

**Legend:**

- = unimplemented read as '0'. Shaded cells are not used for Timer2 module.
* Page provides register information.
24.0 DUAL CAPTURE/COMPARE (CCD) MODULE

The Dual Capture/Compare module is a peripheral that allows the user to time and control different events. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. This module is only available in the MCP19123 device.

24.1 Capture Mode

Capture mode makes use of the 16-bit Timer1 resource. When an event occurs on the CCDx pin, the 16-bit CCxRH:CCxRL register pair captures and stores the 16-bit value of the TMR1H:TMR1L register pair, respectively. An event is defined as one of the following and is configured by the CCxM<3:0> bits of the CCDCON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCDxIF of the PIR2 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCxRH:CCxRL register pair is read, the old captured value is overwritten by the new captured value.

Figure 24-1 shows a simplified diagram of the Capture operation.

24.1.1 CCDX PIN CONFIGURATION

In Capture mode, the CCDx pin should be configured as an input by setting the associated TRIS control bit.

Note: If the CCDx pin is configured as an output, a write to the port can cause a capture condition.

FIGURE 24-1: CAPTURE MODE OPERATION BLOCK DIAGRAM

Example 24-1 demonstrates the code to perform this function.

24.1.2 SOFTWARE INTERRUPT MODE

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCDxIE interrupt enable bit of the PIE2 register clear to avoid false interrupts. Additionally, the user should clear the CCDxIF interrupt flag bit of the PIR2 register following any change in Operating mode.

Note: Clocking Timer1 from the system clock (Fosc) should not be used in Capture mode. In order for Capture mode to recognize the trigger event on the CCDx pin, Timer1 must be clocked from the instruction clock (Fosc/4).

24.1.3 CCP1 PRESCALER

There are four prescaler settings specified by the CCxM<3:0> bits of the CCDCON register. Whenever the CCDx module is turned off, or the CCDx module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCDCON register before changing the prescaler. Example 24-1 demonstrates the code to perform this function.

EXAMPLE 24-1: CHANGING BETWEEN CAPTURE PRESCALERS

BANKSEL CCDCON ;Set Bank bits to point to CCDCON
CLRF CCDCON ;Turn CCDx module off
MOVLW NEW_CAPT_PS ;Load the W reg with the new prescaler
MOVWF CCDCON ;move value and CCDx ON
MOVWF CCDCON ;Load CCDCON with this value

Note: Clocking Timer1 from the system clock (Fosc) should not be used in Capture mode. In order for Capture mode to recognize the trigger event on the CCDx pin, Timer1 must be clocked from the instruction clock (Fosc/4).
24.2 Compare Mode

Compare mode makes use of the 16-bit Timer1 resource. The 16-bit value of the CCxRH:CCxRL register pair is constantly compared against the 16-bit value of the TMR1H:TMR1L register pair. When a match occurs, one of the following events can occur:

- Toggle the CCDx output
- Set the CCDx output
- Clear the CCDx output
- Generate a Special Event Trigger
- Generate a Software Interrupt

The action on the pin is based on the value of the CCXM<3:0> control bits of the CCDCON register. At the same time, the interrupt flag CCDxIF bit is set.

All Compare modes can generate an interrupt. Figure 24-2 shows a simplified diagram of the Compare operation.

FIGURE 24-2: COMPARE MODE OPERATION BLOCK DIAGRAM

24.2.1 CCDx PIN CONFIGURATION

The user must configure the CCDx pin as an output by clearing the associated TRIS bit.

Note: Clearing the CCDCON register will force the CCDx compare output latch to the default low level. This is not the PORT I/O data latch.

24.2.2 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen (CCxM<3:0> = 1010), the CCD module does not assert control of the CCDx pin (see the CCP1CON register).

24.2.3 SPECIAL EVENT TRIGGER

When Special Event Trigger mode is chosen (CCxM<3:0> = 1011), the CCD module does the following:

- Starts an ADC conversion if ADC is enabled

The CCD module does not assert control of the CCDx pin in this mode.

The Special Event Trigger output of the CCDx occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCxRH, CCxRL register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. The Special Event Trigger output starts an A/D conversion (if the A/D module is enabled). This allows the CCxRH, CCxRL register pair to effectively provide a 16-bit programmable period register for Timer1.

TABLE 24-1: SPECIAL EVENT TRIGGER

<table>
<thead>
<tr>
<th>Device</th>
<th>CCD1/CCD2</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP19123</td>
<td>CCD1/CCD2</td>
</tr>
</tbody>
</table>

Note 1: The Special Event Trigger from the CCD module does not set interrupt flag bit TMR1IF of the PIR1 register.

24.2.4 COMPARE DURING SLEEP

The Compare mode is dependent upon the system clock (FOSC) for proper operation. Since FOSC is shut down during Sleep mode, the Compare mode will not function properly during Sleep.

Refer to A/D Section for more information.
### 24.3 CCP Control Registers

**REGISTER 24-1: CCDCON: DUAL CAPTURE/COMPARE CONTROL REGISTER**

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC2M3</td>
<td>CC2M2</td>
<td>CC2M1</td>
<td>CC2M0</td>
<td>CC1M3</td>
<td>CC1M2</td>
<td>CC1M1</td>
<td>CC1M0</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Reset
- **'1'** = Bit is set
- **'0'** = Bit is cleared

#### bit 7-4

**CC2M<3:0>: Capture/Compare Register Set 2 Mode Select bits**

- **00xx** = Capture/Compare off (resets module)
- **0100** = Capture mode: every falling edge
- **0101** = Capture mode: every rising edge
- **0110** = Capture mode: every 4th rising edge
- **0111** = Capture mode: every 16th rising edge
- **1000** = Compare mode: set output on match (CC2IF bit is set)
- **1001** = Compare mode: clear output on match (CC2IF bit is set)
- **1010** = Compare mode: toggle output on match (CC2IF bit is set)
- **1011** = Reserved
- **11xx** = Compare mode: generate software interrupt on match (CC2IF bit is set, CMP2 pin is unaffected and configured as an I/O port)
- **1111** = Compare mode: trigger special event (CC2IF bit is set; CCD2 does not rest TMR1 and starts an A/D conversion, if the A/D module is enabled. CMP2 pin is unaffected and configured as an I/O port).

#### bit 3-0

**CC1M<3:0>: Capture/Compare Register Set 1 Mode Select bits**

- **00xx** = Capture/Compare off (resets module)
- **0100** = Capture mode: every falling edge
- **0101** = Capture mode: every rising edge
- **0110** = Capture mode: every 4th rising edge
- **0111** = Capture mode: every 16th rising edge
- **1000** = Compare mode: set output on match (CC1IF bit is set)
- **1001** = Compare mode: clear output on match (CC1IF bit is set)
- **1010** = Compare mode: toggle output on match (CC1IF bit is set)
- **1011** = Reserved
- **11xx** = Compare mode: generate software interrupt on match (CC1IF bit is set, CMP1 pin is unaffected and configured as an I/O port)
- **1111** = Compare mode: trigger special event (CC1IF bit is set; CCD1 does not rest TMR1 and starts an A/D conversion, if the A/D module is enabled. CMP1 pin is unaffected and configured as an I/O port).

**Note:** When a Compare interrupt is set, the TMR1 is not reset. This is different than standard Microchip microcontroller operation.
25.0 INTERNAL TEMPERATURE INDICATOR MODULE

The MCP19122/3 is equipped with a temperature circuit designed to measure the operating temperature of the silicon die. The circuit's range of the operating temperature falls between –40°C and +125°C. The output is a voltage that is proportional to the device temperature. The output of the temperature indicator is internally connected to the device ADC.

25.1 Temperature Output

The output of the circuit is measured using the internal analog-to-digital converter. Channel 10 is reserved for the temperature circuit output. Refer to Section 19.0 “Analog-to-Digital Converter (ADC) Module” for detailed information.

The temperature of the silicon die can be calculated by the ADC measurement by using Equation 25-1.

**Equation 25-1: SILICON DIE TEMPERATURE**

\[
\text{TEMP}_\text{DIE} = \frac{\text{ADC READING} - 305}{3.08 mV/\degree C}
\]

The 10-bit ADC value located at memory address 2089h can be used to obtain a more accurate reading of the silicon die. This factory stored ADC value is obtained by measuring the silicon die temperature with an ambient temperature of 25°C (+/-5°C). Equation 25-2 shows how to use this stored value.

**Equation 25-2: USING CALWD 10 TO OBTAIN SILICON DIE TEMPERATURE**

\[
\text{TEMP}_\text{DIE} / \degree C = \left( \frac{\text{ADC READING (counts)} - \text{ADC25\degree C READING (counts)}}{3 \text{ (counts}/\degree C) + 25 \degree C} \right)
\]

---

**Figure 25-1: TEMPERATURE CIRCUIT DIAGRAM**

![Temperature Circuit Diagram](image)
26.0 ENHANCED PWM MODULE

The PWM module implemented on the MCP19122/3 is a modified version of the Capture/Compare/PWM (CCP) module found in standard mid-range microcontrollers. The module only features the PWM module, which is slightly modified from standard mid-range microcontrollers. In the MCP19122/3, the PWM module is used to generate the system clock or system oscillator. This system clock will control the MCP19122/3 switching frequency, as well as set the maximum allowable duty cycle. The PWM module does not continuously adjust the duty cycle to control the output voltage. This is accomplished by the analog control loop and associated circuitry.

26.1 Standard Pulse-Width Modulation (PWM) Mode

The PWM module output signal is used to set the operating switching frequency and maximum allowable duty cycle of the MCP19122/3. The actual duty cycle on the HDRV and LDRV is controlled by the analog PWM control loop. However, this duty cycle cannot be greater than the value in the PWMRL register.

There are two modes of operation that concern the system clock PWM signal. These modes are stand-alone (non-frequency synchronization) and frequency synchronization.

26.1.1 STAND-ALONE (NON-FREQUENCY SYNCHRONIZATION) MODE

When the MCP19122/3 is running stand-alone, the PWM signal functions as the system clock. It is operating at the programmed switching frequency with a programmed maximum duty cycle ($D_{CLOCK}$). The programmed maximum duty cycle is not adjusted on a cycle-by-cycle basis to control the MCP19122/3 system output. The required duty cycle ($D_{BUCK}$) to control the output is adjusted by the MCP19122/3 analog control loop and associated circuitry. $D_{CLOCK}$ does, however, set the maximum allowable $D_{BUCK}$.

**EQUATION 26-1:**

$$D_{BUCK} < 1 - D_{CLOCK}$$

26.1.2 SWITCHING FREQUENCY SYNCHRONIZATION MODE

The MCP19122/3 can be programmed to be a switching frequency MASTER or SLAVE device. The MASTER device functions as described in Section 26.1.1 “Stand-Alone (Non-Frequency Synchronization) Mode” with the exception of the 8 MHz system clock also being applied to GPB3 and the synchronization signal applied to GPA1.

A SLAVE device will receive the MASTER 8 MHz system clock on GPB3 and synchronization signal on GPA1. The synchronization signal will be ORed with the output of the TIMER2 module. This ORed signal will latch PWMRL into PWMRH and PWMPHL into PWMPHH.

Figure 26-1 shows a simplified block diagram of the CCP module in PWM mode.

The PWMPHL register allows for a phase shift to be added to the SLAVE system clock.

It is desired to have the MCP19122/3 SLAVE devices system clock start point shifted by a programmed amount from the MASTER system clock. This SLAVE phase shift is specified by writing to the PWMPHL register. The SLAVE phase shift can be calculated by using the following equation.

**EQUATION 26-2:**

$$SLAVE\ phase\ shift = PWMPHL \cdot T_{OSC} \cdot (T2\ prescale\ value)$$
A PWM output (Figure 26-2) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

**FIGURE 26-1: SIMPLIFIED PWM BLOCK DIAGRAM**

**FIGURE 26-2: PWM OUTPUT**

26.1.3 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following equation:

**EQUATION 26-3:**

\[
PWM\ Period = \left( \frac{(PR2)+1}{T_{OSC}} \right) \times T_{2\ PreScale\ Value}
\]

When TMR2 is equal to PR2, the following two events occur on the next increment cycle:

- TMR2 is cleared
- The PWM duty cycle is latched from PWMRL into PWMRH
26.1.4 PWM DUTY CYCLE (D\text{CLOCK})

The PWM duty cycle (D\text{CLOCK}) is specified by writing to the PWMRL register. Up to 8-bit resolution is available. The following equation is used to calculate the PWM duty cycle (D\text{CLOCK}):

\begin{equation}
\text{PWM DUTY CYCLE} = \text{PWMRL} \times T\text{OSC} \times (T2 \text{ PRESCALE VALUE})
\end{equation}

The PWMRL bits can be written to at any time, but the duty cycle value is not latched into PWMRH until after a match between PR2 and TMR2 occurs.

26.2 Operation during Sleep

When the device is placed in Sleep, the allocated timer will not increment and the state of the module will not change. If the CLKPIN pin is driving a value, it will continue to drive that value. When the device wakes up, it will continue from this state.

### TABLE 26-1: SUMMARY OF REGISTERS ASSOCIATED WITH PWM MODULE

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Register on Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>T2CON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TMR2ON</td>
<td>164</td>
</tr>
<tr>
<td>PR2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Timer2 Module Period Register</td>
<td>172*</td>
</tr>
<tr>
<td>PWMRL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PWM Register Low Byte</td>
<td>171*</td>
</tr>
<tr>
<td>PWMPHL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SLAVE Phase Shift Byte</td>
<td>171*</td>
</tr>
</tbody>
</table>

**Legend:** — = Unimplemented locations, read as ‘0’. Shaded cells are not used by Capture mode.

* Page provides register information.
27.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

27.1 MSSP Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module in the MCP19122/3 only operates in Inter-Integrated Circuit (I²C) mode.

The I²C interface supports the following modes and features:
- Master mode
- Slave mode
- Byte NACKing (Slave mode)
- Limited Multi-Master support
- 7-bit and 10-bit addressing
- Start and Stop interrupts
- Interrupt masking
- Clock stretching
- Bus collision detection
- General call address matching
- Dual Address masking
- Address Hold and Data Hold modes
- Selectable SDA hold times

Figure 27-1 is a block diagram of the I²C interface module in Master mode. Figure 27-2 is a diagram of the I²C interface module in Slave mode.
27.2 \( \text{I}^2\text{C} \) MODE OVERVIEW

The Inter-Integrated Circuit Bus (\( \text{I}^2\text{C} \)) is a multi-master serial data communication bus. Devices communicate in a master/slave environment, where the master devices initiate the communication. A Slave device is controlled through addressing.

The \( \text{I}^2\text{C} \) bus specifies two signal connections:

- Serial Clock (SCL)
- Serial Data (SDA)

Both the SCL and SDA connections are bidirectional open-drain lines, each requiring pull-up resistors for the supply voltage. Pulling the line to ground is considered a logical zero; letting the line float is considered a logical one.

Figure 27-3 shows a typical connection between two devices configured as master and slave.

The \( \text{I}^2\text{C} \) bus can operate with one or more master devices and one or more slave devices.

There are four potential modes of operation for a given device:

- Master Transmit mode (master is transmitting data to a slave)
- Master Receive mode (master is receiving data from a slave)
- Slave Transmit mode (slave is transmitting data to a master)
- Slave Receive mode (slave is receiving data from a master)

To begin communication, a master device starts out in Master Transmit mode. The master device sends out a Start bit followed by the address byte of the slave it intends to communicate with. This is followed by a single Read/Write bit, which determines whether the master intends to transmit to or receive data from the slave device.

If the requested slave exists on the bus, it will respond with an Acknowledge bit, otherwise known as an \( \text{ACK} \). The master then continues in either Transmit mode or Receive mode and the slave continues in the complement, either in Receive mode or Transmit mode, respectively.

A Start bit is indicated by a high-to-low transition of the SDA line while the SCL line is held high. Address and data bytes are sent out Most Significant bit (MSb) first. The Read/Write bit is sent out as a logical one when the master intends to read data from the slave, and is sent out as a logical zero when it intends to write data to the slave.

The Acknowledge bit (\( \text{ACK} \)) is an active-low signal that holds the SDA line low to indicate to the transmitter that the slave device has received the transmitted data and is ready to receive more.

The transition of a data bit is always performed while the SCL line is held low. Transitions that occur while the SCL line is held high are used to indicate Start and Stop bits.

If the master intends to write to the slave, it repeatedly sends out a byte of data, with the slave responding after each byte with an \( \text{ACK} \) bit. In this example, the master device is in Master Transmit mode and the slave is in Slave Receive mode.

If the master intends to read from the slave, it repeatedly receives a byte of data from the slave and responds after each byte with an \( \text{ACK} \) bit. In this example, the master device is in Master Receive mode and the slave is Slave Transmit mode.
On the last byte of data communicated, the master device may end the transmission by sending a Stop bit. If the master device is in Receive mode, it sends the Stop bit in place of the last ACK bit. A Stop bit is indicated by a low-to-high transition of the SDA line while the SCL line is held high.

In some cases, the master may want to maintain control of the bus and re-initiate another transmission. If so, the master device may send another Start bit in place of the Stop bit or last ACK bit when it is in Receive mode.

The I²C bus specifies three message protocols:

• Single message where a master writes data to a slave
• Single message where a master reads data from a slave
• Combined message where a master initiates a minimum of two writes, or two reads, or a combination of writes and reads, to one or more slaves

When one device is transmitting a logical one, or letting the line float, and a second device is transmitting a logical zero, or holding the line low, the first device can detect that the line is not a logical one. This detection, when used on the SCL line, is called clock stretching. Clock stretching gives slave devices a mechanism to control the flow of data. When this detection is used on the SDA line, it is called arbitration. Arbitration ensures that there is only one master device communicating at any single time.

27.2.1 CLOCK STRETCHING

When a slave device has not completed processing data, it can delay the transfer of more data through the process of Clock Stretching. An addressed slave device may hold the SCL clock line low after receiving or sending a bit, indicating that it is not yet ready to continue. The master that is communicating with the slave will attempt to raise the SCL line in order to transfer the next bit, but will detect that the clock line has not yet been released. Because the SCL connection is open-drain, the slave has the ability to hold that line low until it is ready to continue communicating.

Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data.

27.2.2 ARBITRATION

Each master device must monitor the bus for Start and Stop bits. If the device detects that the bus is busy, it cannot begin a new message until the bus returns to an idle state.

However, two master devices may try to initiate a transmission at or about the same time. When this occurs, the process of arbitration begins. Each transmitter checks the level of the SDA data line and compares it to the level that it expects to find. The first transmitter to observe that the two levels don't match loses arbitration and must stop transmitting on the SDA line.

For example, if one transmitter holds the SDA line to a logical one (lets it float) and a second transmitter holds it to a logical zero (pulls it low), the result is that the SDA line will be low. The first transmitter then observes that the level of the line is different than expected and concludes that another transmitter is communicating.

The first transmitter to notice this difference is the one that loses arbitration and must stop driving the SDA line. If this transmitter is also a master device, it must also stop driving the SCL line. It then can monitor the lines for a Stop condition before trying to reissue its transmission. In the meantime, the other device that has not noticed any difference between the expected and actual levels on the SDA line continues with its original transmission. It can do so without any complications, because so far the transmission appears exactly as expected, with no other transmitter disturbing the message.

Slave Transmit mode can also be arbitrated, when a master addresses multiple slaves, but this is less common.

If two master devices are sending a message to two different slave devices at the address stage, the master sending the lower slave address always wins arbitration. When two master devices send messages to the same slave address, and addresses can sometimes refer to multiple slaves, the arbitration process must continue into the data stage.

Arbitration usually occurs very rarely, but it is a necessary process for proper multi-master support.
27.3 I2C MODE OPERATION

All MSSP I2C communication is byte-oriented and shifted out MSb first. Six SFR registers and two interrupt flags interface the module with the PIC microcontroller and with the user’s software. Two pins, SDA and SCL, are exercised by the module to communicate with other external I2C devices.

27.3.1 BYTE FORMAT

All communication in I2C is done in 9-bit segments. A byte is sent from a Master to a Slave or vice versa, followed by an Acknowledge bit sent back. After the 8th falling edge of the SCL line, the device outputting data on the SDA changes that pin to an input and reads in an acknowledge value on the next clock pulse.

The clock signal, SCL, is provided by the master. Data is valid to change while the SCL signal is low, and sampled on the rising edge of the clock. Changes on the SDA line while the SCL line is high define special conditions on the bus, explained in the following sections.

27.3.2 DEFINITION OF I2C TERMINOLOGY

There is language and terminology in the description of I2C communication that have definitions specific to I2C. Such word usage is defined in Table 27-1 and may be used in the rest of this document without explanation. The information in this table was adapted from the Philips I2C specification.

27.3.3 SDA AND SCL PINS

Selecting any I2C mode with the SSPEN bit set forces the SCL and SDA pins to be open-drain. These pins should be set by the user to inputs by setting the appropriate TRIS bits.

Note: Data is tied to output zero when an I2C mode is enabled.

27.3.4 SDA HOLD TIME

The hold time of the SDA pin is selected by the SDAHT bit in the SSPCON3 register. Hold time is the time SDA is held valid after the falling edge of SCL. Setting the SDAHT bit selects a longer 300 ns minimum hold time and may help on buses with large capacitance.

**TABLE 27-1: I2C BUS TERMS**

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmitter</td>
<td>The device that shifts data out onto the bus</td>
</tr>
<tr>
<td>Receiver</td>
<td>The device that shifts data in from the bus</td>
</tr>
<tr>
<td>Master</td>
<td>The device that initiates a transfer, generates clock signals and terminates a transfer</td>
</tr>
<tr>
<td>Slave</td>
<td>The device addressed by the master</td>
</tr>
<tr>
<td>Multi-Master</td>
<td>A bus with more than one device that can initiate data transfers</td>
</tr>
<tr>
<td>Arbitration</td>
<td>Procedure to ensure that only one master at a time controls the bus. Winning arbitration ensures that the message is not corrupted.</td>
</tr>
<tr>
<td>Synchronization</td>
<td>Procedure to synchronize the clocks of two or more devices on the bus</td>
</tr>
<tr>
<td>Idle</td>
<td>No master is controlling the bus and both SDA and SCL lines are high</td>
</tr>
<tr>
<td>Active</td>
<td>Any time one or more master devices are controlling the bus</td>
</tr>
<tr>
<td>Addressed Slave</td>
<td>Slave device that has received a matching address and is actively being clocked by a master</td>
</tr>
<tr>
<td>Matching Address</td>
<td>Address byte that is clocked into a slave that matches the value stored in SSPADDx</td>
</tr>
<tr>
<td>Write Request</td>
<td>Slave receives a matching address with R/W bit clear and is ready to clock in data</td>
</tr>
<tr>
<td>Read Request</td>
<td>Master sends an address byte with the R/W bit set, indicating that it wishes to clock data out of the Slave. This data is the next and all following bytes until a Restart or Stop.</td>
</tr>
<tr>
<td>Clock Stretching</td>
<td>When a device on the bus holds SCL low to stall communication</td>
</tr>
<tr>
<td>Bus Collision</td>
<td>Any time the SDA line is sampled low by the module while it is outputting and expected high state</td>
</tr>
</tbody>
</table>
27.3.5 START CONDITION
The I\textsuperscript{2}C specification defines a Start condition as a transition of SDA from a high state to a low state, while the SCL line is high. A Start condition is always generated by the master and signifies the transition of the bus from an Idle to an Active state. Figure 27-4 shows the wave forms for Start and Stop conditions.

A bus collision can occur on a Start condition if the module samples the SDA line low before asserting it low. This does not conform to the \textit{I}^2\textit{C} Specification that states no bus collision can occur on a Start.

27.3.6 STOP CONDITION
A Stop condition is a transition of the SDA line from low-to-high state while the SCL line is high.

\begin{note}
At least one SCL low time must appear before a Stop is valid. Therefore, if the SDA line goes low then high again while the SCL line stays high, only the Start condition is detected.
\end{note}

27.3.7 RESTART CONDITION
A Restart is valid any time that a Stop is valid. A master can issue a Restart if it wishes to hold the bus after terminating the current transfer. A Restart has the same effect on the slave that a Start would, resetting all slave logic and preparing it to clock in an address. The master may want to address the same or another slave.

In 10-bit Addressing Slave mode, a Restart is required for the master to clock data out of the addressed slave. Once a slave has been fully addressed, matching both high and low address bytes, the master can issue a Restart and the high address byte with the R/W bit set. The slave logic will then hold the clock and prepare to clock out data.

After a full match with R/W clear in 10-bit mode, a prior match flag is set and maintained. Until a Stop condition, a high address with R/W clear or a high address match fails.

27.3.8 START/STOP CONDITION
INTERRUPT MASKING
The SCIE and PCIE bits in the SSPCON3 register can enable the generation of an interrupt in Slave modes that do not typically support this function. These bits will have no effect on slave modes where interrupt on Start and Stop detect are already enabled.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{i2c_start_stop_conditions.png}
\caption{I\textsuperscript{2}C START AND STOP CONDITIONS}
\end{figure}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{i2c_restart_condition.png}
\caption{I\textsuperscript{2}C RESTART CONDITION}
\end{figure}
27.3.9 ACKNOWLEDGE SEQUENCE

The 9th SCL pulse for any transferred byte in I^2^C is dedicated as an Acknowledge. It allows receiving devices to respond back to the transmitter by pulling the SDA line low. The transmitter must release control of the line during this time to shift in the response. The Acknowledge (ACK) is an active-low signal, pulling the SDA line low, indicating to the transmitter that the device has received the transmitted data and is ready to receive more.

The result of an ACK is placed in the ACKSTAT bit in the SSPCON2 register.

Slave software, when the AHEN and DHEN bits are set, allows the user to set the ACK value sent back to the transmitter. The ACKDT bit in the SSPCON2 register is set/cleared to determine the response.

Slave hardware will generate an ACK response if the AHEN and DHEN bits in the SSPCON3 register are clear.

There are certain conditions where an ACK will not be sent by the slave. If the BF bit in the SSPSTAT register or the SSPOV bit in the SSPCON1 register are set when a byte is received, the ACK will not be sent.

When the module is addressed, after the 6th falling edge of SCL on the bus, the ACKTIM bit in the SSPCON3 register is set. The ACKTIM bit indicates the acknowledge time of the active bus. The ACKTIM status bit is only active when the AHEN or DHEN bits are enabled.

27.4 I^2^C SLAVE MODE OPERATION

The MSSP Slave mode operates in one of the four modes selected in the SSPM bits in SSPCON1 register. The modes can be divided into 7-bit and 10-bit Addressing mode. 10-bit Addressing mode operates the same as 7-bit, with some additional overhead for handling the larger addresses.

Modes with Start and Stop bit interrupts operate the same as the other modes, with SSPIF additionally getting set upon detection of a Start, Restart or Stop condition.

27.4.1 SLAVE MODE ADDRESSES

The SSPADD register contains the Slave mode address. The first byte received after a Start or Restart condition is compared against the value stored in this register. If the byte matches, the value is loaded into the SSPBUF register and an interrupt is generated. If the value does not match, the module goes idle and no indication is given to the software that anything happened.

The SSPMSK1 register affects the address matching process. Refer to Section 27.4.10 “SSPMSK1 Register” for more information.

27.4.2 SECOND SLAVE MODE ADDRESS

The SSPADD2 register contains a second 7-bit Slave mode address. The first byte received after a Start or Restart condition is compared against the value stored in this register. If the byte matches, the value is loaded into the SSPBUF register and an interrupt is generated. If the value does not match, the module goes idle and no indication is given to the software that anything happened.

The SSPMSK2 register affects the address matching process. Refer to Section 27.4.10 “SSPMSK1 Register” for more information.

27.4.2.1 I^2^C Slave 7-Bit Addressing Mode

In 7-bit Addressing mode, the LSB of the received data byte is ignored when determining if there is an address match.

27.4.2.2 I^2^C Slave 10-Bit Addressing Mode

In 10-bit Addressing mode, the first received byte is compared to the binary value of ‘1 1 1 1 0 A9 A8 0’. A9 and A8 are the two MSb of the 10-bit address and are stored in bits 2 and 1 in the SSPADD register. After the high byte has been acknowledged, the UA bit is set and SCL is held low until the user updates SSPADD with the low address and are stored in bits 2 and 1 in the SSPADD register. The low address byte is clocked in, and all 8 bits are compared to the low address value in SSPADD. Even if there is no address match, SSPIF and UA are set and SCL is held low until SSPADD is updated to receive a high byte again. When SSPADD is updated, the UA bit is cleared. This ensures the module is ready to receive the high address byte on the next communication.

A high and low address match as a write request is required at the start of all 10-bit addressing communication. A transmission can be initiated by issuing a Restart once the slave is addressed, and clocking in the high address with the R/W bit set. The slave hardware will then acknowledge the read request and prepare to clock out data. This is only valid for a slave after it has received a complete high and low address-byte match.

27.4.3 SLAVE RECEPTION

When the R/W bit of a matching received address byte is clear, the R/W bit in the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register and acknowledged.

When an overflow condition exists for a received address, then Not Acknowledge is given. An overflow condition is defined as either bit BF in the SSPSTAT register is set, or bit SSPOV in the SSPCON1 register is set. The BOEN bit in the SSPCON3 register modifies this operation. For more information, refer to Register 27-4.
An MSSP interrupt is generated for each transferred data byte. Flag bit SSPIF must be cleared by software. When the SEN bit in the SSPCON2 register is set, SCL will be held low (clock stretch) following each received byte. The clock must be released by setting the CKP bit in the SSPCON1 register, except sometimes in 10-bit mode.

27.4.3.1 7-Bit Addressing Reception

This section describes a standard sequence of events for the MSSP module configured as an I2C Slave in 7-bit Addressing mode, including all decisions made by hardware or software and their effect on reception. Figures 27-5 and 27-6 are used as a visual reference for this description.

This is a step-by-step process of what typically must be done to accomplish I2C communication.

1. Start bit detected.
2. S bit in the SSPSTAT register is set; SSPIF is set if interrupt on Start detect is enabled.
3. Matching address with R/W bit clear is received.
4. The slave pulls SDA low, sending an ACK to the master, and sets SSPIF bit.
5. Software clears the SSPIF bit.
6. Software reads received address from SSPBUF clearing the BF flag.
7. If SEN = 1, Slave software sets CKP bit to release the SCL line.
8. The master clocks out a data byte.
9. Slave drives SDA low sending an ACK to the master, and sets SSPIF bit.
10. Software clears SSPIF.
11. Software reads the received byte from SSPBUF clearing BF.
12. Steps 8–12 are repeated for all received bytes from the Master.

27.4.3.2 7-Bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operates the same as without these options with extra interrupts and clock stretching added after the 8th falling edge of SCL. These additional interrupts allow the slave software to decide whether it wants the ACK to receive address or data byte, rather than the hardware.

This list describes the steps that need to be taken by slave software to use these options for I2C communication. Figure 27-7 displays a module using both address and data holding. Figure 27-8 includes the operation with the SEN bit in the SSPCON2 register set.

1. S bit in the SSPSTAT register is set; SSPIF is set if interrupt on Start detect is enabled.
2. Matching address with R/W bit clear is clocked in. SSPIF is set and CKP cleared after the 8th falling edge of SCL.
3. Slave clears the SSPIF.
4. Slave can look at the ACKTIM bit in the SSPCON3 register to determine if the SSPIF was after or before the ACK.
5. Slave reads the address value from SSPBUF, clearing the BF flag.
6. Slave sets ACK value clocked out to the master by setting ACKDT.
7. Slave releases the clock by setting CKP.
8. SSPxIF is set after an ACK, not after a NACK.
9. If SEN = 1 the slave hardware will stretch the clock after the ACK.
10. Slave clears SSPIF.

Note: SSPIF is still set after the 9th falling edge of SCL even if there is no clock stretching and BF has been cleared. Only if NACK is sent to Master is SSPIF not set.
FIGURE 27-6: \( \text{I}^2\text{C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 0, DHEN = 0)} \)

- **Receiving Address**: A7 A6 A5 A4 A3 A2 A1 ACK
- **Receiving Data**: D7 D6 D5 D4 D3 D2 D1 D0 ACK

**From Slave to Master**:
- SSPIF set on 9th falling edge of SCL
- First byte of data is available in SSPBUF
- SSPOV set because SSPBUF is still full. ACK is not sent.

**Cleared by software**:
- SSPBUF is read
- SSPIF set on 9th falling edge of SCL

**Bus Master sends Stop condition**
FIGURE 27-7:  I\(^2\)C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)

<table>
<thead>
<tr>
<th>SDA</th>
<th>Receive Address</th>
<th>Receive Data</th>
<th>Receive Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEN</td>
<td>R/W=0</td>
<td>ACK</td>
<td>ACK</td>
</tr>
<tr>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
</tr>
<tr>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
</tr>
</tbody>
</table>

SDA: Address Bus
SCL: Clock Bus

SSPIF: Set by first stop condition
BF: Set by write to '1' in software
SSPOV: Set when SSPBUF is full
CKP: Clock is held low until CKP is set to '1'

Bus Master sends Stop condition

Clock is held low until CKP is set to '1'

Cleared by software

First byte of data is available in SSPBUF

SSPOV set because SSPBUF is still full. ACK is not sent.

CKP written to '1' in software, releasing SCL

SSPBUF is read

Cleared by software

SSPIF set on 9\(^{th}\) falling edge of SCL

CKP written to '1' in software, releasing SCL

ACK is not sent.

SCL is not held low because ACK = 1
FIGURE 27-8: \( ^2 \text{C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 1, DHEN = 1)} \)

Master Releases SDAX to slave for ACK sequence

<table>
<thead>
<tr>
<th>SDA</th>
<th>Receiving Address</th>
<th>ACK</th>
<th>Receiving Data</th>
<th>ACK</th>
<th>Received Data</th>
<th>ACK</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>( A ) ( A ) ( A ) ( A ) ( A ) ( A )</td>
<td>( D ) ( D ) ( D )</td>
<td>( D ) ( D ) ( D )</td>
<td>( D ) ( D ) ( D )</td>
<td>( D ) ( D ) ( D )</td>
<td></td>
</tr>
<tr>
<td>SCL</td>
<td>( S ) ( S ) ( S ) ( S ) ( S ) ( S )</td>
<td>( P ) ( A ) ( A ) ( A ) ( A ) ( A )</td>
<td>( P ) ( P ) ( P ) ( P ) ( P ) ( P )</td>
<td>( P ) ( P ) ( P ) ( P ) ( P ) ( P )</td>
<td>( P ) ( P ) ( P ) ( P ) ( P ) ( P )</td>
<td>( P ) ( P ) ( P ) ( P ) ( P ) ( P )</td>
</tr>
</tbody>
</table>

SSPIF
- If \( AHEN = 1 \), SSPIF is set
- SSPIF is set on 9th falling edge of SCL, after ACK
- Cleared by software

BF
- Address is read from SSBUF
- Data is read from SSPBUF

ACKDT
- Slave software clears ACKDT to ACK the received byte
- Slave software sets ACKDT to not ACK

CKP
- When \( AHEN = 1 \): CKP is cleared by hardware and SCL is stretched
- When \( DHEN = 1 \): CKP is cleared by hardware on 8th falling edge of SCL
- CKP set by software, SCL is released

ACKTIM
- ACKTIM set by hardware on 8th falling edge of SCL
- ACKTIM cleared by hardware on 9th rising edge of SCL
- ACKTIM set by hardware on 8th falling edge of SCL

Master sends Stop condition

Slave software clears ACKDT to ACK the received byte

S
- Master Releases SDAX to slave for ACK sequence
- \( S \) \( S \) \( S \) \( S \) \( S \) \( S \)

P
- Master sends Stop condition
- \( P \) \( P \) \( P \) \( P \) \( P \) \( P \)
FIGURE 27-9: \( \text{\textsuperscript{i2}C} \) SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 1, DHEN = 1)

- \( R/W = 0 \)
- Master releases SDA to slave for ACK sequence
- SDA
- SCL
- Receiving Address
- A7 | A6 | A5 | A4 | A3 | A2 | A1
- Receive Data
- ACK
- D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0
- Receive Data
- D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0
- ACK
- Master sends Stop condition
- S
- P
- Master releases SDA to slave for ACK sequence
- SDA to slave for ACK sequence
- No interrupt after if not ACK from Slave
- SSPBUF
- Received address is loaded into SSPBUF
- Received data is available on SSPBUF
- SSPBUF can be read any time before next byte is loaded
- Slave software clears ACKDT to ACK the received byte
- Slave sends not ACK
- Slave sends not ACK
- CKP
- When AHEN = 1:
  - on the 8\textsuperscript{th} falling edge of SCL of an address byte, CKP is cleared
- When DHEN = 1:
  - on the 8\textsuperscript{th} falling edge of SCL of a received data byte, CKP is cleared
- ACKTIM
- ACKTIM is set by hardware on 8\textsuperscript{th} falling edge of SCL
- ACKTIM is cleared by hardware on 9\textsuperscript{th} rising edge of SCL
- ACKDT
- ACKDT
- BF
- ACK
- R/W = 0
- ACK
- S
- P
- R/W = 0
- ACK
- S
- P
27.4.4 SLAVE TRANSMISSION

When the R/W bit of the incoming address byte is set and an address match occurs, the R/W bit in the SSPSTAT register is set. The received address is loaded into the SSPBUF register and an ACK pulse is sent by the slave on the 9th bit.

Following the ACK, slave hardware clears the CKP bit and the SCL pin is held low. Refer to Section 27.4.7 “Clock Stretching” for more details. By stretching the clock, the master will be unable to assert another clock pulse until the slave is done preparing the transmit data.

The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then the SCL pin should be released by setting the CKP bit in the SSPCON1 register. The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time.

The ACK pulse from the master-receiver is latched on the rising edge of the 9th SCL input pulse. This ACK value is copied to the ACKSTAT bit in the SSPCON2 register. If ACKSTAT is set (not ACK), the data transfer is complete. In this case, when the not ACK is latched by the slave, the slave goes idle and waits for another occurrence of the Start bit. If the SDA line was low (ACK), the next transmit data must be loaded into the SSPBUF register. Again, the SCL pin must be released by setting bit CKP.

An MSSP interrupt is generated for each data transfer byte. The SSPIF bit must be cleared by software, and the SSPSTAT register is used to determine the status of the byte. The SSPIF bit is set on the falling edge of the 9th clock pulse.

27.4.4.1 Slave Mode Bus Collision

A slave receives a Read request and begins shifting data out on the SDA line. If a bus collision is detected and the SBCDE bit in the SSPCON3 register is set, the BCLIF bit in the PIR register is set. Once a bus collision is detected, the slave goes idle and waits to be addressed again. The user’s software can use the BCLIF bit to handle a slave bus collision.

27.4.4.2 7-Bit Transmission

A master device can transmit a read request to a slave, and then it clocks data out of the slave. The list below outlines what software for a slave will need to do to accomplish a standard transmission. Figure 27-10 can be used as a reference to this list.

1. Master sends a Start condition on SDA and SCL.
2. If bit in the SSPSTAT register is set; SSPIF is set if interrupt on Start detect is enabled.
3. Matching address with R/W bit set is received by the Slave setting SSPIF bit.
4. Slave hardware generates an ACK and sets SSPIF.
5. SSPIF bit is cleared by user.
6. Software reads the received address from SSPBUF, clearing BF.
7. R/W is set so CKP was automatically cleared after the ACK.
8. The slave software loads the transmit data into SSPBUF.
9. CKP bit is set releasing SCL, allowing the master to clock the data out of the slave.
10. SSPIF is set after the ACK response from the master is loaded into the ACKSTAT register.
11. SSPIF bit is cleared.
12. The slave software checks the ACKSTAT bit to see if the master wants to clock out more data.

**Note 1:** If the master ACKs, the clock will be stretched.

**Note 2:** ACKSTAT is the only bit updated on the rising edge of SCL (9th) rather than on the falling edge.

13. Steps 9–13 are repeated for each transmitted byte.
14. If the master sends a not ACK, the clock is not held but SSPIF is still set.
15. The master sends a Restart condition or a Stop.
16. The slave is no longer addressed.
FIGURE 27-10: \( \text{\textcopyright I} \text{C \textit{SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 0)}} \)

- Receiving Address: \( \textstyle R/W = 1 \) Automatic
- Transmitting Data: \( \textstyle \text{Automatic} \)
- Transmitting Data: \( \textstyle \text{ACK} \)
- Master sends Stop condition
- SDA
- SCL
- SSPIF
- BF
- CKP
- ACKSTAT
- R/W
- D/A
- S
- P
27.4.4.3  7-Bit Transmission with Address Hold Enabled

Setting the AHEN bit in the SSPCON3 register enables additional clock stretching and interrupt generation after the 8th falling edge of a received matching address. Once a matching address has been clocked in, CKP is cleared and the SSPIF interrupt is set.

Figure 27-11 displays a standard waveform of a 7-bit Address Slave Transmission with AHEN enabled.

1. Bus starts idle.
2. Master sends Start condition; the S bit in the SSPSTAT register is set; SSPIF is set if interrupt on Start detect is enabled.
3. Master sends matching address with R/W bit set. After the 8th falling edge of the SCL line, the CKP bit is cleared and SSPIF interrupt is generated.
4. Slave software clears SSPIF.
5. Slave software reads ACKTIM bit in the SSPCON3 register and R/W and D/A bits in the SSPSTAT register to determine the source of the interrupt.
6. Slave reads the address value from the SSPBUF register, clearing the BF bit.
7. Slave software decides from this information if it wishes to ACK or not ACK, and sets ACKDT bit in the SSPCON2 register accordingly.
8. Slave sets the CKP bit releasing SCL.
9. Master clocks in the ACK value from the slave.
10. Slave hardware automatically clears the CKP bit and sets SSPIF after the ACK if the R/W bit is set.
11. Slave software clears SSPIF.
12. Slave loads value to transmit to the master into SSPBUF setting the BF bit.

d| Note: | SSPBUF cannot be loaded until after the ACK.

13. Slave sets CKP bit releasing the clock.
14. Master clocks out the data from the slave and sends an ACK value on the 9th SCL pulse.
15. Slave hardware copies the ACK value into the ACKSTAT bit in the SSPCON2 register.
16. Steps 10–15 are repeated for each byte transmitted to the master from the slave.
17. If the master sends a not ACK, the slave releases the bus, allowing the master to send a Stop and end the communication.

d| Note: | Master must send a not ACK on the last byte to ensure that the slave releases the SCL line to receive a Stop.
FIGURE 27-11: \(^{2}\)C SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 1)

- **SDA**: Receiving Address, R/W = 1
- **SCL**: Automatic, Transmitting Data
- **SSPIF**: ACK
- **BF**: Received address is read from SSPBUF
- **ACKDT**: Slave clears ACKDT to ACK
- **ACKSTAT**: ACK
- **CKP**: When AHEN = 1: CKP is cleared by hardware after receiving matching address.
  - When R/W = 1: CKP is always cleared after ACK
- **ACKTIM**: ACKTIM is set on 8\(^{th}\) falling edge of SCL
  - ACKTIM is set on 9\(^{th}\) rising edge of SCL
- **R/W**: Master's ACK response is copied to SSPSTAT
- **D/A**: CKP not cleared after not ACK

Master sends Stop condition
27.4.5 SLAVE MODE 10-BIT ADDRESS RECEPTION

This section describes a standard sequence of events for the MSSP module configured as an I²C Slave in 10-bit Addressing mode.

Figure 27-12 is used as a visual reference for this description.

This is a step-by-step process of what must be done by slave software to accomplish I²C communication:

1. Bus starts idle.
2. Master sends Start condition; S bit in the SSPSTAT register is set; SSPIF is set if interrupt on Start detect is enabled.
3. Master sends matching high address with R/W bit clear; UA bit in the SSPSTAT register is set.
4. Slave sends ACK and SSPIF is set.
5. Software clears the SSPIF bit.
6. Software reads received address from SSPBUF, clearing the BF flag.
7. Slave loads low address into SSPADD, releasing SCL.
8. Master sends matching low-address byte to the Slave; UA bit is set.
9. Slave sends ACK and SSPIF is set.

**Note:** Updates to the SSPADD register are not allowed until after the ACK sequence.

10. Slave clears SSPIF.
11. Slave reads the received matching address from SSPBUF, clearing BF.
12. Slave loads high address into SSPADD.
13. Master clocks a data byte to the slave and clocks out the slave's ACK on the 9th SCL pulse; SSPIF is set.
14. If SEN bit in the SSPCON2 register is set, CKP is cleared by hardware and the clock is stretched.
15. Slave clears SSPIF.
16. Slave reads the received byte from SSPBUF, clearing BF.
17. If SEN is set, the slave sets CKP to release the SCL.
18. Steps 13–17 are repeated for each received byte.
19. Master sends Stop to end the transmission.

27.4.6 10-BIT ADDRESSING WITH ADDRESS OR DATA HOLD

Reception using 10-bit addressing with AHEN or DHEN set is the same as with 7-bit modes. The only difference is the need to update the SSPADD register using the UA bit. All functionality, specifically when the CKP bit is cleared and the SCL line is held low, is the same. Figure 27-13 can be used as a reference of a slave in 10-bit addressing with AHEN set.

Figure 27-14 shows a standard waveform for a slave transmitter in 10-bit Addressing mode.

**Note:** If the low address does not match, SSPIF and UA are still set so that the slave software can set SSPADD back to the high address. BF is not set because there is no match. CKP is unaffected.
FIGURE 27-12: \( \text{i}^2\text{C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)} \)

- **Receive First Address Byte**: SDA: 1 1 1 0 A9 A8 ACK A7 A6 A5 A4 A3 A2 A1 A0 ACK
- **Receive Second Address Byte**: SDA: 1 1 1 0 D7 D6 D5 D4 D3 D2 D1 D0 ACK
- **Receive Data**: SDA: 1 1 1 0 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 D7 D6 D5 D4 D3 D2 D1 D0 ACK

**SSPIF**:
- Set by hardware on 9th falling edge
- Cleared by software

**BF**:
- If address matches SSPADD, it is loaded into SSPBUF
- Receive address is read from SSPBUF
- Data is read from SSPBUF

**UA**:
- When UA = 1: SCL is held low
- Software updates SSPADD and releases SCL

**CKP**:
- When SEN = 1: CKP is cleared after 9th falling edge of received byte
- Set by software, releasing SCL

**SCL**:
- SCL is held low while CKP = 0

**Master sends Stop condition**

**SDA** and **SCL**:
- Master sends Stop condition

**Software updates SSPADD**
- Releasing SCL

**Receive address is read from SSPBUF**
- Data is read from SSPBUF
**FIGURE 27-13: I²C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 1, DHEN = 0)**

<table>
<thead>
<tr>
<th>SDA</th>
<th>SCL</th>
<th>Receive First Address Byte</th>
<th>R/W = 0</th>
<th>Receive Second Address Byte</th>
<th>Receive Data</th>
<th>Receive Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>A9</td>
<td>A8</td>
<td>ACK</td>
<td>A7</td>
<td>A6</td>
</tr>
<tr>
<td></td>
<td>S</td>
<td>1</td>
<td></td>
<td></td>
<td>2</td>
<td>3</td>
</tr>
</tbody>
</table>

- **SSPIF**: Set by hardware on 9th falling edge, cleared by software.
- **BF**: SSPBUF can be read anytime before the next received cycle.
- **ACKDT**: Slave software clears ACKDT to ACK the received byte.
- **UA**: Received data is read from SSPBUF.
- **CKP**: Set CKP with software releases SCL.
- **ACKTIM**: ACKTIM is set by hardware on 8th falling edge of SCL.

If when AHEN = 1:
- on the 8th falling edge of SCL of an address byte, CKP is cleared.
- Update to SSPADD is not allowed until 9th falling edge of SCL.
- Update of SSPADD clears UA and releases SCL.

Cleared by software when:
- R/W = 0
- S
- B
- ACK
FIGURE 27-14: $i^2$C SLAVE, 10-BIT ADDRESS, TRANSMISSION (SEN = 0, AHEN = 0, DHEN = 0)

- Receiving Address, $R/W = 0$:
  - Receiving Second Address Byte
  - Receive First Address Byte

- Transmitting Data Byte, $ACK = 1$:
  - Stop condition
  - Master sends not ACK

- Master sends Restart event

- Set by hardware:
  - UA indicates SSPADD must be updated
  - ACKSTAT

- Cleared by software:
  - SSPBUF loaded with received address
  - UA
  - BF

- SSPBUF loaded with received address

- Received address is read from SSPBUF

- Data to transmit is loaded into SSPBUF

- UA is cleared and SCL is released

- After SSPADD is updated, high address is loaded back into SSPADD

- SSPADD loaded

- When $R/W = 1$:
  - CKP is cleared on 9th falling edge of SCL
  - ACKSTAT

- Set by software releases SCL

- Master's not ACK is copied

- Indicates an address has been received

- R/W is copied from the matching address byte
27.4.7 CLOCK STRETCHING

Clock stretching occurs when a device on the bus holds the SCL line low, effectively pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching, as it is stretching anytime it is active on the bus and not transferring data. Any stretching done by a slave is invisible to the master software and handled by the hardware that generates SCL.

The CKP bit in the SSPCON1 register is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. Setting CKP will release SCL and allow more communication.

27.4.7.1 Normal Clock Stretching

Following an ACK, if the R/W bit in the SSPSTAT register is set, causing a read request, the slave hardware will clear CKP. This allows the slave time to update SSPBUF with data to transfer to the master. If the SEN bit in the SSPCON2 register is set, the slave hardware will always stretch the clock after the ACK sequence. Once the slave is ready, CKP is set by software and communication resumes.

Note 1: The BF bit has no effect on whether the clock will be stretched or not. This is different than previous versions of the module that would not stretch the clock or clear CKP if SSPBUF was read before the 9th falling edge of SCL.

2: Previous versions of the module did not stretch the clock for a transmission if SSPBUF was loaded before the 9th falling edge of SCL. It is now always cleared for read requests.

27.4.7.2 10-Bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set, the clock is always stretched. This is the only time the SCL is stretched without CKP being cleared. SCL is released immediately after a write to SSPADD.

Note: Previous versions of the module did not stretch the clock if the second address byte did not match.

27.4.7.3 Byte NACKing

When AHEN bit in the SSPCON3 register is set, CKP is cleared by hardware after the 8th falling edge of SCL for a received matching address byte. When DHEN bit in the SSPCON3 register is set, CKP is cleared after the 8th falling edge of SCL for received data.

Stretching after the 8th falling edge of SCL allows the slave to look at the received address or data and decide if it wants to ACK the received data.

27.4.8 CLOCK SYNCHRONIZATION AND THE CKP BIT

Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. However, clearing the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external I2C master device has already asserted the SCL line. The SCL output will remain low until the CKP bit is set and all other devices on the I2C bus have released SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (refer to Figure 27-16).

Note: Previous versions of the module did not stretch the clock if the second address byte did not match.

FIGURE 27-15: CLOCK SYNCHRONIZATION TIMING
27.4.9 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the I²C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address, which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

The general call address is a reserved address in the I²C protocol, defined as address 0x00. When the GCEN bit in the SSPCON2 register is set, the slave module will automatically ACK the reception of this address regardless of the value stored in SSPADD. After the slave clocks in an address of all zeros with the R/W bit clear, an interrupt is generated and slave software can read SSPBUF and respond. Figure 27-17 shows a general call reception sequence.

In 10-bit Address mode, the UA bit will not be set on the reception of the general call address. The slave will prepare to receive the second byte as data, just as it would in 7-bit mode.

If the AHEN bit in the SSPCON3 register is set, just as with any other address reception, the slave hardware will stretch the clock after the 8th falling edge of SCL. The slave must then set its ACKDT value and release the clock with communication progressing as it would normally.

FIGURE 27-16: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE

27.4.10 SSPMSK1 REGISTER

An SSP Mask (SSPMSK1) register is available in I²C Slave mode as a mask for the value held in the SSPSR register during an address comparison operation. A zero ('0') bit in the SSPMSK1 register has the effect of making the corresponding bit of the received address a “don’t care”.

This register is reset to all ‘1’ s upon any Reset condition and, therefore, has no effect on standard SSP operation until written with a mask value.

The SSPMSK1 register is active during:

• 7-bit Address mode: address compare of A<7:1>.
• 10-bit Address mode: address compare of A<7:0> only. The SSP mask has no effect during the reception of the first (high) byte of the address.
27.5 I²C MASTER MODE

Master mode is enabled by setting and clearing the appropriate SSPM bits in the SSPCON1 register and by setting the SSPEN bit. In Master mode, the SDA and SCK pins must be configured as inputs. The MSSP peripheral hardware will override the output driver TRIS controls when necessary, to drive the pins low.

The Master mode of operation is supported by interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit is set or the bus is idle.

In Firmware-Controlled Master mode, user code conducts all I²C bus operations based on Start and Stop bit condition detection. Start and Stop condition detection is the only active circuitry in this mode. All other communication is done by the user’s software directly manipulating the SDA and SCL lines.

The following events will cause the SSP Interrupt Flag bit (SSPIF) to be set (SSP interrupt, if enabled):

- Start condition detected
- Stop condition detected
- Data transfer byte transmitted/received
- Acknowledge transmitted/received
- Repeated Start generated

### Note 1:
The MSSP module, when configured in I²C Master mode, does not allow queuing of events. For instance, the user is not allowed to initiate a Start condition and immediately write the SSPBUF register to initiate transmission before the Start condition is complete. In this case, the SSPBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPBUF did not occur.

### Note 2:
When in Master mode, Start/Stop detection is masked and an interrupt is generated when the SEN/PEN bit is cleared and the generation is complete.

27.5.1 I²C MASTER MODE OPERATION

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer ends with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmit mode, serial data is output through SDA while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/W) bit. In this case, the R/W bit will be logic ‘0’. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an Acknowledge bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/W bit. In this case, the R/W bit will be logic ‘1’. Thus, the first byte transmitted is a 7-bit slave address followed by a ‘1’ to indicate the receive bit. Serial data is received via SDA, while SCL outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

A Baud Rate Generator is used to set the clock frequency output on SCL. Refer to Section 27.6 “Baud Rate Generator” for more details.

27.5.2 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit or Repeated Start/Stop condition, releases the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the Baud Rate Generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<7:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 27-17).
27.5.3 WCOL STATUS FLAG

If the user writes the SSPBUF when a Start, Restart, Stop, Receive or Transmit sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write does not occur). Any time the WCOL bit is set, it indicates that an action on SSPBUF was attempted while the module was not idle.

Note: Because queuing of events is not allowed, writing to the lower 5 bits in the SSPCON2 register is disabled until the Start condition is complete.

27.5.4 I2C MASTER MODE START CONDITION TIMING

To initiate a Start condition, the user sets the Start Enable bit, SEN, in the SSPCON2 register. If the SDA and SCL pins are sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<7:0> and starts its count. If SCL and SDA are both sampled high when the Baud Rate Generator times out (TBRG), the SEN bit in the SSPCON2 register will be automatically cleared by hardware; the Baud Rate Generator is suspended, leaving the SDA line held low and the Start condition is complete.

Note 1: If, at the beginning of the Start condition, the SDA and SCL pins are already sampled low, or if, during the Start condition, the SCL line is sampled low before the SDA line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCLIF, is set, the Start condition is aborted and the I2C module is reset into its idle state.

2: The Philips I2C Specification states that a bus collision cannot occur on a Start.
27.5.5 \( \text{I}^2\text{C} \) MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition occurs when the RSEN bit in the SSPCON2 register is programmed high and the Master state machine is no longer active. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (\( T_{\text{BRG}} \)). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded and begins counting. SDA and SCL must be sampled high for one \( T_{\text{BRG}} \). This action is then followed by assertion of the SDA pin (SDA = 0) for one \( T_{\text{BRG}} \) while SCL is high. SCL is asserted low. Following this, the RSEN bit in the SSPCON2 register will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit in the SSPSTAT register will be set. The SSPIF bit will not be set until the Baud Rate Generator has timed out.

**FIGURE 27-19: REPEAT START CONDITION WAVEFORM**

Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.

Note 2: A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low to high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data ‘1’.
27.5.6 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address is accomplished by simply writing a value to the SSPBUF register. This action will set the Buffer Full (BF) flag bit and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted. SCL is held low for one Baud Rate Generator rollover count \( T_{BRG} \). Data should be valid before SCL is released high. When the SCL pin is released high, it is held that way for \( T_{BRG} \). The data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the 8th bit is shifted out (the falling edge of the 8th clock), the BF flag is cleared and the master releases the SDA. This allows the slave device being addressed to respond with an ACK bit during the 9th bit time if an address match occurred or if data was received properly. The status of \( \text{ACK} \) is written into the ACKSTAT bit on the rising edge of the 9th clock. If the master receives an Acknowledge, the Acknowledge Status bit (ACKSTAT) is cleared. If not, the bit is set. After the 9th clock, the SSPF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSPBUF, leaving SCL low and SDA unchanged (Figure 27-20).

After the write to the SSPBUF, each bit of the address will be shifted out on the falling edge of SCL until all seven address bits and the R/W bit are completed. On the falling edge of the 8th clock, the master will release the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the 9th clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the \( \text{ACK} \) bit is loaded into the ACKSTAT status bit in the SSPCON2 register. Following the falling edge of the 9th clock transmission of the address, the SSPF is set, the BF flag is cleared and the Baud Rate Generator is turned off until another write to the SSPBUF takes place, holding SCL low and allowing SDA to float.

27.5.6.1 BF Status Flag

In Transmit mode, the BF bit in the SSPSTAT register is set when the CPU writes to SSPBUF and is cleared when all 8 bits are shifted out.

27.5.6.2 WCOL Status Flag

If the user writes the SSPBUF when a transmit is already in progress (i.e., SSPSR is still shifting out a data byte), the WCOL is set and the contents of the buffer are unchanged (the write does not occur). WCOL must be cleared by software before the next transmission.

27.5.6.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit in the SSPCON2 register is cleared when the slave has sent an Acknowledge \((\text{ACK} = 0)\) and is set when the slave does not Acknowledge \((\text{ACK} = 1)\). A slave sends an Acknowledge when it has recognized its address (including a general call) or when the slave has properly received its data.

27.5.6.4 Typical Transmit Sequence:

1. The user generates a Start condition by setting the SEN bit in the SSPCON2 register.
2. SSPIF is set by hardware on completion of the Start.
3. SSPIF is cleared by software.
4. The MSSP module will wait the required start time before any other operation takes place.
5. The user loads the SSPBUF with the slave address to transmit.
6. Address is shifted out the SDA pin until all 8 bits are transmitted. Transmission begins as soon as SSPBUF is written to.
7. The MSSP module shifts in the \( \text{ACK} \) bit from the slave device and writes its value into the ACKSTAT bit in the SSPCON2 register.
8. The MSSP module generates an interrupt at the end of the 9th clock cycle by setting the SSPIF bit.
9. The user loads the SSPBUF with 8 bits of data.
10. Data is shifted out the SDA pin until all 8 bits are transmitted.
11. The MSSP module shifts in the \( \text{ACK} \) bit from the slave device and writes its value into the ACKSTAT bit in the SSPCON2 register.
12. Steps 8-11 are repeated for all transmitted data bytes.
13. The user generates a Stop or Restart condition by setting the PEN or RSEN bits in the SSPCON2 register. Interrupt is generated once the Stop/Restart condition is complete.
FIGURE 27-20: I²C MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)

Write SSPCON2<0> SEN = 1
Start condition begins

SEN = 0
Transmit Address to Slave
R/W = 0
ACK = 0
Transmitting Data or Second Half of 10-bit Address

SSPBUF written with 7-bit address and R/W start transmit

SCL held low while CPU responds to SSPIF

Cleared by software service routine from SSP interrupt

Cleared by software

SSBUF written

Cleared by software

SSPBUF is written by software

After Start condition, SEN cleared by hardware

ACKSTAT in SSPCON2 = 1

From slave, clear ACKSTAT bit SSPCON2<6>

ACK

P
27.5.7  I2C MASTER MODE RECEPTION

Master mode reception is enabled by programming the Receive Enable (RCEN) bit in the SSPCON2 register.

Note: The MSSP module must be in an idle state before the RCEN bit is set or the RCEN bit will be disregarded.

The Baud Rate Generator begins counting and, upon each rollover, the state of the SCL pin changes (high-to-low/low-to-high) and data is shifted into the SSPSR. After the falling edge of the 8th clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag bit is set, the SSPIF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSP is now in idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable (ACKEN) bit in the SSPCON2 register.

27.5.7.1  BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when the SSPBUF register is read.

27.5.7.2  SSPOV Status Flag

In receive operation, the SSPOV bit is set when 8 bits are received into the SSPSR and the BF flag bit is already set from a previous reception.

27.5.7.3  WCOL Status Flag

If the user writes the SSPBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

27.5.7.4  Typical Receive Sequence:

1. The user generates a Start condition by setting the SEN bit in the SSPCON2 register.
2. SSPIF is set by hardware on completion of the Start.
3. SSPIF is cleared by software.
4. User writes SSPBUF with the slave address to transmit and the R/W bit set.
5. Address is shifted out the SDA pin until all 8 bits are transmitted. Transmission begins as soon as SSPBUF is written to.
6. The MSSP module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit in the SSPCON2 register.
7. The MSSP module generates an interrupt at the end of the 9th clock cycle by setting the SSPIF bit.
8. User sets the RCEN bit in the SSPCON2 register and the Master clocks in a byte from the slave.
9. After the 8th falling edge of SCL, SSPIF and BF are set.
10. Master clears SSPIF and reads the received byte from SSPUF, then clears BF.
11. Master sets ACK value sent to slave in ACKDT bit in the SSPCON2 register and initiates the ACK by setting the ACKEN bit.
12. Masters ACK is clocked out to the Slave and SSPIF is set.
13. The user clears SSPIF.
14. Steps 8-13 are repeated for each received byte from the slave.
15. Master sends a not ACK or Stop to end communication.

Note: The MSSP module must be in an idle state before the RCEN bit is set or the RCEN bit will be disregarded.
FIGURE 27-21: \( I^2C \) MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)

- **Write to SSPCON2<0>** (SEN = 1), begin Start condition:
  - SEN = 0
  - Write to SSPBUF occurs here, start XMIT
  - ACK from Slave
  - Receiving Data from Slave
  - RCEN cleared automatically

- **SDA = 0, SCL = 1**, while CPU responds to SSPxIR:
  - BF (SSPSTAT<0>)
  - Cleared by software
  - Cleared by software
  - Cleared by software

- **SSPIF**
  - Set SSPIF interrupt at end of receive
  - Last bit is shifted into SSPSR and contents are unloaded into SSPBUF

- **SSPOV**
  - Set SSPOV is set because SSPBUF is still full

- **ACKEN**
  - Master configured as a receiver by programming SSPCON2<3> (RCEN = 1)
  - RCEN cleared automatically
  - ACK from Master
  - SDX = ACKDT = 0

- **RCEN**
  - Master configured as a receiver by programming SSPCON2<3> (RCEN = 1)
  - RCEN cleared automatically
  - ACK from Master
  - SDX = ACKDT = 0
  - RCEN cleared automatically

- **Set ACKEN, start Acknowledge sequence SDA = ACKDT (SSPCON2<5>) = 0**
  - Set SPOV, start Acknowledge sequence

- **Set P bit (SSPSTAT<4>) and SSPIF**
  - ACC is not set
  - Bus master terminates transfer

- **Set SSPIF interrupt at end of Acknowledge sequence**
  - ACC cleared in software

- **Set SSPIF interrupt at end of receive**
  - ACC cleared in software

- **Write to SSPBUF occurs here, start XMIT**
  - ACK from Slave
  - Receiving Data from Slave
  - RCEN cleared automatically

- **ACK from Master**
  - SDX = ACKDT = 0
  - RCEN = 1, start next receive
  - Receiving Data from Slave

- **RCEN cleared automatically**
  - PEN bit = 1 written here
27.5.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable (ACKEN) bit in the SSPCON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (T_{BRG}) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for T_{BRG}. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into Idle mode (Figure 27-22).

27.5.8.1 WCOL Status Flag

If the user writes the SSPBUF when an Acknowledge sequence is in progress, WCOL is set and the contents of the buffer are unchanged (the write does not occur).

27.5.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN, in the SSPCON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the 9th clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and then, one T_{BRG} (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit in the SSPSTAT register, is set. A T_{BRG} later, the PEN bit is cleared and the SSPIF bit is set (Figure 27-23).

27.5.9.1 WCOL Status Flag

If the user writes the SSPBUF when a Stop sequence is in progress, the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).
27.5.10 SLEEP OPERATION
While in Sleep mode, the I²C slave module can receive addresses or data and, when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

27.5.11 EFFECTS OF A RESET
A Reset disables the MSSP module and terminates the current transfer.

27.5.12 MULTI-MASTER MODE
In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit in the SSPSTAT register is set or the bus is idle, with both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed by hardware with the result placed in the BCLIF bit.

The states where arbitration can be lost are:
• Address Transfer
• Data Transfer
• A Start Condition
• A Repeated Start Condition
• An Acknowledge Condition

27.5.13 MULTI-MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION
Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a ‘1’ on SDA by letting SDA float high, and another master asserts a ‘0’. When the SCL pin floats high, data should be stable. If the expected data on SDA is a ‘1’ and the data sampled on the SDA pin is ‘0’, a bus collision has taken place. The master will set the Bus Collision Interrupt Flag (BCLIF) and reset the I²C port to its Idle state (Figure 27-24).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are deasserted and the SSPBUF can be written to. When the user services the bus collision Interrupt Service Routine and if the I²C bus is free, the user can resume communication by asserting a Start condition.

If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are deasserted and the respective control bits in the SSPCON2 register are cleared. When the user services the bus collision Interrupt Service Routine and if the I²C bus is free, the user can resume communication by asserting a Start condition.

A write to the SSPBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I²C bus can be taken when the P bit is set in the SSPSTAT register, or the bus is idle and the S and P bits are cleared.

---

**FIGURE 27-24: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE**

![Diagram showing bus collision timing for transmit and acknowledge](image-url)
27.5.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

a) SDA or SCL are sampled low at the beginning of the Start condition (Figure 27-25)
b) SCL is sampled low before SDA is asserted low (Figure 27-26)

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low or the SCL pin is already low, all of the following occur:
• the Start condition is aborted
• the BCLIF flag is set and
• the MSSP module is reset to its Idle state (Figure 27-25)

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data ‘1’ during the Start condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 27-27). If, however, a ‘1’ is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCL pin is sampled as ‘0’ during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

**Note:** The reason why bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.

**FIGURE 27-25: BUS COLLISION DURING A START CONDITION (SDA ONLY)**

- SDA goes low before the SEN bit is set.
  - Set BCLIF,
  - S bit and SSPIF set because SDA = 0, SCL = 1.

- Set SEN, enable Start condition if SDA = 1, SCL = 1

- SDA sampled low before Start condition.
  - Set BCLIF. S bit and SSPIF set because SDA = 0, SCL = 1.

- SEN cleared automatically because of bus collision.
  - SSP module reset into Idle state.

- SSPIF and BCLIF are cleared by software

- S

- SSPIF

SSPIF and BCLIF are cleared by software
FIGURE 27-26: BUS COLLISION DURING A START CONDITION (SCL = 0)

SDA = 0, SCL = 1

---

Set SEN, enable Start sequence if SDA = 1, SCL = 1

SCL = 0 before SDA = 0, bus collision occurs. Set BCLIF.

---

SCL = 0 before BRG time out, bus collision occurs. Set BCLIF.

---

Interrupt cleared by software

SDA = 0, SCL = 1

---

Set S

---

Set SSPIF

---

SDAx = 0, SCL = 1, set SSPIF

---

Interrupts cleared by software

FIGURE 27-27: BRG RESET DUE TO SDA ARBITRATION DURING START CONDITION

SDA = 0, SCL = 1

---

Set S

---

Set SSPIF

---

SDAx = 0, SCL = 1, set SSPIF

---

Interrupts cleared by software
27.5.13.2  Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDA when SCL goes from low level to high level
b) SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data ‘1’

When the user releases SDA and the pin is allowed to float high, the BRG is loaded with SSPADD and counts down to zero. The SCL pin is then deasserted and, when sampled high, the SDA pin is sampled.

If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data ‘0’; see Figure 27-28). If SDA is sampled high, the BRG is loaded and begins counting. If SDA goes from high to low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

If SCL goes from high to low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data ‘1’ during the Repeated Start condition (refer to Figure 27-29).

If, at the end of the BRG time out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated Start condition is complete.

FIGURE 27-28:  BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

FIGURE 27-29:  BUS COLLISION DURING A REPEATED START CONDITION (CASE 2)
27.5.13.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

a) After the SDA pin has been deasserted and allowed to float high, SDA is sampled low after the BRG has timed out.

b) After the SCL pin is deasserted, SCL is sampled low before SDA goes high.

The Stop condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSPADD and counts down to 0. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data ‘0’ (Figure 27-30). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data ‘0’ (Figure 27-31).
TABLE 27-2: SUMMARY OF REGISTERS ASSOCIATED WITH I²C OPERATION

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Reset Values on Page:</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>IOCE</td>
<td>T0IF</td>
<td>INTF</td>
<td>IOCF</td>
<td>102</td>
</tr>
<tr>
<td>PIE1</td>
<td>TXIE</td>
<td>RCIE</td>
<td>BCLIE</td>
<td>SSPIE</td>
<td>CC2IE</td>
<td>CC1IE</td>
<td>TMR2E</td>
<td>TMR1E</td>
<td>103</td>
</tr>
<tr>
<td>PIR1</td>
<td>TXIF</td>
<td>RCIF</td>
<td>BCLIF</td>
<td>SSPIF</td>
<td>CC2IF</td>
<td>CC1IF</td>
<td>TMR2F</td>
<td>TMR1F</td>
<td>105</td>
</tr>
<tr>
<td>TRISGPA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>—</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td>119</td>
</tr>
<tr>
<td>TRISGPB</td>
<td>TRISB7</td>
<td>TRISB6</td>
<td>TRISB5</td>
<td>TRISB4</td>
<td>—</td>
<td>—</td>
<td>TRISB1</td>
<td>TRISB0</td>
<td>125</td>
</tr>
<tr>
<td>TRISGPA</td>
<td>TRISA7</td>
<td>TRISA6</td>
<td>TRISA5</td>
<td>—</td>
<td>TRISA3</td>
<td>TRISA2</td>
<td>TRISA1</td>
<td>TRISA0</td>
<td>119</td>
</tr>
<tr>
<td>TRISGPB</td>
<td>TRISB7</td>
<td>TRISB6</td>
<td>TRISB5</td>
<td>TRISB4</td>
<td>—</td>
<td>—</td>
<td>TRISB1</td>
<td>TRISB0</td>
<td>125</td>
</tr>
<tr>
<td>SSPADD</td>
<td>ADD7</td>
<td>ADD6</td>
<td>ADD5</td>
<td>ADD4</td>
<td>ADD3</td>
<td>ADD2</td>
<td>ADD1</td>
<td>ADD0</td>
<td>215</td>
</tr>
<tr>
<td>SSPBUF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Synchronous Serial Port Receive Buffer/Transmit Register 175*</td>
</tr>
<tr>
<td>SSPCON1</td>
<td>WCOL</td>
<td>SSPOV</td>
<td>SSPEN</td>
<td>CKP</td>
<td>SSPM3</td>
<td>SSPM2</td>
<td>SSPM1</td>
<td>SSPM0</td>
<td>212</td>
</tr>
<tr>
<td>SSPCON2</td>
<td>GCEN</td>
<td>ACKSTAT</td>
<td>ACKDT</td>
<td>ACKEN</td>
<td>RCEN</td>
<td>PEN</td>
<td>RSEN</td>
<td>SEN</td>
<td>213</td>
</tr>
<tr>
<td>SSPCON3</td>
<td>ACKTIM</td>
<td>PCIE</td>
<td>SCIE</td>
<td>BOEN</td>
<td>SDAHT</td>
<td>SBCDE</td>
<td>AHEN</td>
<td>DHEN</td>
<td>214</td>
</tr>
<tr>
<td>SSPMSK1</td>
<td>MSK7</td>
<td>MSK6</td>
<td>MSK5</td>
<td>MSK4</td>
<td>MSK3</td>
<td>MSK2</td>
<td>MSK1</td>
<td>MSK0</td>
<td>215</td>
</tr>
<tr>
<td>SSPSTAT</td>
<td>SMP</td>
<td>CKE</td>
<td>D/A</td>
<td>P</td>
<td>S</td>
<td>R/W</td>
<td>UA</td>
<td>BF</td>
<td>211</td>
</tr>
<tr>
<td>SSPMSK2</td>
<td>MSK27</td>
<td>MSK26</td>
<td>MSK25</td>
<td>MSK24</td>
<td>MSK23</td>
<td>MSK22</td>
<td>MSK21</td>
<td>MSK20</td>
<td>216</td>
</tr>
<tr>
<td>SSPADD2</td>
<td>ADD27</td>
<td>ADD26</td>
<td>ADD25</td>
<td>ADD24</td>
<td>ADD23</td>
<td>ADD22</td>
<td>ADD21</td>
<td>ADD20</td>
<td>216</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented, read as ‘0’. Shaded cells are not used by the MSSP module in I²C mode.  
* Page provides register information.
27.6 Baud Rate Generator

The MSSP module has a Baud Rate Generator available for clock generation in the I²C Master mode. The Baud Rate Generator (BRG) reload value is placed in the SSPADD register. When a write occurs to SSPBUF, the Baud Rate Generator will automatically begin counting down.

Once the given operation is complete, the internal clock will automatically stop counting and the clock pin will remain in its last state.

An internal signal “Reload” in Figure 27-32 triggers the value from SSPADD to be loaded into the BRG counter. This occurs twice for each oscillation of the module clock line. The logic dictating when the reload signal is asserted depends on the mode the MSSP is being operated in.

Table 27-3 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPADD.

**EQUATION 27-1:**

\[ F_{CLOCK} = \frac{F_{OSC}}{(SSPADD + 1)(4)} \]

**FIGURE 27-32: BAUD RATE GENERATOR BLOCK DIAGRAM**

![Baud Rate Generator Block Diagram]

Note: Values of 0x00, 0x01 and 0x02 are not valid for SSPADD when used as a Baud Rate Generator for I²C. This is an implementation limitation.

**TABLE 27-3: MSSP CLOCK RATE W/BRG**

<table>
<thead>
<tr>
<th>Fosc</th>
<th>FCY</th>
<th>BRG Value</th>
<th>F_{CLOCK} (2 Rollovers of BRG)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 MHz</td>
<td>2 MHz</td>
<td>04h</td>
<td>400 kHz(1)</td>
</tr>
<tr>
<td>8 MHz</td>
<td>2 MHz</td>
<td>0Bh</td>
<td>166 kHz</td>
</tr>
<tr>
<td>8 MHz</td>
<td>2 MHz</td>
<td>13h</td>
<td>100 kHz</td>
</tr>
</tbody>
</table>

Note 1: The I²C interface does not conform to the 400 kHz I²C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.
REGISTER 27-1: SSPSTAT: SSP STATUS REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>SMP: Data Input Sample bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 = Slew rate control disabled for standard-speed mode (100 kHz and 1 MHz)</td>
</tr>
<tr>
<td></td>
<td>0 = Slew rate control enabled for high-speed mode (400 kHz)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 6</th>
<th>CKE: Clock Edge Select bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 = Enable input logic so that thresholds are compliant with SM bus specification</td>
</tr>
<tr>
<td></td>
<td>0 = Disable SM bus specific inputs</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 5</th>
<th>D/A: Data/Address bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 = Indicates that the last byte received or transmitted was data</td>
</tr>
<tr>
<td></td>
<td>0 = Indicates that the last byte received or transmitted was address</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 4</th>
<th>P: Stop bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)</td>
</tr>
<tr>
<td></td>
<td>1 = Indicates that a Stop bit has been detected last (this bit is ‘0’ on Reset)</td>
</tr>
<tr>
<td></td>
<td>0 = Stop bit was not detected last</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 3</th>
<th>S: Start bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)</td>
</tr>
<tr>
<td></td>
<td>1 = Indicates that a Start bit has been detected last (this bit is ‘0’ on Reset)</td>
</tr>
<tr>
<td></td>
<td>0 = Start bit was not detected last</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 2</th>
<th>R/W: Read/Write bit information</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit, or not ACK bit.</td>
</tr>
<tr>
<td></td>
<td><strong>In I²C Slave mode:</strong></td>
</tr>
<tr>
<td></td>
<td>1 = Read</td>
</tr>
<tr>
<td></td>
<td>0 = Write</td>
</tr>
<tr>
<td></td>
<td><strong>In I²C Master mode:</strong></td>
</tr>
<tr>
<td></td>
<td>1 = Transmit is in progress</td>
</tr>
<tr>
<td></td>
<td>0 = Transmit is not in progress</td>
</tr>
<tr>
<td></td>
<td>OR-ing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSP is in Idle mode.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 1</th>
<th>UA: Update Address bit (10-bit I²C mode only)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1 = Indicates that the user needs to update the address in the SSPADD register</td>
</tr>
<tr>
<td></td>
<td>0 = Address does not need to be updated</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 0</th>
<th>BF: Buffer Full status bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Receive:</td>
</tr>
<tr>
<td></td>
<td>1 = Receive complete, SSPBUF is full</td>
</tr>
<tr>
<td></td>
<td>0 = Receive not complete, SSPBUF is empty</td>
</tr>
<tr>
<td></td>
<td>Transmit:</td>
</tr>
<tr>
<td></td>
<td>1 = Data transmit in progress (does not include the ACK and Stop bits), SSPBUF is full</td>
</tr>
<tr>
<td></td>
<td>0 = Data transmit complete (does not include the ACK and Stop bits), SSPBUF is empty</td>
</tr>
</tbody>
</table>

Legend:

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
### REGISTER 27-2: SSPCON1: SSP CONTROL REGISTER 1

<table>
<thead>
<tr>
<th>R/C/HS-0</th>
<th>R/C/HS-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>WCOL</td>
<td>SSPOV</td>
<td>SSPOE</td>
<td>CKP</td>
<td>SSPM&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 6</td>
<td>bit 5</td>
<td>bit 4</td>
<td>bit 3-0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **HS** = Bit is set by hardware
- **C** = User cleared

#### bit 7
**WCOL:** Write Collision Detect bit

**Master mode:**
- 1 = A write to the SSPBUF register was attempted while the I^2^C conditions were not valid for a transmission to be started
- 0 = No collision

**Slave mode:**
- 1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
- 0 = No collision

#### bit 6
**SSPOV:** Receive Overflow Indicator bit\(^{(1)}\)

- 1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a “don’t care” in Transmit mode (must be cleared in software).
- 0 = No overflow

#### bit 5
**SSPEN:** Synchronous Serial Port Enable bit

In both modes, when enabled, these pins must be properly configured as input or output
- 1 = Enables the serial port and configures the SDA and SCL pins as the source of the serial port pins\(^{(2)}\)
- 0 = Disables serial port and configures these pins as I/O port pins

#### bit 4
**CKP:** Clock Polarity Select bit

**In I^2^C Slave mode:** SCL release control
- 1 = Enable clock
- 0 = Holds clock low (clock stretch). (Used to ensure data setup time.)

**In I^2^C Master mode:** Unused in this mode

#### bit 3-0
**SSPM<3:0>:** Synchronous Serial Port Mode Select bits

- 0000 = Reserved
- 0001 = Reserved
- 0010 = Reserved
- 0011 = Reserved
- 0100 = Reserved
- 0101 = Reserved
- 0110 = I^2^C Slave mode, 7-bit address
- 0111 = I^2^C Slave mode, 10-bit address
- 1000 = I^2^C Master mode, clock = \( F_{OSC} / (4 \times (SSPADD+1)) \)^{(3)}
- 1001 = Reserved
- 1010 = Reserved
- 1011 = I^2^C Firmware-Controlled Master mode (Slave idle)
- 1100 = Reserved
- 1101 = Reserved
- 1110 = I^2^C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
- 1111 = I^2^C Slave mode, 10-bit address with Start and Stop bit interrupts enabled

**Note 1:** In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.

**2:** When enabled, the SDA and SCL pins must be configured as inputs.

**3:** SSPADD values of 0, 1 or 2 are not supported for I^2^C mode.
REGISTER 27-3:  SSPCON2: SSP CONTROL REGISTER 2

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R-0/0</th>
<th>R/W-0/0</th>
<th>R/S/HS-0/0</th>
<th>R/S/HS-0/0</th>
<th>R/S/HS-0/0</th>
<th>R/S/HS-0/0</th>
<th>R/W/HS-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>GCEN</td>
<td>ACKSTAT</td>
<td>ACKDT</td>
<td>ACKEN</td>
<td>RCEN</td>
<td>PEN</td>
<td>RSEN</td>
<td>SEN</td>
</tr>
</tbody>
</table>

bit 7  GCEN: General Call Enable bit (in I2C Slave mode only)
1 = Enable interrupt when a general call address (0x00 or 00h) is received in the SSPSR register
0 = General call address disabled

bit 6  ACKSTAT: Acknowledge Status bit (in I2C mode only)
1 = Acknowledge was not received
0 = Acknowledge was received

bit 5  ACKDT: Acknowledge Data bit (in I2C mode only)
In Receive mode:
Value transmitted when the user initiates an Acknowledge sequence at the end of a receive
1 = Not Acknowledge
0 = Acknowledge

bit 4  ACKEN: Acknowledge Sequence Enable bit (in I2C Master mode only)
In Master Receive mode:
1 = Initiate Acknowledge sequence on SDA and SCL pins and transmit ACKDT data bit. Automatically cleared by hardware.
0 = Acknowledge sequence idle

bit 3  RCEN: Receive Enable bit (in I2C Master mode only)
1 = Enables Receive mode for I2C
0 = Receive idle

bit 2  PEN: Stop Condition Enable bit (in I2C Master mode only)
SCK Release Control:
1 = Initiate Stop condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Stop condition idle

bit 1  RSEN: Repeated Start Condition Enabled bit (in I2C Master mode only)
1 = Initiate Repeated Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Repeated Start condition idle

bit 0  SEN: Start Condition Enabled bit (in I2C Master mode only)
In Master mode:
1 = Initiate Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Start condition idle
In Slave mode:
1 = Clock stretching is enabled for both Slave Transmit and Slave Receive (stretch enabled)
0 = Clock stretching is disabled

Note 1: For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I2C module is not in the Idle mode, this bit may not be set (no spooling) and the SSPBUF may not be written (or writes to the SSPBUF are disabled).
REGISTER 27-4:  SSPCON3: SSP CONTROL REGISTER 3

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACKTIM</td>
<td>PCIE</td>
<td>SCIE</td>
<td>BOEN</td>
<td>SDAHT</td>
<td>SBCDE</td>
<td>AHEN</td>
<td>DHEN</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ’1’ = Bit is set
- ’0’ = Bit is cleared

bit 7  **ACKTIM**: Acknowledge Time status bit (I²C mode only)
1 = Indicates the I²C bus is in an Acknowledge sequence, set on 8th falling edge of SCL clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCL clock

bit 6  **PCIE**: Stop Condition Interrupt Enable bit (I²C mode only)
1 = Enable interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled

bit 5  **SCIE**: Start Condition Interrupt Enable bit (I²C mode only)
1 = Enable interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled

bit 4  **BOEN**: Buffer Overwrite Enable bit
In I²C Master mode:
This bit is ignored.
In I²C Slave mode:
1 = SSPBUF is updated and ACK is generated for a received address/data byte, ignoring the state of the SSPOV bit only if the BF bit = 0.
0 = SSPBUF is only updated when SSPOV is clear.

bit 3  **SDAHT**: SDA Hold Time Selection bit
1 = Minimum of 300 ns hold time on SDA after the falling edge of SCL
0 = Minimum of 100 ns hold time on SDA after the falling edge of SCL

bit 2  **SBCDE**: Slave Mode Bus Collision Detect Enable bit (I²C Slave mode only)
If, on the rising edge of SCL, SDA is sampled low when the module outputs a high state, the BCLIF bit in the PIR1 register is set and bus goes idle.
1 = Enable slave bus collision interrupts
0 = Slave bus collision interrupts are disabled

bit 1  **AHEN**: Address Hold Enable bit (I²C Slave mode only)
1 = Following the 8th falling edge of SCL for a matching received address byte; CKP bit in the SSPCON1 register will be cleared and the SCL will be held low.
0 = Address holding is disabled

bit 0  **DHEN**: Data Hold Enable bit (I²C Slave mode only)
1 = Following the 8th falling edge of SCL for a received data byte; slave hardware clears the CKP bit in the SSPCON1 register and SCL is held low.
0 = Data holding is disabled

**Note 1**: This bit has no effect in Slave modes where Start and Stop condition detection is explicitly listed as enabled.

**Note 2**: The ACKTIM status bit is only active when the AHEN bit or DHEN bit is set.
REGISTER 27-5:  SSPMSK1: SSP MASK REGISTER 1

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSK&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n = Value at POR
- '1' = Bit is set
- '0' = Bit is cleared

bit 7-1  MSK<7:1>: Mask bits
1 = The received address bit n is compared to SSPADD<n> to detect I^2C address match
0 = The received address bit n is not used to detect I^2C address match

bit 0  MSK<0>: Mask bit for I^2C Slave mode, 10-bit Address
I^2C Slave mode, 10-bit address (SSPM<3:0> = 0111 or 1111):
1 = The received address bit 0 is compared to SSPADD<0> to detect I^2C address match
0 = The received address bit 0 is not used to detect I^2C address match
I^2C Slave mode, 7-bit address, the bit is ignored

REGISTER 27-6:  SSPADD: MSSP ADDRESS AND BAUD RATE REGISTER 1

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- u = Bit is unchanged
- x = Bit is unknown
- -n = Value at POR
- '1' = Bit is set
- '0' = Bit is cleared

Master mode:
bit 7-0  ADD<7:0>: Baud Rate Clock Divider bits
SCL pin clock period = ((ADD<7:0> + 1) * 4)/FOSC

10-Bit Slave mode — Most Significant Address byte:
bit 7-3  Not used: Unused for Most Significant Address byte. Bit state of this register is a "don't care". Bit pattern sent by master is fixed by I^2C specification and must be equal to '11110'. However, those bits are compared by hardware and are not affected by the value in this register.

bit 2-1  ADD<2:1>: Two Most Significant bits of 10-bit address.
bit 0  Not used: Unused in this mode. Bit state is a "don't care".

10-Bit Slave mode — Least Significant Address byte:
bit 7-0  ADD<7:0>: Eight Least Significant bits of 10-bit address

7-Bit Slave mode:
bit 7-1  ADD<7:1>: 7-bit address
bit 0  Not used: Unused in this mode. Bit state is a "don't care".
REGISTER 27-7:  SSPMSK2: SSP MASK REGISTER 2

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n = Value at POR
‘1’ = Bit is set  ‘0’ = Bit is cleared

bit 7-1  MSK2<7:1>: Mask bits
1 = The received address bit n is compared to SSPADD2<n> to detect \( I^2C \) address match
0 = The received address bit n is not used to detect \( I^2C \) address match

bit 0  MSK2<0>: Mask bit for \( I^2C \) Slave mode, 10-bit Address
\( I^2C \) Slave mode, 10-bit address (SSPM<3:0> = 0111 or 1111):
1 = The received address bit 0 is compared to SSPADD2<0> to detect \( I^2C \) address match
0 = The received address bit 0 is not used to detect \( I^2C \) address match

REGISTER 27-8:  SSPADD2: MSSP ADDRESS 2

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
u = Bit is unchanged  x = Bit is unknown  -n = Value at POR
‘1’ = Bit is set  ‘0’ = Bit is cleared

Master mode:

bit 7-0  ADD2<7:0>: Baud Rate Clock Divider bits
SCL pin clock period = \(((ADD<7:0> + 1) * 4)/F_{OSC}\)

10-Bit Slave mode — Most Significant Address byte:

bit 7-3  Not used: Unused for Most Significant Address byte. Bit state of this register is a “don’t care”. Bit pattern sent by master is fixed by \( I^2C \) specification and must be equal to ‘11110’. However, those bits are compared by hardware and are not affected by the value in this register.

bit 2-1  ADD2<2:1>: Two Most Significant bits of 10-bit address
bit 0  Not used: Unused in this mode. Bit state is a “don’t care”.

10-Bit Slave mode — Least Significant Address byte:

bit 7-0  ADD2<7:0>: Eight Least Significant bits of 10-bit address

7-Bit Slave mode:

bit 7-1  ADD2<7:1>: 7-bit address
bit 0  Not used: Unused in this mode. Bit state is a “don’t care”.

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28.0 INSTRUCTION SET SUMMARY

The MCP19122/3 instruction set is highly orthogonal and comprises three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each instruction is a 14-bit word divided into an **opcode**, which specifies the instruction type, and one or more **operands**, which further specify the operation of the instruction. The formats for each of the categories is presented in **Figure 28-1**, while the various opcode fields are summarized in **Table 28-1**.

**Table 28-2** lists the instructions recognized by the MPASMTM assembler.

For **byte-oriented** instructions, ‘f’ represents a file register designator and ‘d’ represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If ‘d’ is zero, the result is placed in the W register. If ‘d’ is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, ‘b’ represents a bit field designator, which selects the bit affected by the operation, while ‘f’ represents the address of the file in which the bit is located.

For **literal and control** operations, ‘k’ represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 µs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a **NOP**.

All instruction examples use the format ‘0xhh’ to represent a hexadecimal number, where ‘h’ signifies a hexadecimal digit.

### 28.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (RMW) operation. The register is read, the data is modified, and the result is stored according to either the instruction or the destination designator ‘d’. A read operation is performed on a register even if the instruction writes to that register.

For example, a **CLRF PORTA** instruction will read PORTGPA, clear all the data bits, then write the result back to PORTGPA. This example would have the unintended consequence of clearing the condition that set the IOCF flag.

#### TABLE 28-1: OPCODE FIELD DESCRIPTIONS

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>f</td>
<td>Register file address (0x00 to 0x7F)</td>
</tr>
<tr>
<td>W</td>
<td>Working register (accumulator)</td>
</tr>
<tr>
<td>b</td>
<td>Bit address within an 8-bit file register</td>
</tr>
<tr>
<td>k</td>
<td>Literal field, constant data or label</td>
</tr>
<tr>
<td>x</td>
<td>Don’t care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.</td>
</tr>
<tr>
<td>d</td>
<td>Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.</td>
</tr>
<tr>
<td>PC</td>
<td>Program Counter</td>
</tr>
<tr>
<td>TO</td>
<td>Time-Out bit</td>
</tr>
<tr>
<td>C</td>
<td>Carry bit</td>
</tr>
<tr>
<td>DC</td>
<td>Digit carry bit</td>
</tr>
<tr>
<td>Z</td>
<td>Zero bit</td>
</tr>
<tr>
<td>PD</td>
<td>Power-Down bit</td>
</tr>
</tbody>
</table>

#### FIGURE 28-1: GENERAL FORMAT FOR INSTRUCTIONS

### Byte-Oriented file register operations

<table>
<thead>
<tr>
<th>13</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPCODE</td>
<td>d</td>
<td>f (FILE #)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- d = 0 for destination W
- d = 1 for destination f
- f = 7-bit file register address

### Bit-Oriented file register operations

<table>
<thead>
<tr>
<th>13</th>
<th>10</th>
<th>9</th>
<th>7</th>
<th>6</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPCODE</td>
<td>b (BIT #)</td>
<td>f (FILE #)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- b = 3-bit bit address
- f = 7-bit file register address

### Literal and control operations

#### General

<table>
<thead>
<tr>
<th>13</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPCODE</td>
<td>k (literal)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- k = 8-bit immediate value

#### CALL and GOTO instructions only

<table>
<thead>
<tr>
<th>13</th>
<th>11</th>
<th>10</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPCODE</td>
<td>k (literal)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- k = 11-bit immediate value
## TABLE 28-2: MCP19122/3 INSTRUCTION SET

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycles</th>
<th>14-Bit Opcode</th>
<th>Status Affected</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSb</td>
<td>LSb</td>
<td></td>
</tr>
<tr>
<td><strong>BYTE-ORIENTED FILE REGISTER OPERATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADDWF, f, d</td>
<td>Add W and f</td>
<td>1</td>
<td>00 0111 dffe</td>
<td>fffe</td>
<td>C, DC, Z</td>
</tr>
<tr>
<td>ANDWF, f, d</td>
<td>AND W with f</td>
<td>1</td>
<td>00 0101 dffe</td>
<td>fffe</td>
<td>Z</td>
</tr>
<tr>
<td>CLRF, f</td>
<td>Clear f</td>
<td>1</td>
<td>00 0001 1ffe</td>
<td>fffe</td>
<td>Z</td>
</tr>
<tr>
<td>CLRW</td>
<td>Clear W</td>
<td>1</td>
<td>00 0001 0xxx</td>
<td>xxxx</td>
<td>Z</td>
</tr>
<tr>
<td>COMF, f, d</td>
<td>Complement f</td>
<td>1</td>
<td>00 1001 dffe</td>
<td>fffe</td>
<td>Z</td>
</tr>
<tr>
<td>DECF, f, d</td>
<td>Decrement f</td>
<td>1</td>
<td>00 0011 dffe</td>
<td>fffe</td>
<td>Z</td>
</tr>
<tr>
<td>DECFSZ, f, d</td>
<td>Decrement f, Skip if 0</td>
<td>1(2)</td>
<td>00 1011 dffe</td>
<td>fffe</td>
<td>Z</td>
</tr>
<tr>
<td>INCF, f, d</td>
<td>Increment f</td>
<td>1</td>
<td>00 1010 dffe</td>
<td>fffe</td>
<td>Z</td>
</tr>
<tr>
<td>INCFSZ, f, d</td>
<td>Increment f, Skip if 0</td>
<td>1(2)</td>
<td>00 1111 dffe</td>
<td>fffe</td>
<td>Z</td>
</tr>
<tr>
<td>IORWF, f, d</td>
<td>Inclusive OR W with f</td>
<td>1</td>
<td>00 0100 dffe</td>
<td>fffe</td>
<td>Z</td>
</tr>
<tr>
<td>MOVF, f, d</td>
<td>Move f</td>
<td>1</td>
<td>00 1000 dffe</td>
<td>fffe</td>
<td>Z</td>
</tr>
<tr>
<td>MOVWF, f</td>
<td>Move W to f</td>
<td>1</td>
<td>00 0000 1ffe</td>
<td>fffe</td>
<td>Z</td>
</tr>
<tr>
<td>NOP</td>
<td>No Operation</td>
<td>1</td>
<td>00 0000 0xx0</td>
<td>0000</td>
<td>C, DC, Z</td>
</tr>
<tr>
<td>RLF, f, d</td>
<td>Rotate Left f through Carry</td>
<td>1</td>
<td>00 1110 dffe</td>
<td>fffe</td>
<td>C</td>
</tr>
<tr>
<td>RRF, f, d</td>
<td>Rotate Right f through Carry</td>
<td>1</td>
<td>00 1100 dffe</td>
<td>fffe</td>
<td>C</td>
</tr>
<tr>
<td>SUBWF, f, d</td>
<td>Subtract W from f</td>
<td>1</td>
<td>00 0010 dffe</td>
<td>fffe</td>
<td>C, DC, Z</td>
</tr>
<tr>
<td>SWAPF, f, d</td>
<td>Swap nibbles in f</td>
<td>1</td>
<td>00 1110 dffe</td>
<td>fffe</td>
<td>1, 2</td>
</tr>
<tr>
<td>XORWF, f, d</td>
<td>Exclusive OR W with f</td>
<td>1</td>
<td>00 0110 dffe</td>
<td>fffe</td>
<td>Z</td>
</tr>
<tr>
<td><strong>BIT-ORIENTED FILE REGISTER OPERATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BCF, f, b</td>
<td>Bit Clear f</td>
<td>1</td>
<td>01 00bb bffe</td>
<td>fffe</td>
<td>1, 2</td>
</tr>
<tr>
<td>BSF, f, b</td>
<td>Bit Set f</td>
<td>1</td>
<td>01 01bb bffe</td>
<td>fffe</td>
<td>1, 2</td>
</tr>
<tr>
<td>BTFSC, f, b</td>
<td>Bit Test f, Skip if Clear</td>
<td>1 (2)</td>
<td>01 10bb bffe</td>
<td>fffe</td>
<td>3</td>
</tr>
<tr>
<td>BTFSS, f, b</td>
<td>Bit Test f, Skip if Set</td>
<td>1 (2)</td>
<td>01 11bb bffe</td>
<td>fffe</td>
<td>3</td>
</tr>
<tr>
<td><strong>LITERAL AND CONTROL OPERATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADDLW, k</td>
<td>Add literal and W</td>
<td>1</td>
<td>11 111x kkkk</td>
<td>kkkk</td>
<td>C, DC, Z</td>
</tr>
<tr>
<td>ANDLW, k</td>
<td>AND literal with W</td>
<td>1</td>
<td>11 1001 kkkk</td>
<td>kkkk</td>
<td>Z</td>
</tr>
<tr>
<td>CALL, k</td>
<td>Call Subroutine</td>
<td>2</td>
<td>10 kkkk kkkk</td>
<td>kkkk</td>
<td>TO, PD</td>
</tr>
<tr>
<td>CLRWDT</td>
<td>Clear Watchdog Timer</td>
<td>1</td>
<td>00 0000 0110 0100</td>
<td>0100</td>
<td></td>
</tr>
<tr>
<td>GOTO, k</td>
<td>Go to address</td>
<td>2</td>
<td>10 1kkk kkkk</td>
<td>kkkk</td>
<td>Z</td>
</tr>
<tr>
<td>IORLW, k</td>
<td>Inclusive OR literal with W</td>
<td>1</td>
<td>11 1000 kkkk</td>
<td>kkkk</td>
<td>Z</td>
</tr>
<tr>
<td>MOVLW, k</td>
<td>Move literal to W</td>
<td>1</td>
<td>11 00xx kkkk</td>
<td>kkkk</td>
<td>Z</td>
</tr>
<tr>
<td>RETFIE</td>
<td>Return from interrupt</td>
<td>2</td>
<td>00 0000 0000 1001</td>
<td>1001</td>
<td></td>
</tr>
<tr>
<td>RETLW, k</td>
<td>Return with literal in W</td>
<td>2</td>
<td>11 01xx kkkk</td>
<td>kkkk</td>
<td>Z</td>
</tr>
<tr>
<td>RETURN</td>
<td>Return from Subroutine</td>
<td>2</td>
<td>00 0000 0000 1000</td>
<td>1000</td>
<td></td>
</tr>
<tr>
<td>SLEEP, k</td>
<td>Go into Standby mode</td>
<td>1</td>
<td>00 0000 0110 0011</td>
<td>0011</td>
<td></td>
</tr>
<tr>
<td>SUBLW, k</td>
<td>Subtract W from literal</td>
<td>1</td>
<td>11 110x kkkk</td>
<td>kkkk</td>
<td>C, DC, Z</td>
</tr>
<tr>
<td>XORLW, k</td>
<td>Exclusive OR literal with W</td>
<td>1</td>
<td>11 1010 kkkk</td>
<td>kkkk</td>
<td>Z</td>
</tr>
</tbody>
</table>

**Note 1:** When an I/O register is modified as a function of itself (e.g., \texttt{MOVF PORTA, 1}), the value used will be that value present on the pins themselves. For example, if the data latch is ‘1’ for a pin configured as input and is driven low by an external device, the data will be written back with a ‘0’.

**Note 2:** If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

**Note 3:** If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a \texttt{NOP}.
### 28.2 Instruction Descriptions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ADDLW</strong> Add literal and W</td>
<td>The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.</td>
</tr>
<tr>
<td><strong>ADDWF</strong> Add W and f</td>
<td>Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.</td>
</tr>
<tr>
<td><strong>ANDLW</strong> AND literal with W</td>
<td>The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.</td>
</tr>
<tr>
<td><strong>ANDWF</strong> AND W with f</td>
<td>AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.</td>
</tr>
<tr>
<td><strong>BCF</strong> Bit Clear f</td>
<td>Bit 'b' in register 'f' is cleared.</td>
</tr>
<tr>
<td><strong>BSF</strong> Bit Set f</td>
<td>Bit 'b' in register 'f' is set.</td>
</tr>
</tbody>
</table>
| **BTFSC** Bit Test f, Skip if Clear | If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b' in register 'f' is '0', the next instruction is discarded, and a NOP is executed instead, making this a two-cycle instruction.
<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
</table>
| **BTFSS** Bit Test f, Skip if Set | Syntax: `[ label ] BTFSS f,b  
Operands: 0 ≤ f ≤ 127  
0 ≤ b < 7  
Operation: skip if (f<b) = 1  
Status Affected: None  
Description: If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a two-cycle instruction.** |
| **CALL** Call Subroutine | Syntax: `[ label ] CALL k  
Operands: 0 ≤ k ≤ 2047  
Operation: (PC)+ 1 → TOS,  
k → PC<10:0>,  
(PCLATH<4:3>) → PC<12:11>  
Status Affected: None  
Description: Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The 11-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.** |
| **CLRF** Clear f | Syntax: `[ label ] CLRF f  
Operands: 0 ≤ f ≤ 127  
Operation: 00h → (f),  
1 → Z  
Status Affected: Z  
Description: The contents of register ‘f’ are cleared and the Z bit is set.** |
| **CLRWD** Clear Watchdog Timer | Syntax: `[ label ] CLRWD  
Operands: None  
Operation: 00h → WDT  
0 → WDT prescaler,  
1 → TO  
1 → PD  
Status Affected: TO, PD  
Description: CLRWD instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits TO and PD are set.** |
| **COMF** Complement f | Syntax: `[ label ] COMF f,d  
Operands: 0 ≤ f ≤ 127  
d ∈ [0,1]  
Operation: (f) → (destination)  
Status Affected: Z  
Description: The contents of register ‘f’ are complemented. If ‘d’ is ‘0’, the result is stored in W. If ‘d’ is ‘1’, the result is stored back in register ‘f’.** |
| **CLRW** Clear W | Syntax: `[ label ] CLRW  
Operands: None  
Operation: 00h → (W),  
1 → Z  
Status Affected: Z  
Description: W register is cleared. Zero bit (Z) is set.** |
| **DECF** Decrement f | Syntax: `[ label ] DECF f,d  
Operands: 0 ≤ f ≤ 127  
d ∈ [0,1]  
Operation: (f) - 1 → (destination)  
Status Affected: Z  
Description: Decrement register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.** |
<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DECFSZ</strong></td>
<td>Decrement f, Skip if 0</td>
</tr>
<tr>
<td>Syntax:</td>
<td><code>[ label ] DECFSZ  f,d</code></td>
</tr>
</tbody>
</table>
| Operands:   | $0 \leq f \leq 127$  
              | $d \in [0,1]$ |
| Operation:  | $(f) - 1 \rightarrow \text{(destination)}$; 
              | skip if result = 0 |
| Status Affected: | None |
| Description: | The contents of register ‘f’ are decremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. If the result is ‘1’, the next instruction is executed. If the result is ‘0’, a NOP is executed instead, making it a two-cycle instruction. |

<table>
<thead>
<tr>
<th><strong>GOTO</strong></th>
<th>Unconditional Branch</th>
</tr>
</thead>
<tbody>
<tr>
<td>Syntax:</td>
<td><code>[ label ] GOTO  k</code></td>
</tr>
<tr>
<td>Operands:</td>
<td>$0 \leq k \leq 2047$</td>
</tr>
</tbody>
</table>
| Operation:  | $k \rightarrow \text{PC}<10:0>$  
              | $\text{PCLATH}<4:3> \rightarrow \text{PC}<12:11>$ |
| Status Affected: | None |
| Description: | **GOTO** is an unconditional branch. The eleven-bit immediate value is loaded into PC bits $<10:0>$. The upper bits of PC are loaded from PCLATH $<4:3>$. **GOTO** is a two-cycle instruction. |

<table>
<thead>
<tr>
<th><strong>INCFSZ</strong></th>
<th>Increment f, Skip if 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Syntax:</td>
<td><code>[ label ] INCFSZ  f,d</code></td>
</tr>
</tbody>
</table>
| Operands:   | $0 \leq f \leq 127$  
              | $d \in [0,1]$ |
| Operation:  | $(f) + 1 \rightarrow \text{(destination)}$; 
              | skip if result = 0 |
| Status Affected: | None |
| Description: | The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. |

<table>
<thead>
<tr>
<th><strong>IORLW</strong></th>
<th>Inclusive OR literal with W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Syntax:</td>
<td><code>[ label ] IORLW  k</code></td>
</tr>
<tr>
<td>Operands:</td>
<td>$0 \leq k \leq 255$</td>
</tr>
<tr>
<td>Operation:</td>
<td>$(W) \text{ .OR. } k \rightarrow (W)$</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>Z</td>
</tr>
<tr>
<td>Description:</td>
<td>The contents of the W register are OR’ed with the 8-bit literal ‘k’. The result is placed in the W register.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>INCF</strong></th>
<th>Increment f</th>
</tr>
</thead>
<tbody>
<tr>
<td>Syntax:</td>
<td><code>[ label ] INCF  f,d</code></td>
</tr>
</tbody>
</table>
| Operands:   | $0 \leq f \leq 127$  
              | $d \in [0,1]$ |
| Operation:  | $(f) + 1 \rightarrow \text{(destination)}$ |
| Status Affected: | Z |
| Description: | The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. |

<table>
<thead>
<tr>
<th><strong>IORWF</strong></th>
<th>Inclusive OR W with f</th>
</tr>
</thead>
<tbody>
<tr>
<td>Syntax:</td>
<td><code>[ label ] IORWF  f,d</code></td>
</tr>
</tbody>
</table>
| Operands:   | $0 \leq f \leq 127$  
              | $d \in [0,1]$ |
| Operation:  | $(W) \text{ .OR. } (f) \rightarrow \text{(destination)}$ |
| Status Affected: | Z |
| Description: | Inclusive OR the W register with register ‘f’. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. |
MOVF  Move f

Syntax: \[
[\text{label}] \quad \text{MOVF} \quad f, \text{d}
\]

Operands: 
- \(0 \leq f \leq 127\)
- \(d \in \{0, 1\}\)

Operation: \(f \rightarrow (\text{dest})\)

Status Affected: \(Z\)

Description: The contents of register 'f' is moved to a destination dependent upon the status of 'd'. If \(d = 0\), destination is W register. If \(d = 1\), the destination is file register 'f' itself. \(d = 1\) is useful to test a file register since Status flag Z is affected.

Words: 1
Cycles: 1

Example: MOVF FSR, 0

After Instruction
- \(W = \text{value in FSR register}\)
- \(Z = 1\)

MOVLW  Move literal to W

Syntax: \[
[\text{label}] \quad \text{MOVLW} \quad k
\]

Operands: \(0 \leq k \leq 255\)

Operation: \(k \rightarrow (W)\)

Status Affected: None

Description: The eight-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.

Words: 1
Cycles: 1

Example: MOVLW 0x5A

After Instruction
- \(W = 0x5A\)

MOVWF  Move W to f

Syntax: \[
[\text{label}] \quad \text{MOVWF} \quad f
\]

Operands: \(0 \leq f \leq 127\)

Operation: \((W) \rightarrow (f)\)

Status Affected: None

Description: Move data from W register to register 'f'.

Words: 1
Cycles: 1

Example: MOVW OPTION F

Before Instruction
- \(\text{OPTION} = 0xFF\)
- \(W = 0x4F\)

After Instruction
- \(\text{OPTION} = 0x4F\)
- \(W = 0x4F\)

NOP  No Operation

Syntax: \[
[\text{label}] \quad \text{NOP}
\]

Operands: None

Operation: No operation

Status Affected: None

Description: No operation.

Words: 1
Cycles: 1

Example: NOP
<table>
<thead>
<tr>
<th><strong>RETFIE</strong></th>
<th><strong>Return from Interrupt</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Syntax:</td>
<td>[ label ] RETFIE</td>
</tr>
<tr>
<td>Operands:</td>
<td>None</td>
</tr>
<tr>
<td>Operation:</td>
<td>TOS → PC, ( 1 ) → GIE</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>None</td>
</tr>
<tr>
<td>Description:</td>
<td>Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON&lt;7&gt;). This is a two-cycle instruction.</td>
</tr>
<tr>
<td>Words:</td>
<td>1</td>
</tr>
<tr>
<td>Cycles:</td>
<td>2</td>
</tr>
<tr>
<td>Example:</td>
<td>RETFIE</td>
</tr>
</tbody>
</table>

After Interrupt

\[
\begin{align*}
\text{PC} &= \text{TOS} \\
\text{GIE} &= \ 1
\end{align*}
\]

<table>
<thead>
<tr>
<th><strong>RETLW</strong></th>
<th><strong>Return with literal in W</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Syntax:</td>
<td>[ label ] RETLW ( k )</td>
</tr>
<tr>
<td>Operands:</td>
<td>( 0 \leq k \leq 255 )</td>
</tr>
<tr>
<td>Operation:</td>
<td>( k ) → (W); TOS → PC</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>None</td>
</tr>
<tr>
<td>Description:</td>
<td>The W register is loaded with the 8-bit literal ‘k’. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.</td>
</tr>
<tr>
<td>Words:</td>
<td>1</td>
</tr>
<tr>
<td>Cycles:</td>
<td>2</td>
</tr>
<tr>
<td>Example:</td>
<td>CALL TABLE;W contains</td>
</tr>
<tr>
<td></td>
<td>;table offset</td>
</tr>
<tr>
<td></td>
<td>;value</td>
</tr>
<tr>
<td></td>
<td>GOTO DONE</td>
</tr>
<tr>
<td></td>
<td>TABLE</td>
</tr>
<tr>
<td></td>
<td>•</td>
</tr>
<tr>
<td></td>
<td>•</td>
</tr>
<tr>
<td></td>
<td>ADDWF PC ;W = offset</td>
</tr>
<tr>
<td></td>
<td>RETLW k1 ;Begin table</td>
</tr>
<tr>
<td></td>
<td>RETLW k2 ;</td>
</tr>
<tr>
<td></td>
<td>•</td>
</tr>
<tr>
<td></td>
<td>•</td>
</tr>
<tr>
<td></td>
<td>RETLW kn ;End of table</td>
</tr>
<tr>
<td></td>
<td>DONE</td>
</tr>
</tbody>
</table>

Before Instruction

\[
W = 0x07
\]

After Instruction

\[
W = \text{value of k8}
\]

<table>
<thead>
<tr>
<th><strong>RETURN</strong></th>
<th><strong>Return from Subroutine</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Syntax:</td>
<td>[ label ] RETURN</td>
</tr>
<tr>
<td>Operands:</td>
<td>None</td>
</tr>
<tr>
<td>Operation:</td>
<td>TOS → PC</td>
</tr>
<tr>
<td>Status Affected:</td>
<td>None</td>
</tr>
<tr>
<td>Description:</td>
<td>Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.</td>
</tr>
</tbody>
</table>
### RLF  Rotate Left f through Carry

**Syntax:**  
\[ \text{[label]} \] RLF  \text{f,d}  

**Operands:**  
\[ 0 \leq f \leq 127\]  
\[ d \in [0,1] \]  

**Operation:**  
See description below  

**Status Affected:**  
C  

**Description:**  
The contents of register ‘f’ are rotated one bit to the left through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

**Words:**  
1  

**Cycles:**  
1  

**Example:**  
RLF REG1,0  

**Before Instruction**  
\[
\begin{align*}
\text{REG1} &= 1110 \\
0110 &= 0 \\
C &= 0
\end{align*}
\]  

**After Instruction**  
\[
\begin{align*}
\text{REG1} &= 1110 \\
0110 &= W \\
1100 &= 1100 \\
C &= 1
\end{align*}
\]

### RRF  Rotate Right f through Carry

**Syntax:**  
\[ \text{[label]} \] RRF  \text{f,d}  

**Operands:**  
\[ 0 \leq f \leq 127\]  
\[ d \in [0,1] \]  

**Operation:**  
See description below  

**Status Affected:**  
C  

**Description:**  
The contents of register ‘f’ are rotated one bit to the right through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.

### SLEEP  Enter Sleep mode

**Syntax:**  
\[ \text{[label]} \] SLEEP  

**Operands:**  
None  

**Operation:**  
00h \rightarrow \text{WDT},  
0 \rightarrow \text{WDT prescaler},  
1 \rightarrow \text{TO},  
0 \rightarrow \text{PD}  

**Status Affected:**  
\text{TO, PD}  

**Description:**  
The power-down Status bit, \text{PD} is cleared. Time-out Status bit, \text{TO} is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

### SUBLW  Subtract W from literal

**Syntax:**  
\[ \text{[label]} \] SUBLW  \text{k}  

**Operands:**  
\[ 0 \leq k \leq 255 \]  

**Operation:**  
k - (W) \rightarrow (W)  

**Status Affected:**  
C, DC, Z  

**Description:**  
The W register is subtracted (two’s complement method) from the 8-bit literal ‘k’. The result is placed in the W register.

<table>
<thead>
<tr>
<th>Result</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>C = 0</td>
<td>W &gt; k</td>
</tr>
<tr>
<td>C = 1</td>
<td>W ≤ k</td>
</tr>
<tr>
<td>DC = 0</td>
<td>W&lt;3:0&gt; &gt; k&lt;3:0&gt;</td>
</tr>
<tr>
<td>DC = 1</td>
<td>W&lt;3:0&gt; ≤ k&lt;3:0&gt;</td>
</tr>
</tbody>
</table>
### MCP19122/3

#### SUBWF

**Subtract W from f**

**Syntax:** \([ label ]\) SUBWF f,d

**Operands:**

- \(0 \leq f \leq 127\)
- \(d \in [0,1]\)

**Operation:** \((f) - (W) \rightarrow (\text{destination})\)

**Status Affected:** C, DC, Z

**Description:** Subtract (two's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

<table>
<thead>
<tr>
<th>C = 0</th>
<th>W &gt; f</th>
</tr>
</thead>
<tbody>
<tr>
<td>C = 1</td>
<td>W ≤ f</td>
</tr>
<tr>
<td>DC = 0</td>
<td>W&lt;3:0&gt; &gt; f&lt;3:0&gt;</td>
</tr>
<tr>
<td>DC = 1</td>
<td>W&lt;3:0&gt; ≤ f&lt;3:0&gt;</td>
</tr>
</tbody>
</table>

#### XORWF

**Exclusive OR W with f**

**Syntax:** \([ label ]\) XORWF f,d

**Operands:**

- \(0 \leq f \leq 127\)
- \(d \in [0,1]\)

**Operation:** \((W) . \text{XOR.} (f) \rightarrow (\text{destination})\)

**Status Affected:** Z

**Description:** Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

#### SWAPF

**Swap Nibbles in f**

**Syntax:** \([ label ]\) SWAPF f,d

**Operands:**

- \(0 \leq f \leq 127\)
- \(d \in [0,1]\)

**Operation:**

- \((f<3:0>) \rightarrow \text{(destination<7:4>)}\)
- \((f<7:4>) \rightarrow \text{(destination<3:0>)}\)

**Status Affected:** None

**Description:** The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

#### XORLW

**Exclusive OR literal with W**

**Syntax:** \([ label ]\) XORLW k

**Operands:**

- \(0 \leq k \leq 255\)

**Operation:** \((W) . \text{XOR.} k \rightarrow (W)\)

**Status Affected:** Z

**Description:** The contents of the W register are XOR'ed with the 8-bit literal 'k'. The result is placed in the W register.
29.0 IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

ICSP programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process, allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP programming:
- ICSPCLK
- ICSPDAT
- MCLR
- VDD
- VSS

In Program/Verify mode the Program Memory, User IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input. The device is placed into a Program/Verify mode by holding the ICSPDAT and ICSPCLK pins low, while raising the MCLR pin from VIL to VIHH.

29.1 Common Programming Interfaces

Connection to a target device is typically done through an ICSP header. A commonly found connector on development tools is the RJ-11 in the 6P6C (6-pin, 6-connector) configuration. See Figure 29-1.

**FIGURE 29-1: ICD RJ-11 STYLE CONNECTOR INTERFACE**

Another connector often found in use with the PICkit™ programmers is a standard 6-pin header with 0.1 inch spacing. Refer to Figure 29-2.

**FIGURE 29-2: PICkit-STYLE CONNECTOR INTERFACE**

*The 6-pin header (0.100" spacing) accepts 0.025" square pins.*
For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices, such as resistors, diodes, or even jumpers. See Figure 29-3 for more information.

FIGURE 29-3: TYPICAL CONNECTION FOR ICSP PROGRAMMING

29.2 In-Circuit Debugger

In-circuit debugging requires access to the ICDCLK, ICDDATA and MCLR pins. These pins are only available on the MCP19123 device.
30.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/
    MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for
    Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards,
  Evaluation Kits and Starter Kits
- Third-party development tools

30.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:
- Color syntax highlighting
- Smart code completion makes suggestions and
  provides hints as you type
- Automatic code formatting based on user-defined
  rules
- Live parsing

User-Friendly, Customizable Interface:
- Fully customizable interface: toolbars, toolbar
  buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:
- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:
- Local file history feature
- Built-in support for Bugzilla issue tracker
30.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip’s 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

• Support for the entire device instruction set
• Support for fixed-point and floating-point data
• Command-line interface
• Rich directive set
• Flexible macro language
• MPLAB X IDE compatibility

30.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

• Integration into MPLAB X IDE projects
• User-defined macros to streamline assembly code
• Conditional assembly for multipurpose source files
• Directives that allow complete control over the assembly process

30.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

• Efficient linking of single libraries instead of many smaller files
• Enhanced code maintainability by grouping related modules together
• Flexible creation of libraries with easy module listing, replacement, deletion and extraction

30.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

• Support for the entire device instruction set
• Support for fixed-point and floating-point data
• Command-line interface
• Rich directive set
• Flexible macro language
• MPLAB X IDE compatibility
### 30.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers. The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

### 30.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip’s next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer’s PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradeable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to 3 meters) interconnection cables.

### 30.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip’s most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer’s PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

### 30.9 PICkit 3 In-Circuit Debugger/Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer’s PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

### 30.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at \( V_{DD_MIN} \) and \( V_{DD_MAX} \) for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.
30.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELoo® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC and flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

30.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

• Device programmers and gang programmers from companies such as SoftLog and CCS
• Software tools from companies such as Gimpel and Trace Systems
• Protocol analyzers from companies such as Saleae and Total Phase
• Demonstration boards from companies such as MikroElektronika, Digilent® and Olimex
• Embedded Ethernet solutions from companies such as EZ Web Lynx, WIZnet and IPLogika®
31.0 PACKAGING INFORMATION

31.1 Package Marking Information

Legend:

XX...X Customer-specific information
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WWW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code
* Pb-free JEDEC designator for Matte Tin (Sn)

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
24-Lead Plastic Quad Flat, No Lead Package (MJ) – 4x4x0.9 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

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**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-143A
24-Lead Plastic Quad Flat, No Lead Package (MJ) - 4x4 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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**RECOMMENDED LAND PATTERN**

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Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2143B
28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing C04-140C Sheet 1 of 2
28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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Microchip Technology Drawing C04-140C Sheet 2 of 2
28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5 mm Body [QFN] Land Pattern With 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2140A
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<td>Package</td>
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Device:
- MCP19122: Digitally Enhanced Power Analog Controller with Integrated Synchronous Driver
- MCP19123: Digitally Enhanced Power Analog Controller with Integrated Synchronous Driver

Tape and Reel Option:
- Blank = Standard packaging (tube)
- T = Tape and Reel

Temperature Range:
- E = -40°C to +125°C (Extended)

Package:
- MJ = 24-Lead Plastic Quad Flat, No Lead Package - 4x4 mm Body (QFN)
- MQ = 28-Lead Plastic Quad Flat, No Lead Package - 5x5 mm Body (QFN)

Examples:
- a) MCP19122-E/MJ: Extended temperature, 24 LD QFN 4x4 package
- b) MCP19122T-E/MJ: Tape and Reel, Extended temperature, 24 LD QFN 4x4 package
- a) MCP19123-E/MQ: Extended temperature, 28 LD QFN 5x5 package
- b) MCP19123T-E/MQ: Tape and Reel, Extended temperature, 28 LD QFN 5x5 package

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