Features

- Hyper Speed Control® Architecture Enables:
  - High Input to Output Voltage Conversion Ratio Capability (VIN = 75V and VOUT = 0.6V)
  - Small Output Capacitance
- 4.5V to 75V Input Voltage
- 5A Output Current Capability with up to 95% Efficiency
- Adjustable Output Voltage from 0.6V to 32V
- ±1% FB Accuracy
- Any Capacitor™ Stable:
  - Zero-ESR to High-ESR Output Capacitors
- 270 kHz to 800 kHz Adjustable Switching Frequency
- Internal Compensation
- Built-in 5V Regulator for Single-Supply Operation
- Auxiliary Bootstrap LDO for Improving System Efficiency
- Internal Bootstrap Diode
- Adjustable Soft Start Time
- Programmable Current Limit
- "Hiccup" Mode Short-Circuit Protection
- Thermal Shutdown
- Supports Safe Start-up into a Prebiased Output
- -40°C to +125°C Junction Temperature Range
- Available in 32-Pin, 6 mm x 6 mm VQFN Package

Applications

- Distributed Power Systems
- Communications/Networking Infrastructure
- Industrial Power Supplies
- Solar Energy

General Description

The MIC28514 is an adjustable frequency, synchronous buck regulator that features a unique adaptive on-time control architecture. The MIC28514 operates over an input supply range of 4.5V to 75V, and provides a regulated output of up to 5A of output current. The output voltage is adjustable down to 0.6V with an accuracy of ±1%.

Hyper Speed Control architecture allows for an ultra-fast transient response, while reducing the output capacitance, and also makes high-VIN/low-VOUT operation possible. This adaptive on-time control architecture combines the advantages of fixed frequency operation and fast transient response in a single device.

The MIC28514 offers a full suite of features that ensure the protection of the Integrated Circuit (IC) during Fault conditions. These features include Undervoltage Lockout (UVLO) to ensure proper operation under power sag conditions, soft start to reduce inrush current, "Hiccup" mode short-circuit protection and thermal shutdown.

Typical Application Circuit
1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

PVIN, SVIN, FREQ to PGND ................................................................. -0.3V to +76V
PVDD, VDD to PGND ........................................................................ -0.3V to +6V
SW, ILIM to PGND ........................................................................... -0.3V to (PVIN + 0.3V)
VBST to VSW .................................................................................... -0.3V to +6V
VBST to PGND .................................................................................-0.3V to +82V
EN to AGND ..................................................................................... -0.3V to (SVIN + 0.3V)
FB, PG to AGND ............................................................................. -0.3V to (VDD + 0.3V)
EXTVDD to AGND ...........................................................................-0.3V to +12V
PGND to SGND ................................................................................-0.3V to +0.3V
Junction Temperature .................................................................... +150°C
Storage Temperature ...................................................................... -65°C to +150°C
ESD Rating(1) .................................................................................. 1 kV

Operating Ratings‡

Supply Voltage (SVIN, PVIN) ............................................................ 4.5V to 75V
Bias Voltage (PVDD, VDD) ............................................................... 4.5V to 5.5V
EN, FB, PG ...................................................................................... 0V to VDD
EXTVDD .......................................................................................... 0V to 12V
Junction Temperature ................................................................... -40°C to +125°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not ensured to function outside its operating ratings.

TABLE 1-1: ELECTRICAL CHARACTERISTICS(1)

<p>| Electrical Characteristics: PVIN = 12V, VOUT = 5V, VDD = 5V, VBST - VSW = 5V; fSW = 300 kHz, RCL = 1.42 kΩ, L = 8.2 µH; TA = +25°C, unless noted. Boldface values indicate -40°C ≤ TJ ≤ +125°C. |
|---|---|---|---|---|
| Electrical Characteristics: PVIN = 12V, VOUT = 5V, VDD = 5V, VBST - VSW = 5V; fSW = 300 kHz, RCL = 1.42 kΩ, L = 8.2 µH; TA = +25°C, unless noted. Boldface values indicate -40°C ≤ TJ ≤ +125°C. |</p>
<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Input</td>
<td>PVIN, SVIN</td>
<td>4.5</td>
<td>—</td>
<td>75</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VDD Bias Voltage</td>
<td>VDD</td>
<td>4.8</td>
<td>5.1</td>
<td>5.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Operating Bias Voltage</td>
<td>VDD</td>
<td>4.8</td>
<td>5.1</td>
<td>5.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Undervoltage Lockout Trip Level</td>
<td>UVLO</td>
<td>3.7</td>
<td>4.2</td>
<td>4.6</td>
<td>V</td>
<td>VDD rising</td>
</tr>
<tr>
<td>UVLO Hysteresis</td>
<td>UVLO_HYS</td>
<td>—</td>
<td>600</td>
<td>—</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>VDD Dropout Voltage</td>
<td>VDD</td>
<td>700</td>
<td>—</td>
<td>1250</td>
<td>mV</td>
<td>VIN = 5.5V, IPVDD = 25 mA</td>
</tr>
<tr>
<td>EXTVD Switchover Voltage</td>
<td>EXTVD</td>
<td>4.4</td>
<td>4.6</td>
<td>4.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>EXTVD Switchover Hysteresis</td>
<td>EXTVD</td>
<td>—</td>
<td>0.2</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Quiescent Supply Current</td>
<td>IQ</td>
<td>—</td>
<td>1.25</td>
<td>—</td>
<td>mA</td>
<td>VFB = 1.5V</td>
</tr>
<tr>
<td>Shutdown Supply Current</td>
<td>IQSHDN</td>
<td>—</td>
<td>0.15</td>
<td>2</td>
<td>μA</td>
<td>Power from VIN, VEN = 0V</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>35</td>
<td>60</td>
<td>μA</td>
<td>VIN = VDD = 5.5V, VEN = 0V</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Devices are ESD-sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

Note 2: Specification for packaged product only.

The IC is trimmed to get the current in the limits at room temperature.
### TABLE 1-1: ELECTRICAL CHARACTERISTICS (1) (CONTINUED)

Electrical Characteristics: \(\text{PV}_{\text{IN}} = 12\text{V}, \text{V}_{\text{OUT}} = 5\text{V}, \text{V}_{\text{DD}} = 5\text{V}, \text{V}_{\text{BST}} = \text{V}_{\text{SW}} = 5\text{V}; f_{\text{SW}} = 300\text{kHz}, \text{R}_{\text{CL}} = 1.42\text{k}\Omega, \text{L} = 8.2\mu\text{H}; T_{\text{A}} = 25^\circ\text{C}, \text{unless noted. Boldface values indicate } -40^\circ\text{C} \leq T_{\text{J}} \leq +125^\circ\text{C.} \)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Feedback Reference Voltage</td>
<td>(V_{\text{FB}})</td>
<td>0.597</td>
<td>0.6</td>
<td>0.603</td>
<td>V</td>
<td>(T_{\text{J}} = +25^\circ\text{C})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.594</td>
<td>0.6</td>
<td>0.606</td>
<td>V</td>
<td>-40^\circ\text{C} \leq T_{\text{J}} \leq +125^\circ\text{C}</td>
</tr>
<tr>
<td>Load Regulation</td>
<td></td>
<td></td>
<td>0.04</td>
<td></td>
<td>%</td>
<td>(I_{\text{OUT}} = 0\text{A} \text{ to } 5\text{A})</td>
</tr>
<tr>
<td>Line Regulation</td>
<td></td>
<td></td>
<td>0.1</td>
<td></td>
<td>%</td>
<td>(\text{PV}_{\text{IN}} = 7\text{V} \text{ to } 75\text{V})</td>
</tr>
<tr>
<td>FB Bias Current</td>
<td>(I_{\text{FB_BIAS}})</td>
<td>—</td>
<td>0.05</td>
<td>0.5</td>
<td>(\mu\text{A})</td>
<td>(V_{\text{FB}} = 0.6\text{V})</td>
</tr>
<tr>
<td>Enable Control</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN Logic Level High</td>
<td>(E_{\text{NH}})</td>
<td>1.6</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>EN Logic Level Low</td>
<td>(E_{\text{NL}})</td>
<td>—</td>
<td>—</td>
<td>0.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>EN Bias Current</td>
<td>(I_{\text{EN_BIAS}})</td>
<td>—</td>
<td>6</td>
<td>30</td>
<td>(\mu\text{A})</td>
<td>(V_{\text{EN}} = 0\text{V})</td>
</tr>
<tr>
<td>On Timer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Switching Frequency</td>
<td>(F_{\text{REQ}})</td>
<td>720</td>
<td>800</td>
<td>880</td>
<td>kHz</td>
<td>(F_{\text{REQ}} = \text{PV}<em>{\text{IN}}, I</em>{\text{OUT}} = 5\text{A})</td>
</tr>
<tr>
<td>Minimum Switching Frequency</td>
<td>(F_{\text{REQ}})</td>
<td>230</td>
<td>270</td>
<td>300</td>
<td>kHz</td>
<td>(F_{\text{REQ}} = 33% \text{PV}_{\text{IN}})</td>
</tr>
<tr>
<td>Maximum Duty Cycle</td>
<td>(D_{\text{MAX}})</td>
<td>—</td>
<td>85</td>
<td>—</td>
<td>%</td>
<td>(V_{\text{FB}} = 0\text{V}, F_{\text{REQ}} = \text{PV}_{\text{IN}}) (Note 1)</td>
</tr>
<tr>
<td>Minimum Duty Cycle</td>
<td>(D_{\text{MIN}})</td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>%</td>
<td>(V_{\text{FB}} &gt; 0.6\text{V})</td>
</tr>
<tr>
<td>Minimum Off-Time</td>
<td>(t_{\text{OFF(MIN)}})</td>
<td>100</td>
<td>200</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Minimum On-Time</td>
<td>(t_{\text{ON(MIN)}})</td>
<td>60</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Soft Start</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Soft Start Current Source</td>
<td>(I_{\text{SS}})</td>
<td>0.8</td>
<td>1.4</td>
<td>3</td>
<td>(\mu\text{A})</td>
<td></td>
</tr>
<tr>
<td>Soft Start Period Range</td>
<td>—</td>
<td>2.5</td>
<td></td>
<td>40</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>Current Limit</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Limit</td>
<td>(I_{\text{CLIM}})</td>
<td>5.75</td>
<td>6.25</td>
<td>6.75</td>
<td>A</td>
<td>(R_{\text{CL}} = 1.42\text{k}\Omega) (Note 2)</td>
</tr>
<tr>
<td>(I_{\text{LIM}}) Source Current</td>
<td>(I_{\text{CL}})</td>
<td>—</td>
<td>135</td>
<td>—</td>
<td>(\mu\text{A})</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{LIM}}) Source Current Tempco</td>
<td>—</td>
<td>—</td>
<td>0.3</td>
<td>—</td>
<td>(\mu\text{A/}^\circ\text{C})</td>
<td></td>
</tr>
<tr>
<td>Internal FETs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Top MOSFET (R_{\text{DS(ON)}})</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>—</td>
<td>m(\Omega)</td>
<td></td>
</tr>
<tr>
<td>Bottom MOSFET (R_{\text{DS(ON)}})</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>—</td>
<td>m(\Omega)</td>
<td></td>
</tr>
<tr>
<td>SW Leakage Current</td>
<td>(I_{\text{SWLEAK}})</td>
<td>—</td>
<td>—</td>
<td>5</td>
<td>(\mu\text{A})</td>
<td>(\text{PV}<em>{\text{IN}} = 48\text{V}, V</em>{\text{EN}} = 0\text{V})</td>
</tr>
<tr>
<td>(\text{PV}_{\text{IN}}) Leakage Current</td>
<td>(I_{\text{VINLEAK}})</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>(\mu\text{A})</td>
<td>(\text{PV}<em>{\text{IN}} = 48\text{V}, V</em>{\text{EN}} = 0\text{V})</td>
</tr>
<tr>
<td>BST Leakage Current</td>
<td>(I_{\text{BSTLEAK}})</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>(\mu\text{A})</td>
<td>(\text{PV}<em>{\text{IN}} = 48\text{V}, V</em>{\text{EN}} = 0\text{V})</td>
</tr>
<tr>
<td>Power Good (PG)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PG Threshold</td>
<td>(V_{\text{PG_TH}})</td>
<td>85</td>
<td>90</td>
<td>95</td>
<td>%</td>
<td>(V_{\text{FB}}) rising</td>
</tr>
<tr>
<td>PG Threshold Hysteresis</td>
<td>(V_{\text{PG_HYS}})</td>
<td>—</td>
<td>6</td>
<td>—</td>
<td>%</td>
<td>(V_{\text{FB}}) falling</td>
</tr>
<tr>
<td>PG Delay Time</td>
<td>(t_{\text{PG_DLY}})</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>(\mu\text{s})</td>
<td>(V_{\text{FB}}) rising</td>
</tr>
<tr>
<td>PG Low Voltage</td>
<td>(V_{\text{PG_LOW}})</td>
<td>—</td>
<td>70</td>
<td>200</td>
<td>mV</td>
<td>(V_{\text{FB}} &lt; 90% \times V_{\text{NOM}}, I_{\text{PG}} = 1\text{mA})</td>
</tr>
<tr>
<td>Thermal Protection</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overtemperature Shutdown</td>
<td>(T_{\text{SHD}})</td>
<td>—</td>
<td>150</td>
<td>—</td>
<td>(^\circ\text{C})</td>
<td>(T_{\text{J}}) rising</td>
</tr>
<tr>
<td>Overtemperature Shutdown Hysteresis</td>
<td>(T_{\text{SHD_HYS}})</td>
<td>—</td>
<td>15</td>
<td>—</td>
<td>(^\circ\text{C})</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Specification for packaged product only.
Note 2: The \(I_{\text{CL}}\) is trimmed to get the current in the limits at room temperature.
### TABLE 1-2: TEMPERATURE SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Temperature Ranges</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction Operating Temperature</td>
<td>T_J</td>
<td>-40</td>
<td></td>
<td>+125</td>
<td>°C</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>T_S</td>
<td>-65</td>
<td></td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>T_J</td>
<td></td>
<td></td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Lead Temperature</td>
<td></td>
<td></td>
<td></td>
<td>+260</td>
<td>°C</td>
<td>Soldering, 10s</td>
</tr>
<tr>
<td><strong>Package Thermal Resistance</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 6 mm x 6 mm, QFN-32LD</td>
<td>( \theta_{JA} )</td>
<td></td>
<td>33.3</td>
<td></td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., \( T_A, T_J, \theta_{JA} \)). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.
2.0 TYPICAL CHARACTERISTIC CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

**Note:** Unless otherwise indicated, \( V_{IN} = 12V \), \( V_{OUT} = 5V \), \( I_{OUT} = 0A \), \( f_{SW} = 300\ kHz \), \( R_{CL} = 1.42\ k\Omega \), \( L = 8.2\ \mu H \).

**FIGURE 2-1:** Efficiency vs. Output Current (\( V_{IN} = 5V \)).

**FIGURE 2-2:** Efficiency vs. Output Current (\( V_{IN} = 12V \)).

**FIGURE 2-3:** Efficiency vs. Output Current (\( V_{IN} = 24V \)).

**FIGURE 2-4:** Efficiency vs. Output Current (\( V_{IN} = 48V \)).

**FIGURE 2-5:** Output Voltage vs. Output Current (\( V_{OUT} = 1V \)).

**FIGURE 2-6:** Output Voltage vs. Output Current (\( V_{OUT} = 1.8V \)).
Note: Unless otherwise indicated, \( V_{IN} = 12\,\text{V}, V_{OUT} = 5\,\text{V}, I_{OUT} = 0\,\text{A}, f_{SW} = 300\,\text{kHz}, R_{CL} = 1.42\,\text{k}\Omega, L = 8.2\,\mu\text{H} \).

**FIGURE 2-7:** Output Voltage vs. Output Current (\( V_{OUT} = 3.3\,\text{V} \)).

**FIGURE 2-8:** Output Voltage vs. Output Current (\( V_{OUT} = 5\,\text{V} \)).

**FIGURE 2-10:** Output Voltage vs. Input Voltage (\( V_{OUT} = 1.8\,\text{V} \)).

**FIGURE 2-11:** Output Voltage vs. Input Voltage (\( V_{OUT} = 3.3\,\text{V} \)).

**FIGURE 2-9:** Output Voltage vs. Input Voltage (\( V_{OUT} = 1\,\text{V} \)).

**FIGURE 2-12:** Output Voltage vs. Input Voltage (\( V_{OUT} = 5\,\text{V} \)).
Note: Unless otherwise indicated, \( V_{\text{IN}} = 12 \text{V} \), \( V_{\text{OUT}} = 5 \text{V} \), \( I_{\text{OUT}} = 0 \text{A} \), \( f_{\text{SW}} = 300 \text{kHz} \), \( R_{\text{CL}} = 1.42 \text{k}\Omega \), \( L = 8.2 \mu\text{H} \).

**FIGURE 2-13:** \( V_{\text{IN}} \) Operating Supply Current vs. Input Voltage.

**FIGURE 2-14:** \( V_{\text{IN}} \) Operating Supply Current vs. Temperature.

**FIGURE 2-15:** \( V_{\text{IN}} \) Shutdown Current vs. Input Voltage.

**FIGURE 2-16:** \( V_{\text{IN}} \) Shutdown Current vs. Temperature.

**FIGURE 2-17:** \( V_{\text{DD}} \) Voltage vs. Input Voltage.

**FIGURE 2-18:** \( V_{\text{DD}} \) Voltage vs. Temperature.
Note: Unless otherwise indicated, $V_{IN} = 12\text{V}$, $V_{OUT} = 5\text{V}$, $I_{OUT} = 0\text{A}$, $f_{SW} = 300\ \text{kHz}$, $R_{CL} = 1.42\ \text{k}\Omega$, $L = 8.2\ \mu\text{H}$.

**FIGURE 2-19:** Enable Threshold vs. Input Voltage.

**FIGURE 2-20:** Enable Threshold vs. Temperature.

**FIGURE 2-21:** Switching Frequency vs. Input Voltage.

**FIGURE 2-22:** Switching Frequency vs. Temperature.

**FIGURE 2-23:** Output Current Limit vs. Input Voltage.

**FIGURE 2-24:** Output Current Limit vs. Temperature.
Note: Unless otherwise indicated, $V_{IN} = 12\,V$, $V_{OUT} = 5\,V$, $I_{OUT} = 0\,A$, $f_{SW} = 300\,kHz$, $R_{CL} = 1.42\,k\Omega$, $L = 8.2\,\mu\text{H}$.

**FIGURE 2-25:** Power Good Threshold vs. Temperature.

**FIGURE 2-26:** Undervoltage Lockout vs. Temperature.

**FIGURE 2-27:** Feedback Voltage vs. Temperature.

**FIGURE 2-28:** Enable Turn-On and Rise Time.

**FIGURE 2-29:** Enable Turn-Off.

**FIGURE 2-30:** $V_{IN}$ Start-up with Prebiased Output.
Note: Unless otherwise indicated, $V_{IN} = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 0A$, $f_{SW} = 300$ kHz, $R_{CL} = 1.42 \, k\Omega$, $L = 8.2 \, \mu H$.

**FIGURE 2-31:** Enable Turn-On and Turn-Off.

**FIGURE 2-32:** Switching Waveform ($I_{OUT} = 0A$).

**FIGURE 2-33:** Switching Waveform ($I_{OUT} = 5A$).

**FIGURE 2-34:** Enable into Short Circuit.

**FIGURE 2-35:** Power-up into Short Circuit.

**FIGURE 2-36:** Behavior when Entering Short Circuit.
Note: Unless otherwise indicated, $V_{IN} = 12\, \text{V}$, $V_{OUT} = 5\, \text{V}$, $I_{OUT} = 0\, \text{A}$, $f_{SW} = 300\, \text{kHz}$, $R_{CL} = 1.42\, \text{k}\Omega$, $L = 8.2\, \text{µH}$.

**FIGURE 2-37:** Recovery from Short Circuit.

**FIGURE 2-38:** Behavior when Entering Thermal Shutdown.

**FIGURE 2-39:** Recovery from Thermal Shutdown.

**FIGURE 2-40:** Load Transient Response (0 to 2.5A).

**FIGURE 2-41:** Load Transient Response (0 to 5A).

**FIGURE 2-42:** Line Transient Response (12V to 18V).
**Note:** Unless otherwise indicated, $V_{IN} = 12\,\text{V}$, $V_{OUT} = 5\,\text{V}$, $I_{OUT} = 0\,\text{A}$, $f_{SW} = 300\,\text{kHz}$, $R_{CL} = 1.42\,\text{k}\Omega$, $L = 8.2\,\mu\text{H}$.

**FIGURE 2-43:** Line Transient Response (12V to 24V).

**FIGURE 2-44:** Thermal Picture ($I_{OUT} = 2.5\,\text{A}$).

**FIGURE 2-45:** Thermal Picture ($I_{OUT} = 5\,\text{A}$).
3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( I_{\text{lim}} )</td>
<td>Current Limit Adjust Input. Connect a resistor from ( I_{\text{lim}} ) to the SW node to set the current limit. Refer to Section 4.3 “Current Limit” for more details.</td>
</tr>
<tr>
<td>2, 16, 17, 18, 19, 22, 29</td>
<td>PGND</td>
<td>Power Ground. PGND is the ground path for the MIC28514 buck converter power stage. The PGND pin connects to the sources of the low-side N-channel internal MOSFET, the negative terminals of the input capacitors and the negative terminals of the output capacitors. The loop for the Power Ground should be as small as possible and separate from the Analog Ground (AGND) loop.</td>
</tr>
<tr>
<td>3, 12, 13, 14, 15, 20</td>
<td>SW</td>
<td>Switch Node (Output). Internal connection for the high-side MOSFET source and low-side MOSFET drain. Connect one terminal of the Inductor to the SW node.</td>
</tr>
<tr>
<td>4</td>
<td>BST</td>
<td>Boost Pin (Output). Bootstrapped voltage to the high-side N-channel internal MOSFET driver. An internal diode is connected between the PVDD pin and the BST pin. A boost capacitor of 0.1 ( \mu )F is connected between the BST pin and the SW pin.</td>
</tr>
<tr>
<td>5, 6, 7, 8, 9, 10, 11</td>
<td>PVIN</td>
<td>High-Side Internal N-Channel MOSFET Drain Connection (Input). The PVIN operating voltage range is from 4.5V to 75V. Input capacitors between the PVIN pins and the Power Ground (PGND) are required and the connection should be kept as short as possible.</td>
</tr>
<tr>
<td>21</td>
<td>PVDD</td>
<td>Supply for the MOSFET Drivers. Connect to VDD through a 2( \Omega ) series resistor. Connect a minimum 4.7 ( \mu )F low-ESR ceramic capacitor from PVDD to PGND.</td>
</tr>
<tr>
<td>23</td>
<td>EXTVDD</td>
<td>Auxiliary LDO Input. Connect to a supply higher than 4.7V (typical) to bypass the internal high-voltage LDO or leave unconnected/connected to ground. Connect a 2.2 ( \mu )F low-ESR ceramic capacitor between EXTVDD and PGND when EXTVDD is connected to an external supply.</td>
</tr>
<tr>
<td>24</td>
<td>EN</td>
<td>Enable (Input). A logic level control of the output. The EN pin is CMOS-compatible. Logic high = enable, logic low = shutdown. In the OFF state, the VDD supply current of the device is reduced. Do not pull the EN pin above the VDD supply.</td>
</tr>
<tr>
<td>25</td>
<td>FREQ</td>
<td>Frequency Programming Input. Connect to ( V_{\text{IN}} ) to set the switching frequency to 800 kHz. Connect to the mid-point of a resistor divider from PVIN to AGND to set the switching frequency. Refer to Section 5.1 “Setting the Switching Frequency”.</td>
</tr>
<tr>
<td>26</td>
<td>SS</td>
<td>Soft Start Adjustment Pin. Connect a capacitor from the SS pin to AGND to adjust the soft start time. See more details in Section 5.0 “Application Information”.</td>
</tr>
<tr>
<td>27</td>
<td>FB</td>
<td>Feedback (Input). Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.6V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.</td>
</tr>
<tr>
<td>28</td>
<td>AGND</td>
<td>Analog Ground. Reference node for all the control logic circuits inside the MIC28514. Connect AGND to PGND at one point; see Section 6.0 “PCB Layout Guidelines” for details.</td>
</tr>
<tr>
<td>30</td>
<td>VDD</td>
<td>VDD Bias (Input). Power to the internal reference and control sections of the MIC28514. The VDD operating voltage range is from 4.5V to 5.5V. A 2.2 ( \mu )F ceramic capacitor from the VDD pin to the PGND pin must be placed next to the IC.</td>
</tr>
<tr>
<td>31</td>
<td>SVIN</td>
<td>Input Voltage to the internal regulator, which powers the internal reference and control section of the MIC28514. Connect to PVIN through a 2( \Omega ) resistor. Connect a 1 ( \mu )F capacitor from this pin to AGND.</td>
</tr>
<tr>
<td>32</td>
<td>PG</td>
<td>Open-Drain Power Good Output. PG is pulled to ground when the output voltage is below 90% of the target voltage. Pull-up to VDD through a 10 k( \Omega ) resistor to set a logic high level when the output voltage is above 90% of the target voltage.</td>
</tr>
</tbody>
</table>
4.0 FUNCTIONAL DESCRIPTION

The MIC28514 is an adaptive on-time synchronous, step-down DC/DC regulator. It is designed to operate over a wide input voltage range, from 4.5V to 75V, and provides a regulated output voltage at up to 5A of output current. An adaptive on-time control scheme is employed in order to obtain a constant switching frequency and to simplify the control compensation. Overcurrent protection is implemented with the use of an external sense resistor which sets the current limit. The device includes a programmable soft start function that reduces the power supply input surge current at start-up by controlling the output voltage rise time.

4.1 Theory of Operation

The MIC28514 Functional Block Diagram appears on page 2. The output voltage is sensed by the MIC28514 Feedback pin, FB, via the voltage dividers, R1 and R2, and compared to a 0.6V reference voltage (VREF), at the main comparator, through a low-gain transconductance (gm) amplifier. If the feedback voltage decreases and the output of the gm amplifier is below 0.6V, then the main comparator will trigger the control logic and generate an on-time period. The on-time period is predetermined by the fixed tON estimator circuitry value from Equation 4-1:

\[
EQUATION 4-1: \quad t_{\text{ON(ESTIMATED)}} = \frac{V_{\text{OUT}}}{V_{\text{IN}} \times f_{\text{SW}}} \\
\text{Where:} \\
V_{\text{OUT}} = \text{Output Voltage} \\
V_{\text{IN}} = \text{Power Stage Input Voltage} \\
f_{\text{SW}} = \text{Switching Frequency}
\]

At the end of the on-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The off-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the gm amplifier is below 0.6V, the on-time period is triggered and the off-time period ends. If the off-time period, determined by the feedback voltage, is less than the minimum off-time, tOFF(MIN), which is about 240 ns, then the MIC28514 control logic will apply the tOFF(MIN) instead. The minimum tOFF(MIN) period is required to maintain enough energy in the Boost Capacitor (CBST) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 240 ns tOFF(MIN):

\[
EQUATION 4-2: \quad D_{\text{MAX}} = \frac{t_{\text{S}} - t_{\text{OFF(MIN)}}}{t_{\text{S}}} = 1 - \frac{240 \text{ns}}{t_{\text{S}}}
\]

Where:
\[
t_{\text{S}} = \frac{1}{f_{\text{SW}}}
\]

It is not recommended to use the MIC28514 with an off-time close to tOFF(MIN) during steady-state operation. The actual on-time and resulting switching frequency will vary with the part-to-part variation in the rise and fall times of the internal MOSFETs, the output load current, and variations in the VDD voltage. Also, the minimum tON results in a lower switching frequency in high VIN to VOUT applications, such as 75V to 1.0V.

Figure 4-1 shows the MIC28514 control loop timing during steady-state operation. During steady-state operation, the gm amplifier senses the feedback voltage ripple. The feedback ripple is proportional to the output voltage ripple, and the inductor current ripple, to trigger the on-time period. The on-time is predetermined by the tON estimator. The termination of the off-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when VFB falls below VREF, the off period ends and the next on-time period is triggered through the control logic circuitry.
Figure 4-2 shows the operation of the MIC28514 during load transient. The output voltage drops due to the sudden load increase, which causes $V_{FB}$ to be less than $V_{REF}$. This will cause the error comparator to trigger an on-time period. At the end of the on-time period, a minimum off-time is generated to charge $C_{BST}$ because the feedback voltage is still below $V_{REF}$. Then, the next on-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in the MIC28514 converter.

Unlike true Current-mode control, the MIC28514 uses the output voltage ripple to trigger an on-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough.

In order to meet the stability requirements, the MIC28514 feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the $g_m$ amplifier. The recommended feedback voltage ripple is 20 mV ~ 100 mV. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the $g_m$ amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. For these applications, ripple injection is required to ensure proper operation. Refer to Section 5.8 “Ripple Injection” under Section 5.0 “Application Information” for details about the ripple injection technique.

4.2 Soft Start

Soft start reduces the power supply input surge current at start-up by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC28514 features an adjustable soft start time. The soft start time can be adjusted by adjusting the value of the capacitor connected from the SS pin to AGND. The soft start time can be adjusted from 5 ms to 100 ms. The MIC28514 forces 1.4 µA current from the SS pin. This constant current flows through the capacitor connected from the SS pin to AGND to adjust the soft start time.

4.3 Current Limit

The MIC28514 uses the low-side MOSFET $R_{DS(ON)}$ to sense the inductor current. In each switching cycle of the MIC28514 converter, the inductor current is sensed by monitoring the voltage across the low-side MOSFET during the off period of the switching cycle, during which, the low-side MOSFET is on. An internal current source of 135 µA generates a voltage across the external Current Limit Setting Resistor, $R_{CL}$.

The $I_{ILIM}$ Pin Voltage ($V_{ILIM}$) is the difference of the voltage across the low-side MOSFET and the voltage across the resistor ($V_{CL}$). The sensed voltage, $V_{ILIM}$, is compared with the Power Ground (PGND) after a blanking time of 150 ns.

If the absolute value of the voltage drop across the low-side MOSFET is greater than the absolute value of the voltage across the current setting resistor ($V_{CL}$), the MIC28514 triggers the current limit event. A consecutive eight current limit events trigger the Hiccup mode. Once the controller enters into Hiccup mode, it initiates a soft start sequence after a hiccup time-out of 4 ms (typical). Both the high-side and low-side MOSFETs are turned off during a hiccup time-out. The hiccup sequence, including the soft start, reduces the stress on the switching FETs, and protects the load and supply from severe short conditions.

Since the MOSFET $R_{DS(ON)}$ varies from 30% to 40% with temperature, it is recommended to consider the $R_{DS(ON)}$ variation, while calculating $R_{CL}$ in the above equation, to avoid false current limiting due to increased MOSFET junction temperature rise.

To improve the current limit variation, the MIC28514 adjusts the internal Current Limit Source Current ($I_{CL}$) at a rate of 0.3 µA/°C when the MIC28514 junction temperature changes to compensate the $R_{DS(ON)}$ variation of the low-side MOSFET. Figure 2-23 indicates the temperature variation of the current limit with $R_{CL} = 1.5 \text{k}\Omega$. 

![FIGURE 4-2: MIC28514 Load Transient Response.](image-url)
A small capacitor (C_{CL}) can be connected from the I_{LIM} pin to PGND to filter the switch node ringing during the off period, allowing a better current sensing. The time constant of R_{CL} and C_{CL} should be less than the minimum off-time.

4.4  Negative Current Limit

The MIC28514 implements a negative current limit by sensing the SW voltage when the low-side MOSFET is on. If the SW node voltage exceeds 48 mV, typical, or an equivalent of 2A, the device turns off the low-side MOSFET for 500 ns.

4.5  Internal MOSFET Gate Drive

The functional block diagram shows a bootstrap circuit, consisting of an internal diode from PVDD to BST and an external capacitor connected from the SW pin to the BST pin (C_{BST}). This circuit supplies energy to the high-side drive circuit. Capacitor, C_{BST}, is charged while the low-side MOSFET is on and the voltage on the SW pin is approximately 0V. Energy from C_{BST} is used to turn on the high-side MOSFET. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN}. The internal diode is reverse-biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10 mA, so a 0.1 μF to 1 μF is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle (i.e., ΔBST = 10 mA x 4 μs/0.1 μF = 400 mV). When the low-side MOSFET is turned back on, C_{BST} is recharged through D1. A small resistor in series with C_{BST} can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the PVDD supply voltage. The nominal low-side gate drive voltage is PVDD and the nominal high-side gate drive voltage is approximately PVDD – V_{DIODE}, where V_{DIODE} is the voltage drop across the internal diode. An approximate 30 ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

4.6  Auxiliary Bootstrap LDO (EXTVDD)

The MIC28514 features an auxiliary bootstrap LDO which improves the system efficiency by supplying the MIC28514 internal circuit bias power and gate drivers from the converter output voltage. This LDO is enabled when the voltage on the EXTVDD pin is above 4.6V (typical), and at the same time, the main LDO which operates from V_{IN} is disabled to reduce power consumption.
5.0 APPLICATION INFORMATION

5.1 Setting the Switching Frequency

The MIC28514 is an adjustable frequency, synchronous buck regulator that features an adaptive on-time control architecture. The switching frequency can be adjusted between 270 kHz and 800 kHz by changing the resistor divider network, consisting of R3 and R4. Equation 5-1 gives the estimated switching frequency.

**EQUATION 5-1:**

\[
f_{SW(ADJ)} = f_O \times \frac{R_3}{R_3 + R_4}
\]

Where:
- \( f_O \) = Switching Frequency when \( R_4 \) is 100 k\( \Omega \) and \( R_3 \) is open. \( f_O \) is typically 800 kHz.

A typical value of \( R_1 \) can be between 3 k\( \Omega \) and 10 k\( \Omega \). If \( R_1 \) is too large, it may allow noise to be introduced into the voltage feedback loop. If \( R_1 \) is too small, it will decrease the efficiency of the power supply, especially at light loads. Once \( R_1 \) is selected, \( R_2 \) can be calculated using **Equation 5-4**.

**EQUATION 5-4:**

\[
R_2 = \frac{V_{FB} \times R_1}{V_{OUT} - V_{FB}}
\]

5.2 Setting the Soft Start Time

The output soft start time can be set by connecting a capacitor from SS to AGND.

The value of the capacitor can be calculated using **Equation 5-2**.

**EQUATION 5-2:**

\[
C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{REF}}
\]

Where:
- \( C_{SS} \) = Capacitor from SS pin to AGND
- \( I_{SS} \) = Internal Soft Start Current (1.4 \( \mu \)A, typical)
- \( t_{SS} \) = Output Soft Start Time
- \( V_{REF} \) = 0.6 V

5.3 Setting Output Voltage

The MIC28514 requires two resistors to set the output voltage, as shown in **Figure 5-1**.

The output voltage is determined by **Equation 5-3**:

**EQUATION 5-3:**

\[
V_O = V_{FB} \times \left( 1 + \frac{R_1}{R_2} \right)
\]

Where:
- \( V_{FB} = 0.6 \) V

A typical value of \( R_1 \) can be between 3 k\( \Omega \) and 10 k\( \Omega \). If \( R_1 \) is too large, it may allow noise to be introduced into the voltage feedback loop. If \( R_1 \) is too small, it will decrease the efficiency of the power supply, especially at light loads. Once \( R_1 \) is selected, \( R_2 \) can be calculated using **Equation 5-4**.

5.4 Setting the Current Limit

The Source Current Limit (\( I_{CL} \)) is trimmed at the factory to achieve a higher current limit accuracy with \( R_{CL} = 1.42 \) k\( \Omega \), as specified in **Table 1-1 in Section 1.0 “Electrical Characteristics”**. It is possible to adjust other current limits by changing the \( R_{CL} \) value using **Equation 5-5**.

**EQUATION 5-5:**

\[
R_{CL} = \frac{\left( I_{LIM} + \frac{\Delta I_{LPP}}{2} \right) \times R_{DS(ON)}}{I_{CL}}
\]

Where:
- \( I_{LIM} \) = Load Current Limit
- \( R_{DS(ON)} \) = On-Resistance of the Low-Side MOSFET (25 m\( \Omega \), typical)
- \( \Delta I_{LPP} \) = Inductor Ripple Current
- \( I_{CL} \) = Current Limit Source Current (135 \( \mu \)A, typical)
5.5 Inductor Selection

Values for inductance, peak and RMS currents are required to select the inductor. The input voltage, output voltage, switching frequency and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value, and therefore, a larger and more expensive inductor. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by Equation 5-6.

EQUATION 5-6:

\[
L = \frac{V_{\text{OUT}} \times (V_{\text{IN(MAX)}} - V_{\text{OUT}})}{V_{\text{IN(MAX)}} \times f_{\text{SW}} \times 20\% \times I_{\text{OUT(MAX)}}}
\]

Where:
- \( f_{\text{SW}} \) = Switching Frequency
- \( 20\% \) = Ratio of AC Ripple Current to DC Output Current
- \( V_{\text{IN(MAX)}} \) = Maximum Power Stage Input Voltage

For a selected inductor, the peak-to-peak inductor current ripple is:

EQUATION 5-7:

\[
\Delta I_{\text{L(PP)}} = \frac{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}{V_{\text{IN}} \times f_{\text{SW}} \times L}
\]

The peak inductor current is equal to the average output current plus one-half of the peak-to-peak inductor current ripple.

EQUATION 5-8:

\[
I_{\text{L(PK)}} = I_{\text{OUT}} + 0.5 \times \Delta I_{\text{L(PP)}}
\]

The RMS inductor current is used to calculate the \( I^2R \) losses in the inductor.

EQUATION 5-9:

\[
I_{\text{L(RMS)}} = \sqrt{I_{\text{OUT}}^2 + \frac{\Delta I_{\text{L(PP)}}^2}{12}}
\]

Maximizing efficiency requires the proper selection of core material while minimizing the winding resistance. The high-frequency operation of the MIC28514 requires the use of ferrite materials for all but the most cost-sensitive applications. Lower cost iron powder cores may be used, but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized, although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be significant. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by Equation 5-10.

EQUATION 5-10:

\[
P_{\text{INDUCTOR(CU)}} = I_{\text{L(RMS)}}^2 \times R_{\text{WINDING}}
\]

The resistance of the copper wire, \( R_{\text{WINDING}} \), increases with the temperature. The value of the winding resistance used should be at the operating temperature.

EQUATION 5-11:

\[
R_{\text{WINDING(HT)}} = R_{\text{WINDING(20C)}} \times (1 + 0.004 \times (T_{\text{H}} - T_{20C}))
\]

Where:
- \( T_{\text{H}} \) = Temperature of Wire Underload
- \( T_{20C} \) = Ambient Temperature
- \( R_{\text{WINDING(20C)}} \) = Room Temperature Winding Resistance (usually specified by the manufacturer)

5.6 Output Capacitor Selection

The type of the output capacitor is usually determined by its Equivalent Series Resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are ceramic, low-ESR aluminum electrolytic, OS-CON, and POSCAP. The output capacitor’s ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of the ESR is calculated using Equation 5-12.

EQUATION 5-12:

\[
\text{ESR}_{\text{COUT}} \leq \frac{\Delta V_{\text{OUT(PP)}}}{\Delta I_{\text{L(PP)}}}
\]

Where:
- \( \Delta V_{\text{OUT(PP)}} \) = Peak-to-Peak Output Voltage Ripple
- \( \Delta I_{\text{L(PP)}} \) = Peak-to-Peak Inductor Current Ripple
The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 5-13.

**EQUATION 5-13:**

\[
\Delta V_{\text{OUT}(\text{PP})} = \left( \frac{\Delta I_{\text{L}(\text{PP})}}{C_{\text{OUT}} \times f_{\text{SW}} \times 8} \right)^2 + \left( \frac{\Delta I_{\text{L}(\text{PP})} \times ESR \times C_{\text{OUT}}}{8} \right)^2
\]

Where:
- \( C_{\text{OUT}} \) = Output Capacitance Value
- \( f_{\text{SW}} \) = Switching Frequency

As described in Section 4.1 “Theory of Operation”, a subsection of Section 4.0 “Functional Description”, the MIC28514 requires at least 20 mV peak-to-peak ripple at the FB pin to make the \( g_m \) amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors’ value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide enough feedback voltage ripple. Refer to Section 5.8 “Ripple Injection” for details.

The voltage rating of the capacitor should be 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated in Equation 5-14.

**EQUATION 5-14:**

\[
I_{C_{\text{OUT}}} = \frac{\Delta I_{\text{L}(\text{PK})}}{\sqrt{2}}
\]

The power dissipated in the output capacitor is:

**EQUATION 5-15:**

\[
P_{\text{DISS(COUT)}} = I_{C_{\text{OUT}}}^2 \times ESR_{C_{\text{OUT}}}
\]

5.7 **Input Capacitor Selection**

The input capacitor for the power stage input, \( V_{\text{IN}} \), should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents caused by turning on the input supply. A tantalum input capacitor’s voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON and multilayer polymer film capacitors can handle the higher inrush currents without voltage derating. The input voltage ripple will primarily depend on the input capacitor’s ESR. The peak input current is equal to the peak inductor current, so:

**EQUATION 5-16:**

\[
\Delta V_{\text{IN}} = I_{L(PK)} \times C_{\text{ESR}}
\]

The input capacitor must be rated for the input current ripple. The RMS value of the input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current is low:

**EQUATION 5-17:**

\[
I_{C_{\text{IN}}} = I_{C_{\text{OUT}}} \times \sqrt{D \times (1 - D)}
\]

The power dissipated in the input capacitor is:

**EQUATION 5-18:**

\[
P_{\text{DISS(CIN)}} = I_{C_{\text{IN}}}^2 \times ESR
\]
5.8 Ripple Injection

The $V_{FB}$ ripple required for proper operation of the MIC28514 $g_m$ amplifier and comparator is 20 mV to 100 mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For low output voltages, such as 1V, the output voltage ripple is only 10 mV to 20 mV and the feedback voltage ripple is less than 20 mV. If the feedback voltage ripple is so small that the $g_m$ amplifier and comparator cannot sense it, then the MIC28514 loses control and the output voltage is not regulated. In order to have sufficient $V_{FB}$ ripple, a ripple injection method should be applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

1. **Enough ripple at the feedback voltage due to the large ESR of the output capacitors (Figure 5-2).** The converter is stable without any ripple injection.

![Figure 5-2: Enough Ripple at FB.](image)

**EQUATION 5-19:**

$$\Delta V_{FB(PP)} = \frac{R_2}{R_1 + R_2} \times ESR_{C_{OUT}} \times \Delta I_{L(PP)}$$

Where:
- $\Delta I_{L(PP)}$ = Peak-to-Peak Value of the Inductor Current Ripple

2. **Inadequate ripple at the feedback voltage due to the small ESR of the output capacitors.**

In this situation, the output voltage ripple is fed into the FB pin through a Feed-Forward Capacitor, $C_{ff}$, as shown in Figure 5-3. The typical $C_{ff}$ value is between 1 nF and 22 nF.

![Figure 5-3: Inadequate Ripple at FB.](image)

**EQUATION 5-20:**

$$\Delta V_{FB(PP)} \approx ESR_{C_{OUT}} \times \Delta I_{L(PP)}$$

3. **Virtualy no ripple at the FB pin voltage due to the very low-ESR of the output capacitors.**

In this situation, the output voltage ripple is less than 20 mV. Therefore, additional ripple is injected into the FB pin from the Switching Node, SW, via a resistor, $R_{INJ}$, and a capacitor, $C_{INJ}$, as shown in Figure 5-4.

![Figure 5-4: Invisible Ripple at FB.](image)

**EQUATION 5-21:**

$$\Delta V_{FB(PP)} = V_{IN} \times K_{DIV} \times D \times (1 - D) \times \frac{1}{f_{SW} \times \tau}$$

Where:
- $V_{IN}$ = Power Stage Input Voltage
- $D$ = Duty Cycle
- $f_{SW}$ = Switching Frequency
- $\tau = (R_1 // R_2 // R_{INJ}) \times C_{ff}$

**EQUATION 5-22:**

$$K_{DIV} = \frac{R_1 // R_2}{R_{INJ} + R_1 // R_2}$$

In Equation 5-21 and Equation 5-22, it is assumed that the time constant associated with $C_{ff}$ must be much greater than the switching period:

**EQUATION 5-23:**

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} < 1$$
If the voltage divider resistors, R1 and R2, are in the kΩ range, a $C_{ff}$ of 1 nF to 22 nF can easily satisfy the large time constant requirements. Also, a 100 nF Injection Capacitor, $C_{INJ}$, is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is as follows.

1. Select $C_{ff}$ to feed all output ripples into the Feedback pin and make sure the large time constant assumption is satisfied. A typical choice for $C_{ff}$ is 1 nF to 22 nF if R1 and R2 are in the kΩ range.

2. Select $R_{INJ}$ according to the expected feedback voltage ripple using Equation 5-24:

   \[
   K_{DIV} = \frac{\Delta V_{FBR}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (I - D)}
   \]

   Then, the value of $R_{INJ}$ is obtained as:

   \[
   R_{INJ} = \left(\frac{1}{K_{DIV}}\right) \times \left(\frac{1}{K_{DIV}} - 1\right)
   \]

3. Select $C_{INJ}$ as 100 nF, which could be considered as short for a wide range of the frequencies.

### 5.9 Thermal Measurements

Measuring the IC’s case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermocouple that comes with a thermal meter. This thermocouple wire gauge is large, typically 22 gauge, and behaves like a heat sink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermocouple wire or an infrared thermometer. If a thermocouple wire is used, it must be constructed of 36 gauge wire or higher (smaller wire size) to minimize the wire heat sinking effect. In addition, the thermocouple tip must be covered in either thermal grease or thermal glue to make sure that the thermocouple junction is making good contact with the case of the IC.

Wherever possible, an infrared thermometer is recommended. An optional stand makes it easy to hold the beam on the IC for long periods of time.
6.0 PCB LAYOUT GUIDELINES

PCB layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths. The thickness of the copper planes is also important in terms of dissipating heat. The 2 oz. copper thickness is adequate from a thermal point of view and a thick copper plain helps in terms of noise immunity. Keep in mind, thinner planes can be easily penetrated by noise. The following guidelines should be followed to ensure proper operation of the MIC28514 converter.

6.1 IC

• The 2.2 µF ceramic capacitor, which is connected to the VDD pin, must be located right at the IC. The VDD pin is very noise-sensitive and placement of the capacitor is very critical. Use wide traces to connect to the VDD pin.
• The Signal Ground pin (SGND) must be connected directly to the ground planes. The SGND and PGND connection should be done at a single point near the IC. Do not route the SGND pin to the PGND pad on the top layer.
• Use thick traces to route the input and output power lines.

6.2 Input Capacitor

• Place the input capacitor next to the power pins.
• Place the input capacitors on the same side of the board and as close to the IC as possible.
• Keep both the PV IN pin and PGND connections short.
• Place several vias to the ground plane, close to the input capacitor ground terminal.
• Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U-type capacitors.
• If a tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
• In hot-plug applications, a tantalum or electrolytic bypass capacitor must be used to limit the overvoltage spike seen on the input supply when power is suddenly applied.

6.3 Inductor

• Keep the inductor connection to the Switch Node (SW) short.
• Do not route any digital lines underneath or close to the inductor.
• Keep the Switch Node (SW) away from the Feedback (FB) pin.

6.4 Output Capacitor

• Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
• Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
• The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

Legend:

| XX...X | Customer-specific information |
| Y      | Year code (last digit of calendar year) |
| YY     | Year code (last 2 digits of calendar year) |
| WW     | Week code (week of January 1 is week ‘01’) |
| NNN    | Alphanumeric traceability code |
| ³      | Pb-free JEDEC designator for Matte Tin (Sn) |
| *      | This package is Pb-free. The Pb-free JEDEC designator (³) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
32-Lead Very Thin Plastic Quad Flat, No Lead Package (PHA) - 6x6 mm Body [VQFN]
Wettable Flanks, Multiple Exposed Pads

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing C04-1196A Sheet 1 of 2
32-Lead Very Thin Plastic Quad Flat, No Lead Package (PHA) - 6x6 mm Body [VQFN] Wettable Flanks, Multiple Exposed Pads

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

### SECTION A-A

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Terminals</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Terminal Thickness</td>
<td>A3</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D2</td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E2</td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D3</td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E3</td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D4</td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D5</td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E5</td>
</tr>
<tr>
<td>Terminal Width</td>
<td>b</td>
</tr>
<tr>
<td>Terminal Length</td>
<td>L</td>
</tr>
<tr>
<td>Terminal-to-Exposed Pad</td>
<td>K1</td>
</tr>
<tr>
<td>Exposed Pad-to-Exposed Pad</td>
<td>K2</td>
</tr>
<tr>
<td>Pacakge Edgel-to-Exposed Pad</td>
<td>K3</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.
32-Lead Very Thin Plastic Quad Flat, No Lead Package (PHA) - 6x6 mm Body [VQFN]
Wettable Flanks, Multiple Exposed Pads

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Width (X32)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X32)</td>
<td>Y1</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C1</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C2</td>
</tr>
<tr>
<td>Inner Pad Length</td>
<td>X2</td>
</tr>
<tr>
<td>Inner Pad Width</td>
<td>Y2</td>
</tr>
<tr>
<td>Inner Pad Length</td>
<td>X3</td>
</tr>
<tr>
<td>Inner Pad Width</td>
<td>Y3</td>
</tr>
<tr>
<td>Inner Pad Length</td>
<td>X4</td>
</tr>
<tr>
<td>Inner Pad Length</td>
<td>X5</td>
</tr>
<tr>
<td>Inner Pad Width</td>
<td>Y5</td>
</tr>
<tr>
<td>Thermal Via Diameter (X26)</td>
<td>V</td>
</tr>
<tr>
<td>Thermal Via Pitch</td>
<td>EV</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process
APPENDIX A: REVISION HISTORY

Revision A (February 2017)

• Original Release of this Document.
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>X</th>
<th>X</th>
<th>XXX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>Media Type</td>
<td>Temperature</td>
<td>Package</td>
</tr>
<tr>
<td>MIC28514T</td>
<td>T</td>
<td>E</td>
<td>PHA</td>
</tr>
</tbody>
</table>

- **Device**: MIC28514T: 75V, 5A Hyper Speed Control® Synchronous DC/DC Buck Regulator with External Soft Start
- **Media Type**: T = 5000/Reel
- **Temperature**: E = Extended Temperature Range (-40°C to +125°C)
- **Package**: PHA = 32-Lead, 6x6 mm VQFN

**Examples:**

- a) MIC28514T-E/PHA: 75V, 5A Synchronous Buck Regulator, Hyper Speed Control® with Soft Start, -40°C to +125°C, Extended Temperature Range, 32-Lead QFN package
Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company’s quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Trademarks
The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BeaconThings, BitCloud, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPW, Helda, JukeBox, KEELOQ, KEELOQ logo, Kleer, LANCheck, LINK MD, maXStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, RightTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.


SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Silicon Storage Technology in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2017, Microchip Technology Incorporated, All Rights Reserved.
ISBN: 978-1-5224-1386-8