HV9801A

Switch-Dimmable LED Driver

Features

- Four-level Switch Dimming
- Highly Accurate Current Regulator
- Output Overcurrent or Short-circuit Protection
- IC Overtemperature Protection

Applications

- Switch-dimmable LED Bulbs and Fixtures

General Description

The HV9801A LED driver is ideally suited for switch-dimmable applications using LED bulbs and fixtures.

Through switch dimming, the lamp can be adjusted to four discrete brightness levels by rapid cycling of the light switch. The brightness levels are traversed in an up-and-down manner. Brightness resumes at the highest level when power is removed for more than a second.

The device can be powered directly from rectified AC through an internal VDD regulator rated at 450V.

Package Types

See Table 2-1 for pin information.
Typical Application Circuit
1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>VIN</td>
<td>15</td>
<td>—</td>
<td>450</td>
<td>V</td>
<td>Note 2</td>
</tr>
<tr>
<td>Input Current</td>
<td>IIN</td>
<td>—</td>
<td>1</td>
<td>2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Supply Current, OTP Shutdown</td>
<td>IIN, OT</td>
<td>—</td>
<td>—</td>
<td>500</td>
<td>μA</td>
<td>Note 1</td>
</tr>
<tr>
<td>Undervoltage Lockout Threshold</td>
<td>UVLO</td>
<td>6.45</td>
<td>6.7</td>
<td>7.1</td>
<td>V</td>
<td>VIN rising (Note 2)</td>
</tr>
<tr>
<td>Undervoltage Lockout Hysteresis</td>
<td>UVLO, Δ</td>
<td>—</td>
<td>500</td>
<td>—</td>
<td>mV</td>
<td>VIN falling</td>
</tr>
<tr>
<td>Maximum Input Current, Limited by UVLO</td>
<td>UVLO, I</td>
<td>3.5</td>
<td>—</td>
<td>—</td>
<td>mA</td>
<td>TA = 25°C (Note 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.5</td>
<td>—</td>
<td>—</td>
<td>mA</td>
<td>TA = 125°C (Note 1)</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>VDD</td>
<td>7.25</td>
<td>7.5</td>
<td>7.75</td>
<td>V</td>
<td>CGATE = 500 pF, RT = 226 kΩ</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>VDD, Δ</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>V</td>
<td>VIN = 15V to 450V, CGATE = 500 pF, RT = 226 kΩ</td>
</tr>
<tr>
<td>VDD Voltage Margin</td>
<td>VDD(UV), Δ</td>
<td>500</td>
<td>—</td>
<td>—</td>
<td>mV</td>
<td>ΔVDD(UV) = VDD–VUVLO, FALL (Note 2)</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>VDD, LOAD, Δ</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>mV</td>
<td>IVD = 0 mA to 1 mA, CGATE = 500 pF, RT = 226 kΩ</td>
</tr>
</tbody>
</table>

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Specifications are at TA = 25°C, VIN = 15V unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>VIN</td>
<td>15</td>
<td>—</td>
<td>450</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Current</td>
<td>IIN</td>
<td>—</td>
<td>1</td>
<td>2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Supply Current, OTP Shutdown</td>
<td>IIN, OT</td>
<td>—</td>
<td>—</td>
<td>500</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Undervoltage Lockout Threshold</td>
<td>UVLO</td>
<td>6.45</td>
<td>6.7</td>
<td>7.1</td>
<td>V</td>
<td>VIN rising (Note 2)</td>
</tr>
<tr>
<td>Undervoltage Lockout Hysteresis</td>
<td>UVLO, Δ</td>
<td>—</td>
<td>500</td>
<td>—</td>
<td>mV</td>
<td>VIN falling</td>
</tr>
<tr>
<td>Maximum Input Current, Limited by UVLO</td>
<td>UVLO</td>
<td>3.5</td>
<td>—</td>
<td>—</td>
<td>mA</td>
<td>TA = 25°C (Note 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.5</td>
<td>—</td>
<td>—</td>
<td>mA</td>
<td>TA = 125°C (Note 1)</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>VDD</td>
<td>7.25</td>
<td>7.5</td>
<td>7.75</td>
<td>V</td>
<td>CGATE = 500 pF, RT = 226 kΩ</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>VDD, Δ</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>V</td>
<td>VIN = 15V to 450V, CGATE = 500 pF, RT = 226 kΩ</td>
</tr>
<tr>
<td>VDD Voltage Margin</td>
<td>VDD(UV), Δ</td>
<td>500</td>
<td>—</td>
<td>—</td>
<td>mV</td>
<td>ΔVDD(UV) = VDD–VUVLO, FALL (Note 2)</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>VDD, LOAD, Δ</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>mV</td>
<td>IVD = 0 mA to 1 mA, CGATE = 500 pF, RT = 226 kΩ</td>
</tr>
</tbody>
</table>

Note 1: Determined by characterization; not production tested
Note 2: Specifications apply over the full operating ambient temperature range of –40°C < TA < +125°C.
**ELECTRICAL CHARACTERISTICS (CONTINUED)**

**Electrical Specifications**: Specifications are at $T_A = 25°C$, $V_{IN} = 15V$ unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leading Edge Blanking Time</td>
<td>$T_{LEB}$</td>
<td>110</td>
<td>—</td>
<td>260</td>
<td>ns</td>
<td>Note 2</td>
</tr>
<tr>
<td>Minimum On-time</td>
<td>$T_{ONX}$</td>
<td>—</td>
<td>—</td>
<td>760</td>
<td>ns</td>
<td>$V_{CS} = V_{CST} + 30$ mV</td>
</tr>
<tr>
<td>Maximum Duty Cycle Maintaining Regulation</td>
<td>$D_{MAX}$</td>
<td>80</td>
<td>—</td>
<td>—</td>
<td>%</td>
<td>LED current falls beyond this duty cycle</td>
</tr>
</tbody>
</table>

**SHORT-CIRCUIT PROTECTION**

- **Hiccup Threshold**
  - $V_{CSH}$: — 440 — mV
- **$V_{CS}$ High to Gate Low Delay**
  - $T_{DLY}$: — 180 ns
  - $V_{CS} = V_{CSH} + 30$ mV
- **Hiccup Time**
  - $T_{SCH}$: 750 — μs
- **Minimum On-time**
  - $T_{ONXSC}$: 430 ns $V_{CS} = V_{DD}$

**$T_{OFF}$ TIMER**

<table>
<thead>
<tr>
<th>Off-time</th>
<th>$T_{OFF}$</th>
<th>32</th>
<th>40</th>
<th>48</th>
<th>μs</th>
<th>$R_T = 1$ MΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>8</td>
<td>10</td>
<td>12</td>
<td></td>
<td>$R_T = 226$ kΩ</td>
</tr>
</tbody>
</table>

**GATE DRIVER**

- **Sourcing Current**
  - $I_{SRC}$: 165 — mA $V_{GATE} = 0V$
- **Sinking Current**
  - $I_{SINK}$: 165 — mA $V_{GATE} = V_{DD}$
- **Rise Time**
  - $t_r$: 30 50 ns $C_{GATE} = 500$ pF
- **Fall Time**
  - $t_f$: 30 50 ns $C_{GATE} = 500$ pF

**OVERTEMPERATURE PROTECTION**

- **Trip Temperature**
  - $T_{TRIP}$: 140 — °C Note 1
- **Hysteresis**
  - $ΔT_{TRIP}$: 20 — °C Note 1

**Note 1**: Determined by characterization; not production tested

**Note 2**: Specifications apply over the full operating ambient temperature range of $–40°C < T_A < +125°C$.

**TEMPERATURE SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
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</thead>
<tbody>
<tr>
<td><strong>TEMPERATURE RANGE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Ambient Temperature</td>
<td>$T_A$</td>
<td>–40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>$T_J$</td>
<td>–40</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>$T_S$</td>
<td>–65</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td><strong>PACKAGE THERMAL RESISTANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8-lead SOIC</td>
<td>$θ_{JA}$</td>
<td>—</td>
<td>101</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>16-lead SOIC</td>
<td>$θ_{JA}$</td>
<td>—</td>
<td>83</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

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2.0 PIN DESCRIPTION

The details on the pins of HV9801A are listed on Table 2-1. See location of pins in Package Types.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>8-lead SOIC Pin Number</th>
<th>16-lead SOIC Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>1</td>
<td>1</td>
<td>Connect to bridge rectifier output. Supplies power to the VDD regulator. Detects light switch power-off event through loss of bridge rectifier output voltage. Do not connect excessive capacitance before or after the bridge to allow VIN to drop rapidly after loss of power.</td>
</tr>
<tr>
<td>CS</td>
<td>2</td>
<td>4</td>
<td>Current sense input</td>
</tr>
<tr>
<td>GND</td>
<td>3</td>
<td>5</td>
<td>Ground</td>
</tr>
<tr>
<td>GATE</td>
<td>4</td>
<td>8</td>
<td>Gate driver output</td>
</tr>
<tr>
<td>VDD</td>
<td>6</td>
<td>12</td>
<td>VDD regulator output. Connect a high-frequency bypass and a hold-up capacitor at VDD. Bypass capacitor to be 100 nF minimum. See Section 3.0 “Application Information” for hold-up capacitance.</td>
</tr>
<tr>
<td>RT</td>
<td>8</td>
<td>14</td>
<td>Off-time programming input. Connect programming resistor to GND.</td>
</tr>
<tr>
<td>DNC</td>
<td>5, 7</td>
<td>2, 3, 6, 7, 9, 10, 11, 13, 15, 16</td>
<td>Stands for “Do Not Connect.”</td>
</tr>
</tbody>
</table>
3.0 APPLICATION INFORMATION

3.1 Current Control

3.1.1 CONTINUOUS CONDUCTION MODE (CCM)

The HV9801A is designed to control a buck converter operating in CCM.

Continuous Conduction Mode operation is characterized by converter operation with non-zero inductor current throughout the switching cycle. Such operation can be achieved by proper selection of the inductance.

3.1.2 LED CURRENT

The HV9801A regulates the LED current with an accuracy far superior to that of competing Peak Current mode controllers.

Average LED current is set by the current sense resistor $R_{CS}$ and the current regulator reference voltage. See Equation 3-1 and Equation 3-2.

EQUATION 3-1:

$$V = I \times R$$

EQUATION 3-2:

$$250mV = I_{LED} \times R_{CS}$$

For example, a 2Ω resistor corresponds to a 125 mA (average) LED current.

3.1.3 CURRENT CONTROL PERFORMANCE

The control method of the HV9801A virtually eliminates the regulation errors associated with Peak Current mode controllers, such as errors caused by inductor tolerance, propagation delay of the current sense comparator, tolerance in the oscillator frequency or off-timer and changes in line and load voltage.

Figure 3-1 compares the load regulation of the HV9801A and that of a device with peak current control. The graph clearly shows the difference in load regulation between the HV9801A and the HV9910B, which is a peak current regulator.

3.2 Duty Cycle, Off-time, On-time and Inductor

3.2.1 DUTY CYCLE

The duty cycle ($D$) is related to the load voltage ($V_{LED}$) and input voltage ($V_{BUS}$) by the simple relation shown in Equation 3-3 and Equation 3-4.

EQUATION 3-3:

$$V_{OUT} = D \times V_{IN}$$

EQUATION 3-4:

$$V_{LED} = D \times V_{BUS}$$

3.2.2 OFF-TIME

The HV9801A operates with constant off-time control, which avoids subharmonic oscillation.

Switching period and switching frequency are related to on-time and off-time as shown in Equation 3-5 and Equation 3-6.

EQUATION 3-5:

$$T_{SW} = T_{ON} + T_{OFF}$$

EQUATION 3-6:

$$F_{SW} = \frac{1}{T_{SW}}$$
On-time is related to off-time and duty cycle. See Equation 3-7.

**EQUATION 3-7:**

\[
D = \frac{T_{ON}}{(T_{ON} + T_{OFF})}
\]

\[
T_{ON} = [D/(1-D)] \times T_{OFF}
\]

With a given \(T_{OFF}\), the HV9801A dynamically adjusts \(T_{ON}\) to regulate the LED current. Specifically, \(T_{ON}\) adapts to the duty cycle associated with the given \(V_{BUS}\) and \(V_{LED}\).

### 3.2.3 OFF-TIME PROGRAMMING

Off-time is programmed by the \(R_T\) resistor as illustrated in Equation 3-8.

**EQUATION 3-8:**

\[
T_{OFF} = (A \times R_T) + B
\]

Where: \(A = 40 \text{ ps} / \Omega\) and \(B = 300 \text{ ns}\)

For instance, a 200 k\(\Omega\) resistor corresponds to 8.3 \(\mu\)s off-time.

An acceptable range for \(R_T\) is 30 k\(\Omega\) to 1 M\(\Omega\), corresponding to an off-time range between 1.5 \(\mu\)s and 40.3 \(\mu\)s.

### 3.2.4 INDUCTOR

Because the converter should operate in CCM, the inductor current should not fall to zero within a switching cycle and the inductor current ripple should be sized accordingly.

A common choice for peak-to-peak inductor current ripple (PPR) is 30% to 40% of nominal LED current.

Inductance can be calculated from the current drop during off-time as shown in Equation 3-9 and Equation 3-10.

**EQUATION 3-9:**

\[
L \times \Delta I = V \times \Delta T
\]

**EQUATION 3-10:**

\[
L \times \text{PPR} \times I_{LED} = V_{LED} \times T_{OFF}
\]

For example, 30% PPR on 350 mA average current equates to 105 mA ripple, which together with 5 \(\mu\)s off-time and 30V LED string voltage corresponds to 1.43 mH inductance.

A design with 30V LED voltage and 150V bus voltage corresponds to a 20% duty cycle, while a 120V bus voltage coincides with a 25% duty cycle. A 20% duty cycle corresponds to 1.25 \(\mu\)s on-time, and a 25% duty cycle corresponds to 1.67 \(\mu\)s on-time. Hence, the switching frequency is 160 kHz at 150V bus voltage and 150 kHz at 120V bus voltage.

### 3.2.5 MAXIMUM DUTY CYCLE

Duty cycle should be limited to the specified maximum of 80%. Accordingly, the targeted LED string voltage and the bus voltage are limited to the same ratio. Operation at a larger desired duty cycle than the maximum duty cycle results in an LED current lower than programmed.

### 3.2.6 MINIMUM DUTY CYCLE

Duty cycle is limited on the low side by the minimum on-time specification (760 ns). Operation at a smaller desired on-time than the minimum causes the LED current to exceed the programmed value.

LED string voltage cannot be made arbitrarily low. Minimum LED string voltage can be determined with Equation 3-11.

**EQUATION 3-11:**

\[
D_{MIN} = \frac{T_{ONX}}{(T_{OFF} + T_{ONX})}
\]

\[
V_{LED} = D_{MIN} \times V_{BUS}
\]

For instance, with 5 \(\mu\)s off-time, the duty cycle should be kept above 13%. Such a duty cycle corresponds to an LED string voltage of 19.5V at 150V bus voltage.

A design that needs a lower LED string voltage requires a longer off-time.

### 3.2.7 SHORT-CIRCUIT PROTECTION

An increase in the LED current sense signal above 440 mV (176% of nominal) trips the short-circuit comparator, thereby causing the converter to switch to Hiccup mode. In Hiccup mode, off-time is lengthened to about 750 \(\mu\)s to allow the inductor current to drop to a safe level.

Without the extended off-time, the inductor current increases with every switching cycle, causing an overcurrent damage to the converter.

The off-time extension can be observed in Figure 3-2 below.

![Short-circuit Inductor Current](image-url)
3.2.8 LEADING EDGE BLANKING

The MOSFET drain current and the current sense signal exhibit a spike at the start of a switching cycle, which arises from the MOSFET gate charging current and the current required for discharging the MOSFET drain node. These two currents typically exceed the inductor by quite a margin.

The current sense signal is blanked at the start of the switching cycle in order to avoid a premature trigger of the current sense and the short-circuit protection comparators.

3.2.9 V_DD REGULATOR

The V_DD regulator generates a source of regulated voltage for operation of internal and external circuits from the power applied at the V_IN pin. Alternatively, the V_DD voltage can be supplied from a source directly connected to the V_DD pin.

3.3 Switch Dimming

3.3.1 GENERAL

Lamp brightness can be adjusted to one of four discrete levels by rapidly cycling power with the light switch. The brightness levels are traversed in an up-and-down manner, the four levels being 100%, 50%, 25% and 12.5%. Brightness resumes at the highest level when power is removed for more than a second.

Reduction of LED current is accomplished through PWM dimming with a PWM dimming frequency of about 1 kHz. The PWM frequency is generated by an internal oscillator, and the PWM duty cycle is controlled by digital logic.

Turning the light switch off and on within one second adjusts LED current to the next level in each dimming step. The direction of dimming depends on the existing position in the dimming sequence. The illustration in Figure 3-3 shows more details. The sequence starts at 100% and adjusts to the next lower level by the first dimming step and then adjusts to the next lower level by the next dimming step. Upon reaching the lowest or highest level, the direction of the sequence reverses. Therefore, the actual overall dimming sequence is 100%, 50%, 25%, 12.5%, 25%, 50%, 100%, and the sequence repeats as the dimming steps continue. When power is removed for more than one second, the dimming sequence is terminated and the brightness is reset to 100% upon turn-on of the light switch.

![FIGURE 3-3: LED Brightness and AC Line Power.](image)

3.3.2 V_DD CAPACITOR

The V_DD voltage should be maintained for at least one second and above the 3.5V level after loss of V_IN power to allow certain timing circuits to function. The minimum V_DD capacitance required can be calculated with Equation 3-12.

**EQUATION 3-12:**

\[
C \times \Delta V = I \times \Delta T \\
C_{DD} \times (7.5V - 3.5V) = I_{VDDX} \times 1s
\]

With 700 µA of I_{VDDX} the bypass capacitance should be 175 µF.

3.3.3 DETECTION OF POWER CYCLING

The presence of AC line power is detected at the V_IN pin. To this end, loss of AC power should result in a rapidly falling voltage at the output of the bridge rectifier.

The V_IN voltage drops due to the current draw from the V_DD regulator. In order to facilitate a quick drop in voltage, a diode should be added to isolate the bus capacitor from the V_IN pin as shown in the Typical Application Circuit.
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

Legend:
- XX...X: Product Code or Customer-specific information
- Y: Year code (last digit of calendar year)
- YY: Year code (last 2 digits of calendar year)
- WW: Week code (week of January 1 is week '01')
- NNN: Alphanumeric traceability code
- (8): Pb-free JEDEC® designator for Matte Tin (Sn)
- *: This package is Pb-free. The Pb-free JEDEC designator (8) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.
8-Lead SOIC (Narrow Body) Package Outline (LG/TG)
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note: This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be a molded mark/identifier, an embedded metal marker, or a printed indicator.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>A</th>
<th>A1</th>
<th>A2</th>
<th>b</th>
<th>D</th>
<th>E</th>
<th>E1</th>
<th>e</th>
<th>h</th>
<th>L</th>
<th>L1</th>
<th>L2</th>
<th>ø1</th>
<th>ø11</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIN</td>
<td>1.35*</td>
<td>0.10</td>
<td>1.25</td>
<td>0.31</td>
<td>4.80*</td>
<td>5.80*</td>
<td>3.80*</td>
<td>0.25</td>
<td>0.40</td>
<td>1.04</td>
<td>0.25</td>
<td>0°</td>
<td>5°</td>
<td></td>
</tr>
<tr>
<td>NOM</td>
<td>-</td>
<td>-</td>
<td>-</td>
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<td>4.90</td>
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<td>-</td>
<td>1.27</td>
<td>REF</td>
<td>0.25</td>
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<tr>
<td>MAX</td>
<td>1.75</td>
<td>0.25</td>
<td>1.65*</td>
<td>0.51</td>
<td>5.00*</td>
<td>6.20*</td>
<td>4.00*</td>
<td>0.50</td>
<td>1.27</td>
<td>8°</td>
<td>15°</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.
16-Lead SOIC (Narrow Body) Package Outline (NG)
9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch

Top View

Side View

View B

View A-A

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:
1. This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal mark; or a printed indicator.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>A</th>
<th>A1</th>
<th>A2</th>
<th>b</th>
<th>D</th>
<th>E</th>
<th>E1</th>
<th>e</th>
<th>h</th>
<th>L</th>
<th>L1</th>
<th>L2</th>
<th>θ</th>
<th>θ1</th>
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<tr>
<td>Dimension (mm) MIN</td>
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<td>0.10</td>
<td>1.25</td>
<td>0.31</td>
<td>9.80</td>
<td>5.80</td>
<td>3.80</td>
<td>0.25</td>
<td>0.40</td>
<td>1.04</td>
<td>1.27</td>
<td>BSC</td>
<td>-</td>
<td></td>
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<tr>
<td>NOM</td>
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<td>-</td>
<td>-</td>
<td>-</td>
<td>9.90</td>
<td>6.00</td>
<td>3.90</td>
<td>1.27</td>
<td>BSC</td>
<td>-</td>
<td>-</td>
<td>1.04</td>
<td>REF</td>
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<tr>
<td>MAX</td>
<td>1.75</td>
<td>0.25</td>
<td>1.65</td>
<td>0.51</td>
<td>10.00</td>
<td>6.20</td>
<td>4.00</td>
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<td>-</td>
<td>-</td>
<td>0.25</td>
<td>BSC</td>
<td></td>
</tr>
</tbody>
</table>

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.
APPENDIX A: REVISION HISTORY

Revision A (September 2017)

- Converted Supertex Doc# DSFP-HV9801A to Microchip DS20005692A
- Updated the part marking format
- Removed the 16-lead SOIC Narrow (NG) M934 media type
- Changed the quantity of the 8-lead SOIC (Narrow) LG package from 2500/Reel to 3300/Reel
- Made minor text changes throughout the document
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<table>
<thead>
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<th>PART NO.</th>
<th>XX</th>
<th>Package Options</th>
<th>X</th>
<th>Environmental</th>
<th>X</th>
<th>Media Type</th>
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<tr>
<td>Packages:</td>
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<td></td>
<td>LG</td>
<td>8-lead SOIC</td>
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<td>16-lead SOIC</td>
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<tr>
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<td>Lead (Pb)-free/RoHS-compliant Package</td>
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<tr>
<td>Media Type:</td>
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<td>3300/Reel for an LG Package</td>
<td></td>
<td></td>
<td></td>
<td>45/Tube for an NG Package</td>
</tr>
</tbody>
</table>

Examples:

a) HV9801ALG-G: Switch-Dimmable LED Driver, 8-lead SOIC Package, 3300/Reel

b) HV9801ANG-G: Switch-Dimmable LED Driver, 16-lead SOIC Package, 45/Tube
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