HV9110/HV9112/HV9113

High-Voltage Current-Mode PWM Controller

Features

• Input Voltage Range of VDD Regulator
  - HV9110: 10V to 120V
  - HV9112: 9V to 80V
  - HV9113: 10V to 120V
• Maximum Duty, Feedback Accuracy
  - HV9110: 49%, 1%
  - HV9112: 49%, 2%
  - HV9113: 99%, 1%
• Current Mode Control
• <1 mA Supply Current
• >1 MHz clock

Applications

• DC/DC Power Converters

General Description

HV9110/HV9112/HV9113 are Switch-Mode Power Supply (SMPS) controllers suitable for the control of a variety of converter topologies, including the flyback converter and the forward converter.

The VDD regulator supports an input voltage as high as 80V or 120V.

HV9110/HV9112/HV9113 controllers include all essentials for a power converter design, such as a bandgap reference, an error amplifier, a ramp generator, a high-speed PWM comparator, and a gate driver. A shutdown latch provides on/off control.

The HV9110 and HV9113 feature an input voltage range of 10V to 120V, and the HV9112 has an input voltage range of 9V to 80V. The HV9110 and HV9112 have a maximum duty of 49%, while the HV9113 has a maximum duty of 99%.

Package Type

14-lead SOIC

See Table 3-1 for pin information.
Functional Block Diagram
1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

Input Voltage, \( V_{\text{IN}} \)
- \( \text{HV9110/HV9113} \) .......................................................... 120V
- \( \text{HV9112} \) ........................................................................... 80V

Device Supply Voltage, \( V_{\text{DD}} \)
- \( \text{HV9110/HV9113} \) .......................................................... 15.5V

Logic Input Voltage Range ............................................... \(-0.3\text{V to } V_{\text{DD}} + 0.3\text{V} \)

Linear Input Voltage Range ............................................... \(-0.3\text{V to } V_{\text{DD}} + 0.3\text{V} \)

Storage Temperature Range ........................................... \(-65^\circ\text{C to } +150^\circ\text{C} \)

Operating Temperature Range ....................................... \(-55^\circ\text{C to } +125^\circ\text{C} \)

Power Dissipation: 14-lead SOIC .................................................. 750 mW

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>REFERENCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Output Voltage</td>
<td>( V_{\text{REF}} )</td>
<td>3.92</td>
<td>4</td>
<td>4.08</td>
<td>V</td>
<td>( R_L = 10\ \text{M}\Omega )</td>
</tr>
<tr>
<td>( \text{HV9110/HV9113} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>( \text{HV9112} )</td>
<td>3.88</td>
<td>4</td>
<td>4.12</td>
<td></td>
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<td></td>
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<tr>
<td>( \text{HV9110/HV9113} )</td>
<td>3.82</td>
<td>4</td>
<td>4.16</td>
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<td></td>
<td>( R_L = 10\ \text{M}\Omega, )</td>
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<tr>
<td>( \text{T_A = } –55^\circ\text{C to } +125^\circ\text{C} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Impedance</td>
<td>( Z_{\text{OUT}} )</td>
<td>15</td>
<td>30</td>
<td>45</td>
<td>( \text{k}\Omega )</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>Short Circuit Current</td>
<td>( I_{\text{SHORT}} )</td>
<td>—</td>
<td>125</td>
<td>250</td>
<td>( \mu\text{A} )</td>
<td>( V_{\text{REF}} = \text{GND} )</td>
</tr>
<tr>
<td>Change in ( V_{\text{REF}} ) with Temperature</td>
<td>( \Delta V_{\text{REF}} )</td>
<td>—</td>
<td>0.25</td>
<td>—</td>
<td>( \text{mV/}^\circ\text{C} )</td>
<td>( \text{T_A = } –55^\circ\text{C to } +125^\circ\text{C} ) (Note 1)</td>
</tr>
<tr>
<td>OSCILLATOR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Oscillator Frequency</td>
<td>( f_{\text{MAX}} )</td>
<td>1</td>
<td>3</td>
<td>—</td>
<td>MHz</td>
<td>( R_{\text{OSC}} = 0\Omega )</td>
</tr>
<tr>
<td>Initial Accuracy</td>
<td>( f_{\text{OSC}} )</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>kHz</td>
<td>( R_{\text{OSC}} = 330\ \text{k}\Omega ) (Note )</td>
</tr>
<tr>
<td>( \text{R_{OSC} = 150}\ \text{k}\Omega ) (Note )</td>
<td>160</td>
<td>200</td>
<td>240</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{DD}} ) Regulation</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>15</td>
<td>%</td>
<td>9.5V &lt; ( V_{\text{DD}} ) &lt; 13.5V</td>
</tr>
<tr>
<td>Temperature Coefficient</td>
<td>—</td>
<td>—</td>
<td>170</td>
<td>—</td>
<td>ppm/°C</td>
<td>( T_A = –55^\circ\text{C to } +125^\circ\text{C} ) (Note 1)</td>
</tr>
<tr>
<td>PWM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Duty Cycle</td>
<td>( D_{\text{MAX}} )</td>
<td>49</td>
<td>49.4</td>
<td>49.6</td>
<td>%</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>( \text{HV9110/HV9112} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \text{HV9113} )</td>
<td>95</td>
<td>97</td>
<td>99</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Dead Time</td>
<td>( D_{\text{MIN}} )</td>
<td>—</td>
<td>225</td>
<td>—</td>
<td>ns</td>
<td>( \text{HV9113 only (Note 1)} )</td>
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<tr>
<td>Minimum Duty Cycle</td>
<td>—</td>
<td>—</td>
<td>0</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Pulse Width where Pulse drops out</td>
<td>—</td>
<td>80</td>
<td>125</td>
<td></td>
<td>ns</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>CURRENT LIMIT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Maximum Input Signal</td>
<td>( V_{\text{LIM}} )</td>
<td>1</td>
<td>1.2</td>
<td>1.4</td>
<td>V</td>
<td>( V_{\text{FB}} = 0\text{V} )</td>
</tr>
<tr>
<td>Delay to Output</td>
<td>( t_{\text{D}} )</td>
<td>—</td>
<td>80</td>
<td>120</td>
<td>ns</td>
<td>( V_{\text{CS}} = 1.5\text{V}, V_{\text{COMP}} \leq 2\text{V} ) (Note 1)</td>
</tr>
</tbody>
</table>
# ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: $V_{DD} = 10V, V_{IN} = 48V, V_{DISC} = 0V, R_{BIAS} = 390 \, k\Omega, R_{OSC} = 330 \, k\Omega, T_A = 25^\circ C$ unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
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<tbody>
<tr>
<td><strong>ERROR AMPLIFIER</strong></td>
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<td></td>
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<tr>
<td>Feedback Voltage</td>
<td>HV9110/13</td>
<td>$V_{FB}$</td>
<td>3.96</td>
<td>4</td>
<td>4.04</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>HV9112</td>
<td></td>
<td>3.92</td>
<td>4</td>
<td>4.08</td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>$I_{IN}$</td>
<td>—</td>
<td>25</td>
<td>500</td>
<td>nA</td>
<td>$V_{FB} = 4V$</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>$V_{OS}$</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
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<tr>
<td>Open-loop Voltage Gain</td>
<td>$A_{VOL}$</td>
<td>60</td>
<td>80</td>
<td>—</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Unity Gain Bandwidth</td>
<td>$GB$</td>
<td>1</td>
<td>1.3</td>
<td>—</td>
<td>—</td>
<td>MHz</td>
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<tr>
<td>Output Source Current</td>
<td>$I_{SOURCE}$</td>
<td>—1.4</td>
<td>—2</td>
<td>—</td>
<td>mA</td>
<td>$V_{FB} = 3.4V$</td>
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<tr>
<td>Output Sink Current</td>
<td>$I_{SINK}$</td>
<td>0.12</td>
<td>0.15</td>
<td>—</td>
<td>mA</td>
<td>$V_{FB} = 4.5V$</td>
</tr>
<tr>
<td><strong>HIGH-VOLTAGE REGULATOR AND START-UP</strong></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage</td>
<td>HV9110/13</td>
<td>$V_{IN}$</td>
<td>—</td>
<td>—</td>
<td>120</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>HV9112</td>
<td></td>
<td>—</td>
<td>—</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>Input Leakage Current</td>
<td>$I_{IN}$</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>μA</td>
<td>$V_{DD} &gt; 9.4V$</td>
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<tr>
<td>Regulator Turn-off Threshold Voltage</td>
<td>$V_{TH}$</td>
<td>8</td>
<td>8.7</td>
<td>9.4</td>
<td>V</td>
<td>$I_{IN} = 10 , \mu A$</td>
</tr>
<tr>
<td>Undervoltage Lockout</td>
<td>$V_{LOCK}$</td>
<td>7</td>
<td>8.1</td>
<td>8.9</td>
<td>V</td>
<td></td>
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<td><strong>SUPPLY</strong></td>
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<tr>
<td>Supply Current</td>
<td>$I_{DD}$</td>
<td>—</td>
<td>0.75</td>
<td>1</td>
<td>mA</td>
<td>$C_L &lt; 75 , pF$</td>
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<tr>
<td>Quiescent Supply Current</td>
<td>$I_{Q}$</td>
<td>—</td>
<td>0.55</td>
<td>—</td>
<td>mA</td>
<td>$V_{NSD} = 0V$</td>
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<tr>
<td>Nominal Bias Current</td>
<td>$I_{BIAS}$</td>
<td>—</td>
<td>20</td>
<td>—</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Operating Range</td>
<td>$V_{DD}$</td>
<td>9</td>
<td>—</td>
<td>13.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td><strong>SHUTDOWN LOGIC</strong></td>
<td></td>
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</tr>
<tr>
<td>Shutdown Delay</td>
<td>$t_{SD}$</td>
<td>—</td>
<td>50</td>
<td>100</td>
<td>ns</td>
<td>$C_L = 500 , pF, V_{CS} = 0V$</td>
</tr>
<tr>
<td>NSD Pulse Width</td>
<td>$t_{SW}$</td>
<td>50</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>RST Pulse Width</td>
<td>$t_{RW}$</td>
<td>50</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>(Note 1)</td>
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<tr>
<td>Latching Pulse Width</td>
<td>$t_{LW}$</td>
<td>25</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>$V_{NSD} - V_{RST} = 0V$ (Note 1)</td>
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<tr>
<td>Input Low Voltage</td>
<td>$V_{IL}$</td>
<td>—</td>
<td>—</td>
<td>2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input High Voltage</td>
<td>$V_{IH}$</td>
<td>7</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Current, Input High Voltage</td>
<td>$I_{IH}$</td>
<td>—</td>
<td>1</td>
<td>5</td>
<td>μA</td>
<td>$V_{IN} = V_{DD}$</td>
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<tr>
<td>Input Current, Input Low Voltage</td>
<td>$I_{IL}$</td>
<td>—</td>
<td>—25</td>
<td>—35</td>
<td>μA</td>
<td>$V_{IN} = 0V$</td>
</tr>
<tr>
<td><strong>OUTPUT</strong></td>
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</tr>
<tr>
<td>Output High Voltage</td>
<td>HV9110/13</td>
<td>$V_{OH}$</td>
<td>$V_{DD} - 0.25$</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>HV9112</td>
<td></td>
<td>$V_{DD} - 0.3$</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td>HV9110/13</td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
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<tr>
<td>Output Low Voltage</td>
<td>All</td>
<td>$V_{OL}$</td>
<td>—</td>
<td>—</td>
<td>0.2</td>
<td>V</td>
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<tr>
<td></td>
<td>HV9110/13</td>
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<td>—</td>
<td>—</td>
<td>0.3</td>
<td></td>
</tr>
<tr>
<td>Output Resistance</td>
<td>Pull up</td>
<td>$R_{OUT}$</td>
<td>—</td>
<td>15</td>
<td>25</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Pull down</td>
<td></td>
<td>—</td>
<td>8</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pull up</td>
<td></td>
<td>—</td>
<td>20</td>
<td>30</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Pull down</td>
<td></td>
<td>—</td>
<td>10</td>
<td>30</td>
<td></td>
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<tr>
<td>Rise Time</td>
<td>$t_R$</td>
<td>—</td>
<td>30</td>
<td>75</td>
<td>ns</td>
<td>$C_L = 500 , pF$ (Note 1)</td>
</tr>
<tr>
<td>Fall Time</td>
<td>$t_F$</td>
<td>—</td>
<td>20</td>
<td>75</td>
<td>ns</td>
<td>$C_L = 500 , pF$ (Note 1)</td>
</tr>
</tbody>
</table>

**Note 1:** Design guidance only; Not 100% tested in production.

**Note 2:** Stray capacitance on OSC input pin must be ≤5 pF.
TEMPERATURE SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
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<tr>
<td>TEMPERATURE RANGES</td>
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</tr>
<tr>
<td>Operating Temperature</td>
<td>—</td>
<td>—55</td>
<td>—</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>—</td>
<td>—65</td>
<td>—</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>PACKAGE THERMAL RESISTANCE</td>
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<td></td>
</tr>
<tr>
<td>14-lead SOIC</td>
<td>—</td>
<td>—</td>
<td>83</td>
<td>—</td>
<td>°C/W</td>
<td></td>
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</table>

1.1 Truth Table

TRUTH TABLE

<table>
<thead>
<tr>
<th>SHUTDOWN</th>
<th>RESET</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>H</td>
<td>Normal operation</td>
</tr>
<tr>
<td>H</td>
<td>H → L</td>
<td>Normal operation, no change</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>Off, not latched</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>Off, latched</td>
</tr>
<tr>
<td>L → H</td>
<td>L</td>
<td>Off, latched, no change</td>
</tr>
</tbody>
</table>
2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

**FIGURE 2-1:** Error Amplifier Output Impedance ($Z_0$).

**FIGURE 2-2:** PSRR – Error Amplifier and Reference.

**FIGURE 2-3:** Bias Current vs. Bias Resistance.

**FIGURE 2-4:** Output Switching Frequency vs. Oscillator Resistance.

**FIGURE 2-5:** Error Amplifier Open-loop Gain/Phase.

**FIGURE 2-6:** $R_{DISCHARGE}$ vs. $t_{OFF}$ (HV9113 only).
3.0 PIN DESCRIPTION

Table 3-1 shows the pin description for HV9110/HV9112/HV9113. The locations of the pins are listed in Features.

TABLE 3-1: PIN DESCRIPTION

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>HV9110/HV9112/HV9113 Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BIAS</td>
<td>Internal bias, current set</td>
</tr>
<tr>
<td>2</td>
<td>VIN</td>
<td>High-voltage $V_{DD}$ regulator input</td>
</tr>
<tr>
<td>3</td>
<td>CS</td>
<td>Current sense input</td>
</tr>
<tr>
<td>4</td>
<td>GATE</td>
<td>Gate drive output</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>6</td>
<td>$V_{DD}$</td>
<td>High-voltage $V_{DD}$ regulator output</td>
</tr>
<tr>
<td>7</td>
<td>OSCO</td>
<td>Oscillator output</td>
</tr>
<tr>
<td>8</td>
<td>OSCI</td>
<td>Oscillator input</td>
</tr>
<tr>
<td>9</td>
<td>DISC</td>
<td>Oscillator discharge, current set</td>
</tr>
<tr>
<td>10</td>
<td>$V_{REF}$</td>
<td>4V reference output Reference voltage level can be overridden by an externally applied voltage source.</td>
</tr>
<tr>
<td>11</td>
<td>NSD</td>
<td>Active low input to set shutdown latch</td>
</tr>
<tr>
<td>12</td>
<td>RST</td>
<td>Active high input to reset shutdown latch</td>
</tr>
<tr>
<td>13</td>
<td>COMP</td>
<td>Error amplifier output</td>
</tr>
<tr>
<td>14</td>
<td>FB</td>
<td>Feedback voltage input</td>
</tr>
</tbody>
</table>
4.0 TEST CIRCUITS

The test circuits for characterizing error amplifier output impedance, $Z_{OUT}$, and error amplifier, power supply rejection ratio, PSRR, are shown in Figure 4-1 and Figure 4-2.

**FIGURE 4-1:** Error Amp $Z_{OUT}$

**FIGURE 4-2:** PSRR
5.0  DETAILED DESCRIPTION

5.1  High-Voltage Regulator

The high-voltage regulator included in HV9110/HV9112/HV9113 consists of a high-voltage N-channel Depletion-mode DMOS transistor driven by an error amplifier, providing a current path between the \( V_{IN} \) terminal and the \( V_{DD} \) terminal. The maximum current, about 20 mA, occurs when \( V_{DD} = 0 \), with current reducing as \( V_{DD} \) rises. This path shuts off when \( V_{DD} \) rises to somewhere between 8V and 9.4V. So, if \( V_{DD} \) is held at 10V or 12V by an external source, no current other than leakage is drawn through the high voltage transistor. This minimizes dissipation within the high-voltage regulator.

Use an external capacitor between \( V_{DD} \) and GND. This capacitor should have good high-frequency characteristics. Ceramic caps work well.

The device uses a compound resistor divider to monitor \( V_{DD} \) for both the undervoltage lockout circuit and the shutoff circuit of the high-voltage FET. Setting the undervoltage sense point about 0.6V lower on the string than the FET shutoff point guarantees that the undervoltage lockout releases before the FET shuts off.

5.2  Bias Circuit

HV9110/HV9112/HV9113 require an external bias resistor, connected between the Bias pin and GND, to set currents in a series of current mirrors used by the analog sections of the chip. The nominal external bias current requirement is 15 \( \mu \)A to 20 \( \mu \)A, which can be set by a 390 k\( \Omega \) to 510 k\( \Omega \) resistor if \( V_{DD} = 10V \), or a 510 k\( \Omega \) to 680 k\( \Omega \) resistor if \( V_{DD} = 12V \). A precision resistor is not required, ±5% meets device requirements.

5.3  Clock Oscillator

The clock oscillator of the HV9110/HV9112/HV9113 consists of a ring of CMOS inverters, timing capacitors, and a capacitor-discharge FET. A single external resistor between the OSCI and OSCO sets the oscillator frequency. (See Figure 2-4.)

The HV9110 and HV9112 include a frequency-dividing flip-flop that allows the part to operate with a 50% duty limit. Accordingly, the effective switching frequency of the power converter is half the oscillator frequency. (See Figure 2-4.)

An internal discharge FET resets the oscillator ramp at the end of the oscillator cycle. The discharge FET is externally connected to GND, by way of a resistor. The resistor programs the oscillator dead time at the end of the oscillator period.

The oscillator turns off during shutdown to reduce supply current by about 150 \( \mu \)A.

5.4  Reference

The reference of the HV9110/HV9112/HV9113 consists of a band-gap reference, followed by a buffer amplifier, which scales the voltage up to 4V. The scaling resistors of the buffer amplifier are trimmed during manufacture so that the output of the error amplifier, when connected in a gain of –1 configuration, is as close to 4V as possible. This nulls out the input offset of the error amplifier. As a consequence, even though the observed reference voltage of a specific part may not be exactly 4V, the feedback voltage required for proper regulation will be 4V.

An approximately 50 k\( \Omega \) resistor is located internally between the output of the reference buffer amplifier and the circuitry it feeds—reference output pin and non-inverting input to the error amplifier. This allows overriding the internal reference with a low impedance voltage source ≤ 6V. Using an external reference reinstates the input offset voltage of the error amplifier. Overriding the reference should seldom be necessary.

The reference of the HV9110/HV9112/HV9113 is a high-impedance node, and usually there will be significant electrical noise nearby. Therefore, a bypass capacitor between the reference pin and GND is strongly recommended. The reference buffer amplifier is compensated to be stable with a capacitive load of 0.01 \( \mu \)F to 0.1 \( \mu \)F.

5.5  Error Amplifier

The error amplifier on HV9110/HV9112/HV9113 is a low-power, differential-input, operational amplifier. A PMOS input stage is used, so the common mode range includes ground and the input impedance is high.

5.6  Current Sense Comparators

The HV9110/HV9112/HV9113 use a dual-comparator system with independent comparators for modulation and current limiting. This provides the designer greater latitude in compensation design, as there are no clamps, except ESD protection, on the compensation pin.

5.7  Remote Shutdown

The NSD and RST pins control the shutdown latch. These pins have internal current-source pull-ups so they can be driven from open drain logic. When not used they should be left open or connected to \( V_{DD} \).
5.8 Output Buffer

The output buffer of HV9110/HV9112/HV9113 is of standard CMOS construction P-channel pull-up and N-channel pull-down. Thus, the body-drain diodes of the output stage can be used for spike clipping. External Schottky diode clamping of the output is not required.

![Shutdown Timing Waveforms](image-url)
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

Legend:

- XX...X Product Code or Customer-specific information
- Y Year code (last digit of calendar year)
- YY Year code (last 2 digits of calendar year)
- WW Week code (week of January 1 is week ‘01’)
- NNN Alphanumeric traceability code
- * Pb-free JEDEC® designator for Matte Tin (Sn)
- ©3 This package is Pb-free. The Pb-free JEDEC designator (©3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.
14-Lead SOIC (Narrow Body) Package Outline (NG)
8.65x3.90mm body, 1.75mm height (max), 1.27mm pitch

Top View

View B

Side View

View A-A

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:
1. This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be a molded mark/identifier; an embedded metal marker; or a printed indicator.

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<th>A2</th>
<th>b</th>
<th>D</th>
<th>E</th>
<th>E1</th>
<th>e</th>
<th>h</th>
<th>L</th>
<th>L1</th>
<th>L2</th>
<th>θ</th>
<th>θ1</th>
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<td>0.10</td>
<td>1.25</td>
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<td>8.55*</td>
<td>5.80*</td>
<td>3.80*</td>
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<td>0.40</td>
<td>1.04</td>
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<td>-</td>
<td>8°</td>
<td>15°</td>
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</table>

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.
APPENDIX A: REVISION HISTORY

Revision A (June 2016)

- Merged Supertex Doc #s DSFP-HV9110, DSFP-HV9112 and DSFP-DSFP-HV9113 to Microchip DS20005505A.
- Revised Electrical Characteristics to accommodate the merged products.
- Updated pin names to reflect new naming convention.
- Significant text changes to Detailed Description.
- Minor text changes throughout.
**PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

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<th>Media Type</th>
<th>Options</th>
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<td>NG</td>
<td>G</td>
<td>(blank) =</td>
<td>14-lead SOIC</td>
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<tr>
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<td>High-voltage Current-mode PWM Controller, 10V to 120V Input Voltage Range, 49% Duty Cycle</td>
<td>Lead (Pb)-free/RoHS-compliant Package</td>
<td>53/Tube for an NG package</td>
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<td>HV9112 =</td>
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<td>14-lead SOIC</td>
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<tr>
<td></td>
<td>High-voltage Current-mode PWM Controller, 9V to 80V Input Voltage Range, 49% Duty Cycle</td>
<td></td>
<td></td>
<td>53/Tube</td>
<td></td>
</tr>
<tr>
<td></td>
<td>HV9113 =</td>
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<td></td>
<td>14-lead SOIC</td>
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<tr>
<td></td>
<td>High-voltage Current-mode PWM Controller, 10V to 120V Input Voltage Range, 99% Duty Cycle</td>
<td></td>
<td></td>
<td>53/Tube</td>
<td></td>
</tr>
</tbody>
</table>

**Examples:**

a) HV9110NG-G: High-voltage Current-mode PWM Controller 10V to 120V Input Voltage Range, 49% Duty Cycle, 14-lead SOIC Package, 53/Tube
b) HV9112NG-G: High-voltage Current-mode PWM Controller, 9V to 80V Input Voltage Range, 49% Duty Cycle, 14-lead SOIC Package, 53/Tube
c) HV9113NG-G: High-voltage Current-mode PWM Controller, 10V to 120V Input Voltage Range, 99% Duty Cycle, 14-lead SOIC Package, 53/Tube
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