MCP6V31/1U/2/4

23 µA, 300 kHz Zero-Drift Op Amps

Features:

- High DC Precision:
  - $V_{OS}$ Drift: ±50 nV/°C (maximum)
  - $V_{OS}$: ±8 µV (maximum)
  - $A_{OL}$: 120 dB (minimum, $V_{DD} = 5.5$V)
  - PSRR: 120 dB (minimum, $V_{DD} = 5.5$V)
  - CMRR: 120 dB (minimum, $V_{DD} = 5.5$V)
  - $E_{ni}$: 1.0 µVP-P (typical), $f = 0.1$ Hz to 10 Hz
  - $E_{ni}$: 0.33 µVP-P (typical), $f = 0.01$ Hz to 1 Hz
- Low Power and Supply Voltages:
  - $I_{Q}$: 23 µA/amplifier (typical)
  - Wide Supply Voltage Range: 1.8V to 5.5V
- Small Packages:
  - Singles in SC70, SOT-23
  - Duals in MSOP-8, 2×3 TDFN
  - Quads in TSSOP-14
- Easy to Use:
  - Rail-to-Rail Input/Output
  - Gain Bandwidth Product: 300 kHz (typical)
  - Unity Gain Stable
- Extended Temperature Range: -40°C to +125°C

Typical Applications:

- Portable Instrumentation
- Sensor Conditioning
- Temperature Measurement
- DC Offset Correction
- Medical Instrumentation

Design Aids:

- SPICE Macro Models
- FilterLab® Software
- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Related Parts:

- MCP6V01/2/3: Auto-Zeroed, Spread Clock
- MCP6V06/7/8: Auto-Zeroed
- MCP6V26/7/8: Auto-Zeroed, Low Noise
- MCP6V11/1U/2/4: Zero-Drift, Low Power

Description:

The Microchip Technology Inc. MCP6V31/1U/2/4 family of operational amplifiers provides input offset voltage correction for very low offset and offset drift. These are low-power devices, with a gain bandwidth product of 300 kHz (typical). They are unity gain stable, have virtually no 1/f noise, and have good Power Supply Rejection Ratio (PSRR) and Common Mode Rejection Ratio (CMRR). These products operate with a single supply voltage as low as 1.8V, while drawing 23 µA/amplifier (typical) of quiescent current.

The Microchip Technology Inc. MCP6V31/1U/2/4 op amps are offered in single (MCP6V31 and MCP6V31U), dual (MCP6V32) and quad (MCP6V34) packages. They were designed using an advanced CMOS process.
Typical Application Circuit

Offset Voltage Correction for Power Driver
1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

VDD – VSS .............................................................................................................................. 6.5V
Current at Input Pins ................................................................................................................. ±2 mA
Analog Inputs (VIN+ and VIN−) (Note 1) ............................................................................ VSS + 1.0V to VDD + 1.0V
All other Inputs and Outputs ................................................................................................. VSS + 0.3V to VDD + 0.3V
Difference Input voltage ........................................................................................................... |VDD – VSS|
Output Short Circuit Current ................................................................................................... Continuous
Current at Output and Supply Pins .......................................................................................... ±30 mA
Storage Temperature ............................................................................................................. -65°C to +150°C
Maximum Junction Temperature ........................................................................................... +150°C
ESD protection on all pins (HBM, CDM, MM) ..................................................................... ≥ 2 kV, 1.5 kV, 400V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical Characteristics:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parameters</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>VOS</td>
<td>-8</td>
<td>—</td>
<td>+8</td>
<td>µV</td>
<td>TA = +25°C</td>
</tr>
<tr>
<td>Input Offset Voltage Drift with</td>
<td>TC1</td>
<td>-50</td>
<td>—</td>
<td>+50</td>
<td>nV/°C</td>
<td>TA = -40 to +125°C</td>
</tr>
<tr>
<td>Temperature (Linear Temp. Co.)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltage Quadratic Temp. Co.</td>
<td>TC2</td>
<td>—</td>
<td>±0.08</td>
<td>—</td>
<td>nV/°C²</td>
<td>TA = -40 to +125°C</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>PSRR</td>
<td>120</td>
<td>135</td>
<td>—</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Input Bias Current and Impedance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>IB</td>
<td>—</td>
<td>+5</td>
<td>—</td>
<td>pA</td>
<td>TA = +85°C</td>
</tr>
<tr>
<td>Input Bias Current across Temperature</td>
<td>IB</td>
<td>0</td>
<td>+2.9</td>
<td>+5</td>
<td>nA</td>
<td>TA = +125°C</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>IOS</td>
<td>—</td>
<td>±130</td>
<td>—</td>
<td>pA</td>
<td>TA = +125°C</td>
</tr>
<tr>
<td>Input Offset Current across Temperature</td>
<td>IOS</td>
<td>—</td>
<td>±140</td>
<td>—</td>
<td>pA</td>
<td>TA = +85°C</td>
</tr>
<tr>
<td>Common Mode Input Impedance</td>
<td>ZCM</td>
<td>—</td>
<td>10¹³</td>
<td>6</td>
<td>Ω/pF</td>
<td>TA = +125°C</td>
</tr>
<tr>
<td>Differential Input Impedance</td>
<td>ZDIFF</td>
<td>—</td>
<td>10¹³</td>
<td>6</td>
<td>Ω/pF</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: For Design Guidance only; not tested.

2: Figure 2-18 shows how VCMH and VCMH changed across temperature for the first production lot.
### TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

**Electrical Characteristics:** Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +1.8V$ to +5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 \, k\Omega$ to $V_L$ and $C_L = 20 \, pF$ (refer to Figure 1-4 and Figure 1-5).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Common Mode</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common Mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Range Low</td>
<td>$V_{CM}$</td>
<td>$V_{SS}$</td>
<td>$V_{SS}$</td>
<td>$-0.15$</td>
<td>$V$</td>
<td>$(Note \ 2)$</td>
</tr>
<tr>
<td>Common Mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Range High</td>
<td>$V_{CMH}$</td>
<td>$V_{DD} + 0.2$</td>
<td>$V_{DD} + 0.2$</td>
<td>$-0.15$</td>
<td>$V$</td>
<td>$(Note \ 2)$</td>
</tr>
<tr>
<td>Common Mode Rejection Ratio</td>
<td>CMRR</td>
<td>110</td>
<td>125</td>
<td></td>
<td>$dB$</td>
<td>$V_{DD} = 1.8V, V_{CM} = -0.15V \ to \ 2.0V$</td>
</tr>
<tr>
<td></td>
<td>CMRR</td>
<td>120</td>
<td>135</td>
<td></td>
<td>$dB$</td>
<td>$V_{DD} = 5.5V, V_{CM} = -0.15V \ to \ 5.7V$</td>
</tr>
<tr>
<td><strong>Open-Loop Gain</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC Open-Loop Gain (large signal)</td>
<td>$A_{OL}$</td>
<td>103</td>
<td>125</td>
<td></td>
<td>$dB$</td>
<td>$V_{DD} = 1.8V, V_{OUT} = 0.3V \ to \ 1.6V$</td>
</tr>
<tr>
<td></td>
<td>$A_{OL}$</td>
<td>120</td>
<td>135</td>
<td></td>
<td>$dB$</td>
<td>$V_{DD} = 5.5V, V_{OUT} = 0.3V \ to \ 5.3V$</td>
</tr>
<tr>
<td><strong>Output</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Output Voltage Swing</td>
<td>$V_{OL}$</td>
<td>$V_{SS}$</td>
<td>$V_{SS} + 14$</td>
<td>$V_{SS} + 45$</td>
<td>$mV$</td>
<td>$R_L = 10 , k\Omega, G = +2, 0.5V \ input \ overdrive$</td>
</tr>
<tr>
<td>Maximum Output Voltage Swing</td>
<td>$V_{OH}$</td>
<td>$V_{DD} - 45$</td>
<td>$V_{DD} - 14$</td>
<td>$V_{DD}$</td>
<td>$mV$</td>
<td>$R_L = 100 , k\Omega, G = +2, 0.5V \ input \ overdrive$</td>
</tr>
<tr>
<td>Output Short Circuit Current</td>
<td>$I_{SC}$</td>
<td>$\pm 6$</td>
<td>$\pm 6$</td>
<td></td>
<td>$mA$</td>
<td>$V_{DD} = 1.8V$</td>
</tr>
<tr>
<td>Power Supply</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>$V_{DD}$</td>
<td>1.8</td>
<td>5.5</td>
<td></td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>Quiescent Current per amplifier</td>
<td>$I_Q$</td>
<td>12</td>
<td>23</td>
<td>34</td>
<td>$\mu A$</td>
<td>$I_Q = 0, \ MCP6V31/1U$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>21</td>
<td>34</td>
<td>$\mu A$</td>
<td>$I_Q = 0, \ MCP6V32/4$</td>
</tr>
<tr>
<td>POR Trip Voltage</td>
<td>$V_{POR}$</td>
<td>0.9</td>
<td>1.6</td>
<td></td>
<td>$V$</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** For Design Guidance only; not tested.

**Note 2:** Figure 2-18 shows how $V_{CM}$ and $V_{CMH}$ changed across temperature for the first production lot.
### TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated, \( T_A = +25°C, V_{DD} = +1.8V \) to +5.5V, \( V_{SS} = GND, \) \( V_{CM} = V_{DD}/3, \) \( V_{OUT} = V_{DD}/2, \) \( V_L = V_{DD}/2, \) \( R_L = 100 \, k\Omega \) to \( V_L \) and \( C_L = 20 \, pF \) (refer to Figure 1-4 and Figure 1-5).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Amplifier AC Response</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain Bandwidth Product</td>
<td>GBWP</td>
<td>—</td>
<td>300</td>
<td>—</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Slew Rate</td>
<td>SR</td>
<td>—</td>
<td>0.13</td>
<td>—</td>
<td>V/µs</td>
<td></td>
</tr>
<tr>
<td>Phase Margin</td>
<td>PM</td>
<td>—</td>
<td>70</td>
<td>—</td>
<td>°</td>
<td>( G = +1 )</td>
</tr>
<tr>
<td><strong>Amplifier Noise Response</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Noise Voltage</td>
<td>( E_{ni} )</td>
<td>—</td>
<td>0.33</td>
<td>—</td>
<td>( \mu V_{P-P} )</td>
<td>( f = 0.01 ) Hz to 1 Hz</td>
</tr>
<tr>
<td>Input Noise Voltage Density</td>
<td>( e_{ni} )</td>
<td>—</td>
<td>5.00</td>
<td>—</td>
<td>nV/√Hz</td>
<td>( f &lt; 2 ) kHz</td>
</tr>
<tr>
<td>Input Noise Current Density</td>
<td>( i_{ni} )</td>
<td>—</td>
<td>5.00</td>
<td>—</td>
<td>fA/√Hz</td>
<td></td>
</tr>
<tr>
<td><strong>Amplifier Distortion</strong></td>
<td>IMD</td>
<td>52</td>
<td>—</td>
<td>—</td>
<td>( \mu V_{PK} )</td>
<td>( V_{CM} ) tone = 50 mV( V_{PK} ) at 100 Hz, ( G_N = 1 )</td>
</tr>
<tr>
<td><strong>Amplifier Step Response</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Start Up Time</td>
<td>( t_{STR} )</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>ms</td>
<td>( G = +1, ) 0.1% ( V_{OUT} ) settling (Note 2)</td>
</tr>
<tr>
<td>Offset Correction Settling Time</td>
<td>( t_{STL} )</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>µs</td>
<td>( G = +1, ) ( V_{IN} ) step of 2V, ( V_{OS} ) within 100 µV of its final value</td>
</tr>
<tr>
<td>Output Overdrive Recovery Time</td>
<td>( t_{ODR} )</td>
<td>—</td>
<td>120</td>
<td>—</td>
<td>µs</td>
<td>( G = -10, ) ±0.5V input overdrive to ( V_{DD}/2, ) ( V_{IN} ) 50% point to ( V_{OUT} ) 90% point (Note 3)</td>
</tr>
</tbody>
</table>

**Note 1:** These parameters were characterized using the circuit in Figure 1-6. In Figure 2-37 and Figure 2-38, there is an IMD tone at DC, a residual tone at 100 Hz and other IMD tones and clock tones.

2: High gains behave differently; see Section 4.3.3, Offset at Power Up.

3: \( t_{ODR} \) includes some uncertainty due to clock edge timing.

### TABLE 1-3: TEMPERATURE SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for: \( V_{DD} = +1.8V \) to +5.5V, \( V_{SS} = GND. \)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Temperature Ranges</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Specified Temperature Range</td>
<td>( T_A )</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>( T_A )</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>( T_A )</td>
<td>-65</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td><strong>Thermal Package Resistances</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 5L-SC-70</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>209</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 5L-SOT-23</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>201</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 8L-2×3 TDFN</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>53</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 8L-MSOP</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>211</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 14L-TSSOP</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Operation must not cause \( T_J \) to exceed Maximum Junction Temperature specification (+150°C).
1.3 Timing Diagrams

FIGURE 1-1: Amplifier Start Up.

FIGURE 1-2: Offset Correction Settling Time.

FIGURE 1-3: Output Overdrive Recovery.

1.4 Test Circuits

The circuits used for most DC and AC tests are shown in Figure 1-4 and Figure 1-5. Lay the bypass capacitors out as discussed in Section 4.3.10 “Supply Bypassing and Filtering”. $R_N$ is equal to the parallel combination of $R_F$ and $R_G$ to minimize bias current effects.

FIGURE 1-4: AC and DC Test Circuit for Most Non-Inverting Gain Conditions.

FIGURE 1-5: AC and DC Test Circuit for Most Inverting Gain Conditions.

The circuit in Figure 1-6 tests the input’s dynamic behavior (i.e., IMD, $t_{STR}$, $t_{STL}$ and $t_{ODR}$). The potentiometer balances the resistor network ($V_{OUT}$ should equal $V_{REF}$ at DC). The op amp’s Common mode input voltage is $V_{CM} = V_{IN}/2$. The error at the input ($V_{ERR}$) appears at $V_{OUT}$ with a noise gain of 10 V/V.

FIGURE 1-6: Test Circuit for Dynamic Input Behavior.
2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = +1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 100kΩ$ to $V_L$ and $C_L = 20pF$.

2.1 DC Input Precision

**FIGURE 2-1:** Input Offset Voltage.

**FIGURE 2-2:** Input Offset Voltage Drift.

**FIGURE 2-3:** Input Offset Voltage Quadratic Temp. Co.

**FIGURE 2-4:** Input Offset Voltage vs. Power Supply Voltage with $V_{CM} = V_{CML}$.

**FIGURE 2-5:** Input Offset Voltage vs. Power Supply Voltage with $V_{CM} = V_{CMH}$.

**FIGURE 2-6:** Input Offset Voltage vs. Output Voltage.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +1.8V$ to $5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 100 \, k\Omega$ to $V_L$ and $C_L = 20 \, pF$. 

**FIGURE 2-7:** Input Offset Voltage vs. Common Mode Voltage with $V_{DD} = 1.8V$.

**FIGURE 2-8:** Input Offset Voltage vs. Common Mode Voltage with $V_{DD} = 5.5V$.

**FIGURE 2-9:** CMRR.

**FIGURE 2-10:** PSRR.

**FIGURE 2-11:** DC Open-Loop Gain.

**FIGURE 2-12:** CMRR and PSRR vs. Ambient Temperature.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 100\, \text{k}\Omega$ to $V_L$ and $C_L = 20\, \text{pF}$.

**FIGURE 2-13:** DC Open-Loop Gain vs. Ambient Temperature.

**FIGURE 2-14:** Input Bias and Offset Currents vs. Common Mode Input Voltage with $T_A = +85^\circ C$.

**FIGURE 2-15:** Input Bias and Offset Currents vs. Common Mode Input Voltage with $T_A = +125^\circ C$.

**FIGURE 2-16:** Input Bias and Offset Currents vs. Common Mode Input Voltage with $V_{DD} = +5.5V$.

**FIGURE 2-17:** Input Bias Current vs. Input Voltage (below $V_{SS}$).
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +1.8V$ to $5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 100\ \Omega$ to $V_L$ and $C_L = 20\ \text{pF}$.

### 2.2 Other DC Voltages and Currents

**FIGURE 2-18:** Input Common Mode Voltage Headroom (Range) vs. Ambient Temperature.

**FIGURE 2-19:** Output Voltage Headroom vs. Output Current.

**FIGURE 2-20:** Output Voltage Headroom vs. Ambient Temperature.

**FIGURE 2-21:** Output Short Circuit Current vs. Power Supply Voltage.

**FIGURE 2-22:** Supply Current vs. Power Supply Voltage.

**FIGURE 2-23:** Power-on Reset Trip Voltage.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 100 \, k\Omega$ to $V_L$ and $C_L = 20 \, pF$.

**FIGURE 2-24:** Power-on Reset Voltage vs. Ambient Temperature.
Note: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = +1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 100$ kΩ to $V_L$ and $C_L = 20$ pF.

2.3 Frequency Response

**FIGURE 2-25:** CMRR and PSRR vs. Frequency.

**FIGURE 2-26:** Open-Loop Gain vs. Frequency with $V_{DD} = 1.8V$.

**FIGURE 2-27:** Open-Loop Gain vs. Frequency with $V_{DD} = 5.5V$.

**FIGURE 2-28:** Gain Bandwidth Product and Phase Margin vs. Ambient Temperature.

**FIGURE 2-29:** Gain Bandwidth Product and Phase Margin vs. Common Mode Input Voltage.

**FIGURE 2-30:** Gain Bandwidth Product and Phase Margin vs. Output Voltage.
**Note:** Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 100 \, k\Omega$ to $V_L$ and $C_L = 20 \, pF$.

**FIGURE 2-31:** Closed-Loop Output Impedance vs. Frequency with $V_{DD} = 1.8V$.

**FIGURE 2-32:** Closed-Loop Output Impedance vs. Frequency with $V_{DD} = 5.5V$.

**FIGURE 2-33:** Channel-to-Channel Separation vs. Frequency.

**FIGURE 2-34:** Maximum Output Voltage Swing vs. Frequency.
**Note:** Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 100 \, \Omega$ to $V_L$ and $C_L = 20 \, pF$.

2.4 **Input Noise and Distortion**

**FIGURE 2-35:** Input Noise Voltage Density and Integrated Input Noise Voltage vs. Frequency.

**FIGURE 2-36:** Input Noise Voltage Density vs. Input Common Mode Voltage.

**FIGURE 2-37:** Inter-Modulation Distortion vs. Frequency with $V_{CM}$ Disturbance (see Figure 1-6).

**FIGURE 2-38:** Inter-Modulation Distortion vs. Frequency with $V_{DD}$ Disturbance (see Figure 1-6).

**FIGURE 2-39:** Input Noise vs. Time with 1 Hz and 10 Hz Filters and $V_{DD} = 1.8V$.

**FIGURE 2-40:** Input Noise vs. Time with 1 Hz and 10 Hz Filters and $V_{DD} = 5.5V$. 
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +1.8V$ to $5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 100k\Omega$ to $V_L$ and $C_L = 20\, pF$.

2.5 Time Response

FIGURE 2-41: Input Offset Voltage vs. Time with Temperature Change.

FIGURE 2-42: Input Offset Voltage vs. Time at Power Up.

FIGURE 2-43: The MCP6V31/1U/2/4 Family Shows No Input Phase Reversal with Overdrive.

FIGURE 2-44: Non-inverting Small Signal Step Response.

FIGURE 2-45: Non-inverting Large Signal Step Response.

FIGURE 2-46: Inverting Small Signal Step Response.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = +1.8V$ to $5.5V$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/3$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 100 \, k\Omega$ to $V_L$ and $C_L = 20 \, \text{pF}$.

**FIGURE 2-47:** Inverting Large Signal Step Response.

**FIGURE 2-48:** Slew Rate vs. Ambient Temperature.

**FIGURE 2-49:** Output Overdrive Recovery vs. Time with $G = -10 \, V/V$.

**FIGURE 2-50:** Output Overdrive Recovery Time vs. Inverting Gain.
3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

### TABLE 3-1: PIN FUNCTION TABLE

<table>
<thead>
<tr>
<th>MCP6V31</th>
<th>MCP6V31U</th>
<th>MCP6V32</th>
<th>MCP6V34</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOT-23</td>
<td>SOT-23, SC-70</td>
<td>2×3 TDFN</td>
<td>MSOP</td>
<td>TSSOP</td>
<td></td>
</tr>
<tr>
<td>1 VOUT, VOUTA</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Output (Op Amp A)</td>
</tr>
<tr>
<td>2 VIN−, VIN−</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>Inverting Input (Op Amp A)</td>
</tr>
<tr>
<td>3 VIN+, VIN+</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>Non-inverting Input (Op Amp A)</td>
</tr>
<tr>
<td>5 VDD</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>Positive Power Supply</td>
</tr>
<tr>
<td>8 VINB+</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>Non-inverting Input (Op Amp B)</td>
</tr>
<tr>
<td>9 VINB−</td>
<td>9</td>
<td>9</td>
<td>9</td>
<td>9</td>
<td>Inverting Input (Op Amp B)</td>
</tr>
<tr>
<td>11 VOUTB</td>
<td>11</td>
<td>11</td>
<td>11</td>
<td>11</td>
<td>Output (Op Amp B)</td>
</tr>
<tr>
<td>12 VOUTC</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>Output (Op Amp C)</td>
</tr>
<tr>
<td>13 VINC−</td>
<td>13</td>
<td>13</td>
<td>13</td>
<td>13</td>
<td>Inverting Input (Op Amp C)</td>
</tr>
<tr>
<td>14 VINC+</td>
<td>14</td>
<td>14</td>
<td>14</td>
<td>14</td>
<td>Non-inverting Input (Op Amp C)</td>
</tr>
<tr>
<td>15 VSS</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>Negative Power Supply</td>
</tr>
<tr>
<td>16 VIND+</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>Non-inverting Input (Op Amp D)</td>
</tr>
<tr>
<td>17 VIND−</td>
<td>17</td>
<td>17</td>
<td>17</td>
<td>17</td>
<td>Inverting Input (Op Amp D)</td>
</tr>
<tr>
<td>18 VOUTD</td>
<td>18</td>
<td>18</td>
<td>18</td>
<td>18</td>
<td>Output (Op Amp D)</td>
</tr>
<tr>
<td>19 EP</td>
<td>19</td>
<td>19</td>
<td>19</td>
<td>19</td>
<td>Exposed Thermal Pad (EP); must be connected to VSS</td>
</tr>
</tbody>
</table>

3.1 Analog Outputs

The analog output pins (VOUT) are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs (VIN+, VIN−, ...) are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (VDD) is 1.8V to 5.5V higher than the negative power supply (VSS). For normal operation, the other pins are between VSS and VDD.

Typically, these parts are used in a single (positive) supply configuration. In this case, VSS is connected to ground and VDD is connected to the supply. VDD will need bypass capacitors.

3.4 Exposed Thermal Pad (EP)

There is an internal connection between the exposed thermal pad (EP) and the VSS pin; they must be connected to the same potential on the printed circuit board (PCB).

This pad can be connected to a PCB ground plane to provide a larger heat sink. This improves the package thermal resistance (θJA).
4.0 APPLICATIONS

The MCP6V31/1U/2/4 family of zero-drift op amps is manufactured using Microchip’s state of the art CMOS process. It is designed for precision applications with requirements for small packages and low power. Its low supply voltage and low quiescent current make the MCP6V31/1U/2/4 devices ideal for battery-powered applications.

4.1 Overview of Zero-Drift Operation

Figure 4-1 shows a simplified diagram of the MCP6V31/1U/2/4 zero-drift op amps. This diagram will be used to explain how slow voltage errors are reduced in this architecture (much better $V_{OS}$, $\Delta V_{OS}/\Delta T_A (TC_1)$, CMRR, PSRR, $A_{OL}$ and 1/f noise).

![FIGURE 4-1: Simplified Zero-Drift Op Amp Functional Diagram.](image)

4.1.1 BUILDING BLOCKS

The Main Amplifier is designed for high gain and bandwidth, with a differential topology. Its main input pair (+ and - pins at the top left) is used for the higher frequency portion of the input signal. Its auxiliary input pair (+ and - pins at the bottom left) is used for the low-frequency portion of the input signal and corrects the op amp’s input offset voltage. Both inputs are added together internally.

The Auxiliary Amplifier, Chopper Input Switches and Chopper Output Switches provide a high DC gain to the input signal. DC errors are modulated to higher frequencies, while white noise is modulated to low frequency.

The Low-Pass Filter reduces high-frequency content, including harmonics of the Chopping Clock.

The Output Buffer drives external loads at the $V_{OUT}$ pin ($V_{REF}$ is an internal reference voltage).

The Oscillator runs at $f_{OSC_1} = 200$ kHz. Its output is divided by two, to produce the Chopping Clock rate of $f_{CHOP} = 100$ kHz.

The internal POR part starts the part in a known good state, protecting against power supply brown-outs.

The Digital Control block controls switching and POR events.

4.1.2 CHOPPING ACTION

Figure 4-2 shows the amplifier connections for the first phase of the Chopping Clock and Figure 4-3 shows them for the second phase. Its slow voltage errors alternate in polarity, making the average error small.

![FIGURE 4-2: First Chopping Clock Phase; Equivalent Amplifier Diagram.](image)

![FIGURE 4-3: Second Chopping Clock Phase; Equivalent Amplifier Diagram.](image)
4.1.3 INTERMODULATION DISTORTION (IMD)

These op amps will show intermodulation distortion (IMD) products when an AC signal is present.

The signal and clock can be decomposed into sine wave tones (Fourier series components). These tones interact with the zero-drift circuitry’s nonlinear response to produce IMD tones at sum and difference frequencies. Each of the square wave clock’s harmonics has a series of IMD tones centered on it. See Figure 2-37 and Figure 2-38.

4.2 Other Functional Blocks

4.2.1 RAIL-TO-RAIL INPUTS

The input stage of the MCP6V31/1U/2/4 op amps uses two differential CMOS input stages in parallel. One operates at low Common mode input voltage (V_{CM}, which is approximately equal to V_{IN^+} and V_{IN^-} in normal operation) and the other at high V_{CM}. With this topology, the input operates with V_{CM} up to V_{DD} + 0.2V, and down to V_{SS} – 0.15V, at +25°C (see Figure 2-18). The input offset voltage (V_{OS}) is measured at V_{CM} = V_{SS} – 0.15V and V_{DD} + 0.2V to ensure proper operation.

The transition between the input stages occurs when V_{CM} \approx V_{DD} – 0.9V (see Figure 2-7 and Figure 2-8). For the best distortion and gain linearity, with non-inverting gains, avoid this region of operation.

4.2.1.1 Phase Reversal

The input devices are designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-43 shows an input voltage exceeding both supplies with no phase inversion.

4.2.1.2 Input Voltage Limits

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the voltages at the input pins (see Section 1.1 “Absolute Maximum Ratings†”). This requirement is independent of the current limits discussed later on.

The ESD protection on the inputs can be depicted as shown in Figure 4-4. This structure was chosen to protect the input transistors against many (but not all) overvoltage conditions, and to minimize input bias current (I_{B}).
4.2.1.3 Input Current Limits

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents into the input pins (see Section 1.1 “Absolute Maximum Ratings†”). This requirement is independent of the voltage limits discussed previously.

Figure 4-6 shows one approach to protecting these inputs. The resistors R1 and R2 limit the possible current in or out of the input pins (and into D1 and D2). The diode currents will dump onto VDD.

\[ \text{min}(R_1, R_2) > \frac{V_{SS} - \text{min}(V_1, V_2)}{2 \text{ mA}} \]
\[ \text{min}(R_1, R_2) > \frac{\text{max}(V_1, V_2) - V_{DD}}{2 \text{ mA}} \]

**FIGURE 4-6:** Protecting the Analog Inputs Against High Currents.

It is also possible to connect the diodes to the left of resistors R1 and R2. In this case, the currents through the diodes D1 and D2 need to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins (V_{IN+} and V_{IN−}) should be very small.

A significant amount of current can flow out of the inputs (through the ESD diodes) when the Common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-17.

4.2.2 RAIL-TO-RAIL OUTPUT

The output voltage range of the MCP6V31/1U/2/4 zero-drift op amps is V_{DD} - 20 mV (minimum) and V_{SS} + 20 mV (maximum) when R_L = 10 kΩ is connected to V_{DD}/2 and V_{DD} = 5.5V. Refer to Figure 2-19 and Figure 2-20 for more information.

This op amp is designed to drive light loads; use another amplifier to buffer the output from heavy loads.

4.3 Application Tips

4.3.1 INPUT OFFSET VOLTAGE OVER TEMPERATURE

Table 1-1 gives both the linear and quadratic temperature coefficients (TC1 and TC2) of input offset voltage. The input offset voltage, at any temperature in the specified range, can be calculated as follows:

**EQUATION 4-1:**

\[ V_{OS}(T_A) = V_{OS} + TC_1\Delta T + TC_2\Delta T^2 \]

Where:

- \( \Delta T = T_A - 25°C \)
- \( V_{OS}(T_A) = \) input offset voltage at \( T_A \)
- \( V_{OS} = \) input offset voltage at +25°C
- \( TC_1 = \) linear temperature coefficient
- \( TC_2 = \) quadratic temperature coefficient

4.3.2 DC GAIN PLOTS

Figures 2-9 to 2-11 are histograms of the reciprocals (in units of \( \mu V/V \)) of CMRR, PSRR and A_{OL}, respectively. They represent the change in input offset voltage (V_{OS}) with a change in Common mode input voltage (V_{CM}), power supply voltage (V_{DD}) and output voltage (V_{OUT}).

The 1/A_{OL} histogram is centered near 0 \( \mu V/V \) because the measurements are dominated by the op amp’s input noise. The negative values shown represent noise and tester limitations, not unstable behavior. Production tests make multiple V_{OS} measurements, which validates an op amp’s stability; an unstable part would show greater V_{OS} variability, or the output would stick at one of the supply rails.

4.3.3 OFFSET AT POWER UP

When these parts power up, the input offset (V_{OS}) starts at its uncorrected value (usually less than ±5 mV). Circuits with high DC gain can cause the output to reach one of the two rails. In this case, the time to a valid output is delayed by an output overdrive time (like t_{ODR}), in addition to the start-up time (like t_{STR}).

It can be simple to avoid this extra start-up time. Reducing the gain is one method. Adding a capacitor across the feedback resistor (R_F) is another method.
4.3.4 SOURCE RESISTANCES
The input bias currents have two significant components; switching glitches that dominate at room temperature and below, and input ESD diode leakage currents that dominate at +85°C and above.

Make the resistances seen by the inputs small and equal. This minimizes the output offset caused by the input bias currents.

The inputs should see a resistance on the order of 10 Ω to 1 kΩ at high frequencies (i.e., above 1 MHz). This helps minimize the impact of switching glitches, which are very fast, on overall performance. In some cases, it may be necessary to add resistors in series with the inputs to achieve this improvement in performance.

Small input resistances may be needed for high gains. Without them, parasitic capacitances might cause positive feedback and instability.

4.3.5 SOURCE CAPACITANCE
The capacitances seen by the two inputs should be small. Large input capacitances and source resistances, together with high gain, can lead to positive feedback and instability.

4.3.6 CAPACITIVE LOADS
Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop’s phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. These zero-drift op amps have a different output impedance than most op amps, due to their unique topology.

When driving a capacitive load with these op amps, a series resistor at the output (R_ISO in Figure 4-7) improves the feedback loop’s phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

FIGURE 4-7: Output Resistor, R_ISO, Stabilizes Capacitive Loads.

FIGURE 4-8: Recommended R_ISO values for Capacitive Loads.

After selecting R_ISO for your circuit, double check the resulting frequency response peaking and step response overshoot. Modify R_ISO’s value until the response is reasonable. Bench evaluation is helpful.

4.3.7 STABILIZING OUTPUT LOADS
This family of zero-drift op amps has an output impedance (Figure 2-31 and Figure 2-32) that has a double zero when the gain is low. This can cause a large phase shift in feedback networks that have low-impedance near the part’s bandwidth. This large phase shift can cause stability problems.

Figure 4-9 shows that the load on the output is (R_L + R_ISO)||(R_F + R_G), where R_ISO is before the load (like Figure 4-7). This load needs to be large enough to maintain stability; it should be at least 10 kΩ.

FIGURE 4-9: Output Load.

\( G_N \) is the circuit's noise gain. For non-inverting gains, \( G_N \) and the Signal Gain are equal. For inverting gains, \( G_N = 1 + |\text{Signal Gain}| \) (e.g., -1 V/V gives \( G_N = +2 \) V/V).
4.3.8 GAIN PEAKING

Figure 4-10 shows an op amp circuit that represents non-inverting amplifiers (V_M is a DC voltage and V_P is the input) or inverting amplifiers (V_P is a DC voltage and V_M is the input). The capacitances C_N and C_G represent the total capacitance at the input pins; they include the op amp’s Common mode input capacitance (C_{CM}), board parasitic capacitance and any capacitor placed in parallel. The capacitance C_{FP} represents the parasitic capacitance coupling the output and non-inverting input pins.

![Amplifier with Parasitic Capacitance](image)

**FIGURE 4-10:** Amplifier with Parasitic Capacitance.

C_G acts in parallel with R_G (except for a gain of +1 V/V), which causes an increase in gain at high frequencies. C_G also reduces the phase margin of the feedback loop, which becomes less stable. This effect can be reduced by either reducing C_G or R_F||R_G.

C_N and R_N form a low-pass filter that affects the signal at V_P. This filter has a single real pole at 1/(2πR_NC_N). The largest value of R_F that should be used depends on noise gain (see C_N in Section 4.3.6 “Capacitive Loads”). C_G and the open-loop gain’s phase shift. An approximate limit for R_F is:

**EQUATION 4-2:**

\[ R_F \leq \frac{(10 \text{ k}\Omega) \times \frac{12 \text{ pF}}{C_G} \times C_N^2}{10} \]

Some applications may modify these values to reduce either output loading or gain peaking (step response overshoot).

At high gains, R_N needs to be small, in order to prevent positive feedback and oscillations. Large C_N values can also help.

4.3.9 REDUCING UNDESIRABLE NOISE AND SIGNALS

Reduce undesired noise and signals with:

- Low bandwidth signal filters:
  - Minimizes random analog noise
  - Reduces interfering signals
- Good PCB layout techniques:
  - Minimizes crosstalk
  - Minimizes parasitic capacitances and inductances that interact with fast switching edges
- Good power supply design:
  - Isolation from other parts
  - Filtering of interference on supply line(s)

4.3.10 SUPPLY BYPASSING AND FILTERING

With this family of operational amplifiers, the power supply pin (V_DD for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm of the pin for good high-frequency performance.

These parts also need a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other low noise, analog parts.

In some cases, high-frequency power supply noise (e.g., switched mode power supplies) may cause undue intermodulation distortion, with a DC offset shift; this noise needs to be filtered. Adding a resistor into the supply connection can be helpful.

4.3.11 PCB DESIGN FOR DC PRECISION

In order to achieve DC precision on the order of ±1 µV, many physical errors need to be minimized. The design of the Printed Circuit Board (PCB), the wiring, and the thermal environment have a strong impact on the precision achieved. A poor PCB design can easily be more than 100 times worse than the MCP6V31/1U/2/4 op amps’ minimum and maximum specifications.

4.3.11.1 PCB Layout

Any time two dissimilar metals are joined together, a temperature dependent voltage appears across the junction (the Seebeck or thermojunction effect). This effect is used in thermocouples to measure temperature. The following are examples of thermojunctions on a PCB:

- Components (resistors, op amps, …) soldered to a copper pad
- Wires mechanically attached to the PCB
- Jumpers
- Solder joints
- PCB vias
Typical thermojunctions have temperature to voltage conversion coefficients of 1 to 100 µV/°C (sometimes higher).

Microchip’s AN1258 (“Op Amp Precision Design: PCB Layout Techniques”) contains in-depth information on PCB layout techniques that minimize thermojunction effects. It also discusses other effects, such as crosstalk, impedances, mechanical stresses and humidity.

4.3.11.2 Crosstalk
DC crosstalk causes offsets that appear as a larger input offset voltage. Common causes include:
- Common mode noise (remote sensors)
- Ground loops (current return paths)
- Power supply coupling

Interference from the mains (usually 50 Hz or 60 Hz), and other AC sources, can also affect the DC performance. Nonlinear distortion can convert these signals to multiple tones, including a DC shift in voltage. When the signal is sampled by an ADC, these AC signals can also be aliased to DC, causing an apparent shift in offset.

To reduce interference:
- Keep traces and wires as short as possible
- Use shielding
- Use ground plane (at least a star ground)
- Place the input signal source near to the DUT
- Use good PCB layout techniques
- Use a separate power supply filter (bypass capacitors) for these zero-drift opamps

4.3.11.3 Miscellaneous Effects
Keep the resistances seen by the input pins as small and as near to equal as possible, to minimize bias-current-related offsets.

Make the (trace) capacitances seen by the input pins small and equal. This is helpful in minimizing switching glitch-induced offset voltages.

Bending a coax cable with a radius that is too small causes a small voltage drop to appear on the center conductor (the triboelectric effect). Make sure the bending radius is large enough to keep the conductors and insulation in full contact.

Mechanical stresses can make some capacitor types (such as some ceramics) output small voltages. Use more appropriate capacitor types in the signal path and minimize mechanical stresses and vibration.

Humidity can cause electrochemical potential voltages to appear in a circuit. Proper PCB cleaning helps, as does the use of encapsulants.

4.4 Typical Applications

4.4.1 WHEATSTONE BRIDGE
Many sensors are configured as Wheatstone bridges. Strain gauges and pressure sensors are two common examples. These signals can be small and the Common mode noise large. Amplifier designs with high differential gain are desirable.

Figure 4-11 shows how to interface to a Wheatstone bridge with a minimum of components. Because the circuit is not symmetric, the ADC input is single ended, and there is a minimum of filtering; the CMRR is good enough for moderate Common mode noise.

![Figure 4-11: Simple Design.](image)

4.4.2 RTD SENSOR
The ratiometric circuit in Figure 4-12 conditions a two-wire RTD, for applications with a limited temperature range. U₁ acts a difference amplifier, with a low-frequency pole. The sensor’s wiring resistance (R_W) is corrected in firmware. Failure (open) of the RTD is detected by an out-of-range voltage.

![Figure 4-12: RTD Sensor.](image)
4.4.3 OFFSET VOLTAGE CORRECTION

Figure 4-13 shows MCP6V31 (U2) correcting the input offset voltage of another op amp (U1). R2 and C2 integrate the offset error seen at U1’s input; the integration needs to be slow enough to be stable (with the feedback provided by R1 and R3). R4 and R5 attenuate the integrator’s output; this shifts the integrator pole down in frequency.

4.4.4 PRECISION COMPARATOR

Use high gain before a comparator to improve the latter’s performance. Do not use MCP6V31/1U/2/4 as a comparator by itself; the VOS correction circuitry does not operate properly without a feedback loop.
5.0 DESIGN AIDS

Microchip provides the basic design aids needed for the MCP6V31/1U/2/4 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6V31/1U/2/4 op amps is available on the Microchip web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp’s linear region of operation over the temperature range. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip’s FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at www.microchip.com/maps, MAPS is an overall selection tool for Microchip’s product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, a customer can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data Sheets, Purchase and Sampling of Microchip parts.

5.4 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help customers achieve faster time to market. For a complete listing of these boards and their corresponding user’s guides and technical information, visit the Microchip web site at www.microchip.com/analog tools.

Some boards that are especially useful are:
- MCP6V01 Thermocouple Auto-Zeroed Reference Design (P/N MCP6V01RD-TCPL)
- MCP6XXX Amplifier Evaluation Board 1 (P/N DS51667)
- MCP6XXX Amplifier Evaluation Board 2 (P/N DS51668)
- MCP6XXX Amplifier Evaluation Board 3 (P/N DS51673)
- MCP6XXX Amplifier Evaluation Board 4 (P/N DS51681)
- Active Filter Demo Board Kit (P/N DS51614)
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board (P/N SOIC8EV)
- 14-Pin SOIC/TSSOP/DIP Evaluation Board (P/N SOIC14EV)

5.5 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

ADN003: “Select the Right Operational Amplifier for your Filtering Circuits”, DS21821
AN722: “Operational Amplifier Topologies and DC Specifications”, DS00722
AN723: “Operational Amplifier AC Specifications and Applications”, DS00723
AN884: “Driving Capacitive Loads With Op Amps”, DS00884
AN990: “Analog Sensor Conditioning Circuits – An Overview”, DS00990
AN1177: “Op Amp Precision Design: DC Errors”, DS01177
AN1228: “Op Amp Precision Design: Random Noise”, DS01228
AN1258: “Op Amp Precision Design: PCB Layout Techniques”, DS01258

These Application Notes and others are listed in the design guide:
“Signal Chain Design Guide”, DS21825
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

5-Lead SC70 (MCP6V31U)

Example:

**Legend:**
- XX...X Customer-specific information
- Y Year code (last digit of calendar year)
- YY Year code (last 2 digits of calendar year)
- WWW Week code (week of January 1 is week '01')
- NNN Alphanumeric traceability code
- e3 Pb-free JEDEC® designator for Matte Tin (Sn)

- This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
8-Lead TDFN (2x3x0.75 mm) (MCP6V32)

<table>
<thead>
<tr>
<th>Device</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP6V32-E/MNY</td>
<td>ABW</td>
</tr>
<tr>
<td>MCP6V32T-E/MNY</td>
<td>ABW</td>
</tr>
</tbody>
</table>

Note: Applies to 8-Lead 2x3 TDFN.

14-Lead TSSOP (4.4 mm) (MCP6V34)

Example
5-Lead Plastic Small Outline Transistor (LT) [SC70]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com-packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
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</thead>
<tbody>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

**Notes:**
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B
5-Lead Plastic Small Outline Transistor (LT) [SC70]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

![Diagram of the 5-Lead Plastic Small Outline Transistor (LT) with dimensions labeled as E, Gx, C, G, Y, X, and 3, 2, 1, 4, 5.]

**Recommended Land Pattern**

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
</tr>
<tr>
<td>Contact Pad Width</td>
<td>X</td>
</tr>
<tr>
<td>Contact Pad Length</td>
<td>Y</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>Gx</td>
</tr>
</tbody>
</table>

**Notes:**
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061A
5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
<td>NOM</td>
<td>MAX</td>
<td></td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Pitch</td>
<td>e</td>
<td>0.95 BSC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Outside Lead Pitch</td>
<td>e1</td>
<td>1.90 BSC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
<td>0.90</td>
<td>–</td>
<td>1.45</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
<td>0.89</td>
<td>–</td>
<td>1.30</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
<td>0.00</td>
<td>–</td>
<td>0.15</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
<td>2.20</td>
<td>–</td>
<td>3.20</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
<td>1.30</td>
<td>–</td>
<td>1.80</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
<td>2.70</td>
<td>–</td>
<td>3.10</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
<td>0.10</td>
<td>–</td>
<td>0.60</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
<td>0.35</td>
<td>–</td>
<td>0.80</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
<td>0°</td>
<td>–</td>
<td>30°</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
<td>0.08</td>
<td>–</td>
<td>0.26</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
<td>0.20</td>
<td>–</td>
<td>0.51</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B
5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com-packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
</tr>
<tr>
<td>Contact Pad Width (X5)</td>
<td>X</td>
</tr>
<tr>
<td>Contact Pad Length (X5)</td>
<td>Y</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>GX</td>
</tr>
<tr>
<td>Overall Width</td>
<td>Z</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Dimension Limits</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>$\varphi$</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

**RECOMMENDED LAND PATTERN**

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
<th>Dimension Limits</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contact Pitch</td>
<td>E</td>
<td>0.65 BSC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
<td>4.40</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overall Width</td>
<td>Z</td>
<td>5.85</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact Pad Width (X8)</td>
<td>X1</td>
<td>0.45</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact Pad Length (X8)</td>
<td>Y1</td>
<td>1.45</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G1</td>
<td>2.95</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>GX</td>
<td>0.20</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A
8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
</tbody>
</table>

| Number of Pins | N | 8 |
| Pitch | e | 0.50 BSC |
| Overall Height | A | 0.70 | 0.75 | 0.80 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | 0.20 REF |
| Overall Length | D | 2.00 BSC |
| Overall Width | E | 3.00 BSC |
| Exposed Pad Length | D2 | 1.20 | - | 1.60 |
| Exposed Pad Width | E2 | 1.20 | - | 1.60 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.25 | 0.30 | 0.45 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129C Sheet 2 of 2
8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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**RECOMMENDED LAND PATTERN**

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<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Optional Center Pad Width</td>
<td>W2</td>
</tr>
<tr>
<td>Optional Center Pad Length</td>
<td>T2</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C1</td>
</tr>
<tr>
<td>Contact Pad Width (X8)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X8)</td>
<td>Y1</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A
14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing  C04-087C Sheet 1 of 2
### 14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
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<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Molded Package Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>(L1)</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>$\varphi$</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension, Theoretically exact value shown without tolerances,
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

RECOMMENDED LAND PATTERN

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
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</thead>
<tbody>
<tr>
<td>Dimension</td>
<td>Limits MIN NOM MAX</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E 0.65 BSC</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C1 5.90</td>
</tr>
<tr>
<td>Contact Pad Width (X14)</td>
<td>X1 0.45</td>
</tr>
<tr>
<td>Contact Pad Length (X14)</td>
<td>Y1 1.45</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G 0.20</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A
APPENDIX A: REVISION HISTORY

Revision B (March 2014)

The following is the list of modifications:

1. Added new devices to the family: MCP6V32 and MCP6V34, and the related information throughout the document.
2. Updated Table 1-3 with new packages’ thermal resistances.
3. Updated Figures 2-6, 2-19 and 2-22 in Section 2.0 “Typical Performance Curves”. Added new Figure 2-33.
4. Updated Table 3-1 in Section 3.0 “Pin Descriptions” for the new devices.
5. Updated markings and specification drawings in Section 6.0 “Packaging Information”.

Revision A (March 2012)

• Original Release of this Document.
**PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>Device</th>
<th>Tape and Reel</th>
<th>Temperature Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td><a href="-X">X</a></td>
<td>MCP6V31T:</td>
<td>Single Op Amp (Tape and Reel) (SOT-23)</td>
<td>E = -40°C to +125°C (Extended)</td>
<td>LT = Plastic Small Outline Transistor, 5-lead</td>
</tr>
<tr>
<td></td>
<td>MCP6V31UT:</td>
<td>Single Op Amp (Tape and Reel) (SC-70, SOT-23)</td>
<td></td>
<td>OT = Plastic Small Outline Transistor, 5-lead</td>
</tr>
<tr>
<td></td>
<td>MCP6V32:</td>
<td>Dual Op Amp (MSOP, 2x3 TDFN)</td>
<td></td>
<td>MNY* = Plastic Dual Flat, No-Lead - 2×3×0.75 mm</td>
</tr>
<tr>
<td></td>
<td>MCP6V32T:</td>
<td>Dual Op Amp (Tape and Reel) (MSOP, 2x3 TDFN)</td>
<td></td>
<td>Body, 8-lead</td>
</tr>
<tr>
<td></td>
<td>MCP6V34:</td>
<td>Quad Op Amp (TSSOP)</td>
<td></td>
<td>MS = Plastic Micro Small Outline, 8-lead</td>
</tr>
<tr>
<td></td>
<td>MCP6V34T:</td>
<td>Quad Op Amp (Tape and Reel) (TSSOP)</td>
<td></td>
<td>ST = Plastic Thin Shrink Small Outline - 4.4 mm</td>
</tr>
</tbody>
</table>

* Y = Nickel palladium gold manufacturing designator. Only available on the TDFN package.

**Examples:**

- a) MCP6V31T-E/OT: Tape and Reel, Extended temperature, 5LD SOT-23 package
- b) MCP6V31UT-E/LT: Tape and Reel, Extended temperature, 5LD SC70 package
- c) MCP6V32-E/MS: Extended temperature, 8LD MSOP package
- d) MCP6V32T-E/MS: Tape and Reel, Extended temperature, 8LD MSOP package
- e) MCP6V32T-E/MNY: Tape and Reel, Extended temperature, 8LD 2x3 TDFN package
- f) MCP6V34-E/ST: Extended temperature, 14LD TSSOP package
- g) MCP6V34T-E/ST: Tape and Reel, Extended temperature, 14LD TSSOP package

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
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