TC1413/TC1413N
3A High-Speed MOSFET Drivers

Features

- Latch-Up Protected: Withstands 500 mA Reverse Current
- Input Withstands Negative Inputs Up to 5V
- Electrostatic Discharge (ESD) Protected: 2.0 kV (HBM) and 400V (MM)
- High Peak Output Current: 3A
- Wide Input Supply Voltage Operating Range: -4.5V to 16V
- High Capacitive Load Drive Capability:
  - 1800 pF in 20 ns
- Short Delay Time: 35 ns typical
- Matched Delay Times
- Low Supply Current
  - With Logic ‘1’ Input: 500 µA
  - With Logic ‘0’ Input: 100 µA
- Low Output Impedance: 2.7Ω
- Available in Space-Saving 8-pin MSOP Package
- Pinout - same as TC1410/TC1411/TC1412

Applications

- Switch Mode Power Supplies
- Line Drivers
- Pulse Transformer Drive
- Relay Driver

General Description

The TC1413/TC1413N are 3A CMOS buffers/drivers. They do not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking of either polarity occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of current of either polarity being forced back into their output. All terminals are fully protected against electrostatic discharge (ESD) up to 2.0 kV (HBM) and 400V (MM).

As MOSFET drivers, the TC1413/TC1413N can easily charge a 1800 pF gate capacitance in 20 ns with matched rise and fall times. To ensure the MOSFET’s intended state will not be affected even by large transients, low enough impedance in both the ‘On’ and ‘Off’ states are provided. The leading and trailing edge propagation delay times are also matched to allow driving short-duration inputs with greater accuracy.

Package Type

<table>
<thead>
<tr>
<th>8-Pin MSOP/PDIP/SOIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD 1 ●</td>
</tr>
<tr>
<td>IN 2</td>
</tr>
<tr>
<td>TC1413</td>
</tr>
<tr>
<td>NC 3</td>
</tr>
<tr>
<td>GND 4</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>6,7</td>
</tr>
<tr>
<td>Inverting</td>
</tr>
<tr>
<td>VDD 5 ●</td>
</tr>
<tr>
<td>OUT 6</td>
</tr>
<tr>
<td>OUT 7</td>
</tr>
<tr>
<td>NC 12</td>
</tr>
<tr>
<td>GND 13</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>6,7</td>
</tr>
<tr>
<td>Non-Inverting</td>
</tr>
</tbody>
</table>

NC = No Internal Connection

Note: For proper operation, duplicate pins must be connected together.
Functional Block Diagram

Input = 10 pF

Effective Input C = 10 pF

4.7V

GND

300 mV

TC1413

Inverting Outputs

Non-Inverting Outputs

TC1413N

VDD

Output
1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage .....................................................+20V
Input Voltage ......................VDD + 0.3V to GND – 5.0V
Power Dissipation (TA ≤ 70°C)
    MSOP ..........................................................340 mW
    PDIP ............................................................ 730 mW
    SOIC............................................................ 470 mW
Storage Temperature Range.............. -65°C to +150°C
Maximum Junction Temperature...................... +150ºC

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic '1', High Input Voltage</td>
<td>V_H</td>
<td>2.0</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>0V ≤ V_IN ≤ V_DD, TA = +25°C</td>
</tr>
<tr>
<td>Logic '0', Low Input Voltage</td>
<td>V_L</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>-40°C ≤ TA ≤ +85°C</td>
</tr>
<tr>
<td>Input Current</td>
<td>I_IN</td>
<td>-1.0</td>
<td>—</td>
<td>1.0</td>
<td>µA</td>
<td>-40°C ≤ TA ≤ +85°C</td>
</tr>
<tr>
<td>Output</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High Output Voltage</td>
<td>V_OH</td>
<td>V_DD – 0.025</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>DC Test</td>
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<tr>
<td>Low Output Voltage</td>
<td>V_OH</td>
<td>—</td>
<td>—</td>
<td>0.025</td>
<td>V</td>
<td>V_DD = 16V, I_O = 10 mA, TA = +25°C</td>
</tr>
<tr>
<td>Output Resistance</td>
<td>R_O</td>
<td>—</td>
<td>2.7</td>
<td>4.0</td>
<td>Ω</td>
<td>0°C ≤ TA ≤ +70°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>3.3</td>
<td>5.0</td>
<td></td>
<td>-40°C ≤ TA ≤ +85°C</td>
</tr>
<tr>
<td>Peak Output Current</td>
<td>I_PK</td>
<td>—</td>
<td>3.0</td>
<td>—</td>
<td>A</td>
<td>V_DD = 16V</td>
</tr>
<tr>
<td>Latch-Up Protection Withstand</td>
<td>I_REV</td>
<td>—</td>
<td>0.5</td>
<td>—</td>
<td>A</td>
<td>Duty cycle ≤ 2%, t ≤ 300 µs, V_DD = 16V</td>
</tr>
<tr>
<td>Reverse Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Switching Time (Note 1)

<table>
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<tr>
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<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rise Time</td>
<td>t_r</td>
<td>20</td>
<td>28</td>
<td>—</td>
<td>ns</td>
<td>T_A = +25°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>22</td>
<td>33</td>
<td>—</td>
<td></td>
<td>0°C ≤ T_A ≤ +70°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>24</td>
<td>33</td>
<td>—</td>
<td></td>
<td>-40°C ≤ T_A ≤ +85°C, Figure 4-1</td>
</tr>
<tr>
<td>Fall Time</td>
<td>t_f</td>
<td>20</td>
<td>28</td>
<td>—</td>
<td>ns</td>
<td>T_A = +25°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>22</td>
<td>33</td>
<td>—</td>
<td></td>
<td>0°C ≤ T_A ≤ +70°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>24</td>
<td>33</td>
<td>—</td>
<td></td>
<td>-40°C ≤ T_A ≤ +85°C, Figure 4-1</td>
</tr>
<tr>
<td>Delay Time</td>
<td>t_d1</td>
<td>35</td>
<td>45</td>
<td>—</td>
<td>ns</td>
<td>T_A = +25°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>40</td>
<td>50</td>
<td>—</td>
<td></td>
<td>0°C ≤ T_A ≤ +70°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>40</td>
<td>50</td>
<td>—</td>
<td></td>
<td>-40°C ≤ T_A ≤ +85°C, Figure 4-1</td>
</tr>
<tr>
<td>Delay Time</td>
<td>t_d2</td>
<td>35</td>
<td>45</td>
<td>—</td>
<td>ns</td>
<td>T_A = +25°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>40</td>
<td>50</td>
<td>—</td>
<td></td>
<td>0°C ≤ T_A ≤ +70°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>40</td>
<td>50</td>
<td>—</td>
<td></td>
<td>-40°C ≤ T_A ≤ +85°C, Figure 4-1</td>
</tr>
</tbody>
</table>

Power Supply

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply</td>
<td>I_S</td>
<td>0.5</td>
<td>1.0</td>
<td>—</td>
<td>mA</td>
<td>V_IN = 3V, V_DD = 16V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.1</td>
<td>0.15</td>
<td>—</td>
<td></td>
<td>V_IN = 0V</td>
</tr>
</tbody>
</table>

Note 1: Switching times ensured by design.
## TEMPERATURE CHARACTERISTICS

**Electrical Specifications:** Unless otherwise noted, all parameters apply with $4.5V \leq V_{DD} \leq 18V$.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Temperature Ranges</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Specified Temperature Range (C)</td>
<td>$T_A$</td>
<td>0</td>
<td>—</td>
<td>+70</td>
<td>ºC</td>
<td></td>
</tr>
<tr>
<td>Specified Temperature Range (E)</td>
<td>$T_A$</td>
<td>-40</td>
<td>—</td>
<td>+85</td>
<td>ºC</td>
<td></td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>$T_J$</td>
<td>—</td>
<td>—</td>
<td>+150</td>
<td>ºC</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_A$</td>
<td>-65</td>
<td>—</td>
<td>+150</td>
<td>ºC</td>
<td></td>
</tr>
<tr>
<td><strong>Package Thermal Resistances</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 8L-MSOP</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>211</td>
<td>—</td>
<td>ºC/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 8L-PDIP</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>89.3</td>
<td>—</td>
<td>ºC/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 8L-SOIC</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>149.5</td>
<td>—</td>
<td>ºC/W</td>
<td></td>
</tr>
</tbody>
</table>
2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, over operating temperature range with \(4.5V \leq V_{DD} \leq 16V\).

**FIGURE 2-1:** Quiescent Supply Current vs. Supply Voltage.

**FIGURE 2-2:** Input Threshold vs. Supply Voltage.

**FIGURE 2-3:** High State Output Resistance vs. Supply Voltage.

**FIGURE 2-4:** Quiescent Supply Current vs. Temperature.

**FIGURE 2-5:** Input Threshold vs. Temperature.

**FIGURE 2-6:** Low State Output Resistance vs. Supply Voltage.
Note: Unless otherwise indicated, over operating temperature range with $4.5\text{V} \leq V_{\text{DD}} \leq 16\text{V}$.

**FIGURE 2-7:** Rise Time vs. Supply Voltage.

**FIGURE 2-8:** Propagation Delay vs. Supply Voltage.

**FIGURE 2-9:** Rise and Fall Times vs. Capacitive Load.

**FIGURE 2-10:** Fall Time vs. Supply Voltage.

**FIGURE 2-11:** Propagation Delay vs. Supply Voltage.

**FIGURE 2-12:** Propagation Delays vs. Capacitive Load.
3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

### TABLE 3-1: PIN FUNCTION TABLE

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>TC1413 MSOP, PDIP, SOIC</th>
<th>TC1413N MSOP, PDIP, SOIC</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( V_{DD} )</td>
<td>( V_{DD} )</td>
<td>Supply input, 4.5V to 16V</td>
</tr>
<tr>
<td>2</td>
<td>IN</td>
<td>IN</td>
<td>Control input</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td>NC</td>
<td>No connection</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>6</td>
<td>OUT</td>
<td>OUT</td>
<td>CMOS push-pull output, common to pin 7</td>
</tr>
<tr>
<td>7</td>
<td>OUT</td>
<td>OUT</td>
<td>CMOS push-pull output, common to pin 6</td>
</tr>
<tr>
<td>8</td>
<td>( V_{DD} )</td>
<td>( V_{DD} )</td>
<td>Supply input, 4.5V to 16V</td>
</tr>
</tbody>
</table>

3.1 Supply Input (\( V_{DD} \))

The \( V_{DD} \) input is the bias supply for the MOSFET driver and is rated for 4.5V to 16V with respect to the ground pin. The \( V_{DD} \) input should be bypassed to ground with a local ceramic capacitor. The value of the capacitor is chosen based on the capacitive load that is being driven. A value of 1.0 \( \mu \)F is suggested.

3.2 Control Input (IN)

The MOSFET driver input is a high-impedance, TTL/CMOS-compatible input. The input has 300 mV of hysteresis between the high and low thresholds which prevents output glitching even when the rise and fall time of the input signal is very slow.

3.3 CMOS Push-Pull Output (OUT, OUT)

The MOSFET driver output is a low-impedance, CMOS push-pull style output, capable of driving a capacitive load with 3A peak currents.

3.4 Ground (GND)

The ground pins are the return path for the bias current and for the high peak currents that discharge the load capacitor. The ground pins should be tied into a ground plane or have very short traces to the bias supply source return.

3.5 No Connect (NC)

No internal connection.
4.0 APPLICATION INFORMATION

**FIGURE 4-1: Switching Time Test Circuit.**

- **Inverting Driver**
  - Input: +5V
  - Output: 0V
  - $V_{DD} = 16V$
  - $t_{RISE} = t_{FALL} \leq 10\,\text{ns}$

- **Non-Inverting Driver**
  - Input: 0V
  - Output: 0V
  - $C_L = 1800\,\mu\text{F}$
  - $t_{D1}$, $t_{D2}$, $t_{F}$, $t_{R}$

**Input:** 100 kHz, square wave, $t_{RISE} = t_{FALL} \leq 10\,\text{ns}$
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

Legend:
- XX...X: Customer-specific information
- Y: Year code (last digit of calendar year)
- YY: Year code (last 2 digits of calendar year)
- WW: Week code (week of January 1 is week '01')
- NNN: Alphanumeric traceability code
- RoHS Compliant JEDEC® designator for Matte Tin (Sn)

OR

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
TC1413/TC1413N

8-Lead SOIC (3.90 mm)

8-Lead MSOP (3x3 mm)

Example

TC1413C
OAe31318
256

TC1413
COA1318
256

1413E
318256
8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)
TC1413/TC1413N

8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>Dimension Limits</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Pins</td>
<td>N</td>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
<td>.100 BSC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Top to Seating Plane</td>
<td>A</td>
<td></td>
<td>-</td>
<td>.210</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
<td>.115</td>
<td>.130</td>
<td>.195</td>
</tr>
<tr>
<td>Base to Seating Plane</td>
<td>A1</td>
<td>.015</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shoulder to Shoulder Width</td>
<td>E</td>
<td>.290</td>
<td>.310</td>
<td>.325</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
<td>.240</td>
<td>.250</td>
<td>.280</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
<td>.348</td>
<td>.365</td>
<td>.400</td>
</tr>
<tr>
<td>Tip to Seating Plane</td>
<td>L</td>
<td>.115</td>
<td>.130</td>
<td>.150</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
<td>.008</td>
<td>.010</td>
<td>.015</td>
</tr>
<tr>
<td>Upper Lead Width</td>
<td>b1</td>
<td>.040</td>
<td>.060</td>
<td>.070</td>
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<tr>
<td>Lower Lead Width</td>
<td>b</td>
<td>.014</td>
<td>.018</td>
<td>.022</td>
</tr>
<tr>
<td>Overall Row Spacing</td>
<td>eB</td>
<td>-</td>
<td>-</td>
<td>.430</td>
</tr>
</tbody>
</table>

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” per side.
4. Dimensioning and tolerancing per ASME Y14.5M

Microchip Technology Drawing No. C04-018D Sheet 2 of 2
TC1413/TC1413N

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing No. C04-057C Sheet 1 of 2
TC1413/TC1413N

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
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<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
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<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>$</td>
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<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
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<tr>
<td>Overall Length</td>
<td>D</td>
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<tr>
<td>Chamfer (Optional)</td>
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<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
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<tr>
<td>Foot Angle</td>
<td>$</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
<tr>
<td>Mold Draft Angle Top</td>
<td>$\alpha$</td>
</tr>
<tr>
<td>Mold Draft Angle Bottom</td>
<td>$\beta$</td>
</tr>
</tbody>
</table>

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. $§$ Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2
8-Lead Plastic Small Outline (OA) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

### Recommended Land Pattern

---

<table>
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<tr>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td></td>
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</tr>
<tr>
<td>Dimension</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
</tr>
<tr>
<td>Contact Pad Width (X8)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X8)</td>
<td>Y1</td>
</tr>
</tbody>
</table>

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

---

Microchip Technology Drawing No. C04-2057A
8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing C04-111C Sheet 1 of 2
8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

###Dimensions

<table>
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<tr>
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<tr>
<td>Number of Pins</td>
<td>N</td>
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<tr>
<td>Pitch</td>
<td>e</td>
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<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>$\varphi$</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

---

Microchip Technology Drawing C04-111C Sheet 2 of 2
8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

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<td>Overall Width</td>
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<tr>
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<tr>
<td>Distance Between Pads</td>
<td>G1</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>GX</td>
</tr>
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</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A
APPENDIX A: REVISION HISTORY

Revision E (February 2015)
The following is the list of modifications:
• Updated the values for electrostatic discharge in the Features and General Description columns.
• Updated the Pin Description table in Section 3.0, Pin Descriptions.
• Updated package marking information and drawings in Section 5.0, Packaging Information.
• Minor grammatical and spelling corrections.

Revision D (December 2012)
• Added a note to each package outline drawing.

Revision C (March 2003)
• Undocumented changes.

Revision B (May 2001)
• Undocumented changes.

Revision A (March 2001)
• Original Release of this Document.
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>X</th>
<th>/XX</th>
</tr>
</thead>
<tbody>
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<tr>
<td>Temperature Range</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Device:  
TC1413: 3A Single MOSFET Driver, Inverting  
TC1413N: 3A Single MOSFET Driver, Non-Inverting

Temperature Range:  
C = 0°C to +70°C  
E = -40°C to +85°C

Package:  
OA = Plastic SOIC, (150 mil Body), 8-lead  
OA713 = Plastic SOIC, (150 mil Body), 8-lead (Tape and Reel)  
UA = Plastic Micro Small Outline (MSOP), 8-lead *  
UA713 = Plastic Micro Small Outline (MSOP), 8-lead * (Tape and Reel)  
PA = Plastic DIP (300 mil Body), 8-lead  
* MSOP package is only available in E-Temp.

Examples:

a) TC1413COA: 3A Single MOSFET driver, SOIC package, 0°C to +70°C.  
b) TC1413CPA: 3A Single MOSFET driver, PDIP package, 0°C to +70°C.  
c) TC1413EUA713: Tape and Reel, 3A Single MOSFET driver, MSOP package, -40°C to +85°C.

a) TC1413NCPA: 3A Single MOSFET driver, PDIP package, 0°C to +70°C.  
b) TC1413NEPA: 3A Single MOSFET driver, PDIP package, -40°C to +85°C.  
c) TC1413NEUA: 3A Single MOSFET driver, MSOP package, -40°C to +85°C.
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