**TC1232**

**Microprocessor Monitor**

**Features:**
- Precision Voltage Monitor:
  - Adjustable +4.5V or +4.75V
- Reset Pulse Width – 250 ms minimum
- No External Components
- Adjustable Watchdog Timer:
  - 150 ms, 600 ms or 1.2s
- Operating Voltage 4.0V to 5.5V
- Debounced Manual Reset Input for External Override

**General Description:**

The TC1232 is a fully-integrated processor supervisor that provides three important functions to safeguard processor sanity: precision power on/off Reset control, Watchdog Timer and external Reset override.

On power-up, the TC1232 holds the processor in the Reset state for a minimum of 250 ms after VCC is within tolerance to ensure a stable system start-up.

Microprocessor sanity is monitored by the on-board watchdog circuit. The microprocessor must provide a periodic low-going signal on the ST input. Should the processor fail to supply this signal within the selected time-out period (150 ms, 600 ms or 1200 ms), an out-of-control processor is indicated and the TC1232 issues a processor Reset as a result.

The outputs of the TC1232 are immediately driven active when the PB input is brought low by an external push button switch or other electronic signal. When connected to a push button switch, the TC1232 provides contact debounce.

The TC1232 is packaged in a space-saving 8-Pin PDIP or SOIC package, a 16-Pin SOIC (wide) package and requires no external components.

**Block Diagram**

**Package Types**

<table>
<thead>
<tr>
<th>8-Pin PDIP</th>
<th>8-Pin SOIC</th>
<th>16-Pin SOIC (Wide)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PB RST</td>
<td>1</td>
<td>NC</td>
</tr>
<tr>
<td>TD</td>
<td>2</td>
<td>VCC</td>
</tr>
<tr>
<td>TOL</td>
<td>3</td>
<td>NC</td>
</tr>
<tr>
<td>GND</td>
<td>4</td>
<td>NC</td>
</tr>
<tr>
<td>TC1232</td>
<td>5</td>
<td>NC</td>
</tr>
<tr>
<td>VCC</td>
<td>6</td>
<td>NC</td>
</tr>
<tr>
<td>RST</td>
<td>7</td>
<td>NC</td>
</tr>
<tr>
<td>RST</td>
<td>8</td>
<td>NC</td>
</tr>
<tr>
<td>VCC</td>
<td>9</td>
<td>NC</td>
</tr>
<tr>
<td>ST</td>
<td>10</td>
<td>NC</td>
</tr>
<tr>
<td>TD</td>
<td>11</td>
<td>NC</td>
</tr>
<tr>
<td>TOL</td>
<td>12</td>
<td>NC</td>
</tr>
<tr>
<td>GND</td>
<td>13</td>
<td>NC</td>
</tr>
</tbody>
</table>

**Device Features**

<table>
<thead>
<tr>
<th>Device</th>
<th>RST pin Type</th>
<th>RST pin Pull-up Resistor</th>
<th>Active Level</th>
<th>Trip Points (Max)</th>
<th>Minimum Reset Active Time (ms)</th>
<th>WDI Input Typical Timeouts (ms)</th>
<th>MR Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC1232</td>
<td>Open-drain</td>
<td>External</td>
<td>Low</td>
<td>High</td>
<td>4.75V or 4.5V</td>
<td>250</td>
<td>150, 600 or 1200</td>
</tr>
</tbody>
</table>
1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Voltage on Any Pin (With Respect to GND)

.................................................................-0.3V to +5.8V

Operating Temperature Range:

C-Version ........................................ 0°C to +70°C
E-Version......................................-40°C to +85°C

Storage Temperature Range: ............-65°C to +150°C

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, \( T_A = T_{\text{MIN}} \) to \( T_{\text{MAX}} \): \( V_{CC} = +4.0\) to 5.5V.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>( V_{CC} )</td>
<td>4.0</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>ST and PB RST Input High Level</td>
<td>( V_{IH} )</td>
<td>2.0</td>
<td>—</td>
<td>( V_{CC} +0.3 )</td>
<td>V</td>
</tr>
<tr>
<td>ST and PB RST Input Low Level</td>
<td>( V_{IL} )</td>
<td>-0.3</td>
<td>—</td>
<td>+0.8</td>
<td>V</td>
</tr>
<tr>
<td>Input Leakage ST, TOL</td>
<td>( I_L )</td>
<td>-1.0</td>
<td>—</td>
<td>+1.0</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Output Current RST</td>
<td>( I_{OH} )</td>
<td>-1.0</td>
<td>-12</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td>Current RST, RST</td>
<td>( I_{OL} )</td>
<td>2.0</td>
<td>10</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td>Operating Current</td>
<td>( I_{CC} )</td>
<td>—</td>
<td>50</td>
<td>200</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( V_{CC} 5% ) Trip Point</td>
<td>( V_{CCTP} )</td>
<td>4.50</td>
<td>4.62</td>
<td>4.74</td>
<td>V</td>
</tr>
<tr>
<td>( V_{CC} 10% ) Trip Point</td>
<td>( V_{CCTP} )</td>
<td>4.25</td>
<td>4.37</td>
<td>4.49</td>
<td>V</td>
</tr>
</tbody>
</table>

Capacitance Electrical Characteristics: Unless otherwise noted, \( T_A = +25^\circ C \). (Note 4)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>—</th>
<th>—</th>
<th>5</th>
<th>pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Capacitance ST, TOL</td>
<td>( C_{IN} )</td>
<td>—</td>
<td>—</td>
<td>5</td>
<td>pF</td>
</tr>
<tr>
<td>Output Capacitance RST, RST</td>
<td>( C_{OUT} )</td>
<td>—</td>
<td>—</td>
<td>7</td>
<td>pF</td>
</tr>
</tbody>
</table>

Note 1: PB RST is internally pulled up to \( V_{CC} \) with an internal impedance of typically 40 k\( \Omega \).

2: Measured with outputs open.

3: All voltages referenced to GND.

4: Ensured by design.
**FIGURE 1-1:** Rise Time, Fall Time and Reset Detected to Reset Active Timing Waveforms.

**AC CHARACTERISTICS**

**Electrical Specifications:** Unless otherwise noted, $T_A = T_{MIN}$ to $T_{MAX}; V_{CC} = +4.0V$ to $5.5V$.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$ Fall Time</td>
<td>$t_F$</td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$ Rise Time</td>
<td>$t_R$</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$ Trip Point Detected to RST High and RST Low</td>
<td>$t_{RPD}$</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>ns</td>
<td>$V_{CC}$ falling</td>
</tr>
<tr>
<td>$V_{CC}$ Trip Point Detected to RST High and RST Open</td>
<td>$t_{RPU}$</td>
<td>250</td>
<td>610</td>
<td>1000</td>
<td>ms</td>
<td>$V_{CC}$ rising (Note 2)</td>
</tr>
</tbody>
</table>

**Note 1:** Ensured by design.
**Note 2:** $t_R = 5$ µs.

AC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $T_A = T_{MIN}$ to $T_{MAX}$; $V_{CC} = +4.0V$ to 5.5V.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>PB RST Pulse Width</td>
<td>$t_{PB}$</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ms</td>
<td><strong>Note 1</strong></td>
</tr>
<tr>
<td>PB RST Falling Edge Low to</td>
<td>$t_{PBD}$</td>
<td>1</td>
<td>4</td>
<td>20</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>Reset Active</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PB RST Rising Edge High to</td>
<td>$t_{RST}$</td>
<td>250</td>
<td>610</td>
<td>1000</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>Reset Inactive</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ST Pulse Width</td>
<td>$t_{ST}$</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>ST Time-out Period</td>
<td>$t_{TD}$</td>
<td>62.5</td>
<td>150</td>
<td>250</td>
<td>ms</td>
<td>TD Pin = 0V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>250</td>
<td>600</td>
<td>1000</td>
<td>ms</td>
<td>TD Pin = Open</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500</td>
<td>1200</td>
<td>2000</td>
<td>ms</td>
<td>TD Pin = $V_{CC}$</td>
</tr>
</tbody>
</table>

**Note 1:** PB RST must be held low for a minimum of 20 ms to ensure a Reset.

The debounced PB RST input ignores input pulses less than 1 ms and is designed to recognize pulses of 20 ms or greater.
2.0 TYPICAL PERFORMANCE CURVES

Performance Graphs are not available.
### 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Pin Type</th>
<th>Buffer/Driver Type</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PB RST</td>
<td>I</td>
<td>ST</td>
<td>Push Button Reset Input. Input for a Manual Reset Switch. This input debounces (ignores) pulses less than 1 ms in duration and is ensured to recognize inputs of 20 ms or greater. L = Manual Reset Switch is Active, Force RST/RST pins Active H = Manual Reset Switch is Inactive. State of RST/RST pins determined by other system conditions.</td>
</tr>
<tr>
<td>2</td>
<td>TD</td>
<td>I</td>
<td>ST</td>
<td>Time Delay Input. The voltage level on this input determines the Watchdog Timer Time-out period. TD = 0V → $t_{TD} = 150$ ms TD = Open → $t_{TD} = 600$ ms TD = VCC → $t_{TD} = 1.2s$</td>
</tr>
<tr>
<td>3</td>
<td>TOL</td>
<td>I</td>
<td>ST</td>
<td>Tolerance Input. TOL = GND, Max Voltage Trip Point ($V_{CTP}$) = 4.75V (5% tolerance) TOL = VCC, Max Voltage Trip Point ($V_{CTP}$) = 4.5V (10% tolerance)</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>—</td>
<td>P</td>
<td>The ground reference for the device.</td>
</tr>
<tr>
<td>5</td>
<td>RST</td>
<td>O</td>
<td>Push Pull</td>
<td>Reset Output (Active-High) Goes active (High) if one of these conditions occurs: 1. If VCC falls below the selected Reset voltage threshold. 2. If PB RST pin is forced low. 3. If ST pin is not strobed within the minimum selected time-out period. (see TD pin) 4. During power-up.</td>
</tr>
<tr>
<td>6</td>
<td>RST</td>
<td>O</td>
<td>Open Drain</td>
<td>Reset Output (Active-Low) Goes active (Low) if one of these conditions occurs: 1. If VCC falls below the selected Reset voltage threshold. 2. If PB RST pin is forced low. 3. If ST pin is not strobed within the minimum selected time-out period. (see TD pin) 4. During power-up.</td>
</tr>
<tr>
<td>7</td>
<td>ST</td>
<td>I</td>
<td>ST</td>
<td>Strobe Input Input for Watchdog Timer. WDT period determined by state of TD pin Falling Edge → Resets Watchdog Timer counter (no time-out)</td>
</tr>
<tr>
<td>8</td>
<td>VCC</td>
<td>—</td>
<td>P</td>
<td>The positive supply (+5V) for the device.</td>
</tr>
<tr>
<td>—</td>
<td>NC</td>
<td>—</td>
<td>—</td>
<td>No internal connection.</td>
</tr>
</tbody>
</table>
4.0 OPERATIONAL DESCRIPTION

4.1 Power Monitor

The TC1232 provides the function of warning the processor of a power failure. When $V_{CC}$ is detected as being below the voltage levels defined by the TOL pin, the TC1232’s comparator outputs the RST and RST signals to a logic level that warns the system of an out-of-tolerance power supply. The RST and RST signals switch at a threshold value of 4.5V if TOL is tied to $V_{CC}$, and at a value of 4.75V if TOL is grounded. The RST and RST signals are held active for a minimum of 250 ms to ensure that the power supply voltage has been stabilized.

*Figure 4-1* shows the $V_{CC}$ fall time.

*Figure 4-2* shows the $V_{CC}$ rise time.

*Figure 4-3* shows the time from when the voltage trip point is detected to the Reset output pin going active.

*Figure 4-4* shows the time from when the voltage trip point is exited to the Reset output pin going inactive.

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**FIGURE 4-1:** Power-Down Slew Rate.

**FIGURE 4-2:** Power-up Slew Rate.

**FIGURE 4-3:** $V_{CC}$ Detect Reset Output Delay (Power-Down).

**FIGURE 4-4:** $V_{CC}$ Detect Reset Output Delay (Power-Up).
4.2 Push Button Reset Input

The debounced manual Reset input (PB RST) manually forces the Reset outputs into their active states. Figure 4-5 shows a block diagram for using the TC1232 with a push button switch.

Once PB RST has been low for a time $t_{PBD}$ (the push button delay time), the Reset outputs go active. The Reset outputs remain in their active states for a minimum of 250 ms after PB RST rises above $V_{IH}$. Figure 4-6 shows a waveform for the push button switch input and the Reset pins output.

A mechanical push button or active logic signal can drive the PB RST input. The debounced input ignores input pulses less than 1 ms and recognizes pulses of 20 ms or greater. No external pull-up resistor is required because the PB RST input has an internal pull-up to $V_{CC}$ of approximately 100 µA.

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**FIGURE 4-5:** Push Button Reset and Watchdog Timer.

**FIGURE 4-6:** Push Button Reset – PB RST Input.

The debounced PB RST input ignores input pulses less than 1 ms and is designed to recognize pulses of 20 ms or greater.
4.3 Watchdog Timer

When the ST input is not stimulated for a preset time period, the Watchdog Timer function forces RST and RST signals to the active state. The preset time period is determined by the TD inputs to be 150 ms with TD connected to ground, 600 ms with TD floating or 1200 ms with TD connected to VCC (typ.). The Watchdog Timer starts timing-out from the set time period as soon as RST and RST are inactive. If a high-to-low transition occurs on the ST input pin prior to time-out, the Watchdog Timer is reset and begins to time-out again. If the Watchdog Timer is allowed to time-out, the RST and RST signals are driven to the active state for 250 ms, minimum (Figure 4-7).

The software routine that strobes ST is critical. The code must be in a section of software that is executed frequently enough so the time between toggles is less than the Watchdog Time-out period. One common technique controls the microprocessor I/O line from two sections of the program. The software might set the I/O line high while operating in the Foreground mode and set it low while in the Background or Interrupt modes. If both modes do not execute correctly, the Watchdog Timer issues Reset pulses.

tTD is the maximum elapsed time between ST high-to-low transitions (ST is activated by falling edges only), which will keep the Watchdog Timer from forcing the Reset outputs active for a time of tRST. tTD is a function of the voltage at the TD pin, as tabulated below:

<table>
<thead>
<tr>
<th>Condition</th>
<th>tTD Min.</th>
<th>tTD Typ.</th>
<th>tTD Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>TD pin = 0V</td>
<td>62.5 ms</td>
<td>150 ms</td>
<td>250 ms</td>
</tr>
<tr>
<td>TD pin = Open</td>
<td>250 ms</td>
<td>600 ms</td>
<td>1000 ms</td>
</tr>
<tr>
<td>TD pin = VCC</td>
<td>500 ms</td>
<td>1200 ms</td>
<td>2000 ms</td>
</tr>
</tbody>
</table>

Figure 4-7 shows a block diagram for using the TC1232 with a PIC® MCU and the Watchdog input.

4.4 Supply Monitor Noise Sensitivity

The TC1232 is optimized for fast response to negative-going changes in VDD. Systems with an inordinate amount of electrical noise on VDD (such as systems using relays) may require a 0.01 μF or 0.1 μF bypass capacitor to reduce detection sensitivity. This capacitor should be installed as close to the TC1232 as possible to keep the capacitor lead length short.
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

Legend:
- XX...X: Customer-specific information
- Y: Year code (last digit of calendar year)
- YY: Year code (last 2 digits of calendar year)
- WW: Week code (week of January 1 is week ‘01’)
- NNN: Alphanumeric traceability code
- *: Pb-free JEDEC® designator for Matte Tin (Sn)

* This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
8-Lead Plastic Dual In-Line (PA) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>INCHES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Top to Seating Plane</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Base to Seating Plane</td>
<td>A1</td>
</tr>
<tr>
<td>Shoulder to Shoulder Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Tip to Seating Plane</td>
<td>L</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Upper Lead Width</td>
<td>b1</td>
</tr>
<tr>
<td>Lower Lead Width</td>
<td>b</td>
</tr>
<tr>
<td>Overall Row Spacing</td>
<td>eB</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing No. C04-057C Sheet 1 of 2
8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff §</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Chamfer (Optional)</td>
<td>h</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint L1</td>
<td></td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
<tr>
<td>Mold Draft Angle Top</td>
<td>a</td>
</tr>
<tr>
<td>Mold Draft Angle Bottom</td>
<td>b</td>
</tr>
</tbody>
</table>

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2
8-Lead Plastic Small Outline (OA) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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**Recommended Land Pattern**

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<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension</td>
<td>Limit</td>
</tr>
<tr>
<td>E</td>
<td>MIN 1.27 BSC</td>
</tr>
<tr>
<td>C</td>
<td>NOM 5.40</td>
</tr>
<tr>
<td>X1</td>
<td>MAX 0.60</td>
</tr>
<tr>
<td>Y1</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

---

Microchip Technology Drawing No. C04-2057A
16-Lead Plastic Small Outline (OE) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
16-Lead Plastic Small Outline (OE) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>§</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Chamfer (Optional)</td>
<td>h</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Lead Angle</td>
<td>Θ</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>ϕ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
<tr>
<td>Mold Draft Angle Top</td>
<td>α</td>
</tr>
<tr>
<td>Mold Draft Angle Bottom</td>
<td>β</td>
</tr>
</tbody>
</table>

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.
16-Lead Plastic Small Outline (OE) – Wide, 7.50 mm Body [SOIC] Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Dimension Limits</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
</tr>
<tr>
<td>Contact Pad Width</td>
<td>X</td>
</tr>
<tr>
<td>Contact Pad Length</td>
<td>Y</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>Gx</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
NOTES:
APPENDIX A: REVISION HISTORY

Revision E (February 2014)
• Removed the “Preliminary” watermark.

Revision D (November 2012)
• Added a note to the package outline drawing.

Revision C (June 2005)
The following is the list of modifications:
1. Since no data is given in Section 2.0 “Typical Performance Curves”, “Preliminary” was added to the bottom of this document.
2. Corrected Operating Voltage in the Electrical Specifications.
3. General Data Sheet Enhancements.
4. Added Revision History Appendix Section.

Revision B (March 2003)
• Not logged

Revision A (March 2002)
• Original Release of this Document.
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>Device</th>
<th>Temperature Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC1232</td>
<td>Microprocessor Monitor</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| Temperature Range | C = 0°C to +70°C | E = -40°C to +85°C |

| Package | PA = Plastic DIP (300 mil Body), 8-lead | OA = Plastic SOIC, (150 mil Body), 8-lead |
| Tape and Reel |
| OE = Plastic SOIC (300 mil Body), 16-lead |
| Tape and Reel |
| OE713 = Plastic SOIC (300 mil Body), 16-lead |

Examples:

a) TC1232COA: 0°C to +70°C, 8L-SOIC
b) TC1232COA713: 0°C to +70°C, 8L-SOIC, Tape and Reel
c) TC1232COE: 0°C to +70°C, 16L-SOIC
d) TC1232COE713: 0°C to +70°C, 16L-SOIC, Tape and Reel
e) TC1232CPA: 0°C to +70°C, 8L-PDIP
f) TC1232EOA: -40°C to +85°C, 8L-SOIC
g) TC1232EOA713: -40°C to +85°C, 8L-SOIC, Tape and Reel
h) TC1232EOE: -40°C to +85°C, 16L-SOIC
i) TC1232EOE713: -40°C to +85°C, 16L-SOIC, Tape and Reel
j) TC1232EPA: -40°C to +85°C, 8L-PDIP
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