AVR1012: XMEGA A Schematic Checklist

Features
- Power Supplies
- Backup battery for XMEGA A3B
- Reset circuit
- Clocks and crystal oscillators
- External bus interface
- JTAG and PDI

1 Introduction
A good hardware design comes from a proper schematic. Since AVR® XMEGA™ A devices have a fair number of pins and functions, the schematic for these devices can be large and quite complex.

This application note describes a common checklist which should be used when starting and reviewing the schematics for a XMEGA A design.
2 Power Supplies

2.1 Power Supply Connections

![Power Supply schematic](image)

**Table 2-1. Power Supply Connections**

<table>
<thead>
<tr>
<th>Signal name</th>
<th>Recommended pin connection</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>1.6 V to 3.6 V Decoupling/filtering capacitors 100 nF(^{(1)})(^{(2)}) and 10 µF(^{(1)}) Decoupling/filtering inductor 10µH(^{(1)})(^{(3)})</td>
<td>Digital supply voltage</td>
</tr>
<tr>
<td>AVCC</td>
<td>1.6 V to 3.6 V Decoupling/filtering capacitors 100 nF(^{(1)})(^{(2)}) and 10 µF(^{(1)}) Ferrite bead(^{(4)}) prevents the VCC noise interfering the AVCC</td>
<td>Analog supply voltage</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
</tbody>
</table>

**Notes**

1. These values are given only as a typical example.
2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group, low ESR caps should be used for better decoupling.
3. Wire wound inductor should be added between the external power and the VCC for power filtering.
4. Ferrite bead has better filtering performance than the common inductor at high frequency. It can be added between VCC and AVCC for preventing digital noise from entering the analog power. The BEAD should provide enough impedance (e.g. 50Ω at 20 MHz and 220 Ω at 100MHz) for separating the digital power to the analog power.
2.2 Battery Backup Module Connections

This section is only for the application which uses the battery backup function of the XMEGA A3B devices, such as the ATxmega256A3B. Upon main power loss the device will detect this and automatically switch the Battery Backup Module to be powered from the VBAT pin.

**Figure 2-2.** Battery Backup Module Schematic

![Battery Backup Module Schematic](image)

**Table 2-2.** Battery Backup Module Connections

<table>
<thead>
<tr>
<th>Signal name</th>
<th>Recommended pin connection</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VBAT</td>
<td>1.8 V to 3.6 V</td>
<td>Battery Backup Module supply voltage</td>
</tr>
<tr>
<td>GND</td>
<td></td>
<td>Ground</td>
</tr>
</tbody>
</table>

**Notes**

To run the Real Time Counter a 32.768 kHz crystal oscillator must be connected between the TOSC1 and TOSC2 pins when running from VBAT.
2.3 External Analog Reference Connections

The following schematic checklist is only necessary if the design is using the external analog reference. If the internal reference is used, the circuit is not necessary.

**Figure 2-3.** External Analog Reference schematic with Two References

![External Analog Reference schematic with Two References](image)

**Figure 2-4.** External Analog Reference schematic with One Reference

![External Analog Reference schematic with One Reference](image)
### Table 2-3. External Analog Reference Connections

<table>
<thead>
<tr>
<th>Signal name</th>
<th>Recommended pin connection</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AREFA</td>
<td>1.0V to AVCC-0.6V for ADC 1.1V to AVCC-0.6V for DAC Decoupling/filtering capacitors 100 nF(^{(1)(2)}) and 4.7 µF(^{(1)})</td>
<td>External reference from AREF pin on PORT A.</td>
</tr>
<tr>
<td>AREFB</td>
<td>1.0V to AVCC-0.6V for ADC 1.1V to AVCC-0.6V for DAC Decoupling/filtering capacitors 100 nF(^{(1)(2)}) and 4.7 µF(^{(1)})</td>
<td>External reference from AREF pin on PORT B.</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td></td>
</tr>
</tbody>
</table>

---

**Notes**

1. These values are given only as a typical example.
2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group.
3 External Reset circuit

The external reset circuit is connected to RESET pin when the external reset function is used. If internal reset is used, the circuit is not necessary. The reset switch also can be removed, if the manual reset is not necessary.

Figure 3-1. External Reset circuit example schematic

Table 3-1. Reset circuit Connections

<table>
<thead>
<tr>
<th>Signal name</th>
<th>Recommended pin connection</th>
<th>Description</th>
</tr>
</thead>
</table>
| RESET       | Reset low level threshold voltage  
  VCC = 2.7 - 3.6V: Below 0.45*VCC  
  VCC = 1.6 - 2.7V: Below 0.42*VCC | Reset pin |

Notes

This pull-up resistor makes sure that reset does not go low unintended. When the PDI programming and debugging is used, the reset line is used as clock. The reset pull-up should be 10k or weaker, or be removed altogether.

Any reset capacitors should be removed if PDI programming and debugging is used. Other external reset sources should be disconnected.
4 Clocks and crystal oscillators

4.1 External clock source

Figure 4-1. External clock source example schematic

<table>
<thead>
<tr>
<th>Signal name</th>
<th>Recommended pin connection</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XTAL1</td>
<td>XTAL1 is used as input for an external clock signal</td>
<td>Input for inverting Oscillator pin 1</td>
</tr>
<tr>
<td>XTAL2</td>
<td>Can be left unconnected or used as GPIO</td>
<td></td>
</tr>
</tbody>
</table>

4.2 Crystal oscillator

Figure 4-2. Crystal oscillator example schematic
### Table 4-2. Crystal oscillator checklist

<table>
<thead>
<tr>
<th>Signal name</th>
<th>Recommended pin connection</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XTAL1</td>
<td>Biasing capacitor 15 pF(^{(1)(2)})</td>
<td>External crystal between 0.4 MHz to 16 MHz</td>
</tr>
<tr>
<td>XTAL2</td>
<td>Biasing capacitor 15 pF(^{(1)(2)})</td>
<td></td>
</tr>
</tbody>
</table>

1. These values are given only as a typical example. Please refer to the crystal datasheet to determine the capacitor value for the crystal used or refer to the application note “AVR1003: Using the XMEGA Clock System”.

**Notes**

2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group.

#### 4.3 External Real Time Oscillator

The Low-frequency Crystal Oscillator is optimized for use with a 32.768 kHz watch crystal. When selecting crystals, load capacitance and crystal's Equivalent Series Resistance, ESR must be taken into consideration. Both values are specified by the crystal vendor.

XMEGA oscillator is optimized for very low power consumption, and thus when selecting crystals, see Table 4-3 for maximum ESR recommendations on 9 pF and 12.5 pF crystals.

The Low-frequency Crystal Oscillator provides an internal load capacitance of typical 8.0 pF. Crystals with recommended 8.0 pF load capacitance can be without external capacitors as shown in Figure 4-3.

### Table 4-3. Maximum ESR Recommendation for 32.768 kHz Watch Crystal

<table>
<thead>
<tr>
<th>Crystal CL (pF)</th>
<th>Max ESR [kΩ](^{(1)})</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0</td>
<td>65</td>
</tr>
<tr>
<td>12.5</td>
<td>30</td>
</tr>
</tbody>
</table>

Note: 1. Maximum ESR is typical value based on characterization

![Figure 4-3. External real time oscillator without biasing capacitor](image-url)
Crystals specifying load capacitance (CL) higher than 8.0 pF, require external capacitors applied as described in Figure 4-4. To find suitable load capacitance for a 32.768 kHz crystal, please consult the crystal datasheet.

**Figure 4-4. External real time oscillator with biasing capacitor**

![Diagram showing external real time oscillator with biasing capacitors](image)

**Table 4-4. External real time oscillator checklist**

<table>
<thead>
<tr>
<th>Signal name</th>
<th>Recommended pin connection</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOSC1</td>
<td>Biasing capacitor 22 pF(1)(2)</td>
<td>Timer Oscillator pin 1</td>
</tr>
<tr>
<td>TOSC2</td>
<td>Biasing capacitor 22 pF(1)(2)</td>
<td>Timer Oscillator pin 2</td>
</tr>
</tbody>
</table>

1. These values are given only as a typical example. Please refer to the crystal datasheet to determine the capacitor value for the crystal used or refer to the application note “AVR1003: Using the XMEGA Clock System”.

Notes
2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group.
5 External bus interface

The External Bus Interface (EBI) is the interface for connecting external peripheral and memory to access it through the data memory space.

The EBI can interface external SRAM, SDRAM, and/or peripherals such as LCD displays and other memory mapped devices.

5.1 SRAM Configuration

5.1.1 8-bit SRAM No Multiplexing

**Figure 5-1. 8-bit SRAM No Multiplexing Connection**

5.1.2 8-bit SRAM Multiplexing Address Byte 0 and 1

**Figure 5-2. 8-bit SRAM Multiplexing address byte 0 and 1 Connection**
5.1.3 8-bit SRAM Multiplexing Address Byte 0 and 2

Figure 5-3. 8-bit SRAM Multiplexing address byte 0 and 2 Connection

5.1.4 8-bit SRAM Multiplexing Address Byte 0, 1 and 2

Figure 5-4. 8-bit SRAM Multiplexing address byte 0, 1 and 2 Connection
5.2 The SRAM Low Pin Count (LPC) configuration

5.2.1 8-bit SRAM Multiplexing Data with Address Byte 0

Figure 5-5. 8-bit SRAM Multiplexing Data with Address Byte 0 Connection

5.2.2 8-bit SRAM Multiplexing Data with Address Byte 0 and 1

Figure 5-6. 8-bit SRAM Multiplexing Data with Address Byte 0 and 1 Connection
5.3 SDRAM Configuration

5.3.1 4-bit SDRAM 3-Port EBI Configuration

Figure 5-7. 4-bit SDRAM 3-Port EBI Configuration
6 JTAG and PDI ports

6.1 JTAG port interface

**Figure 6-1. JTAG port interface example schematic**

![JTAG port interface example schematic](image)

**Table 6-1. JTAG port interface checklist**

<table>
<thead>
<tr>
<th>Signal name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMS</td>
<td>Test mode select, sampled on rising TCK.</td>
</tr>
<tr>
<td>TDO</td>
<td>Test data output, driven on falling TCK.</td>
</tr>
<tr>
<td>TCK</td>
<td>Test clock, fully asynchronous to system clock frequency.</td>
</tr>
<tr>
<td>RESET</td>
<td>Device external reset line.</td>
</tr>
<tr>
<td>TDI</td>
<td>Test data input, sampled on rising TCK.</td>
</tr>
</tbody>
</table>
6.2 PDI port interface

Figure 6-2. PDI port interface example schematic

Table 6-2. PDI port interface checklist

<table>
<thead>
<tr>
<th>Signal name</th>
<th>Recommended pin connection</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDI_CLK</td>
<td>This pull-up resistor makes sure that reset does not go low unintended. When the PDI programming and debugging is used, the reset line is used as clock. The reset pull-up should be 10k or weaker, or be removed altogether. Any reset capacitors should be removed if PDI programming and debugging is used. Other external reset sources should be disconnected.</td>
<td>PDI clock input / Reset pin</td>
</tr>
<tr>
<td>PDI_DATA</td>
<td></td>
<td>PDI_DATA: PDI data input/output</td>
</tr>
</tbody>
</table>
7 Suggested reading

7.1 Device datasheet

The device datasheet contains block diagrams of the peripherals and details about implementing firmware for the device. The datasheet is available on http://www.atmel.com/AVR in the Datasheets section.

7.2 Evaluation kit schematic

The evaluation kit ATAVRXPLAIN contains the full schematic for the board; it can be used as a reference design. The schematic is available on http://www.atmel.com/AVR in the Tools & Software section.
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