Programming Circuits for AT17F Series Configurators with Xilinx® FPGAs

1. Introduction
Atmel's AT17F series Flash Configuration Memory devices use a simple serial-access procedure to configure one or more Xilinx Field Programmable Gate Arrays (FPGAs). AT17F devices easily interface to Xilinx FPGAs in Master Serial configuration mode, which is the most common and simple configuration mode supported by all Xilinx FPGA families.

This application note provides several drawings, showing Drop-In, In-System and Cascade Programming circuits for AT17F series devices with Xilinx FPGAs. Please note that since older Xilinx devices use the PROGRAM and INIT pin names, the PROG_B and PROGRAM pins can be used interchangeably and so are INIT_B and INIT_B. Since the ATF17F family devices operate at 3.3V, the Xilinx FPGA chips must be set-up to use a 3.3V I/O interface with the configurator. The AT17F devices can be programmed using Atmel's ATDH2200E programming system and are supported by several major third-party programmer vendors.

2. Drop-In Programming Circuits for AT17F Series Configurators with Xilinx FPGAs
The Atmel ATDH2200E programming system allows users to easily program AT17F Configuration Memory devices with FPGA configuration files prior to mounting them on the target system. Once programmed, the configuration device can be placed on the target board to configure the FPGAs.

Figure 2-1 below shows the use of the ATDH2200.
In addition to the ATDH2200E programming system, many third-party programmers support the AT17F Flash memory devices. A list of third-party programmer vendors supporting Atmel products can be found at: http://www.atmel.com/products/Config/thirdparty.asp. Please contact the programmer vendors for support availability.

Figure 2-2 below shows all the required connections between the AT17F configurator and a Xilinx FPGA device when in-system programming is not required. This circuit requires that the AT17F device be programmed either by the ATDH2000E programming system or a third-party programmer prior to mounting or using with target FPGA.

Figure 2-2. Drop-In circuit showing an AT17F Series Device with an Xilinx FPGA

Notes:
1. Use of the READY pin is optional.
2. Refer to the FPGA-specific datasheet.
3. VCC = 3.3V
3. In-System Programming Setup for AT17F Series Configurators with Xilinx FPGAs

To perform In-System Programming (ISP), the ATDH2225 programming dongle is required in order to provide communication between the PC and the configurator targeted for programming. See Figure 3-1.

Figure 3-1. ATDH2225 In-System Programming Setup
4. **In-System Programming Circuits for AT17F Series Configurators with Xilinx FPGAs**

Figure 4-1 below shows all the required connections between the AT17F Configurator, ISP circuits, and a single Xilinx FPGA device.

**Figure 4-1.** In-System Programming Circuit of AT17F Series Devices with a Xilinx FPGA

Notes:
1. The A2 bit-level setting in the Configurator Programming System (CPS) software should match the A2 pin setting in the hardware. By default, it must be set to high for ISP access to Series Device 1 and set to low for Series Device 2.
2. Use of the READY pin is optional.
3. Refer to the device-specific datasheet.
4. IN4001 or equivalent.
5. VCC = 3.3V.
Figure 4-2. In-System-Programming of a Single AT17F Configurator and Cascaded Xilinx FPGA devices

Notes: 1. The A2 bit-level setting in the Configurator Programming System (CPS) software should match the A2 pin setting in the hardware. By default, it must be set to high for ISP access to Series Device 1 and set to low for Series Device 2.

2. Use of the READY pin is optional.

3. Refer to the device-specific datasheet.

4. IN4001 or equivalent.

5. VCC = 3.3V

5. Cascaded Programming Circuits using AT17F Series Configurators with Xilinx FPGAs

AT17F devices provide a feature that allows a large FPGA configuration file that will not fit into one configurator device to be stored and downloaded from two AT17F devices in serial cascade fashion.

When performing in-system programming with cascaded configurators, special attention must be given to the CEO/A2 I/O pins of the two configurator devices. While in configurator programming mode, SEREN = 0, the CEO/A2 pins act as address line input A2. Consequently, in order for the ISP software to individually communicate with each device, each device must have a different address setting. In Figure 5-1, Device 1 uses its internal pull-up resistor to provide the
logic “1” setting to its A2 pin, while the A2 pin of Device 2 is connected to ground for logic “0”. Hence, each configurator responds only to ISP software messages bearing its unique address.

**Figure 5-1.** In-System Programming of Cascaded AT17F Series Devices with a Single Xilinx FPGA

Notes:  
1. The A2 bit-level setting in the Configurator Programming System (CPS) software should match the A2 pin setting in the hardware. By default, it must be set to high for ISP access to Series Device 1 and set to low for Series Device 2.  
2. Use of the READY pin is optional.  
3. Refer to the device-specific datasheet.  
4. IN4001 or equivalent.  
5. VCC = 3.3V
Figure 5-2. In-System Programming of Cascaded AT17F Series Devices with Cascaded Xilinx FPGAs

Notes:
1. The A2 bit-level setting in the Configurator Programming System (CPS) software should match the A2 pin setting in the hardware. By default, it must be set to high for ISP access to Series Device 1 and set to low for Series Device 2.
2. Use of the READY pin is optional.
3. Refer to the device-specific datasheet.
4. IN4001 or equivalent.
5. VCC = 3.3V
6. Using the Multiple Configuration Page Capabilities of AT17F Configurators

AT17F configurators provide a memory page feature that allows users to store four configuration files at four different page locations and instantly configure their FPGA device with the functionality given by each bitstream.

As an example of its usefulness, designs requiring a 1M-bit configuration device may benefit from using the AT17F040A since up to four different configurations can be stored and accessed as needed. This will simplify field upgrades and parts inventory by reducing the need for four 1M-bit devices holding 4 different design implementations, to just one 4M-bit device with four different configurations.

When the PAGE_EN\(^{(1)}\) input of the AT17F device is set to logic “1”, the storage space of the AT17F device is split into four equal size partitions. Upon initiating a FPGA configuration sequence, the configuration bitstream residing at the page given by the Pagesel [1:0] bits, will be downloaded into the FPGA.

CPS software version 8.05 or later can be used to select and program the individual bitstreams at the page locations the user desires. Alternatively, designers who choose to write their own ISP code should note the address page boundaries as shown in Table 6-1.

Additional details on the use of the memory page feature and exact address boundary locations\(^{(2)}\) can be found in the corresponding AT17F device datasheet.

<table>
<thead>
<tr>
<th>PAGE_EN</th>
<th>PAGESEL [1:0]</th>
<th>PAGE</th>
<th>AT17F040 ADDR RANGE</th>
<th>AT17F080 ADDR RANGE</th>
<th>AT17F16 ADDR RANGE</th>
<th>AT17F32 ADDR RANGE</th>
</tr>
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<tr>
<td>0</td>
<td>XX</td>
<td>1-4</td>
<td>00000-3FFFF</td>
<td>00000-7FFFF</td>
<td>00000-FFFFF</td>
<td>00000-1FFFFF</td>
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<tr>
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<td>1</td>
<td>00000-0FFFF</td>
<td>00000-1FFFF</td>
<td>00000-3FFFF</td>
<td>00000-07FFFF</td>
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<td>01</td>
<td>2</td>
<td>10000-1FFFF</td>
<td>20000-3FFFF</td>
<td>40000-7FFFF</td>
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<td>80000-BFFFF</td>
<td>10000-17FFFF</td>
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<td>4</td>
<td>30000-3FFFF</td>
<td>60000-7FFFF</td>
<td>C0000-FFFFF</td>
<td>180000-1FFFFF</td>
</tr>
</tbody>
</table>

Figures 6-1 and 6-2 show circuit drawings, implementing the page enable and page select features of AT17F devices. Use of the page feature is aided by control logic such as a microcontroller, PLD or DIP switch for the purpose of controlling the page selection pins.

Notes: 1. The page enable feature is not available on the low 8-lead LAP package
2. The address ranges reflect that data is stored 16-bits per address.
Notes:
1. The A2 bit-level setting in the Configurator Programming System (CPS) software should match the A2 pin setting in the hardware. By default, it must be set to high for ISP access to Series Device 1 and set to low for Series Device 2.
2. Use of the READY pin is optional.
3. Refer to the device-specific datasheet.
4. IN4001 or equivalent.
5. VCC = 3.3V
Figure 6-2. Manually-Controlled Paging Selection

Notes:
1. The A2 bit-level setting in the Configurator Programming System (CPS) software should match the A2 pin setting in the hardware. By default, it must be set to high for ISP access to Series Device 1 and set to low for Series Device 2.
2. Use of the READY pin is optional.
3. Refer to the device-specific datasheet.
4. IN4001 or equivalent.
5. VCC = 3.3V