In-System Programming Programming Circuits for AT17 Series Configurators with Atmel and Xilinx® FPGAs

Atmel AT17\(^{(1)}\) series configurators use a simple serial-access procedure to configure one or more Field Programmable Gate Arrays (FPGAs) or Field Programmable System Level Integrated Circuits (FPSLIC™) devices.

This application note provides the circuits used to program Atmel and Xilinx FPGAs with an AT17 series configurator. To perform In-System Programming (ISP), a cable is required in order to provide communication between the programmer and the configurator, see Figure 1 and Figure 2.

Figure 1. ATDH2200E In-System Programming

1. AT17=AT17F/LVXXX
   AT17A=AT17F/LVXXXA

Note: AT17N and AT17A series configurators are not recommended for the ISP circuits in this document.
Figure 2. ATDH2225 In-System Programming

Figure 3. In-System Programming of AT17LVXXX Series Devices for AT6K Applications

Note: 1. Reset polarity level of the configurator must be set to active High (RESET/OE) by a programmer.
2. AT17F series configurator’s reset polarity level is permanently set to Low, so it cannot be used in this circuit.
Figure 4. In-System Programming of AT17 Series Devices for AT40K FPGA and AT94K FPSLIC Applications

Note:  
1. Reset polarity level of the configurator must be set to active Low (RESET/OE) by a programmer if an AT17LVXXX series configurator is used.
2. Use of the READY pin is optional.
3. This circuit does not apply to AT17LV020 devices unless a 4.7 kΩ external pull-up resistor is connected to the A2 pin and the A2 bit level is set to active High in the programming software.
4. M1 is not available on AT94K devices.
5. The A2 bit level must set to High in the ISP programming software if an AT17FXXX series configurator is used. Otherwise, the A2 bit level must be set to Low.
6. ATFSXXX series configurators can be used in this circuit for AT94K 0FPSLIC applications.
Figure 5. In-System Programming of AT17 Series Devices for Xilinx/Lattice® FPGA Applications (4)

Notes:
1. Reset polarity level of the configurator must be set to active Low (RESET/OE) by an ISP programmer if an AT17LVXXX series configurator is used.
2. Use of the READY pin is optional.
3. A 330Ω external pull-up resistor on the DONE pin is required for Virtex® and Virtex-II FPGAs. Xilinx FPGAs can use LDC instead of the DONE pin.
4. This circuit does not apply to AT17LV020 devices unless a 4.7 kΩ external pull-up resistor is connected to the A2 pin and the A2 bit level is set to active High in the programming software.
5. Xilinx FPGAs can use RESET instead of the PROGRAM pin. ORCA® FPGAs can use PRGM instead of the PROGRAM pin.
6. The A2 bit level must be set to High in the ISP programming software if an AT17FXXX series configurator is used. Otherwise, the A2 bit level in the ISP programming software must be set to Low.
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