VSC8211

PCB Design and Layout Guide
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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first release of this document. It was published in September 2004.
2 Introduction

The purpose of this application note is to provide specific design and layout guidelines to printed circuit board and software designers utilizing the VSC8211 physical layer device.
3 Power Supply Organization and Decoupling

The VSC8211 requires a 3.3 V and a 1.2 V power supply source for basic operation.

3.1 PCB Power Plane Organization

It is recommended that the PCB power plane(s) in a system be divided into separate regions, as listed in the following table.

Table 1 • Power Supply Plane Regions

<table>
<thead>
<tr>
<th>Plane Region</th>
<th>Description</th>
<th>Associated VSC8221 Power Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDIO (MAC, MICRO, CTRL)</td>
<td>Input/output buffer supply (3.3 V–2.5 V)</td>
<td>VDDIO (MAC, MICRO, CTRL)</td>
</tr>
<tr>
<td>VDD33A</td>
<td>Filtered analog 3.3 V supply</td>
<td>VDD33A</td>
</tr>
<tr>
<td>VDD12A</td>
<td>Filtered analog 1.2 V supply</td>
<td>VDD12A</td>
</tr>
<tr>
<td>VDD12</td>
<td>High-current digital core 1.2 V supply</td>
<td>VDD12</td>
</tr>
</tbody>
</table>

1. This supply is used by three different I/O functions (MAC, MICRO, and CTRL), each of which can operate at a different voltage. The V+IO region should be further divided depending on how many different operating voltages are used.

3.2 Power Supply Filtering and Decoupling

For best performance, each power supply region should contain capacitors for both bulk decoupling and for high-frequency local decoupling. This is summarized in the following table.

Table 2 • Bulk Decoupling for the 100 TF-BGA

<table>
<thead>
<tr>
<th>Power Supply Plane Region</th>
<th>Bulk Decoupling Required</th>
<th>Local Decoupling Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDIO</td>
<td>10 uF</td>
<td>5 0.1 uF capacitor</td>
</tr>
<tr>
<td>VDD33A</td>
<td>10 uF</td>
<td>3 0.1 uF capacitors</td>
</tr>
<tr>
<td>VDD12A</td>
<td>1 uF</td>
<td>1 0.1 uF capacitor</td>
</tr>
<tr>
<td>VDD12</td>
<td>10 uF</td>
<td>6 0.1 uF capacitors</td>
</tr>
</tbody>
</table>

1. These numbers are based on typical performance of pre-production silicon at 25 °C operating in full-duplex 1000BASE-T mode.

Bulk decoupling capacitors should be sintered solid tantalum and can be placed at any convenient position on the board. Local decoupling capacitors should be placed as close to the VSC8211 as possible. The best location for local decoupling capacitors is on the bottom of the board, directly under the VSC8211. This is shown in Figure 2: Decoupling Schematic.
In addition, a ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.

The beads should be chosen to have the following characteristics:

- Current rating of at least 150% of the maximum current of the power supply
- Impedance of 80 Ω to 100 Ω at 100 MHz

Recommended beads are:

- Panasonic EXCELSA39 or similar
- Steward HI1206N101R-00 or similar

Since all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. For this reason, it is recommended that system designers provide an option to replace the ferrite beads with 0 Ω resistors, once thorough evaluation of system performance is completed.
3.3 PCB Chassis Ground Region

To isolate the board from ESD events and to provide a common-mode noise ground path, a separate chassis ground region should be allocated. This should provide an electrical connection to the external chassis and the shield ground for RJ-45 connectors. In addition, the “Bob Smith” termination impedance should be connected between this ground and the cable-side center-taps of the magnetics modules. This is shown in the following figure.

Figure 3 • Ground Plane Layout
4  PHY Magnetics Connections

The magnetics shown in the following figure are available in different configurations. Each of the configurations has its advantages and disadvantages. For details on magnetics, see the Magnetics and EMI Control application note.

Figure 4 • PHY and Magnetics Circuit
5 Design for Signal Integrity

With the high-speed nature of the VSC8211 data signals, careful attention must be paid to PCB layout and design to maintain adequate signal integrity. To simplify board design, the VSC8211 has been designed with SimpliPINTM outputs on certain pins, which automatically calibrate their output resistance to 50 Ω, eliminating the need for series termination resistors.

5.1 Parallel MAC Transmit and Receive Interface Pins

These pins have been designed with extremely fast rise and fall times to allow for 125 MHz operation. To adequately accommodate these signals on a PCB, it is recommended that the traces be designed as either microstrip or stripline transmission lines with a characteristic impedance of 50 Ω. It is also important that an unbroken ground plane exist above and/or below these signals.

For the VSC8211 MAC receive interface, each pin is self-calibrating to an output resistance of 50 Ω. Thus, external series termination resistors are unnecessary as long as the characteristic impedance of the PCB traces are also 50 Ω (see the following figure MAC Tx/Rx Series Termination).

For the VSC8211 MAC transmit interface, careful attention must be paid to the output resistance of the pins on the MAC or switch device. If that resistance is less than 50 Ω, additional series termination resistors are required. These resistors should be placed as close as possible to the MAC or switch device.

Figure 5 • MAC Tx/Rx Series Termination
6 RGMII Design Considerations

Proper operation of the RGMII bus requires careful control of the timing relationship between clock and data signals.

The RGMII specification requires that the signal clock be delayed by 1/2 bit time (2 ns) at the receiving end of the data path. This clock delay can be added externally (extended clock trace length), or by using internal delays built into the VSC8211.

6.1 Clock Delays

When considering the interface between MAC and PHY, the relationship between transmitter and receiver is often confused. Please refer to the following diagram.

Figure 6 • Typical RGMII Circuit

Note: For all traces beginning with "TX", the PHY is the receiver; while for all traces beginning with "RX", the MAC is the receiver.

In order for the input registers (receivers) of the MAC and PHY to see a stable data signal during both rising and falling clock edges, several methods exist for the introduction of a clock delay:

1. A delay of 1.5 ns to 2 ns can be added to the TX_CLK and RX_CLK signals by routing them through a long PCB "trombone" trace delay.
2. An output clock skew can be integrated into the clock signal output of each transmitter. Specifically, this calls for the MAC to provide a clock skew on the TX_CLK, while the PHY must provide a clock skew on the RX_CLK. Devices supporting this type of configuration are defined as "RGMII-ID" in the RGMII standard.

3. A clock skew can be integrated into the PHY for both RX_CLK and TX_CLK. Strictly speaking, this method is not compliant with the RGMII standard. However, this allows a MAC that does not support the RGMII-ID configuration to be connected to a PHY without the use of PCB trace delays.
6.2 Using Integrated Clock Skew to Implement RGMII with VSC8211

The VSC8211 contains an internal delay element connected to the TX_CLK and RX_CLK pin, which can provide the necessary clock delays for the RGMII interface without the need for PCB trace delays. These elements are enabled by proper configuration of the CMODE pins, or by writing to MII register 23, bits 11:10, and 9:8. By writing to MII register 23, the delay for TX_CLK and RX_CLK can be individually set for delays of 0, 1.5, 2.0, or 2.5 ns.

When using internal clock skew control, the TX and RX traces should be independently matched in length to within one inch (approximately 25 mm). It is not necessary to match the lengths of the TX traces and the RX traces on each individual port. TX traces can be a different length from RX traces.
7 High-Speed Serial Interfaces

7.1 Serial MAC/Media Traces (RDP/RDN, TDP/TDN, SCLKP/SCLKN, SDIP/SDIN, SDOP/SDON)

Best performance will result when SerDes traces are placed using the following design rules:

- Traces should be routed as 50 Ω (100 Ω differential) or 75 Ω (150 Ω differential) controlled impedance transmission lines (microstrip, or stripline).
- Traces should be of equal length on each differential pair to minimize EMI and Jitter.
- Traces should be run adjacent to a single ground plane to match impedance and minimize noise. If traces are placed between two ground planes to improve shielding note that this can cause problems if there is an impedance imbalance (noise) between the two planes.
- Traces should avoid vias and layer changes.

The following figure shows a typical MAC PHY serial interface.

![Figure 10 • Typical MAC PHY Serial Interface](image)

In general, these connections require a series capacitor to prevent common mode voltages from interfering with transmit and receive operation. If the common mode input and output specifications for the MAC and VSC8211 are compatible (see data sheet section Ser-Des Specifications), then the series capacitors can be removed.

For example, the VSC8211 Vicm min and max values would need to be equal to or wider than the matching Vocm specification for the MAC. Conversely, the VSC8211 Vocm min/max range must fit inside the MAC Vicm range.

According to the SFP, Multi Source Agreement (MSA) specification, the previously shown AC-coupling capacitors must be on the SFP PCB.

7.2 Twisted-Pair Interface

These pins are the interface to the external CAT-5 cable and are organized in four differential pairs for each port. These are labeled "TXVPx" and "TXVNX", where ‘x’ is the particular pair within a single CAT5 cable. When routing these pairs on a PCB, the characteristics must match one of the following:
• Route each trace single-ended with a characteristic impedance of 50 Ω referenced to ground.
  OR
• Route each pair of positive and negative traces differentially, with a 100 Ω differential characteristic impedance.

The VSC8211 PHY has internal termination for the twisted pair interface and does not need any external resistor on the traces connecting to the “TXVPx” and “TXVNx” pins.
8 Other Design Considerations

8.1 Design for Signal Integrity
With the high-speed nature of the VSC8211 data signals, careful attention must be paid to PCB layout and design to maintain adequate signal integrity. To simplify board design, the VSC8211 has been designed with SimpliPIN™ outputs on certain pins, which automatically calibrate their output resistance to 50 Ω, eliminating the need for series termination resistors.

8.2 125 MHz and 4 MHz Clock Outputs
By default, the VSC8211 provides low-jitter, 125 MHz and 4 MHz output clocks for driving other devices in a system. The output resistance of these pins are self-calibrating to 50 Ω, and should be routed on the PCB using a microstrip or stripline transmission line trace.

For each addition VSC8211 device in the chain, set PLLMODE to 1 by tying the EECLK/PLLMODE pin to VDDIOMICRO. This will enable each device to function using the 125 MHz clock output of the previous device(s) in the chain.

Note that the clock outputs can be disabled by writing a ‘0’ to MII register 18 and 17E, bit 0. Also, the default 4 MHz clock output of the CLKOUTMICRO pin can be changed to a 125 MHz clock by setting extended MII Register 20E.8 to ‘1’ or by using the hardware configuration bit CMODE6 bit 1.

8.3 An Important Note Regarding LED Outputs and JTAG TDO Pins
The LED outputs and JTAG TDO pins for the VSC8211 were designed with the same output driver technology as the high-speed clock outputs above, which provide an extremely fast rise and fall time with integrated series termination resistors (see the following figure, Miscellaneous Series Termination). Even though the overall clock speed is much slower, these signals must be treated as high-speed signals to avoid reflections caused by the extremely fast transitions. This issue can be addressed in one of two ways:

- Route each signal using a microstrip or stripline transmission line trace with a characteristic impedance of 50 Ω.
- Ensure that the lengths of the PCB traces are less than 0.75 inches (approximately 19 mm).

If the LED outputs are only driving LED devices and are not used with other digital devices, it is not necessary to route these traces as transmission lines, nor is it necessary to terminate them.

Figure 11 • Miscellaneous Series Termination
8.3.1 RXLOS Behavior for SFP Application

The VSC8211 is set in SFP mode when hardware configuration bit CMODE1.0 is set to ‘0’. In this mode the RXLOS/SIGDET pin drives the RXLOS output which is meant to be used as the source of the RXLOS signal pin of a standard 20 pin SFP connector as defined in the MSA specification. This RXLOS signal is an active high signal that is asserted whenever the CATS Media link is dropped. The precise behavior requirements of the RXLOS signal may be system dependent and therefore the VSC8211 provides programmability to the RXLOS behavior through MII Registers 30.1:0. This is described in the following table.

Table 3 • RXLOS Behavior

<table>
<thead>
<tr>
<th>MII Register 30.0:1 Setting</th>
<th>Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>RXLOS is always driven low.</td>
</tr>
<tr>
<td>01</td>
<td>RXLOS pulses (low-high-low) on a link down event for a period of 20 ms.</td>
</tr>
<tr>
<td>10</td>
<td>RXLOS pulses (low-high-low) on a link down event for a period of 200 ms.</td>
</tr>
<tr>
<td>11</td>
<td>RXLOS pulses (low-high-low) on a link down event for a period of 500 ms.</td>
</tr>
</tbody>
</table>
9 RJ-45 Connectors and Magnetic Modules

9.1 RJ-45 Connector Recommendations
For system designers, several options exist for the choice of RJ-45 connectors. These are summarized as follows.

- Two tab orientations are available: up or down.
- For multi-port connectors, two orientations are available: stacked and single-row.
- LEDs can also be integrated into the connectors.

Figure 12 • RJ-45 Example Configurations

Most manufacturers can mix or match any combination of features. For example, LEDs can be added to any connector, or single-row multi-port configurations can be tab-up or tab-down. The exception is the stacked connector, which contains both tab-up and tab-down orientations.

An additional consideration is the pinout of tab-up versus tab-down connectors. The pinouts of these two orientations are reversed. While the VSC8211 will work equally well using either orientation, signal routing will be simpler with the tab-down pinout. For the stacked variety, both orientations exist in one package, so both pinouts typically exist in one package. Some manufacturers have provided an option for “vertical” pin orientation, which allows for ease in PCB routing.

9.2 CAT-5 vs. CAT-3 Connectors
When utilizing 1000BASE-T or 100BASE-TX, it is important that “CAT-5” RJ-45 connectors be used as opposed to “CAT-3”. This refers to the amount of crosstalk between the wire pairs within the connector.

In addition to the electrical characteristics, some manufacturers have two options for the connector pinout. These are typically labelled as “standard” and “CAT-5”. This is not to be confused with the electrical specification for the connector. Thus, two versions of a CAT-5 RJ-45 connector are available: one with a “standard” pinout and one with a “CAT-5” pinout, shown as follows.
Figure 13 • Standard vs. CAT-5 Pinout
## Reset Sequence

The following events occur in order when the VSC8211 is brought out of reset. This is triggered by a low-to-high transition of the RESET pin.

1. Values for PLLMODE, EEDAT, and CMODE pins are latched asynchronously immediately out of reset.
2. If the EEPROM is not present then on the first rising edge of REFCLK after reset, the Serial Management Interface (SMI) becomes active. Otherwise the SMI is disabled until the PHY configures itself using the initialization script loaded in the configuration EEPROM.
3. Approximately 11 milliseconds after reset, the reference voltages and currents stabilize.
4. Once a stable reference is available, the PLL requires 50 microseconds to lock.
5. With a locked PLL, the analog-to-digital converter is calibrated, which requires 2.05 milliseconds.
6. Once the ADC is calibrated, the clock outputs are activated.

**Important note:** Since the values of PLLMODE and CMODE pins are latched on the rising edge of the RESET pin, it is required that the power supply is stable before the rising edge of RESET. Therefore, if RESET is tied directly to a logic high on the PCB, the VSC8211 will behave unpredictably. If a design requires the RESET pin to remain high at all times, a small RC circuit can be added to this line to provide the necessary delay.

Also, note that the SMI is enabled prior to the other blocks within the device. For applications which utilize this interface, this sequence provides a short period of time in which to configure the VSC8211 before the device is fully operational. This is useful for setting up MII registers that control items such as LEDs, which must be setup prior to device operation.

Please refer to datasheet section PHY Startup and Initialization for more details on the reset sequence.
11 Thermal Performance

Though the low power consumption of the VSC8211 eliminates the need for external heatsinks or fans in most designs, certain guidelines must be followed for adequate heat dissipation. For proper operation of the VSC8211, a silicon junction temperature ($T_j$) equal to or below 125 °C must be maintained for commercial temperature ranges. Within the constraints of the commercial temperature range, the limits for junction-to-ambient thermal resistance are as follows:

**Figure 14 • Limits for Junction-to-Ambient Thermal Resistance**

$$
\Theta_{ja}^{(Commercial)} \leq \frac{T_j - T_a}{P_d} \leq \frac{125 \degree C - 70 \degree C}{1.1 \text{W}} \leq 50.0 \degree C / \text{W}
$$

where $\Theta_{ja} =$ Junction-to-ambient thermal resistance, $T_j =$ Junction temperature, $T_a =$ Ambient temperature, and $P_d =$ Power dissipation.

For the purpose of maintaining adequate junction temperature, 19 balls in the center of the BGA package have been allocated for thermal relief. Each of these is connected electrically to VSS, allowing the use of PCB ground planes to transfer heat away from the BGA package. When utilized properly, these thermal balls can provide the necessary junction-to-ambient thermal resistance ($\Theta_{ja}$).

For more information, please refer to the Thermal Applications Data section of the VSC8211 datasheet.

For proper cooling, a PCB via must be placed between the thermal BGA ball pads in a checkerboard pattern (see figure Thermal Via Layout, as follows). Each of these thermal vias should then be routed to the BGA ball pads near it with a wide trace or solid copper fill to increase the conductive area on the surface of the PCB.

In order to dissipate heat below the BGA package, the PCB thermal vias must connect to a solid ground plane within the board. It is recommended that the ground plane have a minimum thickness of two ounces (see figure Thermal Ground Plane Connections, as follows).

**Figure 15 • Thermal Via Layout**
Figure 16 • Thermal Ground Plane Connections

When connecting these thermal vias to ground planes, it is advisable not to use thermal-relief connection traces, as these are designed to prevent the flow of heat through the PCB. Instead, the thermal vias should have a solid connection to the traces and planes on each layer (see figure PCB Vias, as follows).

Figure 17 • PCB Vias
12 Voltage Reference Pins Circuit

For proper operation, the VSC8211 must generate an on-chip band gap reference voltage at the REFFILT pin. For this, the following components are required for each VSC8211 in the system:

- 2.0 kΩ reference resistor, 1% tolerance, 1/16 watt.
- Two 0.1 uF capacitors, with 10% tolerance or better. NPO, X7R, or X5R ceramic materials are all acceptable.

12.1 PCB Layout of Voltage Reference Pins Circuit

For best performance, special considerations for the ground connection of the voltage reference circuit are necessary to prevent bus drops that would cause inaccuracy in the reference voltage. This applies to the following elements:

- Ground connection of the 2.0 kΩ reference resistor
- Ground connection of the 0.1 uF reference capacitor

These ground connections should each be connected to a shared PCB signal trace, rather than being connected individually to a common ground plane. This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitors and resistor should be placed as close as possible to the VSC8211, as shown in the following figure.

Figure 18 • Voltage Reference Schematic
PCB Design and Layout Guide

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