TB3146

Analog-to-Digital Converter with Computation Technical Brief

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INTRODUCTION

The Analog-to-Digital Converter (ADC), with computation module (ADC^2), in Microchip's 8-bit microcontroller, has built-in computational features that provide post-processing functions such as oversampling, averaging and low-pass filtering.

This technical brief provides a discussion on the ADC^2 features, methods of configuration, and modes of operation.

ADC^2 MODULE BLOCK DIAGRAM

The block diagram shown in Figure 1 displays the process of converting the analog input signals into a digital form. The diagram is sub-divided into positive channel selection source, the positive and negative voltage reference sources, the conversion clock source, the conversion result and the auto-conversion trigger source. The analog input channel sources are multiplexed into a single sample and hold circuit. The output of the sample and hold circuit is connected to the converter, which generates a binary representation of the analog input. When the ADC is operating with computational features, the conversion result will be passed onto the computational feature block diagram (see Figure 2) for post-processing. The post-processing result is then evaluated using error calculation and threshold comparison.

FIGURE 1: ADC BLOCK DIAGRAM

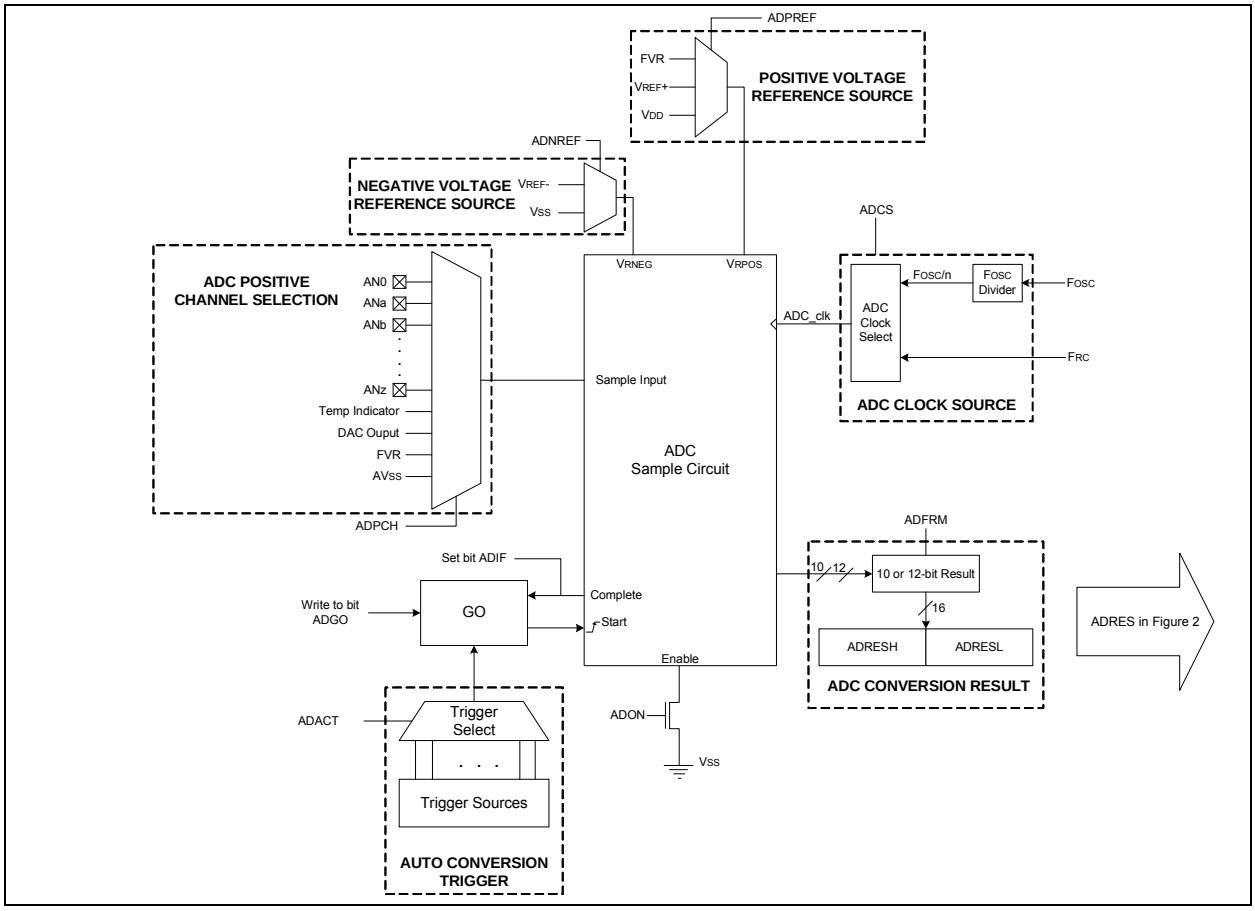

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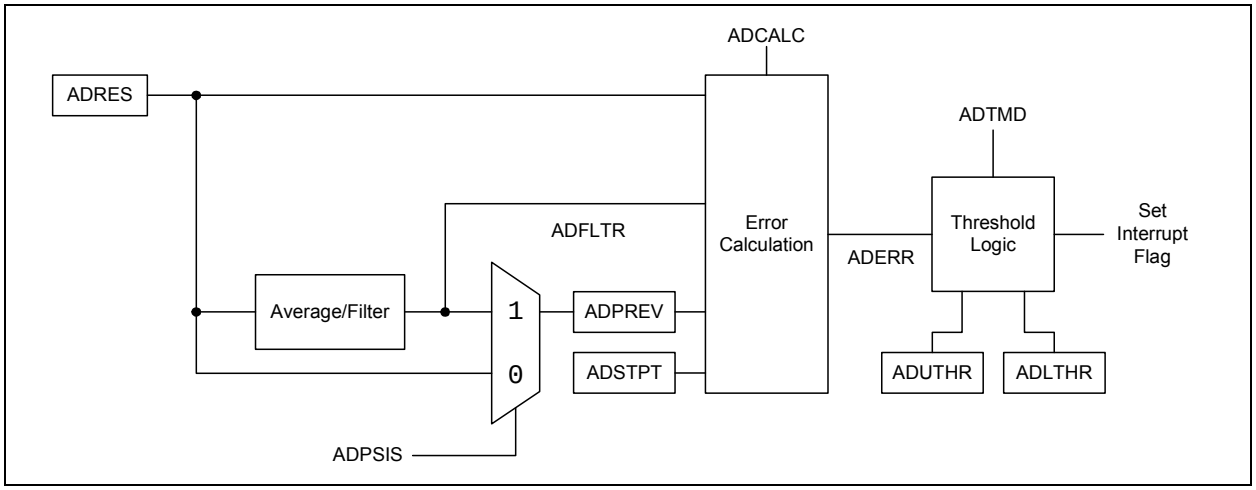
FIGURE 2: ADC COMPUTATIONAL FEATURE BLOCK DIAGRAM



Channel Selection Source

The ADC Positive Channel Selection register (ADPCH) determines which channel is connected to the sample and hold circuit. Channel selection sources are not limited to external analog input sources but can be an output of a peripheral or an internal reference voltage. Refer to the product data sheet for the list of channel selections available.

Note:	Only one channel can be selected and converted at a time in a single ADC module.

Voltage Reference Source

The voltage reference sets the input voltage range of the ADC. It can be an external source from the VREF+/- pins, VDD, FVR, or VSS. The positive and negative voltage references are selected using the ADC Positive Voltage Reference Selection bits (ADPREF) and the ADC Negative Voltage Reference Selection bits (ADNREF) of the ADC Reference Selection register (ADREF).

Note:	Consult the device data sheet since some devices do not have ADNREF bits.

Equation 1 shows how to calculate the ADC result using VREF+/- pins. It is important to note that VREF+ must always be greater than VREF-, and VREF- must have a value greater than or equal to zero.

EQUATION 1: ADC RESULT

$$ADRES = \frac{2^n - 1}{V_{REF+} - V_{REF-}} \times (V_{IN} - V_{REF-})$$

Where: n = 10 for 10-bit ADC
= 12 for 12-bit ADC

Conversion Clock Source

The conversion clock has multiple sources, either from the main oscillator, which is divided by multiples of two (i.e., 2, 4, 6,...128), or from the dedicated internal RC clock. The conversion clock source is controlled by the ADC Clock Selection bit (ADCS) of the ADC Control Register 0 (ADCON0) and the ADC Conversion Clock Select bits (ADCCS) of the ADC Clock Selection register (ADCLK). When ADCS is clear, the clock is supplied by FOSC and is divided according to the value of ADCCS (see Equation 2).

The desired ADC clock should meet the ADC conversion timing specifications provided by the data sheet, (i.e., PIC16F18855 device data sheet (DS40001802), **Table 23-1: ADC Clock Period (TAD) Vs. Device Operating Frequencies)**. When the ADCS is set, the clock is supplied by the dedicated RC oscillator, FRC.

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EQUATION 2: DETERMINING THE VALUE OF ADCCS

$$CLK_{conversion} = \frac{F_{OSC}}{2(ADCCS + 1)}$$

Example:

The system's oscillating frequency runs at 4 MHz. If the conversion clock needs to run at 400 kHz, find the value of the ADC Conversion Clock Select bits ADCCS.

$$CLK_{conversion} = \frac{F_{OSC}}{2(ADCCS + 1)}$$

$$400000 = \frac{4000000}{2(ADCCS + 1)}$$

$$2(ADCCS + 1) = \frac{4000000}{400000}$$

$$2(ADCCS + 1) = 10$$

$$(ADCCS + 1) = 5$$

$$ADCCS = 4$$

$$\mathbf{ADCCS = 0b000100}$$

ADC Acquisition Requirements

Acquisition time is the time required for the ADC to capture the input voltage during sampling. For the ADC to meet its specified accuracy, the sample and hold capacitor (C_{HOLD}) must be given sufficient time to settle to the input channel voltage level before the actual conversion is initiated. If sufficient time is not allowed for acquisition, the conversion will be inaccurate. There are many factors that affect the acquisition time. These are the following: C_{HOLD}, interconnect impedance (R_{IC}), output impedance of the analog source (R_S), and the switch impedance (R_{SS}). The maximum recommended impedance for analog sources in 10-bit and 12-bit ADC is 10 kΩ and 4.4 kΩ, respectively. Refer to the specific device data sheet with regard to the equation that calculates the minimum acquisition time for a particular application.

Auto-Conversion Trigger Source

The Auto-conversion Trigger allows the system to schedule acquisition and conversion sequences without software intervention. When a rising edge of the selected source occurs, the ADGO bit is set. The sources for the auto-conversion trigger can be found on the device data sheet. In an application, these auto-conversion trigger sources can be used to set the sampling period of the ADC. The auto-conversion source is selected using the ADC Auto-conversion Trigger Control register (ADACT).

CONTINUOUS MODE RETRIGGER

The Continuous mode retrigger can be enabled by setting the A/D Continuous Operation Enable bit (ADCONT) of the ADCON0 register to '1' (ADCONT = 1). Enabling the Continuous mode allows an automatic sampling retrigger after the threshold has been tested. In this mode, the A/D Conversion Status bit (ADGO) of the ADCON0 register remains set until the threshold conditions are met, according to the selected ADTMD and the A/D Stop On Interrupt bit (ADSOI) of the ADCON3 register.

SLEEP MODE

Operating the ADC^2 module in Sleep mode requires the ADC clock source to use the dedicated RC oscillator (FRC). When the conversion is complete, the device will wake-up if the ADC interrupt is enabled. If the ADC interrupt is disabled, the device will remain in Sleep.

If an external trigger is received during Sleep while the clock source is set to FRC, the ADC will perform the conversion and set the ADC Interrupt Flag bit (ADIF) upon completion. If an external trigger is received during Sleep while the clock source is set to something other than the FRC, the trigger is recorded but the conversion will not begin until the device exits the Sleep mode.

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CAPACITIVE VOLTAGE DIVIDER (CVD) FEATURE

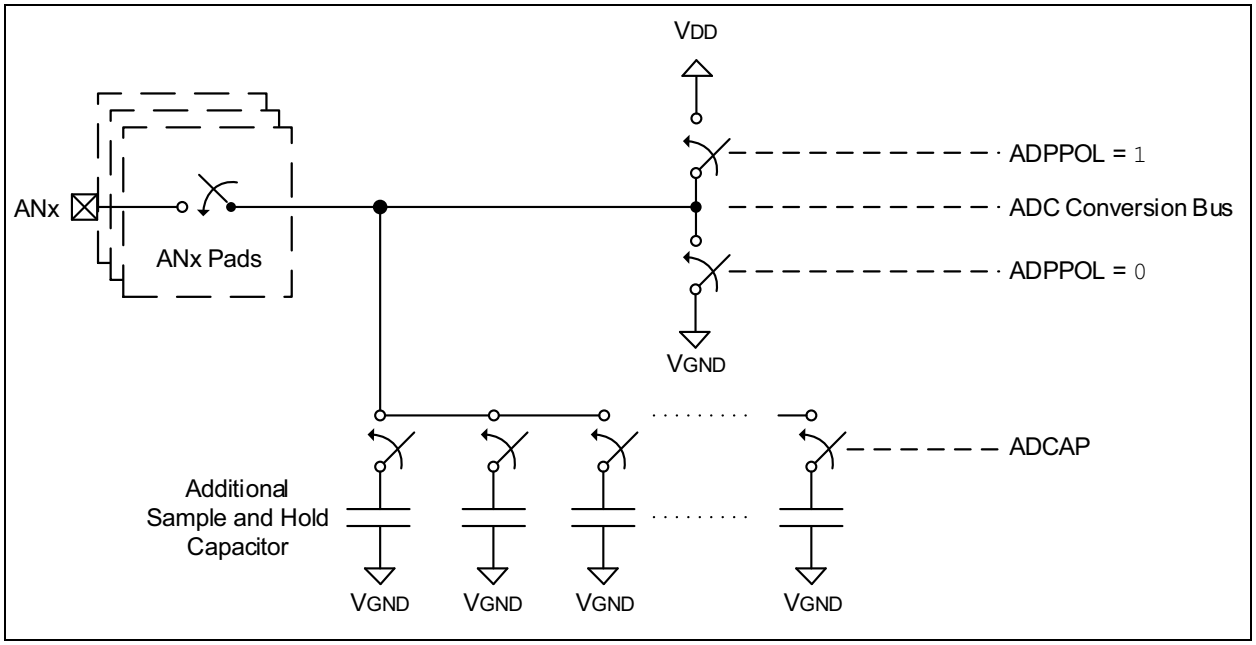
One of the features of ADCC module is the CVD. CVD uses capacitors as components for the voltage divider circuit. Figure 3 shows the block diagram for the hardware CVD portion of the ADCC module. This feature of ADCC allows the user to perform relative capacitance measurement on any ADC channel using the internal ADC CHOLD as a reference.

The CHOLD and the external capacitance sensor connected to the selected analog channel are pre-charged to VDD or VSS depending on the selected pre-charge polarity bit (ADDPOL) of ADCON1 register, while the path between CHOLD and external capacitive sensor is disconnected. The amount of time that this charging occurs depends on the value set in the ADPRE register. This pre-charge stage is enabled by writing a non-zero value to the ADPRE register. If the ADPRE is set to '0' when an ADC conversion begins, the pre-charge stage is skipped.

The acquisition stage is a measured time for the CHOLD voltage to charge or discharge from the selected analog channel. During acquisition, a capacitive voltage divider is formed between the pre-charged CHOLD and the selected analog channel while the selected analog channel is connected to CHOLD. As a result, the charge between the CHOLD and the external capacitance sensor connected to the selected analog channel is now equally distributed. After the charge transfer has been stabilized, the CHOLD voltage is measured by the ADCC and used for determining the capacitance value of the external capacitance.

Another unique feature of CVD hardware is the optional additional capacitance that can be added in parallel with the CHOLD. This additional capacitance can be selected via the ADC Additional Sample Capacitor Selection Register (ADCAP). It is used in CVD applications by improving the match between the internal and external capacitance for better sensing performance.

FIGURE 3: HARDWARE CAPACITIVE VOLTAGE DIVIDER BLOCK DIAGRAM



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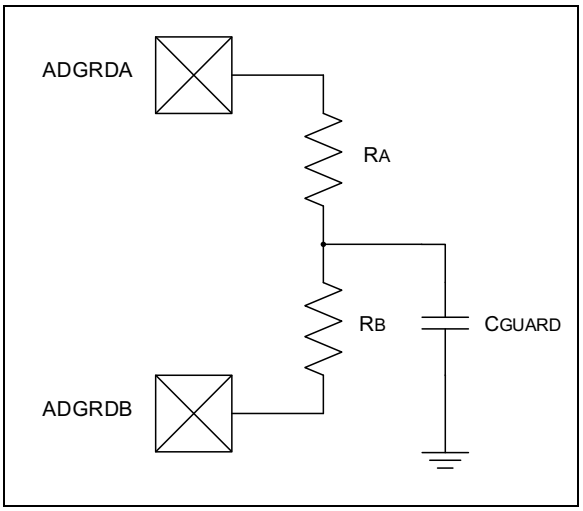
GUARD RING CIRCUIT

ADCC module is also equipped with a guard ring circuit (see Figure 4) which supports the hardware CVD. Two digital outputs and associated voltage divider resistors are used to drive the guard ring voltage. The guard ring circuit is used to generate a signal in phase with the CVD sensing signal to minimize the effects of the parasitic capacitance on sensing electrodes. It can also be used as a mutual drive for mutual capacitive sensing. For more information about active guard and mutual drive, see Application Note AN1478 *"mTouch™ Sensing Solution Acquisition Methods Capacitive Voltage Divider"*, (DS01478).

The ADCC provides two guard ring outputs, ADGRDA and ADGRDB pins. For a device that has Peripheral Pin Select (PPS), the ADGRDA and ADGRDB can be remapped to any output pins using the PPS Output Selection Register (RxyPPS).

The "Rxy" in the RxyPPS is a place holder for the pin identifier (e.g., RB0PPS = 0x24 and RB1PPS = 0x25), where RB0 is configured as ADGRDA output pin and RB1 as ADGRDB output pin. Note that selector values for the PPS of ADGRDA and ADGRDB are device-specific.

FIGURE 4: GUARD RING CIRCUIT



ADCC OUTPUT ACTIONS

Threshold Comparison

The post-processing result of the ADC^2 module can be compared to the threshold value set in the ADC Error Calculation Mode Select bits (ADCALC) of the ADC Threshold register (ADCON3). The ADC Result register (ADRES), ADC Previous Result register (ADPREV), ADC Threshold Setpoint register (ADSTPT), and ADC Filter register (ADFLTR) are involved in the error calculation. The selected Error Calculation mode and Sample Conversion mode determine how the registers are used in the error calculation (see Table 1).

Double Sampling mode is enabled by setting the Double-Sample Enable bit (ADDSEN) of the ADCON1 register. When this bit is set, two conversions are required before the module starts calculating the threshold error. This is not technically true in hardware, but the finished effect is truthfully described by this when ADIF occurs.

TABLE 1: ERROR CALCULATION MODE

ADCALC	Error Calculation		Application
	ADDSEN=0 Single-Sample Mode	ADDSEN=1 CVD Double-Sample Mode(1)	
000	ADRES-ADPREV	ADRES-ADPREV	First derivative of single measurement(2)
			Actual CVD result in CVD(2)
001	ADRES-ADSTPT	(ADRES-ADPREV)-ADFLTR	Actual result vs. setpoint
010	ADRES-ADFLTR	(ADRES-ADPREV)-ADFLTR	Actual result vs. averaged/ filtered value
011	Reserved		
100	ADPREV-ADFLTR	ADPREV-ADFLTR	First derivative of filtered value(3) negative
101	ADFLTR-ADSTPT	ADFLTR-ADSTPT	Average/filtered value vs. setpoint
110	Reserved		
111	Reserved		

Note 1: When ADPSIS = 0, the value of (ADRES-ADPREV) is equal to (S_2-S_1).
2: When ADPSIS = 0.
3: When ADPSIS = 1.

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The calculated result is stored in the ADERR, which can be compared to the selected upper or lower threshold. These two threshold values can be set by changing the ADC Upper Threshold (ADUTH) registers and the ADC Lower Threshold (ADLTH) registers. A result of true, based on the comparison shown in Table 2, will trigger an interrupt. This threshold test is selected via the Threshold Interrupt Mode Select bits (ADTMD) of the ADCON3 register.

TABLE 2: THRESHOLD INTERRUPT MODE

ADTMD	Interrupt Condition	Comparator Outputs		
		ADERR<ADLTH		ADERR>ADUTH
000	Never Interrupt			
001	Error < Lower threshold	True		—
010	Error ≥ Lower threshold	False		—
011	Error is between thresholds	False	AND	False
100	Error is outside thresholds	True	OR	True
101	Error ≤ Upper threshold	—		False
110	Error > Upper threshold	—		True
111	Interrupt for all data	—		—

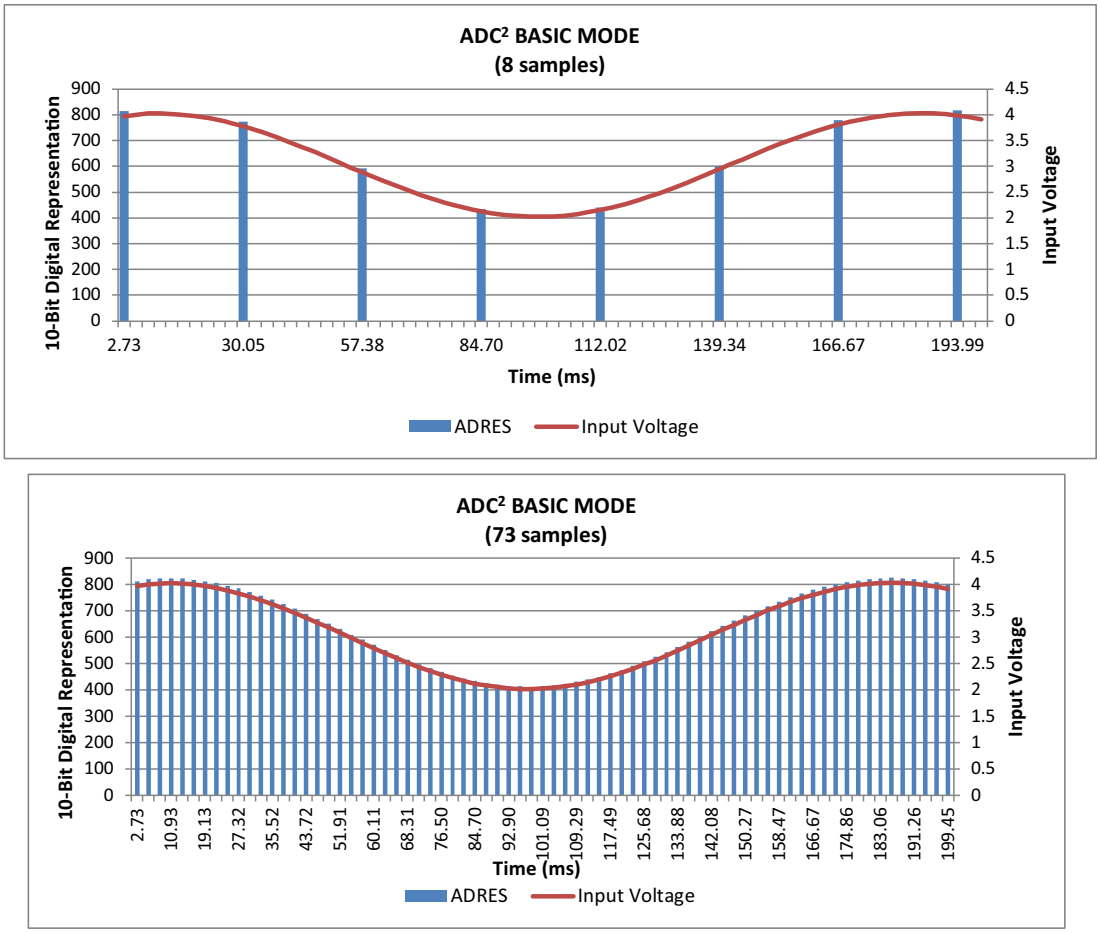
COMPUTATION MODES

Basic Mode

The Basic mode of the ADC^2 mimics the legacy ADC operation. In this mode, the accumulator logic is not active. This means that the A/D Accumulator (ADACC) and A/D Repeat Count (ADCNT) registers values are not used throughout the operation and the ADRES register is used in all modes. The Basic mode of the ADC^2 is selected by setting the A/D Operating Mode selection bits (ADMD) of the A/D Control Register 2 (ADCON2) to 0 (ADMD = `000`). With the auto-trigger feature of the module, input sampling can be easily triggered by other peripherals and external sources. The result of the conversion can be compared to a threshold set point which may trigger the Analog-to-Digital Converter Interrupt Flag bit (ADTIF) of the PIR1 register.

Figure 5 shows the result of the Basic mode ADC conversion using different sampling rates.

FIGURE 5: BASIC MODE



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Accumulate Mode

The Accumulate mode of the ADC[2] is selected by setting the ADMD bits of the ADCON2 register to 1 (ADMD = `001`). In this mode, the digital representation of the analog input signal in the 10-bit or 12-bit ADRES register is accumulated to the 16-bit or 18-bit ADACC register, respectively. With each sample, ADCNT is incremented, indicating the number of samples accumulated. The ADCNT value saturates at 255 samples and does not rollover to zero. Since the value being accumulated to ADACC is a 10-bit or 12-bit ADRES value, the ADACC may overflow after as few as 64 samples. This event will trigger the ADC Accumulator Overflow bit (ADAOV) of the status register, ADSTAT.

The accumulated value can be right-shifted up to six times by changing the value of the ADC Accumulate Calculation Right Shift Select bits (ADCRS) of the ADCON2 register. This means that the accumulated value is effectively divided by a power of two (2^{ADCRS}). The result of the shifted accumulated value is stored in the ADFLTR register. Table 3 shows a sample data of an Accumulator mode with 10-bit ADRES register.

TABLE 3: ACCUMULATOR MODE EXAMPLE

ADCNT	ADCRS	VINPUT	10-bit ADRES	16-bit ADACC	16 bit ADFLTR
1	3	2.5V	514	514	64
2	3	2.5V	514	1028	128
3	3	2.5V	514	1542	192
4	3	2.5V	514	2056	257
5	3	2.5V	514	2570	321
6	3	2.5V	514	3084	385
7	3	2.5V	514	3598	449
8	3	2.5V	514	4112	514

Averaging Mode

The Average mode of the ADC[2] is selected by setting the ADMD bits of the ADCON2 register to 2 (ADMD = `010`). This mode is like an Accumulate mode wherein the ADACC accumulates the data sample and the ADCNT increments with each sample, except that the number of samples being accumulated in this mode is up to the value set in the A/D Repeat Setting register (ADRPT). When the ADCNT is equal to ADRPT, the value stored in the ADC Filter register (ADFLTR) becomes the average value of the input signal. Effectively, the value stored in the ADFLTR is the resulting factor of ADACC and ADRPT. The average value of the input voltage can be correctly calculated when the ADRPT is equal to Equation 3. When the ADCNT exceeds the value of ADRPT, the ADCNT and ADACC registers reset automatically to accumulate again the data samples.

Table 4 shows the data samples for the Averaging mode where the ADCRS is equal to two, and with the ADRPT equal to four. This means that four samples will be accumulated to get the average value, then on the fifth sample, the accumulator will be cleared automatically as shown in Figure 6.

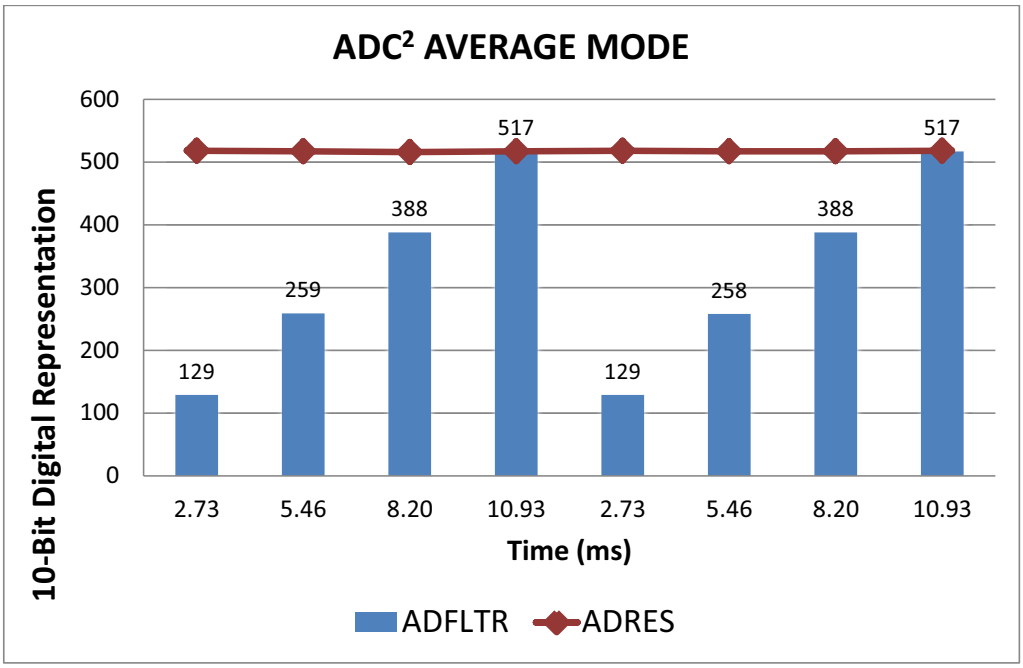
EQUATION 3: NUMBER OF SAMPLES TO BE TAKEN

$$ADRPT = 2^{ADCRS}$$

TABLE 4: AVERAGE MODE EXAMPLE

ADCRS	ADRPT	SAMPLE	ADCNT	10-bit ADRES	ADACC	ADFLTR
2	4	0	1	518	518	129
2	4	1	2	518	1036	259
2	4	2	3	516	1552	388
2	4	3	4	517	2069	517
2	4	4	1	518	518	129
2	4	5	2	517	1035	258
2	4	6	3	517	1552	388
2	4	7	4	518	2070	517
2	4	8	1	517	517	129
2	4	9	2	516	1033	258

FIGURE 6: ADC^2 AVERAGE MODE



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Burst Average Mode

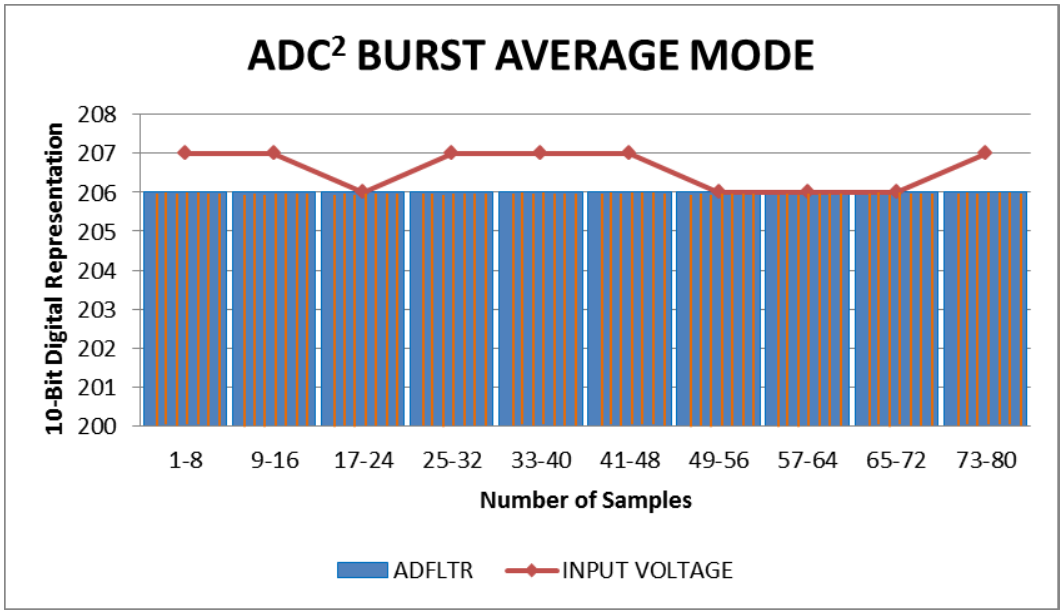
Like Averaging mode, the Burst Average mode averages the input signal except that the sampling is acquired quickly after a single trigger (see Figure 7). This means that in a single conversion, all the data samples are accumulated up to the set ADRPT and when the ADCNT matches the set ADPRT value, the average value of the input signal is attained. Once the burst average value is attained, the threshold comparison can be performed. For further information, see **Section "Threshold Comparison"**. Consequently, ADTIF can only occur at the end of a burst.

The Burst Average mode is selected by setting the ADMD bits of the ADCON2 register to 3 (ADMD = `011`). Table 5 shows the data sample for Burst Average mode.

TABLE 5: BURST AVERAGE MODE EXAMPLE

SAMPLE	TRIGGER	ADCNT	ADCRS	ADRPT	10-bit ADRES	ADACC	ADFLTR
1-8	1	8	3	8	207	1655	206
9-16	2	8	3	8	207	1653	206
17-24	3	8	3	8	206	1653	206
25-32	4	8	3	8	207	1653	206
33-40	5	8	3	8	207	1652	206
41-48	6	8	3	8	207	1653	206
49-56	7	8	3	8	206	1654	206
57-64	8	8	3	8	206	1652	206
65-72	9	8	3	8	206	1655	206
73-80	10	8	3	8	207	1654	206

FIGURE 7: ADC^2 BURST AVERAGE MODE



Low-Pass Filter Mode

A low-pass filter passes signals with frequencies below its cutoff and attenuates frequencies above its cutoff. This mode is selected by setting the ADMD bits of the ADCON2 register to 4 (ADMD = `100`). The ADCRS determines the low-pass filter order. Given the radian value in Table 6, the cutoff frequency (@ – 3dB gain) can be calculated using Equation 4.

EQUATION 4: CUTOFF FREQUENCY AT A GIVEN RADIAN VALUE

$$f_{cutoff} = \frac{\text{radian value @ -3 dB gain}}{2\pi T}$$

Figure 8 shows the bode plot gain of the 10-bit ADCC low-pass filter using a sampling interval T of 1/960 Hz. The figure is actual 10-bit ADC data, and exhibits both sampling and quantization effects

TABLE 6: FILTER CUTOFF FREQUENCY EXAMPLES

ADCRS	Radian Value @ -3 dB Gain (radian)	Gain @ f=1/2T (dB)	T (3) (sec)	F_{cutoff} (3) (Hz)	$F_{Nyquist} = 1/2T$ (3) (Hz)
1	0.72	-9.5	1/960 Hz	110.01	480
2	0.284	-16.9	1/960 Hz	43.39	480
3	0.134	-23.5	1/960 Hz	20.47	480
4	0.065	-29.8	1/960 Hz	9.93	480
5	0.032	-36	1/960 Hz	4.89	480
6	0.016	-42	1/960 Hz	2.44	480

Note 1: Not all values are supported in all devices.
2: T = sampling interval (sec).
3: The T, F_{cutoff} and $F_{Nyquist}$ are examples.

FIGURE 8: BODE PLOT GAIN OF THE LOW-PASS FILTER WITH T = 1/960 Hz

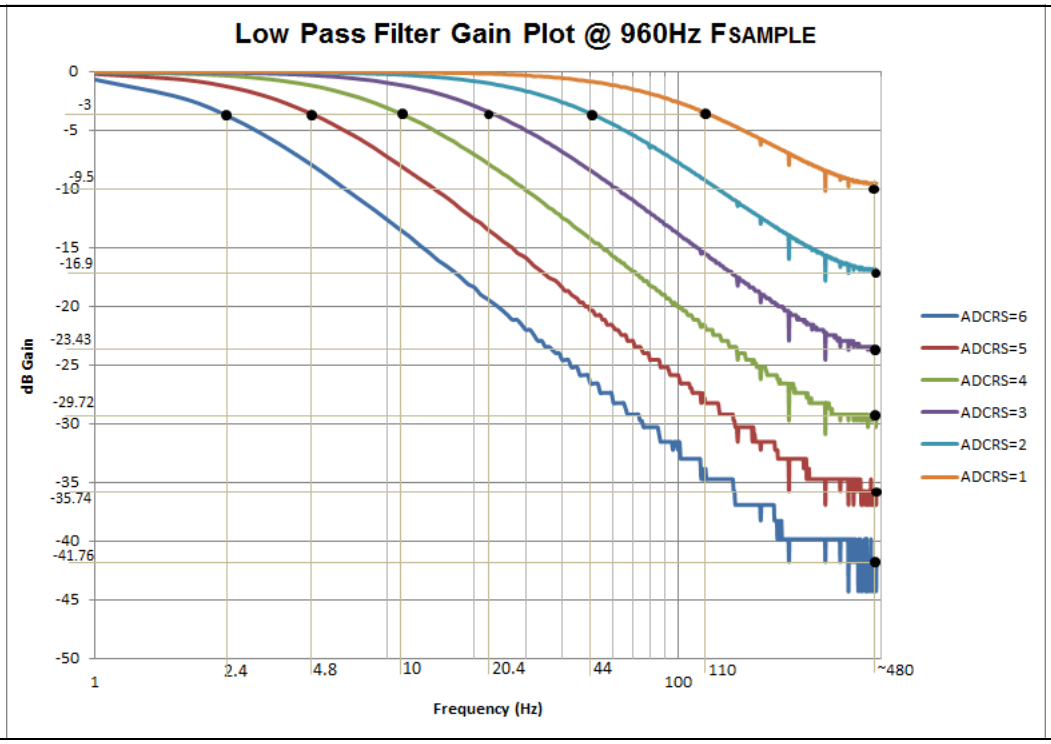


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Table 7 shows the summary of the different operating modes of ADC^2.

TABLE 7: ADC^2 COMPUTATION MODES SUMMARY

Mode	ADMD	Bit Clear Conditions	Value after Trigger Completion		Value at ADTIF Interrupt		
		ADACC and ADCNT	ADACC	ADCNT	ADAOV	ADFLTR	ADCNT
Basic	0	ADACLR = 1	Unchanged	Unchanged	n/a	n/a	Count
Accumulate	1	ADACLR = 1	S+ADACC or (S_2-S_1) + ADACC	ADCNT+1, but not more than 255	ADACC overflow	ADACC/2^{ADCRS}	Count
Average	2	ADACLR = 1 or ADCNT ≥ ADRPT at ADGO set or retrigger	S+ADACC or (S_2-S_1) + ADACC	ADCNT+1, but not more than 255	ADACC overflow	ADACC/2^{ADCRS}	Count
Burst Average	3	ADACLR = 1 or ADGO set or retrigger	Each repetition: same as Average End with sum of all samples	Each repetition: same as Average End with ADCNT = ADRPT	ADACC overflow	ADACC/2^{ADCRS}	ADRPT
Low-pass Filter	4	ADACLR = 1	S + ADACC - ADACC/2^{ADCRS} or $(S_2 - S_1)$ + ADACC - ADACC/2^{ADCRS}	ADCNT+1, but not more than 255	ADACC overflow	Filtered value	Count

Note 1: S = Single sample;
S_2-S_1 = A double sample difference that is used in place of the single sample.

CONCLUSION

This technical brief describes how the Analog-to-Digital Converter with computation module works on PIC® microcontrollers. It covers the ADC^2 built-in computational features and post-processing functions.

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