Introduction

This application note provides the hardware and layout design guidelines, Radio Frequency (RF) measurement setup and antenna pattern measurement for the applications developed using the IS2083BM System-on-Chip (SoC).

- Provides guidelines for PCB layout design, placement and routing, power management, RF circuit and audio/voice circuit
- Describes RF measurement procedure and test setup for certification
- Describes antenna radiation pattern measurement procedure and setup
- Provides application reference schematics
- Describes Mass Production (MP) procedure and setup
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1. **Hardware Guidelines**

This chapter describes the placement and routing of antenna, bypass capacitor, crystal oscillator, audio/video interface, RF traces and components.

1.1 **Placement and Routing Guidelines**

To achieve the best RF performance, it is mandatory to follow the recommendations as listed:

- The board must have a solid ground plane. The center ground pad of the device must be firmly connected to the ground plane by using Vias.
- Keep large metal objects away from the antenna on-board to avoid electromagnetic field blocking.
- The antenna must not be shielded by any metal objects.
- The board components must be positioned in a noise-free environment and must be kept far away from high-frequency clock signals. For better performance, shield those components. Any noise radiated from the main board in this frequency band degrades the sensitivity of the system.

1.2 **Power and Ground**

One layer (second layer as suggested) is dedicated as a ground plane. Make sure that this ground plane is not broken by routes. Power can route on all layers, except the ground layer. Power supply routes must be heavy copper fill planes to ensure the lowest possible inductance. The power pins of the core IC must have a Via direct connect to the power plane as close to the pin as possible. Decoupling capacitors must have a Via right next to the capacitor pin and this Via must go directly down to the power plane; that is, the capacitor must not route to the power plane through a long trace. The ground side of the decoupling capacitor must have a Via right next to the pad, which goes directly down to the ground plane. Each decoupling capacitor must have its own Via directly to the ground plane and power plane right next to the pad. The decoupling capacitors must be placed as close to the pin for filtering.

1.3 **RF Traces and Components**

It is mandatory to follow the recommendations as listed:

- The RF traces from RTX and PA1OP pins of the IS2083BM to the antenna must be 50 Ohm controlled impedance trace.
- Copy exact routing and placement for the RF section layout design (RTX and PA1OP connections) from the reference design module layout. These controlled impedance traces must reference a ground plane on a lower layer and to be adjusted, depending on the dielectric and copper weight used.
- Do not route any other traces in the RF area on any layer. This ground reference plane must extend entirely under the tuner.
- Be sure to add as many ground Vias as possible.
- Connect all the ground layers together (ground stitching) along the RF traces and throughout the area, where the RF traces are routed.
- Add at least two ground Vias for every ground pad around the RF components. Place all the ground Vias along the RF traces on either side.
- Connect the center ground pad of the IS2083BM to the inner ground layer, using a grid of Vias (as suggested in the BM83 module reference design). The ground path going from the ground pad down to the ground plane must be absolutely as low impedance as possible.
- Do not use thermal relief pads for the ground pads of all components in the RF path. These component pads must be filled with the ground copper.
- Ensure that the route from the antenna to IS2083BM is as short as possible and is completely isolated from all other signals on the board. No signals must route under this trace on any layer of the board.
- Ensure that when IS2083BM is active, all the digital signals which are toggled are placed away from the antenna. The digital signals must not be placed near the antenna. All the digital components and switching regulators on the board must be shielded to avoid the noise generated by the antenna.
1.4 Interference Guidelines

The interference affects the RF receiver performance on the board, radiating noise into the antenna or coupling into the RF traces going to input LNA. It is mandatory to follow the interference recommendations as listed:

• Ensure that there is no noise circuit placed anywhere near the antenna or the RF traces. All the noise generating circuits must be shielded so that they do not radiate noise that is picked up by the antenna.
• Ensure that no traces are routed underneath the RF portion of IS2083BM input.
• Ensure that no traces route underneath of the RF traces from the antenna to the IS2083BM. This applies to all layers.
• Even if there is a ground plane on a layer between the RF route and another signal, the ground return current flows on the ground plane and couple into the RF traces.

1.5 Antenna Guidelines

To achieve the best RF performance, it is mandatory to follow the antenna recommendations as listed:

• Choose an antenna that covers the proper frequency band between 2.4 GHz to 2.5 GHz.
• Ensure that the antenna connected to the PCB pad is properly designed for 50 Ohm impedance, which is extremely important. The antenna vendor must specify the pad dimensions, the spacing from the pad to the ground reference plane, and the spacing from the edges of the pad to the ground fill on the same layer as the pad. The ground reference plane for the 50 Ohm trace going from the antenna pad to IS2083BM is probably on a different layer than the ground reference for the antenna pad. Ensure that the pad design contains a proper transition from the pad to the 50 Ohm trace.
• Ensure that the antenna matching components are placed as close to the antenna pad as possible. The antenna cannot be properly matched if the matching components are far away from the antenna.

1.6 Reference PCB Stack-up

The recommended printed circuit board (PCB) stack specifications are listed in the following table:

• FR4, 4 layers, PCB Thickness: 0.6 mm
• 2.4 GHz top layer and bottom layer 50Ω trace width: 6 mils
• 2.4 GHz top layer and bottom layer 50Ω gap width: 6 mils

Table 1-1. PCB Stack Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solder Mask (SM)</td>
<td>0.4 mil</td>
</tr>
<tr>
<td>Top Cu+Plating</td>
<td>0.5 OZ/1.6 mil</td>
</tr>
<tr>
<td>Prepreg</td>
<td>2116/4.3mil</td>
</tr>
<tr>
<td>Metal 1</td>
<td>1 OZ/1.4 mil</td>
</tr>
<tr>
<td>Core 2</td>
<td>Substrate</td>
</tr>
<tr>
<td>Metal 2</td>
<td>1 OZ/1.4 mil</td>
</tr>
<tr>
<td>Prepreg</td>
<td>2116/4.3 mil</td>
</tr>
<tr>
<td>Bottom Cu+Plating</td>
<td>0.5 OZ/1.6 mil</td>
</tr>
<tr>
<td>Solder Mask (SM)</td>
<td>0.4 mil</td>
</tr>
<tr>
<td>Total Thickness</td>
<td>23.6 mil = 0.6 mm</td>
</tr>
</tbody>
</table>
1.7 Buck Layout Guide

To achieve the best buck output voltage performance, it is mandatory to follow the layout recommendations as listed:

- The inductor and capacitor of buck circuit must be placed in the same layer and close to IS2083BM.
- Buck trace width must be at least 15 mils.
- Buck input – refer to Figure 1-1 and Figure 1-2 for IS2083BM pin K1 and K9. Place the buck input capacitor (C86) as close as possible to pin K1 (PMU_BK1_VDD) and K9 (PMU_BK2_VDD). The buck input routing path sequence is from SYS_PWR to C86, then connect C86 to pin K1 and K9. Do not connect SYS_PWR directly to pin K1 and K9 without first connecting to C86.
- Buck Output – refer to Figure 1-1 for IS2083BM pin K3 (BK1_O_1V5). The buck output routing path sequence is PMU_BK1_LX, L2, C87, PMU_BK1_VOUT and must be as short as possible. Trace of buck output to load must be connected from C87.
- Keep no ground trace under inductors L2 and L3 on top layer.
- Place solid ground plane on 2nd layer. The ground path from C87 and C88 to IS2083BM pins F5, F6 and E5 ground must be short and direct without being interrupted by another trace/ traces. The ground of C87 and C88 must be placed at least a ground Via to the ground plane to reduce the ground impedance.

Figure 1-1. Recommended Buck Layout Scheme
To ensure the buck output voltage quality, the wire wound coil high current inductor is recommended for buck inductor. The 10 uH wire wound inductor (ZWP-0805-100K) with high IDC and low DCR are recommended. The following figure is an example considered from ZenithTek.

**Note:** Multi-layer Ceramic Inductor (MLCI) is not recommended to be used as L10 as it may not be able to start up the chip stably. The poor yield rate also affects the quality of voltage.
1.8 Bypass Capacitor Placement and Routing

The bypass capacitor on the power tree trace of IS2083BM must be placed close to the input or output pin, as highlighted in the following figure.
1.9 Crystal Oscillator Routing and Placement

To ensure low noise and frequency precision, the crystal oscillator layout placement is listed as below:

- The crystal trace (XON/XOP) should be as short as possible and the width must be wider than 7 mils.
- The ground plane at the ground layer must be larger than the crystal size and the external load capacitor’s ground needs to be connected to ground plane through Vias directly.
- The external load capacitors must be placed as close as possible to the crystal.
1.10 Audio/Voice Interface Routing

For capless analogy audio interface layout, the following rules ensure better audio noise rejection.

- Width of each trace and the gap must be 8~10 mil.
- The clearance of ground plane must be wider than 10 mils.
- The Via holes of GND must be placed closely along the AOHPR/AOHPL trace.
For single-end analogy audio output layout, the following rules ensure better audio noise rejection.

- The traces of AOHPR and AOHPL must be 1W (10 mils to 15 mils) width, and one ground trace must be added between those traces to prevent the crosstalk condition.
- Width of each trace and the gap must be 8~10 mil.
- The clearance of ground plane must be wider than 10 mils
- The Via holes of GND must be placed tightly beside the AOHPR/AOHPL.

### Figure 1-6. Reference for Capless Audio Output

### Figure 1-7. Reference for Single-end Audio Output

#### 1.11 Analog Microphone Inputs

The differential microphone input circuit and the placement rules are listed below:
• The DC blocking capacitors (C21 and C34) are placed as close as possible to IS2083BM.
• The MIC_BIAS filtering components (R6 and C22) are placed close to the microphone.
• The microphone and signal paths of microphone must be routed on same layer.
• The component on differential path (MICP1, MICN1, MIC_P1 and MIC_N1) must be placed close to each other to reduce common mode noise.

Note:
1. If single microphone is used, change R10 from 2 kΩ to 0Ω.
2. Connect MIC+ with microphone positive side and MIC- to microphone ground.

Figure 1-8. Reference Analog Microphone Inputs Schematic and PCB Routing
2. **Conductive RF Measurement Setup**
   This chapter describes the Conductive RF test procedure.

2.1 **Hardware Test Connection**
   Perform the following steps for hardware test connection:
   1. Remove antenna matching components and solder RF coaxial cable on RF test point.
2. Refer to the following figure. The test mode connection is described as below:
2.1. Connect the test interface of IS2083BM DUT (ADAP_IN, VBAT, GND, HCI_TX, HCI_RX and P3_4) to Edgar III board (USB to UART Converter Board) (5V, BAT, GND, HTX, HRX and P2_0).

2.2. Edgar III connects to PC USB port and DUT connect to RF tester.

2.3. Set the P2_0 of SW1 to ON on Edgar III (P3_4 of DUT pulled to low).

Note: Refer to 7. Appendix A: Edgar III Circuit. Contact Microchip sales or an FAE for Edgar III boards.

Figure 2-2. RF Test Mode Connection

3. Use the ISRT tool to configure RF test parameter.

4. Test with RF equipment and verify RF Tx/Rx performance.

2.2 ISRT Tool Test Procedure

The ISRT tool is generally used for regulatory approval such as BT SIG/QDID, FCC ID, CE and so on. The following ISRT test procedures explain the common usage of the ISRT tool on a Windows® PC. For more details on the ISRT tool, refer to the ISRT User Manual in the ISRT tool release package.

1. Open the ISRT tool and click CREATE to select the test solution.
2. Select IS2083BM device.
3. Select the correct “COM” and “BAUDRATE”, then click Finish.
4. For Continuous Waveform (CW) mode $T_x$ power adjustment, follow the procedure below:
   4.1. In “MODE”, select TX.
   4.2. Select “TX Modulation”: OFF
   4.3. In “Channel”, select the right channel (ch0~ch78).
   4.4. Select “TX POWER TRIM Level” as PL0 or PL2.
   4.5. Click START to perform TX power test.
   4.6. Select Trim Power Up/ Trim Power Down to adjust the RF power to expected power level:
      • For PL0, +10dBm is the recommended target power level
      • For PL2, 0dBm is the recommended target power level
   4.7. Stop test then store the Tx parameters.
   4.8. Select Save To Device to store the trimmed RF power parameter to DUT.
   4.9. Select Save To File to store the trimmed RF power parameter to file as record.
Figure 2-6. TX Power Trim Test

Note: Enable “Temperature Compensation” if temperature range other than room temperature is required.

5. For TX modulation test, follow the procedure as below (non-signaling test):
   5.1. In “MODE”, select TX.
   5.2. Select “TX Modulation”: ON
   5.3. In “Channel”, select the right channel (CH0~CH78).
   5.4. Set “Packet Count” as Continue, “Packet Type” as default 3DH5 and “Payload Type” as PRBS.
   5.5. Click START to test with the RF tester.
5. Note: Enable "Temperature Compensation" if temperature range other than room temperature is required.

6. To enable Test mode for signaling test with RF tester (for example, MT8852B), follow the procedure as below:
   6.1. Select "TEST MODE".
   6.2. Select "Temperature Compensation".
   6.3. Click START to start auto test with tester.
7. For BLE TX test, follow the procedure below:

7.1. In “MODE”, select TX under the **BLE** tab.
7.2. Select “Temperature Compensation”.
7.3. Set “TX POWER TRIM” parameters (TX Modulation ON, Channel Number, Length and Payload Type).
7.4. Click **START** to start TX test with tester.
7.5. Select Power Up/Power Down to adjust the RF power to the expected power level.
7.6. Stop test then store the TX parameters.
7.7. Select **Save To Device** to store the trimmed RF power parameter to DUT.
7.8. Select **Save To File** to store the trimmed RF power parameter to file as record.
Figure 2-9. Bluetooth® Low Energy TX Test
3. **Antenna Guidelines**

   This chapter describes the antenna return loss, radiation pattern measurement and antenna placement.

3.1 **Antenna Return Loss**

   To keep the antenna performance stable, the antenna matching circuit must guarantee the curve of antenna (S11) < -10 dB from 2402 MHz to 2480 MHz. The following figures illustrate the return loss of antenna (S11) and its criteria.

   **Figure 3-1. Suggested Antenna Return Loss from 2402 MHz to 2480 MHz**

3.2 **Antenna Radiation Pattern Measurement**

   Once the antenna and its matching circuit is created, it is suggested that the designer check the quality of antenna performance from the antenna test report.
Table 3-1. Measured Antenna Gain and Efficiency

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>Total Radiation Power (dBm)</th>
<th>Efficiency (%)</th>
<th>Gain (dBi)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2412</td>
<td>-4.60849</td>
<td>34.606</td>
<td>-0.5966</td>
</tr>
<tr>
<td>2417</td>
<td>-4.50071</td>
<td>35.4755</td>
<td>-0.42527</td>
</tr>
<tr>
<td>2422</td>
<td>-4.43394</td>
<td>36.0252</td>
<td>-0.56911</td>
</tr>
<tr>
<td>2427</td>
<td>-4.38346</td>
<td>36.4464</td>
<td>-0.55402</td>
</tr>
<tr>
<td>2432</td>
<td>-4.38017</td>
<td>36.4739</td>
<td>-0.46928</td>
</tr>
<tr>
<td>2437</td>
<td>-4.2799</td>
<td>37.3259</td>
<td>-0.41755</td>
</tr>
<tr>
<td>2442</td>
<td>-4.186</td>
<td>38.1417</td>
<td>-0.32167</td>
</tr>
<tr>
<td>2447</td>
<td>-4.03923</td>
<td>39.4527</td>
<td>-0.23542</td>
</tr>
<tr>
<td>2452</td>
<td>-3.90445</td>
<td>40.6963</td>
<td>-0.03414</td>
</tr>
<tr>
<td>2457</td>
<td>-3.74337</td>
<td>42.2341</td>
<td>-0.131415</td>
</tr>
<tr>
<td>2462</td>
<td>-3.58446</td>
<td>43.808</td>
<td>-0.188512</td>
</tr>
<tr>
<td>2467</td>
<td>-3.47342</td>
<td>44.9426</td>
<td>-0.228235</td>
</tr>
<tr>
<td>2472</td>
<td>-3.43999</td>
<td>45.2899</td>
<td>-0.262527</td>
</tr>
<tr>
<td>2484</td>
<td>-3.56319</td>
<td>44.0231</td>
<td>-0.125341</td>
</tr>
</tbody>
</table>

Figure 3-2. Measured Antenna 3D Pattern
3.3 **Antenna Placement**

The following figure illustrates how to place an antenna on motherboard and how the location affects an antenna performance. It must reserve the clearance area between the ground plane and antenna, where the range extends to \(2\pi(D/\lambda)\) of distance from actual antenna entity.

**Note:** \(D\) is the widest dimension of the antenna perpendicular to the line of propagation and \(\lambda\) is the wavelength of carrier frequency \(f_c\).

**Figure 3-3. Antenna Placement Examples**
4. Bluetooth Qualification and Regulatory

The Bluetooth qualification process is described in the following website: https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/declare-your-product.

Figure 4-1. Qualification and Listing Process

Microchip provides a qualified Bluetooth module for the user to apply on their base product without any additional fee.

If the customer designs the chip down base with the existing Microchip qualified firmware protocol stack, the core QDID can be re-used but need to perform RF testing for new QDID listing.

Declaration ID: D030016
QDID: 110017
Design Name: Bluetooth 5.0 Core System Component

Beside Bluetooth SIG/QDID certification, the following items illustrate the general regulatory approval of country or region. Customer can apply the test service by a qualified test lab.

- United States/FCC
- Canada/IC
- Europe/CE
- Japan/MIC
- Korea/KCC
- Taiwan/NCC
- China/SRRC
5. Reference Circuit

IS2083BM application circuit includes two modes – Host mode and Embedded mode.

In Host mode, IS2083BM interfaces with an external microcontroller (MCU) for application-specific system control, where the Multi-speaker (MSPK) solution can reside on this MCU.

For Embedded mode, the MSPK firmware is natively integrated on the module. Simple system control can be implemented in the module MCU by using the SDK or changing the parameters in the UI configuration tool. DSP parameters, such as equalizer settings, can be set using the configuration tool.

The following figure illustrates the Host mode reference circuit, where IS2083BM interfaces with MCU PIC32MX450F256L and Digital Audio AMP STA369TW for Bluetooth speaker application.

Figure 5-1. IS2083BM Host Mode Bluetooth Speaker Reference Circuit Block Diagram
Figure 5-3. I2083BM Host Mode Reference Schematic - continued.

Figure 5-4. I2083BM Host Mode Reference Schematic - continued.
Figure 5-5. I2083BM Host Mode Reference Schematic - continued.

The following figure illustrates the IS2083BM Embedded mode reference circuit.

Figure 5-6. I2083BM Host Mode Reference Schematic - continued.

15V DC JACK

15V TO 5V GENERATION

5V TO 3V3 GENERATION

CAD Note: Please refer the datasheet for layout activity.
Figure 5-8. IS2083BM Embedded Mode Reference Schematic

Figure 5-9. IS2083BM Embedded Mode Reference Schematic - continued.
Figure 5-10. IS2083BM Embedded Mode Reference Schematic - continued.

PUSH BUTTON

- MTR/Power
- SW5
- D11 100V 220V
- D12 100V 220V
- SW7
- D16 100V 220V
- SW8
- D17 100V 220V
- C24 10uF 16V 5% parent
- C25 10uF 16V 5% parent
- C28 10uF 16V 5% parent
- C30 10uF 16V 5% parent

Reference Circuit

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6. Mass Production Test Board Design

This chapter describes the MPBT and MPMF Test fixture hardware design. For more details on MP tools, refer to the MP Tool User Guide in the MP tool release package.

6.1 Mass Production Tool

There are four tools for mass production:

- `isUpdate.exe` – to merge UI, DSP and Flash code to *.hex file.
- Mass Production Script Editor (MPSE) – to integrate the test condition and calibration level of test item to *.msf file for the Mass Production Board Level Test (MPBT) tool. Test items include RF and PMU.
- The Flash downloads hex file for Mass Production Multi-Flash (MPMF) tool is also merged by MPSE tool.
- Mass Production Board Level Test (MPBT) – to define the test environment and perform MP test.
- Mass Production Multi-Flash (MPMF) – to perform EEPROM and Flash download on multi-site.

**Note:** `isUpdate` tool is not included in the MP tool release package.

The following figure describes the MP tool execution flow:

1. Use `isUpdate` tool to merge GUI, DSP and Flash code to hex file.
2. Use MPSE tool to edit script file (*.msf) by defining the test condition, calibration level for MPBT tool and merge the Flash hex file for MPMF tool.
3. In production line, the MPMF tool and the test fixture include the dedicated *.msf file for Flash download.
4. MPBT tool and the test fixture include the dedicated *.msf file for MP test.

Figure 6-1. MP Tool Execution Flow

**Note:** The Flash code may be released by Microchip’s dedicated turnkey application code, or customer’s code generated by the SDK tool.

6.2 isUpdate tool

Perform the following steps to generate *.hex files for MPMF download purposes:

1. In isUpdate tool, browse and select the highlighted GUI, DSP and Flash code.
2. Click Rehex button to generate the *.hex file, which is used for MPMF.
6.3 MPSE Tool

Perform the following steps in the MPSE (MP SCRIPT EDITOR) window:

1. Select “Solution” as highlighted in the following figure and “RfinDevice” as ISSC VICTORIA.
2. Add 9850 in the “MP Test Item”.
3. Select the highlighted “Application Code Hex File Path” and fill in the “Checksum of Hex File” as 0F40.
4. Click Save for MPMF execution.
MPBT script:

1. Select “Solution” as highlighted in the following figure and “RfinDevice” as MT8852B.
2. Add the required test items. The test items include GPIO, PMU and RF test option.
6.4 MPBT Set-up Note

In the MPBT (MP BOARD LEVEL TEST) window, select RF Meter. The “RF CABLE LOSS” value of PL2 and PL0 should be obtained by the power calibration procedure, which is performed by the measured RF \( T_x \) power difference between conducted \( T_x \) power and MP RF \( T_x \) power test on test fixture.

**Note:** Refer to 8. Appendix B: IS2083BM DUT Test Jig Tx Power Compensation for more information.
### 6.5 MPBT DUT Test Board Design

The IS2083BM MPBT test includes the following items:

#### Table 6-1. IS2083BM MPBT Test Item Description

<table>
<thead>
<tr>
<th>Design Under Test</th>
<th>Test Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO</td>
<td>P32, P16, P26, P05, P00, P27, P37, P03, P07, P06, P01, P02, P23, DP, DM</td>
<td>GPIO open/short test</td>
</tr>
<tr>
<td>PMU</td>
<td>1V2, LDO31_VO, BK2_O_1V8, VCC_RF, BK1_O_1V5, BAT_IN, ADAP_IN</td>
<td>Power measurement and calibration</td>
</tr>
<tr>
<td>RF Test</td>
<td>RTX (RF test point on matching path)</td>
<td>1. Use RF test probe fixed on PCB, contact the RF test point and ground during test. 2. RF Antenna must be bypassed or shielded during test.</td>
</tr>
<tr>
<td>Audio</td>
<td>AOHPR, AOHPL, MIC_P, MIC_N, AIR, AIL</td>
<td>Analog Speaker Output, MIC Input and Aux Audio Input</td>
</tr>
<tr>
<td>Digital Audio Output</td>
<td>DR1, RFS1, SCLK1 and DT1</td>
<td>Digital Audio Output Interface</td>
</tr>
<tr>
<td>Digital Microphone Input</td>
<td>DMIC_CLK, DMIC_R, DMIC_L</td>
<td>Digital Audio Microphone Interface</td>
</tr>
<tr>
<td>LED</td>
<td>LED1 and LED2</td>
<td>LED1 (Blue) and LED2 (Red)</td>
</tr>
<tr>
<td>Mode Control</td>
<td>P3_4</td>
<td>Test Mode Control</td>
</tr>
</tbody>
</table>

The following figure illustrates the block diagram of DUT Test Board.
The following figure illustrates the IS2083BM MPBT Test Board circuit. The DUT socket connects all the test interface to include RF test point, PMU test points, audio input/output test points and the control interface.
The following figure illustrates MPBT Test Fixture that includes DUT test board PCB, socket, Victoria Board (AC102013) and I2S Adapter Board.
Figure 6-8. MPBT Test Fixture Connection Diagram

Note: AC102013 can be ordered from Microchip directly. If a digital audio test is required, contact the local FAE for the I2S adapter board circuit, BOM and Gerber file.

The following MPBT Test fixture includes DUT test board PCB, socket, Victoria Board (AC102013).
Figure 6-9. MPBT Test Fixture Example

Note: During testing, the antenna shield copper paper is used to minimize the RF power leakage to antenna path. The following figure shows the antenna shield copper area on DUT socket, which is used to minimize the RF power leakage to antenna during MPBT RF test. The RF test probe is placed on the DUT RF test point position.
6.6 **MPMF 1x4 Fixture Board Design**

The following figure shows the configure flow in MPMF Configuration window.

2. Select Test (IBDK) mode.
3. Configure the comport number.
4. Select the Log Directory.
5. Click **Apply** to finish the configuration.
6. In MPMF main page, click **RUN** to run the Flash download on the device.
The MPMF test tool can support up to two 1x4 test fixture, which means 8 DUT can execute Flash download at a time.
Figure 6-13. MPMF 1x4 Test Connection
6.7 IS2083BM DUT MPMF 1 to 4 Fixture Board

The board includes USB interface, 5V adapter, 3.3V power supply, USB to UART interface and the test mode controller circuit. The DUT socket is designed by users. The test points GND, P3_4, HCI_TX, HCI_RF, BAT_IN, ADAP_IN, SYS_PWR, VDD_IO, LED1 and LED2 must be connected from the socket for testing.

The following figure illustrates the IS2083BM DUT MPBT Fixture Board circuit.
Figure 6-16. IS2083BM DUT MPMF 1 to 4 Fixture Board Circuit Example - continued.
Figure 6-17. IS2083BM DUT MPMF 1 to 4 Fixture Board Circuit Example - continued.
Appendix A: Edgar III Circuit

Figure 7-1. Edgar III Circuit
8. **Appendix B: IS2083BM DUT Test Jig Tx Power Compensation**

This chapter describes how to find the RF cable loss value on the RF meter window of the IS2083BM MPBT tool. The cable loss value compensates the RF path loss between test fixture RF test point and the tester’s RF port.

Perform the following steps for conductive RF power measurement:

1. Prepare an IS2083BM DUT Board.
2. Remove antenna and place a RF conductive SMA connector on RF test point.
3. Set DUT in Test mode.
4. Connect DUT Board to UART converter and Windows PC via USB cable.
5. Connect SMA connector to RF tester, for example, Anritsu MT8852B.

![Figure 8-1. IS2083BM DUT RF Power Measurement Connection](image)

6. In the ISRT tool, set the following parameters:
   6.1. “Tx Modulation” as OFF (Continue Wave mode)
   6.2. “Channel” as CH38-2440 MHz
   6.3. “TX POWER TRIM Level” as PL0 and PL2 to measure the Tx power respectively.

7. Click **START** and then measure the TX power on MT8852B.
8. Record the measured power of PL0 and PL2 to TXPL0b and TXPL1b.

Perform the following steps for MPBT test fixture RF power measurement:

1. Place IS2083BM DUT on MPBT test fixture, connect interface to PC and RF Tester.
2. Use the Labtest tool on PC to power on test fixture and set Test mode.
   2.1. In “Power Control”, select Victoria V2.5.
   2.2. Click Connect.
   2.3. Select the parameters as highlighted.

3. In the ISRT tool, set the following parameters:
   3.1. “Tx Modulation” as OFF (Continue Wave mode)
   3.2. “Channel” as CH38-2440 MHz
   3.3. “TX POWER TRIM Level” as PL0 and PL2 to measure the Tx power respectively.

4. Click START and then measure the TX power on MT8852B.
5. Record the measured power of PL0 and PL2 TXPL0b and TXPL1b. For example, cable loss calculation of MPBT test fixture:

- Cable loss value of PF0 = TXPL0a - TXPL0b
- Cable loss value of PF2 = TXPL2a - TXPL2b
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