Introduction

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Most power LED drivers use a Switch Mode Power Supply (SMPS) design for their efficiency and small footprint. Nonetheless, most of these designs do not provide a mechanism for dimming, and those that do typically only provide linear current adjustment dimming. To provide stable color control, the LED string must be driven with Pulse-Width Modulated (PWM) constant current pulses, often incorporating a load switch to disconnect the LED string from the output of the driver during the off-time.

The problem with this approach is that most LED drivers in the market are just turning the SMPS on/off to achieve LED dimming. This method suffers from the problem of feedback loop saturation during the dimming off-time, caused when the active feedback loop has a working reference but no feedback signal. The result is a current overshoot when SMPS is turned back on. This causes component stress for both the SMPS and the LEDs, which shortens their life. A second issue is a slow discharge of the output capacitors, through the LEDs, during the dimming off-time. This results in LED color distortion at low brightness, producing a visible shift in the LED color temperature.

This application note describes a simple Dual-Channel SMPS LED driver with an on-chip dimming engine that alleviates both problems. In fact, the integration of the dimming engine into the SMPS control is such that higher dimming PWM rates are possible, making the design highly effective in high-end applications like LED backlights, automotive systems, medical systems, and especially image processing systems.

The driver accomplishes this by suspending the operation of both the SMPS PWM and the active feedback loop, during the off-time of the dimming PWM. Because both systems are suspended, the feedback loop filter saturation is prevented and output overshoot is avoided. The suspension also holds the loop at the nominal drive level, so when the load returns, the loop is prepared to deliver the necessary output current. This suspension is only possible due to the high level of connectivity between the Core Independent Peripherals (CIP) that make up both the SMPS LED driver and the dimming engine.

To demonstrate the operation of the SMPS driver and the dimming engine, a simple battery-powered Dual-Channel LED driver is implemented in this application note using both SMPS and dimming systems.

Note: This design demonstrates a low-power system (<250 mW). As a result, the design methodology presented has been simplified considerably to fit the scope of this document. Designers wishing to produce a full-power design (>1W) have to consult with a qualified SMPS design resource, such as one of Microchip’s FAEs specializing in SMPS design or a third party SMPS design house.

Design Specifications

- The power source for the Dual-Channel LED driver will be three AA alkaline batteries. 
  \[3.0 \text{V} < V_{\text{BATT}} < 4.5 \text{V}\]
- The output LED strings will be one string of three blue indicator LEDs, and one string of three white indicator LEDs. \[V_{\text{LED}} = 8.4 – 9.4 \text{V} @ 20 \text{mA}\]
• Both channels of the LED drive will be capable of independent dimming.
• An undervoltage automatic shutdown is included, which suspends operation below 3.0V.
• A user interface will be included to allow basic dimming control.
# Table of Contents

Introduction......................................................................................................................1

1. Hardware Design.......................................................................................................4  
   1.1. Power Converter Topology......................................................................................4  
   1.2. Component Selection.............................................................................................4  
   1.3. Modulator Design.................................................................................................9  
   1.4. Ramp Generator.....................................................................................................12  
   1.5. Loop Compensation.............................................................................................13  
   1.6. Voltage Reference...............................................................................................18  
   1.7. Dimming Engine...................................................................................................19  
   1.8. Shared Circuitry Between Driver Channels.........................................................20  
   1.9. Protection Circuitry.............................................................................................20  

2. Software Design......................................................................................................24  

3. Conclusions.............................................................................................................26  

4. Memory Usage........................................................................................................27  

5. Appendix..................................................................................................................28  
   5.1. Layout..................................................................................................................28  
   5.2. Schematic............................................................................................................29  

The Microchip Web Site................................................................................................32  
Customer Change Notification Service.........................................................................32  
Customer Support.........................................................................................................32  
Microchip Devices Code Protection Feature...................................................................32  
Legal Notice..................................................................................................................33  
Trademarks...................................................................................................................33  
Quality Management System Certified by DNV............................................................34  
Worldwide Sales and Service.........................................................................................35
1. **Hardware Design**

The hardware design of the driver system is broken into six sections: Power Converter Topology, Modulator Design, Ramp Generator, Loop Compensation, Voltage Reference and Protection Circuitry.

1.1 **Power Converter Topology**

This section of the application note covers the design of the Switch mode power converter, specifically, the selection of an appropriate topology and the selection of the inductor, capacitors, MOSFET, and Schottkey diode used in the design.

Because the output voltage is always greater than the supply voltage, a boost switching topology is used for the LED driver. The operating mode is Continuous Conduction Peak Current mode. The figure below shows the topology section of the design. Note that, instead of using the output voltage as the main loop feedback, the LED current is used. This puts the LED current under direct regulation for more consistent intensity.

**Figure 1-1. Boost Topology, Peak Current Mode**

1.2 **Component Selection**

1.2.1 **Duty Cycle**

In a boost topology, the duty cycle is a function of the LED forward voltage and the battery voltage (see the equation below).

**Equation 1-1.**

\[
D = 1 - \left( \frac{V_{BATT_{min}}}{V_{LED} + V_R} \right)
\]

Where:

- \(D\) = duty cycle
- \(V_{BATT_{min}}\) = minimum battery voltage (3.0V typical for alkaline batteries)
\( \eta = \) estimated efficiency of the conversion (80% estimate)

\( V_{\text{LED}} = \) forward voltage of D2 + D3 + D4 (8.4V blue, 9.4V white)

\( V_{R8} = \) voltage drop across the LED sense resistor R8 (0.44V typical)

- The maximum duty cycle for the blue LED chain is 73%
- The maximum duty cycle for the white LED chain is 76%

**Note:** Because the control is implemented as a peak current control and the duty cycle exceeds 50%, slope compensation is required to maintain stability in the current feedback loop.

- Duty cycle 73%-76%
- Slope compensation required

### 1.2.2 Inductor (L1)

Next, the inductor is selected based upon the LED and battery voltages, the switching frequency, and the estimated inductor ripple current. The following equations show the relationship.

**Equation 1-2.**

\[
L = \frac{V_{\text{BATTmin}}(V_{\text{LED}} - V_{\text{BATTmin}})}{(\Delta I_L)(F_{\text{SWX}})(V_{\text{LED}})}
\]

**Equation 1-3.**

\[
\Delta I_L = \left( K \right) \left( I_{\text{LED}} \right) \frac{V_{\text{LED}}}{V_{\text{BATTmin}}}
\]

Where:

- \( V_{\text{BATTmin}} = \) minimum battery voltage (3.0V typical for alkaline batteries)
- \( V_{\text{LED}} = \) forward voltage of D2 + D3 + D4 (8.4V blue, 9.4V white)
- \( \Delta I_L = \) inductor ripple current (typically .2x to .6x the output current)
- \( I_{\text{LED}} = \) LED forward voltage (20 mA)
- \( F_{\text{SWX}} = \) PWM switching frequency (300 kHz)
- \( K = \) scaling factor, typically between .2 and .4 (0.6 for this design)

A switching frequency of 300 kHz is selected to keep the inductor small. The scaling factor \( K \) has also been increased to reduce the required inductor. Higher values of \( K \) are not typically used because they denote higher ripple currents in the inductor and reduce the output current range for continuous conduction. This increases core losses in the inductor and ESR losses in the output capacitor. However, as this is a low-power design and the output current is fixed, a higher ripple current can be traded for a lower inductance value. The calculated inductance is 191 \( \mu \)H for blue and 198 \( \mu \)H for white. Though, as neither is a typical value, the next size up, 220 \( \mu \)H, is selected.

**Inductance for both blue and white LED driver L1 = 220 \( \mu \)H**

To complete the inductor selection, a maximum current specification is also needed. To calculate the maximum inductor current, **Equation 1-5** is used. Because **Equation 1-5** also requires \( \Delta I_L \), it must also be calculated using **Equation 1-4**.

**Equation 1-4.**

\[
\Delta I_L = \frac{(V_{\text{BATTmin}})(D)}{(F_{\text{SWX}})(L)}
\]
Equation 1-5.

\[ I_{SWX} = \frac{\Delta I_L}{2} + \frac{I_{LED}}{(1-D)} \]

Where:

\( V_{BATTmin} \) = minimum battery voltage (3.0V typical for alkaline batteries)

D = duty cycle

\( \Delta I_L \) = inductor ripple current

\( F_{SWX} \) = PWM switching frequency (300 kHz)

L = inductance

\( I_{LED} \) = LED forward voltage (20 mA)

\( I_{SWX} \) = peak MOSFET switching current

For this design, the maximum ripple current \( \Delta I_L \) is 25.6 mA for both blue and white LED strings, with the peak MOSFET switching current of 86 mA for the blue LED string and 96 mA for the white LED string.

- Peak switching current for the blue LED string is 86 mA
- Peak switching current for the white LED string is 96 mA

A Coilcraft LPS6235-224MRB inductor is chosen as the inductor for both drivers based on the above calculations. While the selection criteria are abbreviated in this low-power design, an actual full-power design would also have to consider the load profile, core material and related derating, saturation points (particularly important for the PWM dimming of the LED drivers), converter efficiency, and Q of the LC filter (created by the inductor and the SMPS output capacitor) to determine an acceptable DCR for the design.

Note that the current ratings of the selected inductor are higher than required by the above calculations. The extra range is needed to handle the brute force soft start strategy of the design. See the section 1.9 Protection Circuitry for further details.

<table>
<thead>
<tr>
<th>Part number</th>
<th>Inductance</th>
<th>DCR</th>
<th>( I_{SAT} )</th>
<th>( I_{RMS} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPS6235-224MRB</td>
<td>220</td>
<td>0.820</td>
<td>0.31</td>
<td>0.45</td>
</tr>
</tbody>
</table>

In a full-power design, the on resistance \( R_{DS(ON)} \) and the related conduction losses would also be a consideration, as would the gate capacitive and its resulting switching losses, as well as the thermal resistance between the MOSFET die and its package.

1.2.3 MOSFET (Q1)

The MOSFET, shown in Figure 1-1, has requirements that fit in both the Component Selection and Modulator Design sections. So, while the component selection aspects will be covered here, the actual selection will be made in the Modulator Design section. In keeping with the abbreviated design methodology used above, the selection criteria will be limited to drain-to-source breakdown voltage, continuous source current, and total gate charge (rise/fall times). Note that total gate charge will be covered in the Modulator Design section.

According to the design specifications, the largest forward voltage for the LED strings is 9.4V. Given that D1 will have a forward voltage of 0.5 – 1.0V, the highest voltage seen by the drain of the MOSFET will be between 9.9V and 10.4V. Therefore, the MOSFET selected must have a drain-to-source breakdown
voltage greater than 10.4V. For this design, the actual requirement will be 20V or greater, just to provide some margin.

According to Equation 1-4 and Equation 1-5, the peak current is 96 mA and the ripple current is 25.6 mA. The transistor must be able to handle both currents for selection. The pulse current specification for a typical MOSFET is generally higher than the DC current limit, so in this instance the maximum current specification of 96 mA or greater is used. For this design, a DC current specification of 300 mA or greater will be used to provide additional protection during start-up.

1.2.4 Diode (D1)
The diode selection is based on the forward voltage of D1, the average current through the diode, the power rating of the diode, and its reverse breakdown voltage. While the reverse breakdown voltage of the diode is easily specified based on Equation 1-7, determining the power rating of the diode is a little more challenging, as the forward voltage of the diode is a function of the current flowing through it and the die temperature. However, the loss in the diode can be approximated by assuming a 0.5V forward voltage, assuming an average diode current of 20 mA, and using Equation 1-6.

Equation 1-6.
\[ P = (V_{FOR})(I_{LED}) \]

Equation 1-7.
\[ V_{REV} = V_{LED} + V_{R8} \]

Where:
- \( P \) = average power dissipation
- \( V_{REV} \) = reverse breakdown voltage
- \( V_{LED} \) = forward voltage of D2 + D3 + D4 (8.4V blue, 9.4V white)
- \( V_{R8} \) = voltage drop across the LED sense resistor R8 (0.44V typical)

For this design, a diode rated for approximately 10 mW and a minimum of 9.84V is required. A BAT54 Schottky is selected as the cheapest alternative with the minimum required specifications.

<table>
<thead>
<tr>
<th>Part number</th>
<th>( I_{FOR} )</th>
<th>( V_{REV} )</th>
<th>( P_D )</th>
</tr>
</thead>
<tbody>
<tr>
<td>BAT54</td>
<td>200 mA</td>
<td>30V</td>
<td>200 mW</td>
</tr>
</tbody>
</table>

Note: The actual forward voltage for a BAT54, running at 20 mA, is 0.325V at 25°C, so the actual power loss in the diode is 6.5 mW.

In a full-power design, the diode capacitance would also be a consideration given the 300 kHz switching frequency of this converter.

1.2.5 Output Capacitor (C3)
To determine the size output capacitor, the dynamic resistance of the output LED must first be determined. This is found by drawing a line tangent to the IV curve of the LED and calculating the equivalent resistance (see Figure 1-2).
Once the dynamic resistance \( R_{\text{LED}} \) is known, the relationship between the output voltage ripple and the LED current ripple can be calculated (see Equation 1-8).

**Equation 1-8.**
\[
\Delta V_{\text{LED}} = (\Delta I_{\text{LEDmax}})(R_{\text{LED}})
\]

Where:
- \( \Delta V_{\text{LED}} \) = maximum output voltage ripple
- \( \Delta I_{\text{LEDmax}} \) = maximum LED current ripple (in this design, +/- 5% or 200 uA)
- \( R_{\text{LED}} \) = dynamic resistance of three LEDs (D2, D3, & D4) in series (24Ω)

From the above equation, the user can determine that the maximum output voltage ripple \( \Delta V_{\text{LED}} \) must be less than 4.8 mV. With this value, the size of the output capacitor and the maximum tolerable ESR for the output capacitor can be determined (see Equation 1-9 and Equation 1-10).

**Equation 1-9.**
\[
C_3 = \frac{(I_{\text{LED}})(D)}{(F_{\text{SWX}})(\Delta V_{\text{LED}})}
\]

Where:
- \( C_3 \) = output capacitance
- \( D \) = duty cycle (73%-76%)
- \( F_{\text{SWX}} \) = PWM switching frequency (300 kHz)
- \( I_{\text{LED}} \) = LED forward voltage (20 mA)
- \( \Delta V_{\text{LED}} \) = maximum output voltage ripple (4.8 mV)

The above equation shows that an output capacitance \( (C_3) \) of 11 uF is required. The maximum ESR of the capacitor is determined using the following equation.

**Equation 1-10.**
\[
R_{\text{ESR}} = \frac{\Delta V_{\text{LED}}}{F_{\text{SWX}}}
\]
Where:

\[ R_{ESR} = \text{maximum capacitor ESR} \]

\[ \Delta V_{\text{LED}} = \text{maximum output voltage ripple (4.8 mV)} \]

\[ I_{SWX} = \text{peak MOSFET switching current (96 mA)} \]

Given the result of Equation 1-10, the maximum output capacitor (C3) ESR (\( R_{ESR} \)) must be less than 50 mΩ. The ripple current, \( I_{SWX} \) (\( K = 0.6 \) from Equation 1-3), may also be considered when deciding on the type of output capacitor to be used. For a full-power design, a ripple current of 60% (\( K = 0.6 \)) would dictate the use of ceramic output capacitors to reduce the ESR switching current losses. For a low-power design, a tantalum capacitor with an ESR of 50 mΩ or less will meet the needs of the design. However, tantalum capacitors with an ESR of less than 50 mΩ are only available in 47 μF or larger capacitors, so the selection for the output capacitor is \( C3 = 47 \mu F, ESR \leq 50 \, \text{mΩ}, 25 \, \text{VDC} \).

### 1.2.6 Supply Capacitor (C2)

In a typical switching power supply design, the supply bypass capacitor is responsible for decoupling the converter from the battery output. This reduces the stress on the battery, as the input current is nearly double the output current for a 2x boost design. The supply bypass capacitor is also needed to supply enough start-up current when the battery is in its worst-case state (low discharge, high temperature). This is particularly important in PWM dimming applications where the load transitions are repeatedly between 0% and 100%.

However, one advantage of the boost is the nearly constant source current, so only a ripple current of 60% of the average current must be supplied by the input capacitor C2. Typically, two capacitors are used: one is a ceramic to supply nearly all the instantaneous ripple current, and the second a larger bulk capacitor to fix the output impedance of the batteries. In this design, the source ripple current is only 60% \( \times (2 \times (20 \, \text{mA output current})) \), or 24 mA. So, a capacitor like the output capacitor may be enough to provide both the required ripple current and protection for the on-board Alkaline battery. The original value for C3 was 11 μF, so a good value for C2 is a 10 μF tantalum capacitor with a low ESR: \( C2 = 10 \, \mu F, \text{low ESR, } 25 \, \text{V} \).

In summary, the topology and basic component selection is listed below:

- Boost topology
- Continuous Conduction Peak Current mode
- Duty Cycle 73%–76%, slope compensation required
- Inductor: LPS6235-224MRB, 220 μH

### 1.3 Modulator Design

The modulator consists of the PWM input to the topology section (Q1), a time base, and feedback from the current sense resistor R3. Together, they form a peak current control loop that accepts its control input from the Programmable Ramp Generator (PRG) (slope compensation).

**Note:** In the following sections, circuitry both inside and external to the microcontroller will be shown. The pin symbol in Figure 1-3 will be used to show the transition from internal to external circuitry.

**Figure 1-3. Pin Connection Symbol**
In general, resistors, capacitors, and inductors are external components, while op amps, timers, comparators, PWMs, CLCs, COGs, and DACs are internal components. All internal connections are made using the internal analog switches and digital multiplexers between the various peripherals. The peripheral to peripheral connections are made using the same SFRs that are used to configure the peripherals.

**Figure 1-4. Peak Current Control Modulator**

The PWM pulse driving MOSFET Q1 is generated by the Complementary Output Generator (COG) peripheral. The rising edge of the pulse is triggered by the rising edge of CCP2 (Capture, Compare, and PWM), configured as a PWM output. The falling edge of the PWM3’s output is used as a fail-safe end for the PWM pulse as well. The comparator (CMP) also provides a falling event based on when the current feedback from R3 rises above the output of the PRG (slope compensation) peripheral. Figure 1-4 shows examples of the typical operating waveforms for the modulator.

TMR2 is configured for the 300 kHz PWM period and PWM3 is configured to generate an 80% duty cycle. This drives the period of the system PWM and provides a maximum duty cycle limit for the modulator of 80%.
The output of the COG is then buffered by the transistor pair Q5A and Q5B, part number PBSS4240DPN. The transistors have a β of 250 minimum and a maximum current rating of over 1A, so the high-level output of the microcontroller’s GPIO fully saturates the transistor, minimizing the rise and fall time of the MOSFET gate voltage.

The MOSFET switch has several requirements:

1. Enough current rating to handle both the peak switching current (100 mA) and the reverse recovery current in the rectifier diode. The amount of reverse recovery current is dependent on: the current flowing through the diode when MOSFET is turned on, the ESR of the output capacitor, the $R_{DS(on)}$ of the MOSFET, its rise time and the reverse recovery time of the diode. This means that the reverse recovery current can actually be greater than the peak switching current, so, for this design, a current rating of at least 2x-3x the peak switching current is used for the minimum current specification.

2. A sufficient breakdown voltage to withstand the output voltage plus the forward voltage of the switching diode (9.4V).

3. A gate threshold voltage low enough to be switched by one of the microcontroller’s output pins, buffered by the BJT driver ($2.6V = V_{DDmin} - V_{satNPN}$).

4. Sufficient power dissipation to handle the required switching current.

Finding a MOSFET with a sufficient current and voltage specification is relatively simple. However, finding a part with a sufficiently low-gate voltage will require some additional math. For this design, the buffer driving the gate is an NPN-PNP transistor pair, see Figure 1-4.

An IRLML2502 MOSFET is chosen for its performance and low cost.

<table>
<thead>
<tr>
<th>Part number</th>
<th>$V_{DSS}$</th>
<th>$I_D$</th>
<th>$V_{GS(th)}$</th>
<th>$P_D$</th>
<th>$Q_G$</th>
<th>$R_{DS(on)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRLML2502</td>
<td>20V</td>
<td>3.4A</td>
<td>1.2V</td>
<td>0.8W</td>
<td>12 nC</td>
<td>45 mΩ</td>
</tr>
</tbody>
</table>

While the current capability (3.4A) is greater than required for the design, its low-gate charge (12 nC) and the low-gate threshold voltage, combined with the device’s low cost, make it a good choice for the design. The worst-case power dissipation is also less than 0.32 mW (see Equation 1-11), so the device is more than sufficiently robust.
Equation 1-11.
\[ P_{SWX} = I_{SWX}^2 \times R_{DS(on)} \times D \]

Where:
- \( P_{SWX} \) = switching loss 0.32 mW
- \( I_{SWX} \) = peak MOSFET switching current (96 mA)
- \( R_{DS(on)} \) = on resistance of MOSFET (45 mΩ)
- \( D \) = duty cycle (73%-76%)

Equation 1-12.
\[ P_{ON} = (I_{SWX} \times V_{LED} \times t_{ON}/2) \times F_{SWX} \]

Where:
- \( P_{ON} \) = power loss turning on MOSFET
- \( t_{ON} \) = turn-on time of MOSFET (use rise time of MOSFET or 1% of 1/300 kHz) (33 ns)
- \( P_{ON} = 4.56 \text{ mW} \)

Equation 1-13.
\[ P_{OFF} = (I_{SWX} \times V_{LED} \times t_{OFF}/2) \times F_{SWX} \]

Where:
- \( P_{OFF} \) = power loss turning off MOSFET
- \( t_{OFF} \) = turn-off time of MOSFET (use rise time of MOSFET or 2% of 1/300 kHz)
- \( P_{OFF} = 9.12 \text{ mW} \)

\[ P_{Dtotal} = P_{ON} + P_{OFF} + P_{SWX} = 4.56 \text{ mW} + 9.12 \text{ mW} + 0.32 \text{ mW} \]
\[ P_{Dtotal} = 14 \text{ mW} \]

Finally, R1 and C4 are chosen to prevent transients, generated by the PWM on the MOSFET gate, from prematurely terminating the pulse. The corner frequency is set at 1.5 MHz (to pass the fundamental frequency of 300 kHz and the second through fifth harmonic), so \( R1 = 330 \Omega \) and \( C4 = 330 \text{ pF} \).

1.4 Ramp Generator

The purpose of the ramp generator is to provide the necessary slope compensation to maintain stability in the current control loop. Because the duty cycle is more than 50%, the gain of the current loop must be reduced with increasing duty cycle to prevent a subharmonic oscillation. This is accomplished by generating a negative ramp on the output of the loop filter using the Programmable Ramp Generator (PRG) - see Figure 1-6.

To provide the synchronization with the PWM output, the trigger for PRG is generated from CCP2 in PWM mode, with a 30% duty cycle. The fall of CCP2 triggers the start of the downward ramp, and the fall of CCP1 (80%) triggers the end of the ramp. The specific ramp rate is determined as part of the loop compensation discussed in the next section.
1.5 Loop Compensation

The operational amplifier (op amp) in the loop compensation section of the design performs three functions: it subtracts the feedback voltage from the reference voltage, it supplies the necessary gain and phase correction to maintain loop stability, and it integrates small errors over time to minimize the output current offset error. The compensation circuit is shown in Figure 1-8.

The filter shown provides both a pole and a zero, as well as an integrator (pole at 0 Hz). The transfer function (versus frequency) is shown in Equation 1-14 and its plot is shown in Figure 1-7. The purpose of the integration term is to accumulate small DC errors and drive their correction. The purpose of the pole and zero is to provide a phase boost that will compensate for the gain of phase behavior of the topology section, as well as the 90-degree phase shift due to the integration term. When designed properly, the phase may cross 180 degrees well after the gain of the system has fallen below 0 dB, ensuring stability.

**Equation 1-14.**

\[
G_{CF}(s) = \frac{\omega_l \left(1 + \frac{s}{\omega_{CZ1}}\right)}{\frac{s}{1} + \frac{s}{\omega_{CP1}}}
\]

Where:

- \(G_{CF}(s)\) = complex gain of compensation network
- \(s = 2 \pi f\) (F = frequency)
- \(\omega_l\) = integrator gain \(\left(\frac{1}{R \cdot C \cdot g}\right)\)
- \(\omega_{CZ1}\) = compensation zero \(\left(\frac{1}{R \cdot C \cdot g}\right)\)
ω_{CP1} = compensation pole \left( \frac{1}{R \ \bar{R} \ \bar{C} \ \bar{Z}} \right)

Figure 1-7. Gain and Phase Plot of Loop Compensation Filter

To determine the value of the necessary pole and zero, as well as the slope compensation necessary for stability, the transfer function of the topology must first be determined. The equation below shows the control to output transfer function of a Continuous Conduction Peak Current mode boost SMPS.

Equation 1-15.

\[ F_p(s) = \frac{(1 - D) R_{load}}{2R3} \times \frac{(1 + \frac{s}{\omega_p})(1 - \frac{s}{\omega_{Z}})}{(1 + \frac{s}{\omega_{Z}})} \]

The dominant pole is located at: \( \omega_p = \frac{2}{R_1 x C_0} \)

Where:
\( \omega_p = \) dominant pole frequency in rad/s
\( R_L = \) load resistance \( V_{LED} / I_{OUT} \)
\( C_O = \) output capacitance

The power stage transfer function zero is determined by the output capacitor:
\[ \omega_z = \frac{1}{R_{esr} \times C_o} \]

Where:
\( \omega_z = \) ESR zero
\( R_{esr} = \) ESR of the output capacitor
\( C_o = \) value of the output capacitor

The right half plane zero is determined by the duty cycle, the load resistance and the inductor:
\[ \omega_{ZRLH} = \frac{R_L (1 - D)^2}{L} \]

Where:
\( \omega_{ZRLH} = \) right half plane zero
\( R_L = \) load resistance \( V_{LED} / I_{OUT} \)
\( D = \) duty cycle
\( L = \) inductance

The gain of the power stage transfer function is:
\[ Gain = \frac{(1 - D) R_L}{2 R_3} \]

Where:
\( Gain = \) power stage transfer function gain
\( R_3 = \) current sense resistor between MOSFET and ground (10Ω)

**Note:** If using the graphical method, gain may be expressed in dB.
\( G (dB) = 20 \log (Gain) \)

See the figure below for the transfer function of the power stage.
At this point in the design, the simplest solution is to determine the required compensation graphically. On log-log graph paper, first plot the power stage transfer function with the integrator gain and slope from Equation 1-14. Then slide the pole and zero of the compensation network up and down the slope until you get a crossover frequency with the needed phase margin (typically 45°).

Optimally, the crossover frequency has to be near the dimming frequency, which in turn has to be 100x the highest visible optical pulse frequency (typically 100-200 Hz), to suppress flicker in the LED. For this design, the 8-bit dimming PWM is generated by the switching PWM (300 kHz), so the full resolution dimming frequency is only 1.2 KHz. The crossover frequency was moved up to a higher frequency for faster loop response and smaller loop filter component values (see Figure 1-10).

Selecting the voltage crossover frequency needs to be adjusted to the dimming frequency and needs to be one magnitude above the current loop fx. This has to be at least one magnitude above the -20 dB point at the highest visible optical frequency (usually 100-200 Hz) to effectively prevent jitter.

So, to achieve a -20 dB suppression of visible flicker frequencies, the fx of the current loop needs to be at >2 kHz, which in return pushes the fx of the voltage loop to ~20 kHz.
Figure 1-10. Plot 2 Loop Transfer Function (Power Stage Compensation)

Placing the compensation zero at 1.86 kHz and the pole at 7.256 kHz produces a crossover frequency of 9.318 kHz and a phase margin of over 45°.

The component values required are:

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
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<td>1.2 nF</td>
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<tr>
<td>C6</td>
<td>8.2 nF</td>
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Given that the current sense resistor for the LED string is only 22Ω, the series resistance into the compensation network is increased to 54Ω: 22Ω from the current sense (R8), a 10Ω isolation resistance, and a 22Ω load resistor for the loop compensation input. See Figure 1-11 for the final configuration.
The final value for compensation of the boost driver is the slope compensation ramp for the PRG peripheral. Typically, this value is between 1x and 2x the discharge ramp of the inductor current. In this design, the ripple current in the inductor is given by the equation below.

**Equation 1-16.**

\[ \Delta I_L = \frac{V_{BATT min} \times D}{F_{SWX} \times L} \]

Where:

- \( V_{BATT min} \) = minimum battery voltage (3.0V typical for alkaline batteries)
- \( \Delta I_L \) = inductor ripple current
- \( F_{SWX} \) = PWM switching frequency (300 kHz)
- \( D \) = duty cycle (73%-76%)

\( \Delta I_L = 30 \text{ mA}, \) so the \( \Delta V \) across the current sense resistor is 0.3V. The discharge takes \((1-D) \times T_{SWX}\), or 800 ns, therefore the discharge ramp is \( 0.375 \text{ V}/\mu\text{s} \). The closest value for PRG is 0.4 \text{ V}/\mu\text{s}, so that is the value that was used.

### 1.6 Voltage Reference

The voltage reference on the input to the error amplifier/loop filter determines the steady state current through the LEDs by driving the boost such that the difference between the voltage reference and the feedback from the output is kept as close to zero as possible. From the initial specifications, the desired output current is 20 mA. To provide a sufficient feedback signal and minimize losses in the sense resistor, the output sense resistor is chosen to be 22Ω. This means the reference voltage is 0.44V. However, the Fixed Voltage Reference (FVR) can only do 1.024V, 2.048V and 4.096V, so a DAC peripheral is needed to scale the FVR for the 0.44V required. DAC1 is 10-bit, so generating the required reference is not difficult (see Figure 1-12).
1.7 Dimming Engine

Once the loop is stable and the output current is in regulation, the dimming engine can be added to the control loop. This involves three additions:

1. A switch that disables the SMPS output PWM during the dimming off-time, to suspend switching PWM operation during the dimming PWM is off-time.
2. A switch disconnecting the LEDs from the output capacitor during the dimming off-time, to prevent decreases in the capacitor charge.
3. A signal to disable the output of the op amp during the dimming off-time, to prevent increases in the feedback control due to the lack of the output current sense feedback.

The following figure shows the additional CIP circuitry required for the dimming engine.

Figure 1-13. Dimming Engine Additions
In the above figure, a new lower frequency dimming PWM is generated by TMR4 and PWM3. The dimming PWM is then used to tri-state the output of the OPA using the override control, disconnect the LEDs using Q2, and disable the COG rise event using the DSM peripheral. The clock for the dimming PWM comes from CCP2.

By clocking the dimming PWM from CCP2, the PWM is synchronized to the end of the switching PWM, preventing truncated switching PWM pulses.

The control of PWM3 is handled by software, and varying its duty cycle results in the PWM of the driver output.

1.8 Shared Circuitry Between Driver Channels

Due to common requirements in both drivers, a portion of the circuitry can be shared. This includes the voltage reference circuitry, the 30% and 80% time bases generated by TMR2/CCP1/CCP2, and the TMR4 which generates the timing for PWM3. The following figure shows the schematic for both drivers.

**Figure 1-14. Both LED Driver Channels**

1.9 Protection Circuitry

While several protection circuits can be put in place, only a limited number are actually implemented due to a shortage of peripherals in the device. The design currently includes the following protection circuitry:

1. Maximum duty cycle
2. Undervoltage lockout
4. Soft start (using maximum inductor current limit and dimming engine)

1.9.1 Maximum Duty Cycle
The duty cycle of the boost circuit is limited by the CCP1 PWM output. The rising edge of the CCP1 PWM triggers the turn-on of the MOSFET by triggering the rising event in COG. The falling event of COG, which triggers the turn-off of the MOSFET, is typically caused by the fall of the CMP output (see Figure 1-4). However, if the CMP output does not fall before the duty cycle reaches 80%, the falling edge of CCP1 PWM will trigger the fall through its connection to the COG falling event input. This limits the maximum duty cycle of the boost to 80%.

While 80% is not significantly larger than the 76% duty cycle predicted for the boost design in normal operation, it is sufficient for slow increases in the output current. Given the boost is designed to have a constant output current, fast increases in current are not expected, so a slow rise time will not be a problem.

1.9.2 Undervoltage Lockout
The undervoltage lockout is implemented using an unused comparator. The inverting input of the comparator is connected to the FVR (1.024V) and the noninverting input is connected to DAC3, which uses $V_{DD}$ as a reference. The output of the comparator is connected to a shutdown input of the COGs for both channels. DAC is then configured to provide 1.024V, when $V_{DD} = 3.0V$ (see figure below).

Figure 1-15. Undervoltage Lockout Protection Circuit

Under normal operation ($V_{DD} > 3.0V$), the boost behaves normally and both COGs produce PWM drives for their respective MOSFETs. When $V_{DD}$ falls below 3.0V, the output of CMP2 falls, and both COGs are forced into shutdown and they stop PWM outputs. Both COGs are configured to require software clearing of the shutdown and the software deliberately does not include code to clear the shutdown event. So, it takes a power cycle to clear the shutdown and restart both boosts. The user has to replace the batteries during a power-down to prevent a repeat of the undervoltage lockout.
1.9.3 Maximum Inductor Current Limit

In a traditional switching mode power supply controller, the inductor current is limited by a series resistor and a voltage clamp on the output of the loop compensation op amp (see Figure 1-16). Another option is to connect a second comparator to the current feedback, with a DAC on the noninverting input and the output connected to a second COG falling event input (see Figure 1-17).

Figure 1-16. Voltage Clamp Circuit

![Figure 1-16. Voltage Clamp Circuit](image1)

Figure 1-17. Comparator Based Current Limit

![Figure 1-17. Comparator Based Current Limit](image2)

1. The connection between the OPA output and the PRG input is internal and does not allow the placement of a series resistor and a voltage clamp in the signal path.

2. Because the slope compensation (PRG) is between the output of the OPA and the input of the comparator, a second comparator will not work either, as the output of the DAC would require a negative slope compensation ramp, similar to the output of the OPA.

To accommodate these limitations, an alternative method was used, which involves the MOSFET driver and the current sense resistor R3 (10Ω). In the Figure 1-18, you can see that the output buffer for the MOSFET transistor is a BJT transistor pair. This limits the drive voltage of the MOSFET to $V_{DD} - 1.4V$. A 0.7V of the drop is due to the output driver of the microcontroller, and another 0.7V drop is due to the base-emitter junction in the transistor. In addition, when the inductor is charging, the voltage across the sense resistor R3 is proportional to the inductor current. Finally, the gate-source voltage of the MOSFET is approximately 1.2V for saturation of the MOSFET.
This means that if the battery voltage is the full 4.5V, the maximum current that the MOSFET can pass, and remain in saturation, is about 190 mA. When \( V_{DD} \) is less than 3.5V, this drops to 90 mA. So, as the inductor current climbs above 190 mA, the MOSFET gate voltage is reduced and the on resistance of the MOSFET begins to climb. This slows the rise of the inductor current and eventually shuts off the MOSFET. An inductor is then chosen with a saturation current well above the 190 mA (450 mA from the IRMS inductor specification). Even if the MOSFET were to short, the maximum current in the inductor is still limited to less than 450 mA due to R3, the output resistance of the battery, and the DCR of the inductor.

Finally, note resistor R2 holds the MOSFET off during start-up. Once the peripherals have been initialized, the PWM output can easily overdrive the pull-down resistor and its influence is removed.

### 1.9.4 Soft Start

When the boost initially turns on, there is a significant difference between the feedback voltage and the voltage reference. This drives the output of the compensation filter to its maximum level and would result in an overcurrent of the inductor. A compounding factor is that the discharge voltage is initially very low, resulting in a longer discharge time for the inductor. The soft start is the process of slowly powering up the boost converter to prevent this problem, and is accomplished by a combination of two features: the dimming engine and the current limit from the previous section.

When the circuit initializes, the dimming engine limits one channel to 50%, and the other to 0%. This provides a periodic longer discharge period for the inductor that allows it to fully discharge its field. As the dimming engine begins ramping up both dimming levels, both converters will be operating for a larger percentage of the time and the output rises accordingly. In addition, the current limit described above also limits the maximum current to which the inductor can charge. Finally, the LED load has a steep knee (see Figure 1-2), so the load during the software start will be significantly less than when the LEDs are in full conduction. This will allow the boost to reach regulation faster than a purely resistive load would allow.

As an alternative, the DAC in the voltage reference could be ramped up from 0V as well to slow the soft start function. However, due to the relatively low reference voltage, there is not a great deal of range available to implement this form of soft start.
2. **Software Design**

The software for the dual LED drive is relatively simple as most of the drive and dimming functions are completely autonomous. The only functions that the software performs are the initial configuration of the peripherals, providing the dual ramping functions for the Autonomous mode, and decoding key presses for the Manual mode. The flow chart of the firmware is shown in the following figure.

**Figure 2-1. Software Flow Chart**
The Configure Peripherals section is generated by the MPLAB® Code Configurator (MCC), based on the selection and configuration information entered. The Preload Variable section preloads all system variables including state machine variables, counters and data buffers. The Start Peripheral section is required to initiate operation for those peripherals that have a GO/STOP function such as the PRG.

The main loop consists of four blocks. The first, Gather Inputs, reads the button inputs and debounces them to generate a stable button press input. The Decide Actions section contains the system command decoder state machine. It accepts the button press input and either changes the system mode, or adjusts the channel intensity based on its current state. The Do Output section takes the decisions from the previous section and makes the appropriate changes to the dimming PWM peripheral’s duty cycle. Finally, the Timer section holds the loop until TMR0 rolls over. This regulates the speed of execution in the system and provides predictable/repeatable timing for the decision state machine.

The state machine in the Decide Actions section has three states: Test, Fade and Man. The Test mode is leftover from the initial testing of the driver circuitry. It is left in the code as a place holder for testing the DC operation of the drivers. The Fade mode handles the automatic ramp up/down mode of operation for the drivers. The ramp is controlled by the DIM1 and DIM2 variables that are incremented or decremented on each call of the state machine. The final state, Man, is the Manual Control mode in which a press of either the CHAN1 or CHAN2 buttons will result in an increase of DIM1 or DIM2, by 10 hex.
3. Conclusions

Included in the design files is a copy of the full test report for the design, which contains the efficiency, thermal and fault test data. The design file also contains the full project directory for the project, including the MCC configuration file with the complete setup of all the CIPs used for both channels of the driver.
### Memory Usage

Table 4-1. Memory

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5. Appendix

5.1 Layout

Figure 5-1.
5.2 Schematic

Figure 5-2. Dual Independent LED Schematic
Figure 5-3. Dual-Channel Power Supply 1 Schematic
Figure 5-4. Dual-Channel Power Supply 2 Schematic
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