EMI Prevention in PCB Design of Atmel ARM-based Microcontrollers

ARM-based Embedded MPU

Scope

Electronic products sold in Europe or in the United States must be EMC (Electromagnetic Compatibility) compliant. They require the CE or FCC certification, respectively. One of the EMC certification requirement is to pass the Electromagnetic Interference (EMI) test. Many products have EMI issues after the PCB design phase, which limits the improvement possibilities.

Consequently, before designing the PCB, it is very important to do some research on EMI prevention.

EMI includes conducted emission, radiated emission and disturbances on power and communication lines. This application note introduces some general methods for preventing Radiated Emission in the PCB board design of Atmel® ARM®-based microcontrollers.

Reference Documents

<table>
<thead>
<tr>
<th>Type</th>
<th>Reference Documentation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Datasheet</td>
<td>SAM9Gxx Series Datasheets</td>
</tr>
<tr>
<td></td>
<td>SAM5D3 Series Datasheet</td>
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1. EMI Fundamentals

1.1 EMI Concept

EMC (Electromagnetic Compatibility) mainly consists of EMI (Electromagnetic Interference) and EMS (Electromagnetic Susceptibility).

EMI includes conducted emission and radiated emission, as shown in Figure 1-1.

1.2 SI and Transmission Lines

Signal integrity (SI) and transmission lines have an impact on EMI.

1.2.1 SI

Ensuring a good Signal Integrity across a transmission medium (cable, PCB trace..) means being able to transmit the signal without altering its content. In particular, for digital signals, this means to have:

- clean and fast transitions
- stable and correct logic levels
- precise placement in time

Signal integrity problems increase with fast transients, which are directly linked with high-frequency switching signals. Throughout this document, the term "high frequency" will be used to refer to these fast transients, and not to the frequency of the signal itself (e.g. a 100-kHz signal with sub-nanoseconds edges may create EMI issues in a system).

1.2.2 Transmission Line

At low frequencies, a metal trace may be considered as a simple resistor.

When the frequency increases, the trace starts to act like a capacitor. At highest frequencies, the trace inductance plays an important role.

At high frequencies, components and PCB traces are no longer ideal. They have parasitic parameters and the traces behave as transmission lines, as shown in Figure 1-2.
The diagram on the left illustrates the real model of a trace \textit{(RLGC wire representation)}. In this diagram:

\[ Z_0 = \left(\frac{R + \frac{L_s}{G + C_s}}{2}\right)^{1/2} \]

The diagram on the right is the first-order approximation model for an ideal transmission line \textit{(First order approximation wire representation)}. In this diagram:

\[ Z_0 = \left(\frac{L}{C}\right)^{1/2} \]

The impedance \( Z_0 \) (known as "intrinsic impedance") of the transmission line is a key parameter to achieve a good level of signal integrity.

\subsection*{1.2.3 EMI Caused by Impedance Mismatch}

Impedance mismatch may cause EMI problems.

There are two main types of impedance mismatch on a transmission line:

- The transmitter output impedance \( Z_S \) does not match the line impedance \( Z_0 \)
  
  Reflection coefficient: \( \frac{Z_S - Z_0}{Z_S + Z_0} \)

- The receiver or load impedance \( Z_L \) does not match the line impedance \( Z_0 \)
  
  Reflection coefficient: \( \frac{Z_L - Z_0}{Z_L + Z_0} \)

For both mismatch types, the transmitted signal is not fully absorbed on the receiver side, and the excess energy is reflected back in the opposite direction. The same reflection occurs on the transmitter side and then, the reflection phenomenon bounces back and forth till the energy declines. This phenomenon is also called "ringing".

Any impedance mismatch along the transmission line produces signal reflection.

An analysis of either the transmitter or the receiver side shows ringing, especially near the rising or falling edges, which means that the signal has an SI issue. This ringing usually involves high-frequency components emitting radiation along the current loop. This radiation causes EMI issues.
To decrease the reflection phenomenon, the line impedance ($Z_0$) should match both the transmitter output impedance ($Z_S$) and the load impedance ($Z_L$). Several methods are available to reduce this phenomenon, including the use of serial termination or parallel termination.

1.3 CE/FCC Radiated Emission Test Method

For details on radiated emissions (30 MHz to 1G, >1G), please refer to the EN55022:2010 or CISPR 22 standards ("Information technology equipment - Radio disturbance characteristics - Limits and methods of measurement"). Table 1-1 and Table 1-2 list the radiated disturbance limits for frequency ranges from 30 MHz to 1 GHz.

<table>
<thead>
<tr>
<th>Table 1-1. Limits for Radiated Disturbance of Class A (Commercial) ITE at a Measuring Distance of 10 m</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Quasi-peak limits in dB (μV/m)</strong></td>
</tr>
<tr>
<td>30 to 230 MHz frequency range</td>
</tr>
<tr>
<td>230 to 1000 MHz frequency range</td>
</tr>
</tbody>
</table>

Notes: 1. The lower limit must apply at the transition frequency. 2. Additional provisions may be required for cases where interference occurs.

<table>
<thead>
<tr>
<th>Table 1-2. Limits for Radiated Disturbance of Class B (Industrial) ITE at a Measuring Distance of 10 m</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Quasi-peak limits in dB (μV/m)</strong></td>
</tr>
<tr>
<td>30 to 230 MHz frequency range</td>
</tr>
<tr>
<td>230 to 1000 MHz frequency range</td>
</tr>
</tbody>
</table>

Notes: 1. The lower limit must apply at the transition frequency. 2. Additional provisions may be required for cases where interference occurs.

2. General EMI Prevention Methods

2.1 PCB Layout Recommendations

2.1.1 PCB Placement

For a good PCB placement, it is recommended to:

- Assign different areas for different circuit types (power circuit, low-frequency digital circuit, high-frequency digital circuit, analog circuit, etc).
- Place the components so as to ensure short ground return paths: the ground current of noisy components should be kept on a short path and placed away from sensitive components (analog circuits or clock generation circuits). For example, a switching power supply component must be placed close to the input connector and not on the opposite side of the board.
- Systematically add a decoupling capacitor to power/ground pairs of integrated circuits. In addition to the large capacitors (10 nF to 1 μF), it is highly recommended to use low-impedance decoupling capacitors (such as 100-pF capacitors) at high frequencies.
- Maintain a distance between the sensitive components (such as crystal and oscillator) and the other components or disturbance signals.
2.1.2 Large GND Reference Plane

Some recommendations related to the GND reference plane are provided in the following list:

- The PCB should include a large and unbroken ground plane. Ideally, one layer of the PCB should be totally filled with ground.
- As many vias as possible should be added to connect this ground plane to the ground islands on the other layers of the board.
- The separation between noisy and sensitive parts of the circuit must be performed by a good placement of the components: as the current always flows in the least resistive/inductive path, an adequate placement of the components can bias the ground-current path that each component follows and thus minimize the shared paths. When this strategy is not possible or not effective enough, two distinct ground planes can be drawn and star connected either with multiple vias or with ferrites. When adopting this strategy, designers must be aware that two adjacent ground planes drawn on a single PCB layer and separated by a gap behave like a dipole antenna during EMC tests.

2.1.3 PCB Routing

For high-speed signals, the trace length must be as short as possible, and the distance between the center of two adjacent wires must be more than three times the wire width (called ‘3W rule’) to prevent crosstalk.

In some applications (such as DDR data lines), wires require controlled lengths.

To achieve this, snake routing \(^1\) can be used. In this case, the distance between the parallel sections of the bus must be higher than 4H (H being the distance between the wire plane and the reference plane).

The following list provides some other guidelines:

- **Recommended procedures**
  - Routing 45° corners
  - Shielding oscillator nets and pads with a ground ring.
  - Routing fast differential signals as close as possible to each other with identical trace lengths (e.g. DDR/DDR2 clocks, USB bus).
  - Minimizing vias and layer changes on fast signals (route them first).

- **Procedures to avoid:**
  - Routing 90° corners (this creates ringing and EMI).
  - Making unnecessary layer changes, especially on fast signals (route them first).
  - Having stubs, such as unconnected tracks. Also beware of disconnected jumpers and not populated components. These stubs function as antennas and may create/receive EMI.
  - Implementing ground and power loops (when traces are used for VCC/GND connections).
  - Splitting the ground plane.
  - Routing high-speed signal over a slot in the ground plane (this creates EMI).

2.1.4 PCB Stack

For high-frequency boards, it is necessary to control the impedance. Consequently, the PCB stack must be adjusted to meet the impedance matching requirements including: thickness of the metal and dielectric layer, wire width, etc.

Some software tools can be used to calculate the impedance. The parameters of the PCB can also be factory-adjusted to meet the customer’s impedance matching requirements.

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\(^1\) Deliberately meandering a track to lengthen its path.
Figure 2-1. Impedance Calculation Tool Output Example
2.2 Board Simulation Using IBIS Model

Many CAD tools are available to perform PCB simulations: Cadence’s Spectra, Altium, Hyperlynx, etc.

Figure 2-2 shows the Hyperlynx simulation tool.

Figure 2-2. PCB trace simulation example

To perform the simulation, the following input is required:

- PCB stacking details and related information
- IBIS model of transmitters and receiver(s)

By setting the correct device frequency, and then running simulation, it is possible to get the signal wave and spectrum in order to determine the prominent frequency rays.
2.3 EMI Suppression Components

Several components are available to reduce the EMI:

- Decoupling capacitors or filter for VCC
- Resistors or ferrite beads
- Spread-spectrum oscillators

2.3.1 Decoupling Capacitor or Filter for VCC

When used on each active device, the bypass or decoupling capacitors must be connected to the power supply and be as close as possible to the device.

An LC filter can also be added at the beginning of every power line branch for each high-current device, as shown in Figure 2-3.

Figure 2-3. LC Filtering scheme

2.3.2 Resistors or Ferrite Beads

Fast transients contain several frequency components. The number of high-frequency components is decreased by limiting the slew rate of fast switching signals.

Resistors of ferrite beads can also be added in series with the signal trace to suppress some special frequency components.
2.3.3 Spread-spectrum Oscillators

In some cases, the spread spectrum oscillators are used to replace quartz oscillators and help the board pass the EMI tests without making any board changes. Figure 2-4 shows the spectrum difference between conventional clock and spread-spectrum oscillator.

Figure 2-4. Spectrum of Oscillator

The following list provides some features of the “Sitime high-performance series sit9001” example:

- Down spread type (-0.5%, -1%, -2%)
- Center spread type (±0.25%, ±0.5%, ±1%)
- Cycle-to-cycle jitter: 29 ps
- Dramatic EMI reduction (up to -16 dB)
- No need for crystal or load capacitors

In applications based on Atmel ARM-based microcontrollers, users can set the MPU in bypass mode (clock signal directly input) when using this type of oscillator externally.
3. Parallel IO Drive Impedance in Atmel ARM-based Microcontrollers

3.1 PIO Drive Capability Adjustment

The External Bus Interface (EBI) is designed to transfer data between several external devices and the embedded Memory Controller in an ARM-based device.

The EBI I/O Drive can be configured by software: 0 = High drive (default), 1 = Low drive. Low drive reduces overshoots.

For other GPIOs or peripherals, three types of drive capabilities are usually available: Low Drive, Medium Drive and High Drive.

More generally, using lower drive helps reduce SI problems at the expense of slower transients. Since steep transients must often be avoided, a simple system analysis and a customized tuning of the drive of the different IOs can greatly reduce SI problems.

The following PIO_DRIVER1 register description is extracted from the Atmel SAM9G15 datasheet.

PIO I/O Drive Register 1

Name: PIO_DRIVER1
Address: 0xFFFFF514 (PIOA), 0xFFFFF714 (PIOB), 0xFFFFF914 (PIOC), 0xFFFFFB14 (PIOD)
Access: Read-write
Reset: 0x0

<table>
<thead>
<tr>
<th>Value</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>HI_DRIVE</td>
<td>High drive</td>
</tr>
<tr>
<td>1</td>
<td>ME_DRIVE</td>
<td>Medium drive</td>
</tr>
<tr>
<td>2</td>
<td>LO_DRIVE</td>
<td>Low drive</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

- LINEx [x=0..15]: Drive of PIO Line x
3.2 DDR2 Signals in Atmel ARM-based Microcontrollers

In some Atmel ARM-based microcontrollers such as the SAMA5D3 series, the DDR2 controller has ODT (On-die Termination), which can be used to make the device output impedance match the PCB trace’s impedance.

The output drive impedance value can be changed by programming “RDIV” in the “MPDDRC I/O Calibration Register”:

This value is given in the following table:

<table>
<thead>
<tr>
<th>Value</th>
<th>Name</th>
<th>Description</th>
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<tbody>
<tr>
<td>1</td>
<td>RZQ_34</td>
<td>LPDDR2 RZQ = 34.3 ohms, DDR2/LPDDR1: Not applicable</td>
</tr>
<tr>
<td>2</td>
<td>RZQ_40_RZQ_33_3</td>
<td>LPDDR2: RZQ = 40 ohms, DDR2/LPDDR1: RZQ = 33.3 ohms</td>
</tr>
<tr>
<td>3</td>
<td>RZQ_48_RZQ_40</td>
<td>LPDDR2: RZQ = 48 ohms, DDR2/LPDDR1: RZQ = 40 ohms</td>
</tr>
<tr>
<td>4</td>
<td>RZQ_60_RZQ_50</td>
<td>LPDDR2: RZQ = 60 ohms, DDR2/LPDDR1: RZQ = 50 ohms</td>
</tr>
<tr>
<td>6</td>
<td>RZQ_80_RZQ_66_7</td>
<td>LPDDR2: RZQ = 80 ohms, DDR2/LPDDR1: RZQ = 66.7 ohms</td>
</tr>
<tr>
<td>7</td>
<td>RZQ_120_RZQ_100</td>
<td>LPDDR2: RZQ = 120 ohms, DDR2/LPDDR1: RZQ = 100 ohms</td>
</tr>
</tbody>
</table>
4. Conclusion

EMI problems are frequent in most electronic products, especially in the case of high-frequency switching signals. This application note provides some general methods to reduce EMIs and help hardware designers solve EMI issues. These solutions range from the pre-manufacturing PCB simulation and line adaptation by hardware, to the post-manufacturing usage of configurable features of the Atmel ARM-based microcontrollers that allow flexible line adaptation and signal shaping by software.
5. Revision History

Table 5-1. EMI Prevention in PCB Design of Atmel ARM-based Microcontrollers Rev. 11236A 09-Jan-14

<table>
<thead>
<tr>
<th>Doc. Rev</th>
<th>Changes</th>
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<tr>
<td>11236A</td>
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