INTRODUCTION

This application note is intended to present a method for intelligent cable compensation. The system presented is capable of measuring the resistance and capacitance of the input stage and compensating accordingly, to ensure stable power delivery over thin, long wires. Although the application note focuses on low-voltage USB-compliant systems, the architecture can be implemented on virtually any system that meets specific criteria.

DESCRIPTION

Power delivery is a very important aspect to be considered in many applications that require high currents that are delivered through long wires. The resistance of the wires and connectors can limit the maximum delivered power in the Device Under Testing (DUT). In order for this loss of power to be compensated, there must be an active mechanism that is able to sense the voltage drop and compensate accordingly. The four-wire measurement technique can be used with very good performance, but this would introduce the disadvantage of modifying the existing cabling and connector interfaces.

Another approach could be a communication mechanism that sends information about the power requirements of the DUT to the power regulation board, which in turn would raise or lower the output voltage. This kind of mechanism offers good performance at the cost of increased complexity both in the DUT and in the power regulation board.

The method that will be presented in the application note is the indirect measurement of cable and connector resistance, without the need to disconnect cable from the setup. This mechanism provides the necessary information for compensation without any modification to the DUT and without any supplementary wires.

After the resistance is known, the power regulation module can compensate the voltage drop of the wires by combining information of the resistance and the input current of the device. An advantage of continuous monitoring of the current is that the power profile of the device can be made and later analyzed, and overcurrent protection can be implemented with relative simplicity.

The concept was tested on an an evaluation board, which is detailed in the Proof of Concept Board chapter. The input range of the board is very large (6 - 16V) and the output is set to 5V (5.5V maximum in order to preserve USB compatibility), therefore up to 0.5V can be compensated. The voltage compensation limit can be programmed in the PIC® microcontroller (MCU) according to the target application and is only inherently limited by the maximum output voltage achieved by the MIC24045.

REFERENCES

- MIC24045 Product Details
- MCP6N16 Product Details
- MCP1754ST Product Details
- MCP6021 Product Details
- PAC1710 Product Details
- PIC16F1509 Product Details
ARCHITECTURE

In order to compensate for voltage drop, the resistance of the wires must be known. The resistance of the wires can be measured without any external intervention only if the model of the system is known or can be approximated. The DUT can range from a simple resistive load to a more complex system, like a smartphone. In general, a load behaves purely resistive when the input voltage is <1V because the input power stage has not yet started to switch. The connection cable has an inductance and a resistance that on the one hand will limit high frequency content and on the other hand will limit the DC current. The input stage of the DUT consists of a capacitor with its associated ESR resistance and a leakage resistor that models load at low input voltage <1V. For compensation of voltage drop across the wire, the cable resistance must be calculated.

FIGURE 1: Cable Compensation Architecture.

In order to calculate the \( R_{\text{WIRE}} \) resistance, several stimuli must be applied to the load through the wire, and the response must be measured. It is preferred that the equations used to solve for the \( R_{\text{WIRE}} \) parameter are as linear as possible, to avoid complex data computation on the PIC MCU and reduce numerical errors. Another requirement is that all the stimuli applied must have a low-frequency spectrum, in order to minimize the impact of the reactance of the cable and to ensure that high-frequency spikes in the wires caused by switching do not affect the samples. The PIC MCU used in the project has a theoretical maximum sampling rate of around 56 kHz, however the actual sampling rate was chosen to be much lower in order for the input capacitor of the PIC MCU to further smooth the samples.

In theory, if the value of the input capacitor could be priorly measured and the \( R_{\text{LEAKAGE}} \) resistance known, it would be trivial to measure the resistance of the wires by simply charging and then discharging the capacitor by the regulation board. The RC time constant could be calculated and if \( C \) were to be known, the \( R_{\text{WIRE}} \) could be calculated. However, the input capacitance of the load is not known prior to the measurement, therefore it must be first determined by the application. To do so, the MIC24045 is programmed at 0.64V and turned on. The input capacitor at the DUT is charged, according to the capacitor voltage-current relationship, shown in Equation 1. The regulated voltage is thus chosen, that it would be insufficient for active components to turn on.

\[
i(t) = C \frac{dV}{dt}
\]

Sampling the instantaneous current and voltage through a capacitor would require a very large bandwidth on the sampling system side, therefore this approach is not suitable. Equation 1 can be integrated resulting in Equation 2; therefore the sampling of the integral could be done anytime. Furthermore, the capacitor potential at \( t = \infty \) is not required to be measured, because it would be equal to \( V_{\text{IN}} (0.64V) \).

\[
v(t) = \frac{1}{C} \int_{0}^{t} i_C(t) dt
\]

Equation 2 is trivial to compute if the integral term is solved in hardware using an integrating OPAMP. The voltage at \( t = \infty \) is also known, thus the capacitance can be calculated using just one sample of the ADC. The main problem is that the equation holds at a time that is...
infinite; therefore impossible to obtain in practice. The solution of the problem is the continuous monitoring of the integral term that will remain constant after complete charging of the capacitor, supposing that the leakage resistance is infinite. In practice, a very low threshold would be set.

Once the value of the capacitor is obtained, the resistance can be calculated using Equation 3.

**EQUATION 3: RESISTANCE FORMULA**

\[ v_c = v_s \cdot e^{-t/RC} \]

Where:
- \( R \) = wire resistance
- \( C \) = input capacitor of target DUT power stage
- \( V_C \) = voltage across the capacitor at time \( t \)
- \( V_S \) = voltage across the capacitor at time 0
- \( RC \) = time constant of the system

By solving the \( R \), Equation 4 is obtained.

**EQUATION 4: WIRE RESISTANCE**

\[ R = \frac{-t}{C \ln \frac{V_c}{V_s}} \]

Once the resistance is calculated, the voltage drop on the wire can be compensated dynamically using a current sensor and solving for the voltage drop using Ohm’s law, then lowering or raising the supply voltage accordingly.

### IMPLEMENTATION

#### Overall Architecture

The overall system architecture (Figure 1) is composed of:

a) A MIC24045 I^2C controllable buck power supply block.

b) A current integrator block used to determine the capacitor.

c) A PAC1710 I^2C addressable current and power sensor.

-d) A PIC16F1509 MCU for determination of wire resistance and active compensation of voltage drop.

e) Several MOSFETS used to interconnect different blocks.

f) An LDO that supplies the 5V rail used by the PIC microcontroller and the operational amplifiers.

#### Regulator

The power regulation board can be supplied from a 9 - 16V DC power supply. The output voltage is regulated using MIC24045. The MIC24045 is an I^2C programmable, high-efficiency, wide input range, 5A synchronous step-down regulator. The MIC24045 is perfectly suited for multiple voltage rail application environments, typically found in computing and telecommunication systems. In the MIC24045 various parameters can be programmed via I^2C such as output voltage, switching frequency, soft-start slope, margining, current limit values and start-up delays. The wide switching frequency adjustment range, valley current-mode control technique, high-performance error amplifier and external compensation allow for the best trade-offs between high efficiency and the smallest possible solution size. The internal architecture of MIC24045 is presented below in Figure 2.

The EN and I^2C pins are tied to the microcontroller.

The maximum output voltage of the MIC24045 is 5.25V, 250 mV lower than the maximum needed output voltage. To achieve higher output voltages, the OUTSNS pin was fitted with a resistive divider that feeds into the regulator a voltage equal to 0.954 * \( V_{OUT} \), raising the maximum output voltage to 5.5V. The schematic used for the regulator block is presented in Figure 3.
FIGURE 2: MIC24045 Block Diagram.

FIGURE 3: MIC24045 Regulator Block.
For this application, a PIC16F1509 was chosen. Its main strengths lie in the eXtreme Low-Power(XLP) technology, having an operating current of 30 \( \mu \text{A/MHz} \) @1.8V. The device features an internal oscillator that can be selected by software to run between 31 kHz and 16 MHz. The program memory is 8 KWords and the data memory is 512 Bytes long. The ADC features 12 external channels and 10-bit resolution crucial for accurate sampling in this project. The device also features 28-bit timers that are used for time measurements. The pin function is presented in Table 1.

### TABLE 1: PIC16F1509

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Function</th>
<th>Direction</th>
<th>Active</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V_DD</td>
<td>+5V supply rail</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>2</td>
<td>RA5</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>3</td>
<td>RA4</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>4</td>
<td>MCLR</td>
<td>MCLR programming pin</td>
<td>INPUT</td>
<td>—</td>
</tr>
<tr>
<td>5</td>
<td>RC5</td>
<td>Q1 Gate signal-current integrator enable</td>
<td>OUTPUT</td>
<td>HIGH</td>
</tr>
<tr>
<td>6</td>
<td>RC4</td>
<td>Q4 Gate signal-enable MIC24045</td>
<td>OUTPUT</td>
<td>HIGH</td>
</tr>
<tr>
<td>7</td>
<td>RC3</td>
<td>MIC24045 Power good signal</td>
<td>INPUT</td>
<td>HIGH</td>
</tr>
<tr>
<td>8</td>
<td>RC6</td>
<td>Q2 Gate signal – Output discharge enable</td>
<td>OUTPUT</td>
<td>HIGH</td>
</tr>
<tr>
<td>9</td>
<td>RC7</td>
<td>Q3 Gate signal – Input to output bypass</td>
<td>OUTPUT</td>
<td>LOW</td>
</tr>
<tr>
<td>10</td>
<td>RB7</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>11</td>
<td>RB6</td>
<td>SCL – I^2C Clock signal</td>
<td>OUTPUT</td>
<td>—</td>
</tr>
<tr>
<td>12</td>
<td>RB5</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>13</td>
<td>RB4</td>
<td>SDA – I^2C Data line</td>
<td>BIDIRECTIONAL</td>
<td>—</td>
</tr>
<tr>
<td>14</td>
<td>RC2</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>15</td>
<td>RC1-AN2</td>
<td>Low-voltage amplifier</td>
<td>INPUT</td>
<td>—</td>
</tr>
<tr>
<td>16</td>
<td>RC0-AN1</td>
<td>Current integrator analog value</td>
<td>INPUT</td>
<td>—</td>
</tr>
<tr>
<td>17</td>
<td>RA2</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>18</td>
<td>ICSPCLK</td>
<td>ICSP Clock line</td>
<td>INPUT</td>
<td>—</td>
</tr>
<tr>
<td>19</td>
<td>ICSPDAT</td>
<td>ICSP Data line</td>
<td>BIDIRECTIONAL</td>
<td>—</td>
</tr>
<tr>
<td>20</td>
<td>V_SS</td>
<td>Ground rail</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Integrating OPAMP Block**

The integrating block is used to determine the input capacitance of the DUT. In order to resolve in hardware the integral term of Equation 2, a differential amplifier and integrator block was designed.

The first stage consists of a differential amplifier. In theory, a simple operational amplifier in differential configuration could be used. However, due to the fact that the second amplifier stage consists of an integrator, the system is very susceptible to input noise; Therefore a very low-noise amplifier needed to be used. The solution to this problem is using a differential instrumentation amplifier in non-inverting configuration.

MCP16N16, which is a zero-drift instrumentation amplifier, was used for this purpose. The internal offset correction of this OPAMP gives high DC precision. Two external resistors are used in order to set the gain, thus minimizing the gain error and drift over temperature. MCP16N16 was designed for single-supply operation making it suitable for this application. The supply voltage can be as high as 5.5V, compatible with the PIC power supply. The amplifier comes in three minimum gain options (1, 10, 100). The minimum gain has to be set in order to ensure stability of the closed loop system. The third device was used because it has a better PSSR (110 dB) and CMRR (112 dB), and because a high-gain stage is needed in order to bring the potential to the 0-5V range required for the PIC MCU’s ADC.

The instrumentation amplifier was used in a non-inverting configuration, over a shunt resistor. Due to the fact that the resistance of the wires is not known, the charging current could vary a lot. This variation is not desirable in this configuration because it could influence the accuracy of the integrated signal. Also ringing from the distributed inductance of the wire could influence the measurements; Therefore a high-value current limiting resistor was placed after the shunt resistor. In order to keep the shunt resistor much smaller than the current limiting resistor, while keeping the current in the mA range and maximizing the voltage
drop on the shunt resistor (for noise immunity), a 2Ω shunt and 2 kΩ limiting resistor were chosen. To ensure stability, the gain was chosen to be $K = 101$, using a resistor divider of 10 kΩ and 10Ω. The connection between the shunt resistor and the input of the amplifier was made using a Kelvin topology.

The second amplifier stage consists of a non-inverting integrator. The amplifier used for this job was chosen to be MCP6021. The MCP6021 is a 10 MHz rail-to-rail amplifier. The rail-to-rail characteristic is important in order to fully utilize the whole range of the microcontroller’s ADC converter, ensuring maximum resolution. The 10 MHz band ensures that the integration is done in as wide of a band as possible, without losing important information.

The non-inverting integrator is a marginally-stable system that is very prone to accumulating error from the input noise. The solution to this problem is adding a high-value resistor on one of the capacitors in order to set the drift direction towards ground potential. This approach solves two problems: first, the integrator resets at 0V, ensuring that the initial conditions are always null; and second, it helps determine the exact point when the charging of the capacitor ends and where the integrator output voltage starts to drift negatively. Ignoring the high-value discharge resistor, the transfer function of the integrator OPAMP is shown in Equation 5.

**EQUATION 5: INTEGRATOR TRANSFER FUNCTION**

$$V_{\text{integrator}}(t) = \frac{1}{R_i C_i} \int_0^t V(t) dt$$

Taking into account that $V(t)$ is actually the input of the differential amplifier, $R_i=R24=R22=1.5\Omega$, $C_i=C7=C5=0.47\mu F$ that translates the current into voltage with a constant factor $K$, Equation 5 can be written as shown in Equation 6.

**EQUATION 6: DIFFERENTIAL INTEGRATOR TRANSFER FUNCTION**

$$V_{\text{integrator}}(t) = \frac{1}{R_i C_i} \int_0^t I_C(t) dt$$

This relation shows how the differential integrator manages to calculate the integral term in hardware. The integral term amplitude can be separated by multiplying the terms with the inverse of the scaling factor:

**EQUATION 7: CURRENT INTEGRAL**

$$V_{\text{integrator}}(t) = \frac{RC_i}{K} \int_0^t I_C(t) dt$$

However, the capacitance of the capacitor is also dependent on the capacitor voltage, according to Equation 2. Introducing Equation 7 into Equation 2, we get the final formula used in the calculation of the capacitor, shown in Equation 8.

**EQUATION 8: CAPACITOR VALUE**

$$C = \frac{1}{V_C(t)} \left( \frac{R C_i}{K} \right)$$

This equation describes the voltage-charge-capacitance relationship across the DUT capacitor in this setup. The time dependent terms $V_C$ and $V_{\text{integrator}}$ are sampled after the variation of the integrator term is no longer positive, the measurement of the integrator term is done with software using the PIC MCU ADC. The existence of an integrator ensures that there is no need for a very close correlation between the time when the DUT capacitor is charged and the time when the PIC MCU samples the voltage. Also, the final voltage on the DUT capacitor is not required to be sampled as it is supplied by the regulator and therefore known.

The differential integrator block is presented in Figure 4. R21, R14 and R19 are used for setting a negative drift of the AN1 output. The series-parallel topology was used in order to allow for nonstandard resistors to be created. Tantalum bypass capacitors were placed close to the IC’s in order to minimize the supply noise, and ensure sufficient current for fast transient response.

**FIGURE 4: Differential Integrator Block.**
Noninverting Amplifier

A noninverting amplifier is placed on the output in order to amplify the low voltage signal that is produced during the wire resistance determination stage. The amplifier gain was set to five in order to cover the most from the PIC MCU ADC range.

In order to be able to use almost the whole 0 - 5V range, a rail-to-rail operation amplifier was chosen. The amplifier suitable for this purpose is MCP6021, the same used in the integrator block.

This OPAMP is used during the resistance determination stage when the output is first set at 0.64V to ensure that the input capacitor of the DUT is charged at a lower voltage than typical IC start-up voltages or switch thresholds. Then, the output is slowly discharged through the discharge block, which consists of a known resistance. After a specified time ‘t’ proportional with the capacitor value that was determined, the discharging block is shut down and the output voltage is measured in a high-Z state. Using the RC discharge formula, shown in Equation 4, the resistance can be calculated.

PAC1710 Current and Power Monitor

The PAC1710 is a single high side bidirectional current sensing monitor with precision voltage measurement capabilities. Each sensor measures the voltage developed across an external sense resistor to represent the high side current of a battery or voltage regulator. The PAC1710 also measures the SENSE+ pin voltage and calculates the average power over the integration period. The PAC1710 can be programmed to assert the ALERT pin when high and low limits are exceeded for Current Sense and Bus Voltage.

The PAC1710 device is good for measuring dynamic power. The long integration time allows for extending system polling cycles without losing any power consumption information. In addition, the alert ensures that transient events are captured between the polling cycles.

In combination with the wire compensation board, PAC1710 could be used to calculate the delivered power from the power supply, the lost power through the wires, and the received power in the DUT. The PAC1710 has an 11-bit resolution making it very suitable for the application by being able to sense even the minute changes in the current. One drawback is that the digital power motorization is slow and overshoots can occur on the output. This limits the solution to be used until the 5.5V threshold, which is defined in the USB standard as the maximum voltage over USB 2.0. Of course, the solution can be extended to incorporate other loads and voltages; Therefore either a large overshoot needs to be tolerated on the line, or a analog control loop needs to be used instead of the digital one. Communication with the PAC1710 is done using the I2C protocol at 400 Khz or at 100 Khz, being SMBus compliant. The I2C address is set using an external resistor and can take any value from the 8 predefined values, thus an application can incorporate up to 16 measurement channels. The architecture of PAC1710 is presented in Figure 5.
FIGURE 5: PAC1710 Architecture.

+5V RAIL

In order to supply +5V to the PIC MCU, operational amplifiers and the PAC1710 current monitor, the MCP1754 LDO was chosen.

The MCP1754/MCP1754S is a family of CMOS low dropout (LDO) voltage regulators that can deliver up to 150 mA of current while consuming only 56.0 µA of quiescent current (typical). The input operating range is specified from 3.6V to 16.0V, making it an ideal choice for four to six primary cell battery powered applications, 12V mobile applications and one to three-cell Li-Ion powered applications.

The MCP1754/MCP1754S is capable of delivering 150 mA with only 300 mV (typical) of input to output voltage differential. The output voltage tolerance of the MCP1754/MCP1754S is typically ±0.2% at +25°C and ±2.0% maximum over the operating junction temperature range of -40°C to +125°C. Line regulation is ±0.01% typical at +25°C.

Output voltages available for the MCP1754/MCP1754S range from 1.8V to 5.5V. The LDO output is stable when using only 1 µF of output capacitance. Ceramic, tantalum or aluminum electrolytic capacitors may all be used for input and output. Overcurrent limit and overtemperature shutdown provide a robust solution for any application.

The MCP1754/MCP1754S family introduces a true current foldback feature. When the load impedance decreases beyond the MCP1754/MCP1754S load rating, the output current and voltage will foldback towards 30 mA at about 0V output. When the load impedance decreases and returns to the rated load, the MCP1754/MCP1754S follows the same foldback curve as the device comes out of current foldback.

Alternate Current Paths

In order for the board to be able to supply high current, a PMOS was used to bypass the current integrator, connecting the MIC24045 to the output through the PAC1710 shunt resistor. The USB 2.0 can deliver currents in excess of 2000 mA, therefore the PMOS device should be able to handle that output current. FDS6375 was chosen for this application due to its very high current (8A) and low gate drive voltage requirements.

Another important current path is the discharge block. The discharge block is used in order to discharge the DUT capacitor during the RC time constant determination stage. It is very important for the discharge block to exhibit a fairly constant resistance and the deviation from this resistance to be kept as minimal as possible, in order not to interfere with the wire resistance. A typical USB cable has a resistance around 200 mΩ, thus the discharge resistor was...
chosen to be 2Ω in order for the discharging current to be fairly constant independent of the conditions. To the resistor the RDS(on) of the transistor that switches the path needs to be added, when computing the resistance, thus a very low RDS(on) transistor should be chosen. IRLML6344 was selected for this application. The maximum RDS(on) is 29 mΩ.
FIGURE 6: Software FSM.

“Initial” State:
Initialize Variables
Discharge Output

“Charge” State:
Charge DUT Capacitor
Sample Integrator
Output

Output
Slope > 0?

“Capacitor Determination” State:
Determine Capacitor Value
Charge Resistor
Wait t Seconds

“Resistor Determination” State:
Discharge Capacitor for t Seconds
Sample Voltage
Determine Resistance

“Power Supply” State:
Read PAC1710 Current State
Compute Voltage Drop
Compensate Voltage Drop
The software part of the project was modeled by a Finite State Machine (FSM). This way, the software can be analyzed more efficiently.

The first state initializes all the variables used by the program, and discharges the DUT capacitor ensuring stable initial conditions. The controlled discharge block is used for this task, therefore the current is limited by a 2.2Ω resistor.

In the second state the DUT capacitor is charged through the current integrator block. The integrator output is sampled by the MCU ADC, and by the means of a crude low-pass filter that verifies that 3 consecutive samples have a negative slope. The charge is stopped and the last value is kept for capacitor determination.

The Capacitor Determination state determines the capacitance using the information provided by the Charge state. The capacitance is then corrected in order to compensate the drift of the OPAMP and also the noise in the circuit. After the capacitance has been determined, the DUT capacitor is charged again to ensure maximum voltage, then the state increments.

The Resistor Determination state is responsible for discharging the DUT capacitor through the discharge resistor. After a time ‘t’ that is proportional with the capacitor value, the discharging is stopped leaving the system in a high-Z state. This ensures that the voltage drop across the wires is null and the sampling of the final value can be done. Using the formula in Equation 2, the resistor value is then calculated and the Power Supply state is started.

The Power Supply state implements a regulation loop, where the sensing element PAC1710 is pooled for current data. Using Ohm’s Law, the voltage drop across the wires is calculated and then the MIC24045 output voltage is increased accordingly.

Testing and Calibration

In order to measure the capacitance, Equation 8 has to be computed on the PIC MCU. Since many variables are fixed (R, C, Vfinal and K) the equation can be simplified as shown in Equation 9.

\[
C = \frac{1.10599V_{\text{integrator}}}{R_i} 
\]

However, this formula does not account for any nonlinearities in the integrator stage, and in order to achieve maximum resolution in the whole range (1 μF - 50 μF) calibration must be done. The calibration was done by first measuring a set of capacitors using an Inductance, Capacitance and Resistance (LCR) meter, then measuring the same set of capacitors using the PIC MCU. Using the polynomial interpolation tool in Excel, the function that maps measured values into true values was calculated. The results are presented in Figure 7.

![Figure 7: True vs. Measured Capacitance.](image)
To test the evaluation board, the DUT was emulated by a board consisting of 0.1 Ω - 1 Ω as wire resistance and 1 μF - 50 μF as target input capacitance. The system was first tested without making any compensation except for the capacitance. The capacitance error holds steady below 5%, as can be seen in Figure 8.

However, the resistance error tends to be more sensitive to measurement errors especially at high capacitances. The initial results can be seen in Figure 9. It can be observed that the error tends to be higher at lower shunt values. Furthermore, a unique property of this system can be observed, the error is always positive, thus it can be minimized using a simple first order term K multiplied by the measured value. It is clear that the term K is defined in the (0,1) interval since the error never gets negative.

In order to determine the optimal value for the unknown term, the squared residual term must be minimized. It can be observed in Figure 10 that the minimum residual term is achieved around 0.75. The true optimal value was found to be 0.738.

In Figure 11, the measured resistance errors are plotted, this time after compensation. It can be observed that the mean error drops to around half of the initial error.

In Figure 12, a current ramp was applied to the output of the device, simulating an increasing load that goes from 0A to 1A. The true resistance of the wire is 500 mΩ, thus at 1A the voltage drop would be 0.5V. The voltage received by the DUT, holds steady within a 100 mV range, while the current ramps from 0 to 1A.
**FIGURE 10:** Residual Terms vs. Minimization Constant.

**FIGURE 11:** Resistance Error After Calibration.
FIGURE 12: $I_{OUT}$ Ramp.
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ISBN: 978-1-5224-3150-3

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