INTRODUCTION

Offline Switched Mode Power Supplies (SMPS) are ubiquitous in most electronic applications, offering reliable power conversion and good efficiency. To ensure specific operation, prevent failure and protect the connected circuits, the power supply needs established limits.

The usual implemented solution to power conversion protecting functions consists of placing a fixed limit to one or more of these measurement points: input voltage, input current, output voltage and output current. This approach encounters various challenges in applications that require isolation, variable input voltage, low component count, board dimension restriction or low cost. This technical brief describes the negative effects caused by the classic power-limiting approach in certain SMPS specifications and a new approach that solves all the challenges. The new approach is implemented with microcontroller peripherals and is able to adapt the limits to any changing variable that influences power conversion, thus maintaining power conversion below specifications.

PROBLEM DESCRIPTION

The current-mode (CM) SMPS can control the input current at every pulse; this is done by comparing the inductor/transformer current sense signal to the error feedback signal, and thus, output regulation is done on every cycle. When a short circuit or overload happens on the output, the input current will tend to become bigger to compensate the output needs; some of the following may happen if the SMPS does not have established limits:

1. The power conversion is higher than what the SMPS was designed to handle and some components fail. The conversion is stopped without damaging the load or the source. In this case, only the SMPS is destroyed.
2. The power delivered to the output is higher than what the load can handle; the load fails and becomes an open circuit. The SMPS enters Idle mode. In this case, only the load is destroyed.
3. The power delivered to the output is higher than what the load can handle, the load fails and becomes a short circuit. The SMPS does not have a limit protection and internal components fail. In this case, both the SMPS and the load are destroyed.
4. The power conversion is higher than what the SMPS was designed for and fails as a short circuit for the source. If the source is a battery, it may explode. In this case, both the source and the SMPS are destroyed.
5. The power delivered to the output is higher than what the load can handle, the load fails and becomes a short circuit. The SMPS fails as a short circuit to the source and if the source is a battery, it may explode. In this case, the source, SMPS and load are destroyed.

These examples show what can happen to a non-protected SMPS and system when the load causes problems, but source changes can also be responsible for a system failure.

LEGACY SOLUTIONS

The power conversion limit is implemented in legacy SMPS controllers in many forms. This chapter describes how these solutions are implemented.

Fixed Duty Cycle Limit

The most basic form of power conversion limit is implemented taking advantage of the maximum allowed duty cycle limit of many controllers. To do this, the SMPS converter is designed to operate close to the duty cycle limit in full load, while the closed loop will become an open-loop control meant to stop the increase of the output power.
Fixed Primary Peak Current Limit
Most legacy SMPS controllers determine a fixed threshold reference on the inductor current that will take over the control loop and will end the pulse earlier. The fixed threshold level can be implemented with a second comparator with the limit level as depicted in Figure 1 or a forced limit on the Error Signal with an internal Zener diode. Multiple protection levels can be implemented with this technique such as:
- One comparator will stop the PWM pulse earlier if the first threshold is passed
- A second comparator with a higher threshold level will stop the IC for a limited time to prevent component damage

Output Current Limit
The safest way to prevent power conversion that exceeds the specified design is to measure the output of the converter where the power is delivered. For a fixed output voltage conversion design, the limit is placed on the delivered output current, while for a fixed output current conversion design, the limit is placed on the measured output voltage. This method is used by most non-isolated designs and works even when the input voltage is variable.

Lockouts and Shutdowns
Limiting techniques are also used to prevent damage or unwanted operation, even when the converted power is within specifications. Such a case can happen when the input voltage is smaller than the rated value; an undervoltage lockout will stop the conversion until the input voltage is within specified levels. Another case where the power conversion can be within specifications is an output overvoltage; in this case, the conversion enters a Shutdown state to protect the load from irreversible damage.

LIMITATIONS OF LEGACY SOLUTIONS
While the presented solutions seem to work well in specific cases, they have very strict limitations as described below.

These limitations were tested using an AC/DC Flyback Converter designed for a 20W output power delivery and 85 VAC-265 VAC input. The output of the SMPS is overloaded to maintain the output voltage constant. The desired power limit is 30W.

Fixed Duty Cycle Limit
1. It works only for a fixed input voltage and fixed output voltage converter. It can be used for power limitation in converters that have only the duty cycle value as part of the transfer function equation (Buck, Boost converter).
2. The converter has to be calculated exactly to limit the desired power limit to the duty cycle and still work properly in normal operation conditions.
3. Once designed, the limit is not configurable.

Figure 3 shows how the output power rises with the increase of the input voltage. This case uses only a maximum duty cycle limit, so there is no current limit from the primary cycle. At 160 VAC input, the load can take 93W of power from the SMPS without losing output regulation; thus, the SMPS components will fail.

Fixed Primary Peak Current Limit
1. The big problem with this solution is that when the input voltage of the converter is variable for the same power transfer, the current signal will become smaller, as shown in Figure . This will result in a higher power transfer before reaching the set limit.
2. As the limit is fixed, configuration is not possible.
The primary peak current limit with a separate comparator or indirectly with a Zener diode on the error signal, shows better limiting results as depicted in Figure 4. Here, the limit is set on the primary current to obtain a maximum of 30W on the output when the input voltage is 90 VAC.

Output Current Limit
1. This method becomes very expensive in isolated designs as having multiple signals pass through the isolation barrier can become very costly.
2. As the limit is fixed, configuration is not possible.
These results prove that the classic limit approach works only if there is direct access to the output current signal. It does not fit with a system with big input variations and isolation needs.
FIGURE 2: CURRENT WAVEFORM CHANGES WHEN THE INPUT VOLTAGE IS CHANGED. THE LIMIT IS THE SAME

a) 90V Input / 20W Output
b) 130V Input / 20W Output

FIGURE 3: OUTPUT POWER INCREASES WITH INPUT VOLTAGE INCREASE. DUTY CYCLE LIMIT

Pout[W]

Exceeding power limitation
A BETTER SOLUTION USING CIPs

Using the PIC® microcontroller that has analog and digital dedicated Core Independent Peripherals (CIPs) for SMPS applications, allows the implementation of a current limit that adapts to the input voltage and can be controlled by the user. This adaptable limit will solve the output power problem and will allow the designer to set the maximum allowed output power.

The adaptable limit can be implemented either with software or hardware supervision.

Adaptive Software Limit

This solution is implemented using one ADC and a DAC to change the set peak current limit.

For this to work, an internal set of limits is defined and attributed to a certain range of input voltages. The ADC measures a proportion of the input voltage and stores it in the memory. After each acquisition, the value is compared to the input voltage attributed in the limit array and the peak current limit is updated in the DAC.

This solution is feasible when the input voltage changes are slow.

Adaptable Hardware Limit

This technique is hardware-based, as opposed to the software approach, and frees the core from important SMPS-related tasks.

The solution changes the current limit inversely-proportional to the input voltage change using one internal op amp and one DAC. A resistor divider scales down the rectified input voltage and the op amp is used to invert the signal, so when the input voltage rises, the current limit will adapt and fall as depicted in Figure 5. The DAC is set as op amp positive input to raise the inverted signal over the 0V line.

This signal is compared with the current from the transformer primary and triggers a falling event on the PWM, if the current reaches the set limit as depicted in Figure 6. The limit trigger can be also set to implement a shutdown or other functions in the circuit.
The external resistors connected and the op amp are used to generate an inversely-proportional waveform to the input voltage, so when the output voltage rises, the limit will drop and adjust. VREF is set by the DAC, and with this value, the designer can control the maximum power delivered to the output. The adaptable output ramp and value can be calculated using Equation 1; the equation can be used to calculate the values of the components when the limit needed and reference are known. In this example, R1 is selected as 1 MOhm to limit the current that goes to the IC, R2 is 51 KOhm and R3 1.5 KOhm, while VREF or the DAC value is set to 2V. With the help of Equation 1 it is possible to calculate that the set limit will be 1.9V when the rectified input voltage is 90 VDC, and 1.5V when the rectified input voltage is 360 VDC.

**EQUATION 1: PEAK CURRENT LIMIT CALCULATION USING THE GIVEN VALUES**

\[
V_{INV} = V_{REF} - R_3 \times \left( \frac{V_{IN}}{R_1} - \frac{V_{REF}}{R_2} \right)
\]
ADVANTAGES OF THE CIP SOLUTION

This solution gives the user full control over the set limit while maintaining a constant power limit over a wide input voltage.

Constant Power Limit Over Variable Input Voltage

The results depicted in Figure 7 show that the maximum output power delivery is almost constant even when the input voltage changes drastically. The limit is set using the DAC to 30W and the maximum measured value is 1.5W, above the set limit. Better component adjustment thus, eliminates even the slightest variation from the set limit.

FIGURE 7: OUTPUT POWER DELIVERY REMAINS CONSTANT WITH INPUT VOLTAGE INCREASE, CIP SOLUTION

No Expensive External Components

This solution uses external resistors to implement the needed function, two resistors to obtain the input voltage proportion and one resistor to control the op amp loop and adjust the voltage following ramp. After that, the limit adapts itself to the changing input voltage.

Once the resistance values are selected to ensure that the input voltage following ramp is proportional throughout the whole input voltage variation, the user does not need to modify or change any external components.

Full Configurability and Control to the User

The CIP solution allows the designer to control the maximum power delivery at any moment during runtime. This feature allows the implementation of a function that reduces the power limit to half after multiple power-exceeding warnings, thus preventing damage and notifying the user. It is possible to apply a time limit to the maximum allowed power conversion and prolong the lifetime of the circuit even for circuits that are designed to physically support higher power values (ex: an 100W converter can be set to deliver maximum 80W after five years of operation to extend the lifetime of the product and prevent wear and tear). Thus, if the user wants to use the same SMPS for multiple applications, the maximum allowed power can be tuned to protect the loads (ex: a user wants to use the 100W/12V converter to power a 100W load, a 60W load and a 20W load separately without the need of having three separate converters). This function does not use the microcontroller core, so the designer can use internal logic to trigger functions when the power delivery is at limit, without compromising the safety of the conversion.

Flexible with Any Topology or Control Method

This method can be used to limit the maximum allowed conversion power for any converter that has variable input voltage and isolation requirements, including voltage mode control or variable frequency control.

Fast Response and Adjustment

Because the solution uses the op amp of the IC, the limit change is done continuously and asynchronously with very fast response times.
CONCLUSION

This document presents the methods of legacy power limitation techniques, showing the major disadvantages. A new way to protect offline SMPS that have variable input voltage is implemented using Microchip microcontroller CIPs, a solution that solves all the legacy mentioned problems. The adaptable primary side power-limiting method offers reliable power limitation and full control to the user from the primary side of the SMPS. This eliminates the need for multiple IC solutions or multiple isolated signals that would otherwise complicate the design and have a major cost impact.

This solution offers the following advantages:

• Limits the total power conversion independent of the input voltage
• Prevents load damage
• Prevents high short-circuit impulses
• Prevents transformer core saturation
• Prevents SMPS hazardous behavior
• The designer has control over the maximum SMPS output power limit

Another great benefit in using a microcontroller core that allows the implementation of software algorithms and communication methods is to enable the user to receive notifications and live updates.
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