INTRODUCTION

The motor control industry has been focusing on designing low-cost motor control drives for various applications. The consumer demand for low-cost motor control applications is driving this trend.

Microchip has recently introduced the PIC32MM family of microcontrollers, which is capable of addressing the low-cost motor control requirements. The low-cost solution benefits from the capability of the Multiple Capture/Compare/PWM (MCCP) module available in Microchip’s PIC32MM controllers. This document illustrates the usage of the MCCP module in the PIC32MM0064GPL036 controller, from Microchip Technology, to deliver a development platform for motor drive applications.

MCCP implementation, similar to the motor control solution discussed in this document, can also be extended to Microchip’s PIC24 and dsPIC33 family of devices which feature MCCP.

SIX-STEP COMMUTATION FOR THREE-PHASE BLDC MOTOR CONTROL

This document describes the algorithm for running a sensorless Brushless DC (BLDC) motor using a six-step trapezoidal or 120° commutation. Figure 1 shows how the six-step commutation works. Each step, or sector, is equivalent to a 60° electrical and six sectors make up a 360° electrical or one electrical revolution.

In Figure 1:

- The arrows in the winding diagram show the direction in which the current flows through the motor windings in each of the six steps.
- The graph shows the potential applied at each lead of the motor during each of the six steps.

Sequencing through these steps moves the motor through one electrical revolution.
Table 1 shows a typical commutation sequence.

TABLE 1: COMMUTATION SEQUENCE

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<tr>
<th>Sector</th>
<th>ATOP</th>
<th>ABOTTOM</th>
<th>BTOP</th>
<th>BBOTTOM</th>
<th>CTOP</th>
<th>CBOTTOM</th>
<th>A</th>
<th>B</th>
<th>C</th>
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<tr>
<td>1</td>
<td>PWM</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
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<td>OFF</td>
<td>—</td>
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<td>OFF</td>
<td>OFF</td>
<td>PWM</td>
<td>OFF</td>
<td>OFF</td>
<td>+</td>
<td>—</td>
<td>OFF</td>
</tr>
<tr>
<td>3</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>PWM</td>
<td>PWM</td>
<td>OFF</td>
<td>OFF</td>
<td>—</td>
<td>+</td>
</tr>
<tr>
<td>4</td>
<td>OFF</td>
<td>PWM</td>
<td>OFF</td>
<td>OFF</td>
<td>PWM</td>
<td>OFF</td>
<td>—</td>
<td>OFF</td>
<td>+</td>
</tr>
<tr>
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<td>OFF</td>
<td>PWM</td>
<td>PWM</td>
<td>OFF</td>
<td>OFF</td>
<td>PWM</td>
<td>—</td>
<td>+</td>
<td>OFF</td>
</tr>
<tr>
<td>6</td>
<td>OFF</td>
<td>OFF</td>
<td>PWM</td>
<td>OFF</td>
<td>OFF</td>
<td>PWM</td>
<td>+</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

For every sector, two windings are energized and the other winding is not energized. The fact that one of the windings is not energized during each sector is an important characteristic of the six-step control that allows the measurement of the Back-EMF (BEMF) in that phase, and thereby, enables the sensorless commutation scheme. Figure 2 shows the PWM signals applied to each winding during the six-step trapezoidal commutation.

FIGURE 2: SIX-STEP TRAPEZOIDAL BLDC COMMUTATION
Bipolar Independent PWM

The three-phase voltages are controlled by applying a PWM-based voltage to the top and bottom MOSFETs/Insulated-Gate Bipolar Transistors (IGBTs). The six-step commutation in this document employs bipolar independent PWM switching. This kind of commutation requires switching the top and bottom MOSFETs diagonally, but the complementary switching on the same phase is not required.

Figure 3 shows an instance of diagonal switching in which Phase A top side (Q1) and Phase B bottom side (Q4) MOSFETs are switched.

FIGURE 3: DIAGONAL SWITCHING
The advantage of this switching scheme is that the BEMF signal is cleaner, and avoiding the complementary switching makes the switching pattern simpler and the dead-time insertion is not needed. The disadvantage of this scheme is the higher switching losses (due to switching both diagonal MOSFETs). However, it is observed that in low-cost solutions, the switching losses are significantly low in magnitude when compared to other losses. Details of the technique are shown in Figure 4.

In Figure 4, the signals are gate driver inputs with High = On and Low = Off.

The signal conventions followed here are:
- PWM1H for Phase A Top (Q1), PWM1L for Phase A Bottom (Q2)
- PWM2H for Phase B Top (Q3), PWM2L for Phase B Bottom (Q4)
- PWM3H for Phase C Top (Q5), PWM3L for Phase C Bottom (Q6)

**FIGURE 4: BIPOLAR INDEPENDENT PWM**
TB3152

Multiple Capture/Compare/PWM (MCCP)

This section describes the configuration of the Multiple/Capture/Compare/PWM (MCCP) module for low-cost BLDC motor control applications, along with a brief description, initialization of the peripheral and the PWM duty cycle control of the MCCP module.

PIC32MM family devices include one or more Capture/Compare/PWM/Timer (CCP) modules. They also provide the functionality of the comparable input capture, output compare and general purpose timer peripherals found in all of the earlier PIC32 devices.

CCP modules can operate in one of three major modes:
- General Purpose Timer
- Input Capture
- Output Compare/PWM

There are two different forms of the module, distinguished by the number of PWM outputs that the module can generate. Single output modules (SCCPs) provide only one PWM output. Multiple output modules (MCCPs) can provide up to six outputs and an extended range of output control features, depending on the pin count of a particular device.

All modules (SCCP and MCCP) include these features:
- User-Selectable Clock Inputs, including System Clock and External Clock Input Pins
- Input Clock Prescaler for Time Base
- Output Postscaler for Module Interrupt Events or Triggers
- Synchronization Output Signal for Coordinating other MCCP/SCCP Modules with User-Configurable Alternate and Auxiliary Source Options
- Fully Asynchronous Operation in all modes and in Low-Power Operation
- Special Output Trigger for Analog-to-Digital Conversions
- 16-Bit and 32-Bit General Purpose Timer modes with Optional Gated Operation for Simple Time Measurements
- Capture Modes:
  - Backward compatible with previous input capture peripherals of the PIC32 family
  - 16-bit or 32-bit capture of time base on an external event
  - Capture source input multiplexer
  - Gated capture operation to reduce noise-induced false captures
- Output Compare/PWM modes:
  - Backward compatible with previous output compare peripherals of the PIC32 family
  - Single Edge and Dual Edge Compare modes
  - Center-Aligned Compare mode
  - Variable Frequency Pulse mode
  - External Input mode

MCCP modules also include these extended PWM features:
- Single Output Steerable mode
- Brush DC Motor (Forward and Reverse) modes
- Half-Bridge with Dead-Time Delay mode
- Push-Pull PWM mode
- Output Scan mode
- Auto-Shutdown with Programmable Source and Shutdown State
- Programmable Output Polarity

The SCCP and MCCP modules can only be operated in one of the three major modes (Capture, Compare or Timer) at any time. For example, if SCCP or MCCP is configured in Compare mode, the same module is not available for Capture or Timer mode unless the module is reconfigured.

Figure 5 shows a conceptual block diagram of the MCCP. All three sub-modules of MCCP use a common Time Base Generator (TBG), Timer register (CCPxTMR) and Compare registers. Other shared hardware components, such as comparators and buffer registers, are activated and used as a particular mode requires.
FIGURE 5: MCCP BLOCK DIAGRAM

Note 1: Buffered Output Compare and PWM modes only.
Configuring MCCP for BLDC Motor Control

This section describes the configuration of the MCCP module for BLDC motor control.

CAPTURE/COMPARE MODE SELECTION
Clearing the CCSEL (CCPxCON1<4>) bit enables the module in Output Compare/PWM or Timer mode.

```c
CCP1CON1bits.CCSEL = 0; // Set MCCP operating mode (Output Compare mode)
```

OUTPUT COMPARE MODE SELECTION
For this application, Dual Edge Buffered Compare (PWM) mode is chosen. In Dual Edge Buffered mode, the MCCP module output is configured to produce a continuous series of pulses.

```c
CCP1CON1bits.MOD = 0b0101; // Set mode (Buffered Dual-Compare/PWM mode)
```

TIMER BASE SELECTION
Dual Edge Buffered Compare mode is only available in 16-bit mode. The T32 bit has no affect.

```c
CCP1CON1bits.T32 = 0; // Set timebase width (16-bit)
```

TIME BASE CLOCK SYNCHRONIZATION
In this application, the time base clock module is not synchronized to the internal system clocks. If the module should operate in Sleep mode, the TMRSYNC bit should remain cleared.

```c
CCP1CON1bits.TMRSYNC = 0; // Set timebase synchronization
```

TIME BASE CLOCK SOURCE AND PRESCALER SELECTION
The time base generator accepts one out of eight possible clock sources (including the system clock, Tcy) and provides a time base for the rest of the module using clock signals available on the microcontroller. For this application, the clock source is selected as Tcy and the prescaler is selected as 1:1.

The clock source should be selected before enabling the module and should not be changed during operation; otherwise, unexpected behavior may occur.

```c
CCP1CON1bits.CLKSEL = 0; // Set the clock source (Tcy)
CCP1CON1bits.TMRPS = 0; // Set the clock pre-scaler (1:1)
```
OUTPUT PIN ENABLE

Each of the output pins controlled by the MCCP module may be enabled separately by setting the OCxEN control bits (CCPxCON2<29:24>). Each of the bits, OCAEN through OCFEN, controls the corresponding CCP output: OCxA through OCxF. If the OCxEN control bit is set, the corresponding I/O pin receives the output compare signal that is generated by the module. If the OCxEN control bit is cleared, the I/O pin is controlled by the port. The user must use care to ensure that the I/O pin will be in the correct state when an OCxEN control bit is cleared.

During initialization, the OCxEN bits are cleared to disable the OCx pins to ensure no MOSFET in the inverter bridge is in the ON state. During motor commutation, the bits associated with the MCCP output enable are enabled/disabled based on the sector information.

In the example code, except for the MCCP outputs (CCPxCON2<29:24>), the remaining bits of the CCPxCON2 register are masked to prevent any changes that can possibly happen while controlling the pin status.

```
CCP1CON2 = ((CCP1CON2 & 0XC0FFFFFF) | PWM_STATE[ADCCommState]);
```

PWM OUTPUT MODE CONTROL

The OUTM<2:0> control bits (CCPxCON3<26:24>) are used to select the Output mode of the MCCP. When operating in Output Compare mode, one of several Output modes may be selected that use the OCxA through OCxF output pins in different ways.

For this application, Steerable Single Output mode is selected. In this mode, the single signal produced by the output compare logic is routed to all available module output pins. This steering functionality is useful in motor and power control applications.

```
CCP1CON3bits.OUTM = 0; // Steerable Single Output Mode
```

RISING AND FALLING EDGE COMPARE VALUES

In Dual Edge Buffered Compare mode, the CCPxRA register is used for setting the rising edge of the next period and the CCPxRB register for setting the falling edge. As shown in Figure 6, the rising edge and falling edge define the duty cycle. Here, as the edge-aligned PWM signals are desired, CCPxRA is maintained with a value of ‘0’. The value corresponding to the desired duty cycle is loaded into the CCPxRB register to output the correct PWM signal.

The following code is part of the MCCP initialization routine.

```
CCP1RAbits.CMPA = 0; // Set to 0 for Edge Aligned PWM
CCP1RBbits.CMPB = 10; // Small Duty Cycle to enable MCCP Interrupt function
```
FIGURE 6: DUAL EDGE COMPARE MODE TIMING

MCCP TIMER PERIOD REGISTER
The PRL<15:0> bits of the CCPxPR SFR are configured to run the PWM at a particular frequency. In this application, the period is set to generate 20 kHz frequency pulses.

\[
\text{CCPxPRbits.PRL} = \left(\frac{\text{FCY}}{\text{FPWM}}\right) - 1; \quad /\!\!/\text{Setting PWM Period}
\]

FCY is configured to run at 24 MIPS and the FPWM is set for a 20 kHz frequency. Effectively, the value, 1999, defines the period for the PWMs to generate output at 20 kHz.
Applying MCCP for BLDC Motor Control

The sensorless commutation scheme described in this technical brief works by measuring the BEMF in the non-energized phase, and comparing it with one-half of the DC bus voltage (Vbus/2) within the ADC Interrupt Service Routine (ISR). The exact point of commutation (zero-crossing event) is determined by utilizing the majority detection filter, which excludes the need for external low-pass filtering and off-chip comparators. Figure 7 shows the circuitry used to implement this method.

FIGURE 7: BEMF VOLTAGE COMPARED TO Vbus/2

Assume that the motor is in commutation Step 1 (refer to Figure 1), in which Phase A is connected to +Vbus through an electronic switch, Phase C is connected to GND through an electronic switch and Phase B is open. The BEMF signal measured on Phase B has a negative slope and its minimum value is almost equal to GND just before the commutation Step 2 occurs. Phase B reaches the value of GND when commutation Step 2 occurs. At this instant, Phase B is connected to GND through an electronic switch, Phase C is now open and Phase A remains connected to Vdc. The BEMF signal observed on Phase C has a positive slope and its maximum value is almost equal to Vdc just before commutation Step 3 occurs. Both slopes observed on Phase B and Phase C are compared with Vdc/2 to determine the zero-crossing event. This is easily implemented in the software using “if-else” routines.

TIMER1 TRIGGERED ADC

In a typical sensorless trapezoidal commutation, the PWM triggers the ADC, resulting in one measurement per PWM cycle.

To have a more effective zero-crossing event detection, the ADC is triggered by Timer1 at a higher rate than that of the PWM. Currently, the algorithm is configured to trigger the ADC interrupt at six times the PWM frequency, which is 120 kHz (6 * 20 kHz). The advantage is that the six ADC reads for every PWM period reduces the majority detection time considerably.

The sensed BEMF signals are then passed through the digital filter (majority function) to get cleaner signals. The concept of the majority function is beyond the scope of this document. For more information, refer to the document listed in “References” section.

ONE ADC CHANNEL INSTEAD OF FOUR

Sensorless trapezoidal algorithms need the BEMF information of the three phases of the motor, and probably a potentiometer read, for speed reference information. This calls for four ADC channels.

PIC32MM series has one ADC channel. The analog input selection is switched in firmware for every phase according to the present motor sector. The potentiometer is read in the time when samples from the motor phase are not needed (immediately after the zero-crossing detection). Figure 8 shows the instances of execution of the ADC and PWM ISRs.
Control Loops
This application software has two control loops that can be selected for use during the compile time:
- Open-Loop Control
- Closed-Loop PI Control

OPEN-LOOP CONTROL
When the load on a motor is constant over its operating range, the response curve of the motor speed relative to the applied voltage is linear. If the supply voltage is well regulated, a motor under constant torque can be operated in an open loop over its entire speed range.

Considering that with a PWM, the effective voltage is linearly proportional to the PWM duty cycle. An open-loop controller can be made by linking the PWM duty cycle to a 16-bit variable, which is generated by a potentiometer that is sampled by an ADC. The block diagram of this mode is shown in Figure 9.

CLOSED-LOOP PI CONTROL
The Closed-Loop mode measures the actual speed of the motor, and based on the difference of the speed with the demand, appropriate corrections are applied. The speed demand is typically set by a potentiometer value, which is scaled to the desired speed range. Figure 10 shows the block diagram of the speed PI Closed-Loop mode.

The Analog-to-Digital conversion value is read in a 10-bit unsigned integer format; hence, the possible conversion values are within the range of 0 to 1023. It is required to scale this conversion value to match the PWM duty cycle range, which is 0 to 1999, as described in the “Configuring MCCP for BLDC Motor Control” section.
To measure the mechanical speed (RPM), the SCCP3 configured in Timer mode is used to measure the time between each commutation (60° electrical). The measured time is then converted to mechanical speed by applying the appropriate scaling factor based on the number of the motor pole pair. Once the current speed is calculated, it is then compared to the desired speed set by the scaled value of the potentiometer. The error is fed to a PI controller and the output is then scaled to match the range of the PWM duty cycle.

SOFTWARE OVERVIEW

ADC ISR

The ADC ISR runs the majority detection filter routine by passing the most updated measurement of the BEMF. Once the zero-crossing event is detected, the ISR also loads the value equivalent to 30° electrical into the SCCP2. The ISR also monitors for any speed input on the potentiometer and scales the ADC value as desired.

MCCP ISR

The MCCP ISR monitors rotor Stall detection while the machine is running, and if detected, it goes to Fault mode and attempts to restart the motor.

SCCP2 ISR

One of the two SCCPs, SCCP2 is configured as a timer for MOSFET commutation. Once the SCCP2 overflows, an interrupt is generated, and inside the ISR, the MOSFET commutation occurs.

CONCLUSION

This paper has discussed the usage of PIC32MM devices’ MCCP in motor control applications by illustrating the usage of the majority detection filter in making the hardware design simpler, while eliminating the need for an external filter. Thus, substantiating that the scheme discussed is perfectly suitable to meet the challenges of the low-cost motor control drives.

REFERENCES

- AN1160, “Sensorless BLDC Control with Back-EMF Filtering Using a Majority Function” (DS01160)
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