INTRODUCTION

This technical brief describes a synchronous buck power supply, based on the PIC16F753 using 100% analog control for output regulation. The implementation has the advantage of not using any processor power, leaving the core free for more complex firmware. Also, the analog loop has a much faster response time to load steps and input voltage changes, making it useful for many applications.

The peripherals needed for the application are:

- One Complementary Output Generator (CWG)
- One Comparator (COMP)
- One Operational Amplifier (OPA)
- One 9-bit Digital-to-Analog Converter (DAC)
- One Fixed Voltage Reference (FVR)
- One Slope Compensation Module (SC)
- One Capture/Compare/PWM Module (CCP)

The peripherals are internally connected through firmware, significantly reducing the number of external pins needed for the implementation.

PERFORMANCE SPECIFICATIONS

Electrical specifications over operating range:
8V ≤ VDD ≤ 16V.

<table>
<thead>
<tr>
<th>TABLE 1: ELECTRICAL SPECIFICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
</tr>
<tr>
<td>Output Voltage</td>
</tr>
<tr>
<td>Output Current</td>
</tr>
<tr>
<td>Output Power</td>
</tr>
<tr>
<td>Code Size</td>
</tr>
<tr>
<td>Ram Size</td>
</tr>
<tr>
<td>Efficiency</td>
</tr>
<tr>
<td>Available Code Size</td>
</tr>
<tr>
<td>Available RAM Size</td>
</tr>
</tbody>
</table>
The output voltage is regulated using Peak Current mode control. The output voltage is compared to the reference voltage by the error amplifier (OPA) and the result is fed to the peak current comparator. The internal slope compensation module subtracts a software programmable ramp from the error amplifier output before the peak current comparator.

The CCP provides a fixed-frequency, fixed duty cycle control signal and the peak current comparator output is selected as a second (level-based) source for the COG falling edge.

**FIGURE 1:** BLOCK DIAGRAM

Figure 1 illustrates the block diagram of the power supply.
This power supply is a fixed-frequency Peak Current mode converter. The operational amplifier (OPA) is used as an error amplifier (EA) for the output voltage and a comparator limits the peak inductor current on each switching cycle based on the EA feedback. The voltage reference for the EA is generated by the DAC and can be changed on-the-fly in firmware. The CCP peripheral generates a fixed-frequency, fixed duty cycle control signal for the COG and the peak current comparator is used to close the loop by selecting it as a second falling edge event source (limits duty cycle on each switching pulse based on EA feedback).

After the peripherals are configured and connected together, the control loop runs by itself, requiring 0% processor time.

Peak current control schemes require slope compensation for duty cycles over 50% to prevent oscillation. For lower duty cycles, slope compensation will also help stabilize the control loop, if the current shunt is small. The PIC16F753 has an internal slope compensation module which can be used to subtract a programmable ramp from the error amplifier output before it is fed to the peak current comparator.

For synchronous switching power supplies, a small dead-time is required for the transistor control signals to avoid current shoot-through. The COG can generate this signal based either on the oscillator frequency or an analog delay chain. The analog delay chain allows the user to set the dead time with a 5 ns resolution, which is more adequate for small transistors. For this particular application, the dead time was set to 30 ns.

For the buck topology, the inductor current is equal to the load current. To be able to measure the peak inductor current using a low-side shunt, some modifications are required. Normally, the shunt sees the filtered output current which is not usable by the peak current control scheme. By connecting the output capacitors to ground through the shunt, ESR is higher but the resulting waveform matches closely the inductor current waveform. The downside of this method is the slightly lower efficiency, but a high-side shunt usually requires an additional circuit (current mirror or specialized IC), which adds to the cost.

Output current limiting is not integrated into the control loop and a second comparator should be used for this purpose and selected as an auto-shutdown source for the COG. The error amplifier output is the inductor peak current limit, so keeping this value low by a resistor divider helps with inrush current problems and catastrophic short-circuit conditions. Of course, the downside of this approach is that system gain is reduced and it will respond slower to transients. The OPA output pin is the same as the slope compensation module input pin, so the two peripherals can be used together without any additional external connectivity. If using a resistor divider to limit OPA output voltage, it must be routed externally to the FVR buffer input pin.

The component values shown in this document are to be treated only as a starting point. They need to be tuned for each design. The converter must be compensated for a specific load and the stability must be verified across the entire range of operating conditions.

Compared to a solution using a specialized PWM controller chip, performance is similar but a PIC® microcontroller-based solution adds invaluable flexibility. Also, the analog control loop runs by itself, so the microcontroller core is 100% free to run user algorithms, measure power supply parameters or transmit relevant information.
APPLICATIONS

The analog control loop makes the power supply fast enough for dynamic loads and input voltage changes. For current-controlled loads like LEDs or thermoelectric cells, the voltage feedback can be replaced by average current feedback. The power supply can be also used for applications which require both voltage and current control like CC/CV battery chargers. The PIC16F753 DAC has nine bits of resolution, which translate into a minimum voltage step of 20 mV with a 1/2 output divider.

MCU PERIPHERAL CONFIGURATION

The application needs one OPA, one comparator and one DAC. The DAC output can be internally routed to the OPA, so this feature saves one pin. The CCP module generates a fixed-frequency, fixed duty cycle signal for the COG. Depending on the user option to limit the OPA output, the resistor divider needs to be externally connected to the FVR buffer input. If not using the resistor divider, only one pin is used instead of two. In this case, the OPA output, which is the same as the SC input, is configured as an analog pin and should not be used for other purposes.

TABLE 2: PIC16F753 PERIPHERAL CONFIGURATION

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>Supply voltage</td>
</tr>
<tr>
<td>10</td>
<td>RC0</td>
<td>Analog input (COMP) – peak current sensing</td>
</tr>
<tr>
<td>9</td>
<td>RC1</td>
<td>Analog input (OPA) – output voltage feedback</td>
</tr>
<tr>
<td>8</td>
<td>RA1</td>
<td>Analog output (OPA) – error amplifier output</td>
</tr>
<tr>
<td>12</td>
<td>RA0</td>
<td>Analog input FVR buffer input for peak current limit from error amplifier</td>
</tr>
<tr>
<td>12</td>
<td>PGC</td>
<td>Programming clock</td>
</tr>
<tr>
<td>5</td>
<td>COG1OUT0</td>
<td>High-side control signal</td>
</tr>
<tr>
<td>6</td>
<td>COG1OUT1</td>
<td>Low-side control signal</td>
</tr>
<tr>
<td>13</td>
<td>PGD</td>
<td>Program data</td>
</tr>
<tr>
<td>14</td>
<td>Vss</td>
<td>Ground reference</td>
</tr>
</tbody>
</table>

The input-only digital pin, MCLR, can be used for a button or a similar functionality. During run-time, the programming data I/O pin (PGD) and two other pins are free for user-specific functionality.

FIGURE 3: PERIPHERAL CONFIGURATION

![PERIPHERAL CONFIGURATION Diagram]
PLOTS OF KEY PARAMETERS

Table 3 contains some characteristics of the charger obtained with an input of 14.3V and an output of 5V. Efficiency is calculated including current shunt power loss. Switching frequency is 250 kHz.

**TABLE 3: POWER SUPPLY CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Output Current (mA)</th>
<th>Duty Cycle (%)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>skipping</td>
<td>N/A</td>
</tr>
<tr>
<td>50</td>
<td>34.7</td>
<td>61.1</td>
</tr>
<tr>
<td>100</td>
<td>34.9</td>
<td>76.8</td>
</tr>
</tbody>
</table>

**FIGURE 4: DUTY CYCLE vs. LOAD CURRENT**

Figure 4 shows the converter duty cycle for 14.3V, 12V and 9V input at different output currents. Once the inductor current becomes continuous, the duty cycle changes very little, only to compensate for component power losses.

**GLOSSARY**

**TABLE 4: ACRONYMS**

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM</td>
<td>Pulse-Width Modulation</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog-to-Digital Converter</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-Analog Converter</td>
</tr>
<tr>
<td>COG</td>
<td>Complementary Output Generator</td>
</tr>
<tr>
<td>FVR</td>
<td>Fixed Voltage Reference</td>
</tr>
<tr>
<td>OPA</td>
<td>Operational Amplifier</td>
</tr>
<tr>
<td>EA</td>
<td>Error Amplifier</td>
</tr>
<tr>
<td>SC(M)</td>
<td>Slope Compensation (Module)</td>
</tr>
<tr>
<td>CCP</td>
<td>Capture Compare PWM</td>
</tr>
</tbody>
</table>
APPENDIX A:

FIGURE 5: SCHEMATIC
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