INTRODUCTION

This technical brief shows how to construct a simple, low-power IR (infrared) remote control transmitter using a PIC16F1708 microcontroller. The remote control transmitter makes use of the Configurable Logic Cell (CLC) and Pulse-Width Modulation (PWM) to create a Pulse Code Modulation (PCM) signal that will be transmitted via an infrared LED. The Peripheral Pin Select (PPS) feature is used to route the PCM signal to an infrared LED.

PCM involves transmission of a carrier frequency that can be easily discerned from the background noise. This signal is then band-pass filtered and demodulated by the receiver to recreate the digital waveform. Television remote controls use different frequencies, but 30 kHz and 38 kHz are very popular. This project can be easily modified to output different carrier frequencies.

A number of IR receivers are available in the marketplace. This project was tested using a Vishay Dale TWOP75230W receiver. This receiver is optimized for receiving a 30 kHz carrier, and also filters out many types of background noise.

With the limited number of components, this project can easily be constructed on a breadboard. The schematic is included in Appendix A: “Schematic”.

The project has been written in assembly, and can be easily ported to other PIC® microcontrollers which contain the CLC. Full source code is included in “Appendix B”. The project uses 124 locations of program memory and five bytes of RAM, leaving lots of room for customization.

Power consumption has been minimized by keeping the microcontroller in a Sleep state when not in use. A button press wakes the device from Sleep, message transmission occurs and the device goes back to its Sleep state when transmission is completed. Very low Sleep current (in the nA range) serves to extend battery life.

This technical brief will also demonstrate how the CLC module can be dynamically updated during operation. Updating the CLC during operation avoids external routing of signals, thereby reducing pin count. The pin count reduction may allow transitioning to lower-cost packages. An intuitive way to construct a PCM signal would be the following (see Figure 1):

FIGURE 1: INTUITIVE CONSTRUCTION OF PCM REMOTE

This will work, but it uses three pins. A simpler configuration can be constructed where the other input to the ‘AND’ gate is controlled from within the CLC module itself (see Figure 2).

FIGURE 2: SIMPLIFIED CONSTRUCTION OF PCM REMOTE

This has the advantage of using two less I/O pins and simplifies the design.
The PWM module will be used to create the 30 kHz signal, and this will then be gated (enabled or disabled) through an ‘AND’ gate in the CLC module. The modulation will be controlled directly by using one of the polarity bits in the CLC module. Using the PWM allows flexibility for creating different frequencies, while controlling the signal from within the CLC module allows for a variety of signal formats, including number of bits, parity, checksum, etc.

The initial configuration of the CLC module is done using the CLC Designer Tool. We initially want the output signal “off”, so we design it such that GATE 4 output will control whether or not the PWM3OUT signal is present at the output pin. This polarity is switched through the CLC1POL<3> bit. This will be the initialized state of the CLC module, where the output signal is turned off (always 0) (see Figure 3).

FIGURE 3:  CLC1 MODULE CONFIGURED TO OUTPUT ‘0’
When the output of GATE 4 is inverted, we get the PWM3OUT signal coming out of the CLC module (see Figure 4):

**FIGURE 4: CLC1 MODULE CONFIGURED TO OUTPUT PWM3OUT SIGNAL**

With the CLC module configured, we also need to configure our PWM to output a 30 kHz waveform.

**EQUATIONS:**

For 30 kHz, we want a period of:

\[ T_{osc} = \frac{1}{F_{osc}} = \frac{1}{30000} = 33.3 \, \mu s \]

PWM period is calculated from the following equation:

\[ PWM \, Period = (PR2 + 1) \times 4 \times T_{osc} \times TMR2 \text{ prescale} \]

Solving for PR2:

\[ PR2 = \left(\frac{PWM \, Period}{(4 \times T_{osc} \times TMR2 \text{ prescale})}\right) - 1 \]

For \( T_{osc} = 62.5 \, \text{ns} \) (16 MHz oscillator clock) and \( TMR2 \) prescale = 1 (no prescale):

\[ PR2 = \left(\frac{33.3 \, \mu s}{(4 \times 62.5 \, \text{ns} \times 1)}\right) - 1 = 132 \]

For a 50% duty cycle, we want to set our PWM duty cycle to half this value: \((132/2) = 66\)

**PERIPHERAL PIN SELECT (PPS) SETTINGS**

Peripheral Pin Select (PPS) is a feature which allows digital peripheral input/output signals to be mapped to physical pins. The photo-diode (and associated resistor) are connected to the RC2 pin (see Figure 5). In order to connect the CLC1 output to the RC2 pin, we need to write a value of \(0x04\) to the RC2PPS register.

**FIGURE 5: SCHEMATIC SHOWING PHOTODIODE CONNECTED TO RC2 PIN**
PUSH-BUTTON OPERATION

This simple example uses one push button, but could easily be extended to add more buttons. The single push button that causes transmission to occur is connected to the RB7 pin. In order to minimize external components, we are using the internal pull-up resistor to pull the pin high. Pressing the button (tied to GND) pulls the signal down and causes the device to wake from Sleep.

PULSE CODE MODULATED (PCM) SIGNAL OUTPUT

With the CLC and PWM module now properly configured, we see that we get the PWM output when the control signal is high, and we get no output when the control signal is low. The top signal (green) is the same signal as CLC1POL<3>, but is replicated on a pin for visualization. It should be noted that a Scope Trigger signal is available on the RC6 pin (see Figure 6).

FIGURE 6: PCM OUTPUT SIGNAL

A closer view verifies that the PWM is generating a 30 kHz waveform (see Figure 7):

FIGURE 7: CLOSE-UP OF PCM SIGNAL TO VERIFY 30 kHz OPERATION

DATA RECEPTION/DEMODULATION

The scope plot below shows the PCM data signal (yellow). Transmitted and received data are also shown (green and purple, respectively). It should be noted that the received data is inverted. Feeding the OUT (TSOP75230W) signal into a microcontroller and sampling in the middle of the bit time easily recreates the transmitted data (see Figure 8).

FIGURE 8: PCM TRANSMITTED AND RECEIVED WAVEFORMS

Zooming in on the start of the transmission, we can see how long it takes for the receiver to demodulate the signal. The receiver takes about eight cycles of the 30 kHz carrier before it transitions (see Figure 9).

FIGURE 9: WAVEFORM SHOWING TIME FOR RECEIVED SIGNAL TO TRANSITION
Capturing the same signal again, but with infinite persistence on the scope, we can see that the receiver chip operates very consistently and causes the signal transition to take place after about eight cycles (@ 30 kHz) (see Figure 10).

**FIGURE 10:** INFINITE PERSISTENCE SHOWING STABLE TRANSITIONS

LOW-POWER SLEEP STATE

In order to reduce current consumption, we will have the device remain in Sleep mode, wake-up when the button is pressed, transmit data, and then return to the Sleep state. The flowchart below (see Figure 11) shows the basic operation of the remote control transmitter.

**FIGURE 11:** REMOTE CONTROL TRANSMITTER BASIC OPERATION
CONCLUSION

This tech brief has demonstrated how to configure the CLC to work with the PWM and act as a PCM transmitter. The CLC module is used with no external pins required for signal routing. This project can be used as a starting point for low-power remote control transmitters.
APPENDIX B:

#include "p16f1708.inc"
#define TX_DATA0x5A ; this is the date that will be transmitted - example.
tx_register equ 0x70 ; RAM location for transmit data (Common RAM)
tx_counter equ 0x71 ; counts bits in the transmission
baud_counta equ 0x72 ; counter for baud rate delay
baud_countb equ 0x73
deb_count equ 0x74 ; counter for debounce

start
    org 0x0000
    nop
    banksel ANSELB
    clrf ANSELB ; make port B digital
    clrf ANSELA ; make port B digital
    clrf ANSELB ; make port C digital
    banksel TRISC
    clrf TRISC ; port C all outputs
    movlw 0x80
    movwf TRISB ; port B all outputs, except RB7
    clrf TRISA ; port A all outputs

    #include "pwm3and.inc" ; load Configurable Logic Cell settings.
    ; these settings allow PWM3 OUT to pass through,
    ; or pin outputs '0'.
    banksel RC2PSS
    movlw 0x04
    movwf RC2PSS ; selects CLC1 output for RC2 pin.
    banksel VREGCON
    movlw 0x03
    movwf VREGCON ; low power mode for Sleep
    banksel WFUB
    movlw 0x80
    movwf WFUB ; turn on weak pull-up on RB7
    banksel OPTION_REG
    bcf OPTION_REG, 7 ; enable weak pull-ups
    banksel IOCN
    bsf IOCN, 7 ; enable interrupt-on-change (falling edge) on RB7
    bcf IOCBF, 7 ; clear interrupt-on-change flag.
    banksel OSCCON
    movlw 0x70
    movwf OSCCON ; 16 MHz oscillator
```assembly
banksel PR2
movlw .132 ; set up period of 30 kHz
movwf PR2 ; for Timer2.

banksel PWM3DCH
movlw .66 ; 50% duty cycle
movwf PWM3DCH ; for PWM3.
clr PWM3DCL
banksel T2CON
clr T2CON ; 1:1 prescaler for Timer2.
bsf T2CON, TMR2ON ; turn on Timer2.
banksel PWM3CON
bsf PWM3CON, 7 ; turn on PWM3
banksel INTCON
bcf INTCON, IOCIF ; make sure interrupt flag is clear
bsf INTCON, IOCIE ; and then enable the interrupt

main_loop

sleep ; go to sleep - low current mode.
nop
nop ; wake-up occurs here.
nop ; does not go to interrupt vector because
    ; GIE is not enabled

debounce

movlw 0xff
movwf deb_count ; initialize debounce counter.

deb_a

call bit_delay
btfss PORTB, 7 ; Has button been released?
goto debounce ; No.
decfsz deb_count ; Yes. Has it been released for a while?
goto deb_a ; No.

movlw TX_DATA ; transmit data
movwf tx_register ; moved to transmit register.
call transmit

transmit

banksel LATC
bsf LATC, 6
bcf LATC, 6 ; scope trigger
movlw 0x08
movwf tx_counter

next_bit

rlf tx_register, F ; rotate left to get next bit.
decfsz tx_counter, F ; decrement bit counter. Am I done?
goto tx_a ; No.
bcf CLC1POL, 3 ; Yes. Drop signal low at end of transmission.
```
transmit_zero
  bcf CLC1POL, 3 ; CLC output = 0
  call bit_delay
  goto next_bit

transmit_one
  bsf CLC1POL, 3 ; CLC outputs PWM3 OUT
  call bit_delay
  goto next_bit

bit_delay
  clrf baud_counta
  clrf baud_countb ; clear counter

bit_delay_loop
  incf baud_counta, F
  btfss STATUS, Z ; did I rollover?
  goto bit_delay_loop ; No
  incf baud_countb, F ; Yes. Increment higher byte
  movlw 0x08
  subwf baud_countb, W
  btfss STATUS, Z ; Am I at end of bit time?
  goto bit_delay_loop ; No.
  return ; Yes.

end
APPENDIX C:

; PPS Initialization

BANKSEL CLCIN0PPS
movlw H'00'
movwf CLCIN0PPS
movlw H'00'
movwf CLCIN1PPS
movlw H'00'
movwf CLCIN2PPS
movlw H'00'
movwf CLCIN3PPS

BANKSEL CLC1GLS0
movlw H'02'
movwf CLC1GLS0
movlw H'00'
movwf CLC1GLS1
movlw H'00'
movwf CLC1GLS2
movlw H'00'
movwf CLC1GLS3
movlw H'0E'
movwf CLC1SEL0
movlw H'00'
movwf CLC1SEL1
movlw H'00'
movwf CLC1SEL2
movlw H'00'
movwf CLC1SEL3
movlw H'06'
movwf CLC1POL
movlw H'82'
movwf CLC1CON
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