INTRODUCTION

The UPD1001/UPD1002 USB Power Delivery Controllers from Microchip are configurable USB Power Delivery Controllers that adhere to USB Power Delivery Specification 1.0 and enable a USB host and devices to provide and/or consume 5-20V at up to 5A using negotiated power contracts.

This document describes common guidelines for designing with the UPD100x family devices.

UPD1001/UPD1002 Features

- Integrated USB Power Delivery (PD) PHY
- Support for Power Delivery Message Protocol
  - Message communications
  - Retry generation
  - Error handling
  - State behavior
- Cable detect logic
- Dead battery support
- Integrated voltage (VMON) and current (IMON) ADC inputs
- On-chip microcontroller
  - Manages I/Os
  - Implements the PD Policy Engine
  - Implements the PD Device Policy Manager
- Standalone configuration profile selection with CFG_SEL pins
  - Provider
  - Consumer/Provider
  - Provider/Consumer (UPD1002)
- Serial Peripheral Interface (SPI) ROM controller
- Internal 3.3V and 1.8V voltage regulators
- 32 pin SQFN (5 x 5 mm) package (UPD1001, UPD1002)
- 28 pin TSSOP (5 x 8.1 mm) package (UPD1001 only)

References

- Microchip Technology Inc., AN 26.2 Implementation Guidelines for SMSC's USB 2.0 and USB 3.0 Hub Devices, Revision 2.0 (07/13)
- Microchip Technology Inc., AN 26.21 USB Device Design Checklist, Revision 1.0 (06/13)
Operation

Upon power-on, the CFG_SELx signals are sampled with the Configuration Select block to select the desired PD Profiles. The microcontroller manages the policy engine and establishes VBUS communications with the Power Delivery AFE block. The I/O controller drives and samples I/O signals as required to control and monitor the power domains on the system. The VMON and IMON signals are sampled to sense PD VBUS voltage and current, respectively.
SYSTEMS DESIGN

The process for designing a UPD100x application begins with selecting the appropriate USB Power Delivery controller. The following table describes target applications by part number.

TABLE 1: SYSTEMS DESIGN

<table>
<thead>
<tr>
<th>UPD1001</th>
<th>Applications</th>
<th>PD Connector</th>
<th>UPD1002</th>
<th>Applications</th>
<th>PD Connector</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Provider</strong></td>
<td>AC Adapters</td>
<td>USB-A</td>
<td><strong>Provider</strong></td>
<td>Monitors</td>
<td>USB-A</td>
</tr>
<tr>
<td></td>
<td>Wall Chargers</td>
<td></td>
<td></td>
<td>Docking Stations</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Desktop PCs</td>
<td></td>
</tr>
<tr>
<td><strong>Consumer/Provider</strong></td>
<td>Monitors</td>
<td>USB-B</td>
<td></td>
<td>Printers</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Docking Stations</td>
<td></td>
<td></td>
<td>Automotive</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Printers</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Consumer</strong></td>
<td>AC Adapters</td>
<td>USB-B</td>
<td><strong>Provider/Consumer</strong></td>
<td>Notebooks</td>
<td>USB-A</td>
</tr>
<tr>
<td>/ <strong>Provider</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>USB-microAB</td>
</tr>
</tbody>
</table>

**UPD1001 Overview**

The UPD1001 is intended for designs which must solely source power for other chargeable devices, such as for AC Adapters and Chargers, using USB-A and USB-B standard connectors. These applications generally do not involve USB data transfers.

There are two base system configurations:

- Utilizing the USB-A connector to enable the Provider role
- Implementing the USB-B connector to enable the Consumer/Provider role

**UPD1001 Provider: USB-A**

In this configuration there are no PD Consumer capabilities, and the system is always a Provider (no role swaps). There are 30 configuration options in this mode, see datasheet for details. All configurations start as a standard USB-A port providing 5V and later may switch to a higher voltage and/or current limit if a contract is established. Cold socket detection is supported with the INSERTION_DETECT signal, therefore no VBUS voltage will be available at the USBPD-A connector until a USB device is connected. The PD_DETECT signal is used to detect the presence of a PD cable and allow PD contracts at > 5V. A port controller such as the Microchip UCS1001 can be used to add USB BC1.2 battery charging in dedicated charging port (DCP) mode, the signal CHG_EMU_EN is used for this. An example application is a USB wall charger that can charge non-PD enabled devices at 5V and suitable PD Consumer devices at higher voltage/current limits.

**UPD1001 Consumer/Provider: USB-B**

In this configuration the system starts as a 5V, 0A PD Consumer, initiating a swap request to become a PD Provider. There are 24 configuration options in this mode. One requirement in this configuration is support for dead battery operation. If no VBUS voltage is detected approximately every 3 seconds a current limited 5V output is enabled. If a bitstream is received the full 5V output is enabled and a contract can be established for higher voltage and/or current. The
PD_ID signal is used to detect the presence of a PD cable and its current capacity by sampling cable markers in the cable. An example application is an AC adapter for a PD enabled laptop. The AC adapter could have multiple USBPD-B ports to charge multiple laptops or other devices.

FIGURE 2: UPD1001 32SQFN EXAMPLE OF TYPE-A PROVIDER
UPD1002 Overview

The UPD1002 is designed for Monitors, Docking stations, Desktop and Notebook PCs, Printers, and Automotive applications. These applications involve USB data transfers and typically include a USB hub. Some example application diagrams are shown to illustrate the following systems:

- A Provider application (such as an automotive breakout box) with the Type-A receptacle
- A Consumer/Provider application (example: docking station) with the Type-B receptacle
- A Provider/Consumer application (as would be required in a notebook computer) with the Type-A receptacle
- A Provider/Consumer application (e.g. a tablet) with the MicroAB receptacle

UPD1002 Provider: USB-A

In this configuration there are no PD Consumer capabilities, the system is always a Provider (no role swaps). There are 5 configuration options in this mode, see Datasheet for details. All configurations start as a standard USB-A port providing 5V and later may switch to a higher voltage and/or current limit if a contract is established. Cold socket detection is supported with the INSERTION_DETECT signal, therefore no VBUS voltage will be available at the USBPD-A connector until a USB device is connected. The PD_DETECT signal is used to detect the presence of a PD cable and allow PD contracts at > 5V. A USB hub with battery charging support such as the Microchip USB5534 can be used to add battery charging capability in DCP and CDP modes. An example application is a USB-A downstream port on a desktop computer monitor. A PD enabled USB device that requires voltages > 5V to operate can be powered from this port directly without the need for an additional power supply.

UPD1002 Consumer/Provider: USB-B

In this configuration the system starts as a 5V, 0A PD Consumer, initiating a swap request to become a PD Provider. There are 9 configuration options in this mode. One requirement in this configuration is support for dead battery operation. If no VBUS voltage is detected approximately every 3 seconds a current limited 5V output is enabled. If a bitstream is received the full 5V output is enabled and a contract can be established for higher voltage and/or current. The signal VBUS_OUT is used to keep the USB hub upstream facing port connected when a valid VBUS voltage is present.
which can range from 4.5V to 20V. There are up to three VSELx_N signals to select the source voltage. The PD_ID signal is used to detect the presence of a PD cable and its current capacity by sampling cable markers in the cable. An example application is a USB-B upstream port on a desktop computer monitor. Connecting a laptop with a USBPD-A port to this port will power and charge the laptop battery.

**UPD1002 Provider/Consumer: USB-A**

There are 10 configuration options in this mode, including 6 PD Consumer options at 12V at 1.5A, 3A, and 5A, and 4 PD Consumer options at 20V at 3A and 5A. All configurations start as a standard USB-A port providing 5V at up to 2A depending on the configuration. If a consumer contract is established a role swap will occur to become a consumer at a higher voltage. Cold socket detection is supported with the INSERTION_DETECT signal, therefore no VBUS voltage will be available at the USBPD-A connector until a USB device is connected. The PD_DETECT signal is used to detect the presence of a PD cable and allow PD contracts at > 5V. A port controller such as the Microchip UCS1001 can be used to add USB BC1.2 battery charging in dedicated charging port (DCP) mode, the signal CHG_EMU_EN is used for this. A USB hub with battery charging support such as the Microchip USB5534 can be used to add battery charging capability in DCP and CDP modes. An example application is a USB-A downstream port on a laptop. This enables the laptop to be powered and battery charged from this port when connected to a suitable PD Consumer/Provider.

**UPD1002 Provider/Consumer: USB-uAB**

There are 6 configuration options in this mode, including 4 PD Consumer options at 12V at 1.5A, and 3A, and 2 PD Consumer options at 20V at 3A. All configurations start as a standard USB-A port providing 5V at up to 2A depending on the configuration. If a consumer contract is established a role swap will occur to become a consumer at a higher voltage. The PD_ID signal is used for insertion detect, uA plug or uB plug detection, and PD cable detection. A USB3 hub with battery charging support such as the Microchip USB5534 can be used to add battery charging capability in DCP and CDP modes using the CHG_EMU_EN signal. An example application is a USB-uAB connector on a tablet. This enables the tablet to be powered and battery charged at a higher voltage (for reduced charging time) from this port when connected to a suitable PD Consumer/Provider.
FIGURE 5: UPD1002 32SQFN EXAMPLE OF TYPE-B CONSUMER/PROVIDER

FIGURE 6: UPD1002 32SQFN EXAMPLE OF TYPE-A PROVIDER/CONSUMER
PD Profile Selection

Once the part is selected the next step is to select the appropriate PD Profile configuration. From the datasheet for the corresponding part the CFG_SELX CONFIGURATION ASSIGNMENTS tables show the configuration options available. There are 54 options available for the UPD1001 and 30 available for the UPD1002. The CFG_SELx bin column entries are then used to select the resistor and capacitor values to use for the selected PD profile. Below are two examples of how to determine the correct configuration to select for UPD1001 and UPD1002 designs.

EXAMPLE 1: UPD1001-BASED DESIGN:

A USB-PD wall charger (Provider) design needs to provide 5V at 2A and 12V at 1.5A, and use the Type-A receptacle. Profile 2 defined by the USB Power Delivery Specification meets these requirements. Using the CFG_SELX CONFIGURATION ASSIGNMENTS list (Table 3-3 and 3-4 in the UPD1001 data-sheet), Configuration 7 matches the requirements for Profile 2 PD support on Type-A receptacles. In order to select Configuration 7, the UPD1001 needs to be strapped with CFG_SEL1=Bin 1 and CFG_SEL0=Bin 7.
TABLE 2: UPD1001 PROFILE SELECTION TABLE EXCERPT

<table>
<thead>
<tr>
<th>Config #</th>
<th>32-SQFN Pin Config.</th>
<th>Receptacle Type</th>
<th>PD Consumer Abilities</th>
<th>PD Provider Abilities</th>
<th>VSEL0_0</th>
<th>VSEL1_0</th>
<th>VSEL2_0</th>
<th>VSEL3_0</th>
<th>CFG_SEL0 Bin</th>
<th>CFG_SEL1 Bin</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>32-A</td>
<td>STD-A</td>
<td>None</td>
<td>Profile 1</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>32-A</td>
<td>STD-A</td>
<td>None</td>
<td>Profile 1, 5V@3A</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>32-A</td>
<td>STD-A</td>
<td>None</td>
<td>Profile 1, 5V@5A</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>32-A</td>
<td>STD-A</td>
<td>None</td>
<td>Profile 1, 9V@2A</td>
<td>5</td>
<td>9</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>32-A</td>
<td>STD-A</td>
<td>None</td>
<td>Profile 1, 20V@3A</td>
<td>5</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>6</td>
<td>32-A</td>
<td>STD-A</td>
<td>None</td>
<td>Profile 1, 20V@5A</td>
<td>5</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>7</td>
<td>32-A</td>
<td>STD-A</td>
<td>None</td>
<td>Profile 2</td>
<td>5</td>
<td>12</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>7</td>
</tr>
</tbody>
</table>

From the CFG_SELX PIN RESISTOR-CAPACITOR BIN ALLOCATION table:
Bin 1: R=2.7k, C=None
Bin 7: R=4.87k, C=4.7nF

TABLE 3: UPD100X CFG_SELX BIN ALLOCATION TABLE

<table>
<thead>
<tr>
<th>Bin</th>
<th>( R_x (+/-1%) )</th>
<th>( C_x (+/-10%) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2.70 kΩ</td>
<td>None</td>
</tr>
<tr>
<td>2</td>
<td>2.70 kΩ</td>
<td>470 pF</td>
</tr>
<tr>
<td>3</td>
<td>4.87 kΩ</td>
<td>470 pF</td>
</tr>
<tr>
<td>4</td>
<td>8.66 kΩ</td>
<td>470 pF</td>
</tr>
<tr>
<td>5</td>
<td>15.40 kΩ</td>
<td>470 pF</td>
</tr>
<tr>
<td>6</td>
<td>2.70 kΩ</td>
<td>4.7 nF</td>
</tr>
<tr>
<td>7</td>
<td>4.87 kΩ</td>
<td>4.7 nF</td>
</tr>
<tr>
<td>8</td>
<td>8.66 kΩ</td>
<td>4.7 nF</td>
</tr>
<tr>
<td>9</td>
<td>15.40 kΩ</td>
<td>4.7 nF</td>
</tr>
<tr>
<td>10</td>
<td>2.70 kΩ</td>
<td>47.0 nF</td>
</tr>
<tr>
<td>11</td>
<td>4.87 kΩ</td>
<td>47.0 nF</td>
</tr>
<tr>
<td>12</td>
<td>8.66 kΩ</td>
<td>47.0 nF</td>
</tr>
<tr>
<td>13</td>
<td>15.40 kΩ</td>
<td>47.0 nF</td>
</tr>
<tr>
<td>14</td>
<td>2.70 kΩ</td>
<td>470 nF</td>
</tr>
<tr>
<td>15</td>
<td>4.87 kΩ</td>
<td>470 nF</td>
</tr>
<tr>
<td>16</td>
<td>8.66 kΩ</td>
<td>470 nF</td>
</tr>
</tbody>
</table>

Note: CFG_SEL0 and CFG_SEL1 bin definitions are identical
The UPD1001 CFG_SELx pins must be connected as shown:

![UPD1001 CFG_SEL Example 1](image)

**EXAMPLE 2: UPD1002-BASED DESIGN**

A Provider/Consumer design needs to provide 5V at 2A and consume 20V at 5A. From the UPD1002 datasheet CFG_SELX CONFIGURATION ASSIGNMENTS Table3-3, Configuration 23 meets these requirements and shows a PD Provider Profile 1 (5V@2A) and a PD Consumer profile of 20V@5A, with CFG_SEL1=Bin 2 and CFG_SEL0=Bin 1.

**TABLE 4: UPD1002 PROFILE SELECTION TABLE EXCERPT**

<table>
<thead>
<tr>
<th>Provider/Consumer</th>
<th>32-PC_A</th>
<th>STD-A</th>
<th><a href="mailto:12V@1.5A">12V@1.5A</a></th>
<th>VSafe5V-L</th>
<th>N/A</th>
<th>N/A</th>
<th>N/A</th>
<th>1</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>12V@3A</td>
<td>VSafe5V-L</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>1</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>12V@3A</td>
<td>Profile 1</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>1</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>12V@3A</td>
<td>Profile 1, PP-200</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>1</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>12V@5A</td>
<td>Profile 1</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>1</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>12V@5A</td>
<td>Profile 1, PP-200</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>1</td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>20V@3A</td>
<td>Profile 1</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>1</td>
<td>7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>20V@3A</td>
<td>Profile 1, PP-200</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>1</td>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>20V@5A</td>
<td>Profile 1</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>2</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>20V@5A</td>
<td>Profile 1, PP-200</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>2</td>
<td>2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

From the CFG_SELX PIN RESISTOR-CAPACITOR BIN ALLOCATION table:

Bin 2: R=2.7k, C=470pF
Bin 1: R=2.7k, C=None
The UPD1002 CFG_SELx pins must be connected as shown:

**FIGURE 9: UPD1002 CFG_SEL EXAMPLE 2**

![Diagram of UPD1002 CFG_SEL Example 2](image)

**Design Requirements and Recommendations**

**UPD100X POWER**

- The required UPD100x filtering/decoupling capacitors are shown in the figure below:

**FIGURE 10: UPD100X POWER AND DECOUPLING**

![Diagram of UPD100x Power and Decoupling](image)

**COMMON USB DATA DESIGN RECOMMENDATIONS**

USB Power Delivery systems which augment existing USB hosts or devices will typically support USB data transfers, and the guidelines for both USB Power Delivery and USB data should be applied to the physical design.

The design priority should be to first utilize the design guidelines for the USB data devices (such as hubs, transceivers, device/host controllers) in the system first and then override those by the VBUS guidelines provided in this document.
USB data path guidelines:

1. In Power Delivery designs, VBUS can experience high dI/dt transients which will couple into adjacent signal paths. USB differential data lines should ideally be routed at least 5 VBUS trace widths away from the VBUS path.

2. Keep USB differential traces as short as practical to minimize parasitic losses and maintain highest signal integrity.

3. Route USB data traces on outer layers, rather than on inner layers.

4. Consider laminates with lower DF and DK ratings, such as:
   - FR408HR
   - FR408HRIS
   - N4000-13SI
   - Rogers
   - Polyimide

5. Try to route USB data signals at a 45-degree angle to the material weave direction so that the trace does not occasionally line up with a high-resin, high-loss path.

Grounding:

- The USB data environment requires that the ground return paths across the system be implemented carefully and that they be substantial and contiguous. Employ “stitching vias” to connect ground floods between multiple layers and to terminate ground flood “spurs”.

Shielding:

Microchip has observed positive EMI and ESD behavior on stand-alone designs when connecting the USB cable shield to digital ground with an RC network (330 Ω resistor and a 0.1 μF capacitor in parallel) at each USB connector as shown in the below figure.

**FIGURE 11:** USB RECEPTACLE SHIELD RECOMMENDATION
USB VBUS

- Because the USB Power Delivery protocol is communicated using FSK modulated packets across the VBUS conductor of the USB cable, the AC signalling path must be separated from the DC path at the receptacle of each Power Delivery device.

**FIGURE 12: VBUS DC POWER AND FSK DATA PATHS**

All power sources, power sinks, and capacitance must be isolated behind an appropriately sized >1uH choke in order to prevent attenuation of the Power Delivery FSK signaling and limit the AC noise introduced to system DC power tree.

- Power Delivery Provider-capable devices must be able to discharge VBUS to below 0.4V within 80 milliseconds in order to meet the specification requirements with margin, and ensure safety of legacy USB devices. In typical applications, this may be achieved using an N-channel power MOSFET with its gate controlled by the UPD100x’s VBUS_DISCHARGE pin.

- The required impedance of the VBUS discharge path to satisfy the discharge timing will differ depending upon each given system’s permitted maximum VBUS voltage and total VBUS source & sink capacitance.

- The VMON pin is an ADC channel input which must be scaled such that 3V at the VMON input represents 24V at the PD VBUS. Using a resistor divider as shown below will provide the correct voltage scaling.

**FIGURE 13: VMON INPUT SCALAR**

- The IMON pin is an ADC channel input which measures current being sourced out of the USB port (e.g. current being provided by the system, to another device) and must be scaled such that 3V at the IMON input represents 6A of current flowing out of the PD VBUS network.

- Note that the IMON input is only interpreted by the UPD100x only when it is in the PD Provider role, for coarse current measurements.

- UPD100x signals which are electrically connected to exposed USB receptacles should be clamped to safe voltages:
  - VMON pin should have external diode clamps, tied to VDDIO and VSS to suppress voltage transients such as power supply transitions and charged cable attach/detach events.
  - PD_DATA pin should have external diode clamps to PD_VDD18 and VSS to suppress voltage transients such as power supply transitions and charged cable attach/detach events.

- When using Power MOSFETs to switch high current rails take extra care to select devices which exhibit low $R_{DS(ON)}$ as the drain to source voltage drops at high currents can be significant.

- Verify high voltage rail behavior during power on and power off to insure that high voltage spikes that can exceed the limits of the circuit and the USB Power Delivery specification are not generated. Clamping diodes, capacitors, transient voltage suppressors, and snubber circuits can be used to help in reducing excessive voltages.
**SPI ROM**

The UPD100X devices operate using an external SPI Flash Memory with the following characteristics:

- 3.3V I/O
- Dual-bit read operations
- 64KByte storage
- >=48MHz clock speed

The Microchip SST25VF064C SPI Flash module is one example device which meets these operational requirements.

**DEAD BATTERY SUPPORT**

- A Consumer/Provider system (classically identified as a “USB device”, e.g. those with Type-B or MicroB receptacles) must periodically provide the vSafeDB current-limited voltage as specified in the USB Power Delivery 1.0 specification, in order to enable charging a battery-powered Provider/Consumer (classically identified as a “USB host”, with its Type-A receptacle) device which is in a dead battery state.
- When the Consumer/Provider identifies that no VBUS is currently being supplied onto the cable by a host, it will drive VBUS with vSafeDB.
- vSafeDB is defined as a current limited voltage supply which operates within the “C/P area of operation” as shown in the below figure, which disallows any current >90mA from being sourced by the vSafeDB supply.
- The specification for vSafeDB requires that a 4 to 5.25V voltage source be periodically applied every 15 seconds or less (typically every 10 seconds) at most. The UPD100x controls the dead battery supply via the VSAFEDB_EN signal.

**FIGURE 14: DEAD BATTERY OPERATIONAL REGIONS**

- When designing a Consumer/Provider system verify that there is a clean monotonic transition from dead battery power to full power (reference the USB Power Delivery 1.0 specification for power transient characteristics)
- For a Provider/Consumer supporting dead battery (UPD1002 only):
  - The UPD100x VBUS pin 5 (available only in 32QFN package) is a 5V power input pin, and is only used with the UPD1002 Provider/Consumer configurations in order to allow the UPD1002 to be powered from the USB VBUS rail during the dead battery condition. In this condition, the power supplied to the UPD VBUS power pin will be used to drive the on-chip 3.3V and 1.8V regulators.
  - If the Power Delivery profile supported by the UPD1002 Provider/Consumer allows for >5V contracts, then a 5V regulator is required to be placed between the USB VBUS network and UPD1002 VBUS pin 5. This connection of the UPD1002 VBUS power pin to the USB VBUS network enables a UPD1001 or UPD1002 Consumer/Provider to power the UPD1002 Provider/Consumer during a dead-battery scenario. **Note:** For all other configurations, the UPD100x pin 5 (32QFN) may be connected to ground.
- The external SPI Flash Memory device must be powered from UPD VDDIO.
- The reset input must be negated by a VDDIO pullup network
- The power tree must be designed such that only the UPD1002, its companion SPI Flash Memory, and a UPD VBUS 5V regulator should be powered via the USB VBUS network, as a current limited supply (<90mA) is providing that power.

- The PD_Data line requires an isolation filter, the recommended circuit is shown below:

```
PD_DATA
24
470nH
5% 300mA
L1
C1
100pF
5% 50V
PD VBUS
USB

L1: Boums CE201210-R47J
C1: Murata GCM1885C1H101JA15D
```

- For successful PD_DATA communications it is critical to pay close attention to noise on VBUS due to supply switching harmonics, poor PCB layout and grounding, and low quality components. The USB PD Specification (chapter 7) includes a noise spectral mask as shown below. VBUS noise levels must meet these requirements for reliable communications.

![Noise Spectral Mask](image)

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>Maximum Allowed Signal Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;10 (A)</td>
<td>-10 (dB) 178.7 (mVpp)</td>
</tr>
<tr>
<td>19.7 (B) to 26.7 (C)</td>
<td>-37 (dB) 7.92 (mVpp)</td>
</tr>
<tr>
<td>&gt;32 (D)</td>
<td>-30 (dB) 17.8 (mVpp)</td>
</tr>
</tbody>
</table>
APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

<table>
<thead>
<tr>
<th>Revision Level</th>
<th>Section/Figure/Entry</th>
<th>Correction</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Note:</strong></td>
<td>AN23.02, Revision A replaces the previous SMSC version, Revision 1.1.</td>
<td></td>
</tr>
</tbody>
</table>
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