INTRODUCTION

Switched Mode Power Supplies (SMPS) are useful and efficient in converting one voltage/current into another. One of the major limitations of an application-specific integrated circuit (ASIC) SMPS solution is right in the name, “application specific”. Practically, this means that the device has been optimized for a specific set of features and system performance specifications. Even devices with optional features and functions are still ultimately fixed due to use of component values and board layout to enable and configure its options. While external circuitry could be used to make a device more configurable, the single chip approach of a Core Independent Peripheral (CIP) based design is both smaller and capable of much greater flexibility. Some Core Independent Peripherals are intelligent analog peripherals (e.g., Comparator, op amp) linked to an 8-bit microcontroller that allow adjustment of many SMPS control-related parameters while the power supply is in operation. This capability opens the possibility for on-the-fly performance evaluation and optimization.

This application note will focus on the advantages of reconfigurability through the evaluation of a few areas of design, such as:

- Flexible control topology implementation
- Multiple control loops with the same IC
- Switching frequency control
- Limits control
- Internal slope compensation control
- Internal blanking, phase-delay and dead-band control
- Advantages of a programmable reference voltage
- Reallocating system resources on demand
- Communication, local data storage and capability to add new functions

To understand the advantages of configurability, a peek is taken into where configuration might be needed; what is the approach that other designs take, existing limitations and how CIP designs help fulfill these needs (with some examples).

Core Independent Peripherals and intelligent analog linked to an 8-bit microcontroller allow adjustment of many SMPS control-related parameters.

THE NEED FOR CONFIGURABILITY

There is a massive collection of SMPS controllers on the market and selecting what is needed for a project has become harder because most are implemented for only one specific application. Any change or new specification during development will require going back to selecting the proper SMPS controller and maybe redoing the layout.

Some of the limitations that show the advantage of configurability in modern SMPS controllers are:

Topology Change

In many cases, the specifications are updated during a project development, which requires a change in topology to adapt to new requirements. The designer is confronted with recalculations and component changes that are time consuming. Being hardwired by their layout, ASIC systems normally operate in a fixed topology configuration. Multiple topologies can be built, but they typically require external switching to facilitate the change.

Typical applications include:

- Buck-Bypass-Boost designs that use a buck configuration to step down voltage for the load when the source voltage is too high, then switch to Bypass mode when the source voltage drops into an acceptable range, and finally, to boost when the source voltage drops too low. This retains the higher efficiency of the buck and bypass, but does require additional switching MOSFETs.
- Bidirectional Buck-Boost designs that use a buck to charge a storage element (battery/super-cap) from a power supply, and then reverse and run in a boost configuration to support the power supply during high load conditions.

Control Mode

The inability to change the control method (Voltage Mode control - > Current Mode Control - > Variable Frequency Control etc.) can lead to the following:

- efficiency problems at low load
- controller change
- multiple controllers on projects with more than one control loop (ex: a two-stage PFC + Isolated Converter need two separate controllers)
Multiple Control Loops on the Same IC

It can be much easier and cost effective to have multiple control loops within one control IC, rather than using multiple ICs for each control loop independently.

Switching Frequency Control

Using external components to create the switching frequency generates noise problems, so internal frequency generation is recommended. The SMPS controller can have usage limitations if the internal switching frequency generator is fixed or limited to 2-4 values.

Improved Parameter Limit Control

Internally-set limits of parameters are usually fixed and do not permit changes. The user is forced to change the IC in order to change the limit values of each parameter.

Slope Compensation Control

Using external components to create slope compensation has linearity and noise problems. Internal slope compensation is a good solution to noise and linearity but in most cases is fixed and limits the IC use to a certain range.

Duty Cycle and PWM Control

For many SMPS applications, having the ability to control duty cycle and PWM-related values such as maximum/minimum duty cycle, blanking time, dead-band time and phase delay has become important. Having fixed internal settings may limit efficiency improvements and versatility of a controller.

Internal Reference Control

ASICs typically have just a fixed reference and the output voltage is determined by the resistor divider in the voltage feedback network. Having a programmable voltage reference allows:

- Output voltage trimming
- Software-based coordinated power-up
- Software-based soft start (custom power-up profile)

Access to Internal Signals and Information

Modern controllers have so many circuits integrated that it becomes hard for the designer to debug a converter. Having some degree of access to internal signals and data may become crucial for improving efficiency and implementing status control of a SMPS converter.

Function Addition

A SMPS controller becomes very limited and extra ICs have to be added to gain additional functions and control over the application. In many cases, the added IC is a microcontroller.

Need for Multiple ICs to Obtain a Complex Solution

Using ASIC controllers to implement a complex and smart SMPS converter often requires multiple ICs. Having everything in one controller may reduce cost, design effort, extra training time, learning curve and board size.

AVAILABLE ASIC SOLUTIONS

The need for configuration and control has spun multiple solutions in ASIC controllers such as:

Potentiometer for Output Voltage Control

The classic solution for controlling output voltage is to replace one of the output divider resistors with a potentiometer as depicted in Figure 1.

FIGURE 1: OUTPUT VOLTAGE CHANGE USING A POTENTIOMETER
Monitoring IC with On/Off Control

A solution that uses an external monitor and control device is used for more control, as depicted in Figure 2. The monitoring device can measure the output voltage and current levels, turn on and off the SMPS controller on Fault or limit conditions and provide monitoring data to the user with I²C communication. This solution adds monitoring while still maintaining an analog control loop. An example of a device that has adopted this solution is the LTC2970/LTC2970-1.

FIGURE 2: MONITORING ADDED TO A SMPS SOLUTION

Communication and Control Over Limited Variables

Figure 3 depicts an approach which provides control and communication for the TPS563900 from Texas Instruments. This controller has two buck converters and an I²C communication module integrated in the same chip.

FIGURE 3: USER HAS LIMITED CONTROL OVER TWO INTEGRATED BUCK CONVERTERS THROUGH THE I²C BUS

The level of control is limited to on/off, slew rate and output voltage level while the communication provides die temperature and output voltage within range status.

Power Management ICs (PMIC) expand this solution to more internal step-down converters with smaller output level range but more monitoring focus.

Communication, Monitoring and Configuration Over Multiple Variables

A more complete approach can be seen in parts like SC493 from Semtech or the LTC3880/LTC3880-1 from Linear Technology. They introduce switching frequency control (in steps), limit change, soft-start timing change and status for input/output voltages and currents as depicted in Figure 4.
FIGURE 4: A MORE DEVELOPED CONFIGURATION SYSTEM FOR SMPS CONTROLLERS

PROBLEMS AND LIMITATIONS TO LEGACY SOLUTIONS

Although legacy solutions to configurability problems provide some degree of control to the user, the following limitations can be seen:

Potentiometer for Output Voltage Control
- Beneficial only for minor output voltage adjustment (major output control may require adjustment of compensation components)
- Can be used only by manual change
- No monitoring capabilities

Monitoring IC with On/Off Control
- Additional external monitor IC required at additional cost
- Higher BOM count
- Larger board dimension
- No control over limits
- Only limited to on/off control over the SMPS loop

Communication and Control Over Limited Variables
- Limited to a dedicated topology and design
- Limited control over SMPS variables
- Monitoring only deliver “in-range” status

Communication, Monitoring and Configuration Over Multiple Variables
- Frequency and limit selection only in specified few steps
- Dedicated to a specific topology and application
- Monitoring only with STATUS register
- No extra functions can be added
- Very expensive solution

CIPs FOR SMPS APPLICATIONS

Before explaining what advantages the CIPs bring to the configuration ability of a SMPS solution, here is a list of intelligent peripherals available in the microcontroller that can be used to implement control loops and several functions:
- Comparators (Comp)
- Operational Amplifiers (op amps)
- Digital-to-Analog Converters (DACs)
- Programmable Slope Compensation
- Fixed Voltage Reference (FVR)
- Timers
- Zero-Cross Detection (ZCD)
- Analog-to-Digital Converter (ADC)
- Temperature Sensor
- Configurable Logic Cell (CLC)
- Complementary Output Generator (COG – used to generate the driver PWM control)

These are used to create multiple SMPS control methods. Besides the peripherals that can be used to implement a SMPS control, the PIC® MCU has storage, computation and communication capabilities that can be used to create and implement more function blocks.

CIP SOLUTION TO CONFIGURABILITY

The PIC16F176X/7X is a microcontroller family (PIC MCU) with CIPs designed to implement SMPS control logic. It offers multiple degrees of flexibility, control, configuration, communication capabilities and Flash memory for storage. The Flash memory can also be used to analyze data, compute and create smart functions.

The PIC® MCU allows a power supply designer to configure his own analog PWM controller. This offers a great opportunity to fix many of the bugs of old analog control chips, while also incorporating the flexibility of digital functions for complex designs. For many applications, this provides the best of both worlds.
The peripherals have the capability to interconnect to other peripherals or to external pins. This capability is maintained during run-time when connections can be changed and functions can be added or removed.

The designer can use the MPLAB Code Configurator plug-in to generate all of the code and to configure the part with just few clicks, with no coding skills being needed.

Superior configuration capabilities over the SMPS control loop offered by the CIPs include:

FLEXIBLE CONTROL TOPOLOGY IMPLEMENTATION

While ASICs enable only fixed functions with options that must be set by layout or external components, the flexibility to change connections between peripherals allows CIPs to be rearranged to obtain different control topologies. This way, the same microcontroller can be used to implement multiple control loops with the same pinout.

The same PIC MCU pinout used to implement the voltage-mode control loop, current-mode control loop, constant on-time control loop and critical conduction mode control loop is depicted in Figure 5.

The converter can run peak current-mode at full load and change during run time into voltage-mode control at light/no load to maintain the output voltage constant. The user is able to change from Continuous Conduction mode to Critical Conduction mode without the need to restart or unplug the application.

MULTIPLE CONTROL LOOPS

Some PIC MCUs has enough SMPS dedicated CIPs to run multiple control loops at the same time without the risk of interacting with each other. The same chip can run two, three or four SMPS topologies at the same time. Figure 6 depicts such an example, where the microcontroller implements two control loops at the same time. The designer can add functions to coordinate the power-up of the loops independently, add combined fault handling to prevent damage, use combined reference voltages or coordinate switching times and frequencies. As a practical example, PIC16F1769 can run two control loops while PIC16F1779 can run four control loops in the same time.
FIGURE 5: IMPLEMENTATION OF FOUR SMPS CONTROL SYSTEMS WITH THE SAME PIN CONNECTIONS OF THE PIC® MCU

Voltage Mode Control Configuration

Simple Constant ON-Time Control Configuration

Current Mode Control Configuration

Critical Conduction Current Mode Control Configuration
SWITCHING FREQUENCY CONTROL FOR FIXED FREQUENCY TOPOLOGIES

A significant issue with most classic SMPS ICs solutions is the susceptibility to noise that generates early clock Resets, timing glitches or frequency and duty-cycle jitter.

When using the microcontroller, the switching frequency for the SMPS is generated internally and no external components are used. The user has full control over the frequency value at any time and he or she can change it without the need of a Reset or Restart. The internal oscillator can create frequencies from 31 kHz to 32 MHz and the timer used to derive the needed switching frequency has 8-bit registers. This gives the user the chance to generate a switching frequency for SMPS control in the range of 0.1 Hz – 8 MHz with accuracy from 32 ns to 625 ms. Compared to other SMPS ICs that offer one fixed frequency or the possibility to change between four fixed available internal frequencies, the PIC MCU allows high configuration possibility.

CONTROL OVER SMPS LIMITS

One of the limitations in legacy designs is that the internal limits of the parameter are fixed and the controller is forced to work only with a specific range of signals. The designer cannot add limits on other signals and control is rarely provided or is very limited. The PIC MCU uses FVR and DAC to set configurable limits and references for Overvoltage Protection (OVP), Undervoltage Protection (UVP), Overcurrent Protection (OCP), Op Amp Reference Voltage (REF) and other limits needed by the designer. The DACs used are of five and ten bits and the value can be changed at any time during run-time for performance evaluation and optimization. External pins can be configured to become comparator inputs.

The ability to change the limits improves the application when a SMPS converter admits high input voltage variations to maintain a constant output voltage level and the primary peak current limit is placed to protect the secondary components. If the set limit is fixed, when the input voltage is changed, the overall limited power conversion is changed and the application may fail. CIPs enable the user to measure the input voltage (a proportion of the input voltage) with an ADC and adapt the primary peak current limit set, as depicted in Figure 7. This maintains a constant maximum allowed power conversion and protects the load. This solution can also be implemented using the op amp CIP, which eliminates any code supervision or ADC bandwidth limitations.
INTERNAL SLOPE COMPENSATION CONTROL

The solution to peak current-mode subharmonic loop instability is well known – adding a compensating ramp (Slope Compensation). Solutions used by ASIC controllers have the following issues:

- Layout noise susceptibility
- External component use
- Nonlinearity
- Design effort
- Non-configurable once the values are set
- Signal separation

The PRG CIP inside the PIC MCU is used to generate both falling and rising ramps. The designer has control over the rising event, falling event and even the slope rate. This allows the PRG to generate the needed sawtooth waveform for the voltage-mode control and the slope compensation ramp for current-mode control. The rising and falling events can come from other internal CIPs or from external sources through an I/O pin.

Because the PRG can generate rising and falling ramps, the designer can add slope compensation on the current sense waveform as a rising ramp or on the error feedback voltage waveform as a falling ramp. The slope rate can be configured by the user at start-up and changed during run time from 0.2V/us to 2.5V/us with steps of 0.05V/us and 0.1V/us.

**Note:** Slope compensation starts at a programmable duty cycle for optimized common-mode range in the error amplifier.

DUTY-CYCLE, BLANKING, DEAD-BAND AND PHASE-DELAY CONTROL

Most ASIC controllers have fixed duty-cycle limits once the external components are selected. This creates control limitation and noise at high duty cycles, which forces the designer to use the parts only in a specific range. A classic solution does not provide blanking and designers have to focus on signal filtering. Newer solutions have fixed blanking and the designer has to adapt the filter to those values.

The COG CIP is used to generate the PWM signal that drives the MOSFET driver and has six modes of operation used for SMPS purpose: steered PWM, synchronous steered PWM, forward full-bridge, reverse full-bridge, half-bridge and push-pull. The COG provides useful duty-cycle control features as dead-band, blanking and phase-delay that tend to become more of a necessity for modern SMPS controllers.

The Half-Bridge and Full-Bridge modes require dead-band control to prevent shoot-through in the power switches and the COG provides two 6-bit dead-band timers for rising and falling event control. The timer counts either using synchronous COG_clock or asynchronous delay chains.

To prevent electrical transients caused by the turn-on/off of power components from generating a false input event, the COG provides a blanking function to mask or blank the inputs for a short period of time.

There are two 6-bit blanking timers: one triggered by the rising event and the other by the falling event.

With the phase-delay counters provided by the COG, it is possible to delay the assertion of either or both the rising and falling events. The delay from the input rising event signal switching to the actual assertion of the events is calculated in the same way as the dead-band and blanking delays and are accessible to the user even during run-time.

To limit the maximum duty cycle in steered PWM mode, the designer can also add an extra CCP as a falling event to the COG, as depicted in Figure 8. The CCP will take control when the loop will require a higher duty cycle than allowed. This is useful when less than 100% duty cycle is wanted or when less than 50% is needed in a current-mode control loop without slope compensation.
The user has control over all these duty cycles and PWM-related functions. This flexibility is not seen in other SMPS controllers and provides advantages for a SMART design.

**FIGURE 8: CCP2 CONTROL OVER THE MAXIMUM ALLOWED DUTY CYCLE**

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**REFERENCE VOLTAGE CONTROL**

The op amp reference voltage has an important role in the control loop of a SMPS. The op amp in the MCU provides the possibility to connect an external source as input reference through an I/O pin or use the internal Fixed Voltage Reference (FVR). When FVR is connected to the DAC and then to the op amp input as depicted in Figure 9, the user has control to configure the value with 10-bit accuracy.

If the internal voltage reference does not satisfy the designer’s needs, an external reference could be used with the DAC.

Eg.: If a current-mode buck-boost converter is controlled by CIPs and the 10-bit DAC is used as reference for the op amp, the user gains control over the output voltage level by changing the DAC value. If the output divider that provides the feedback signal is selected at 1:5 proportion, every DAC value step will change the output voltage by 25 mV. The user can create a buck-boost converter that has output control from close to 0V to almost 25V with 25 mV steps.
FIGURE 9: USER HAS FULL CONTROL OVER THE OP AMP REFERENCE VALUE WITH THE DAC CIP

REUSE OF RESOURCES
One of the limitations in ASIC controller-based designs is that resources in the design are fixed. For example, any resources used for soft-start are basically idle once the supply is at voltage. CIP-based designs don’t have this limitation. Once the power supply has completed its soft-start, the comparator, DAC or CCP can be reassigned on-the-fly to other functions needed during a steady state output. Another example is that, when the controller changes topologies from current-mode to voltage-mode, the same PRG changes from a slope compensation generating block to a sawtooth signal generating block, thus reusing existing CIPs.

ACCESS TO INTERNAL SIGNALS AND INFORMATION
Since ASIC solutions are stand-alone, they rarely provide the necessary connectivity to allow measurement of hard-to-access signals such as peak/average inductor current, duty cycle or the slope compensation signal. CIP solutions not only allow access to these signals, but they also provide peripherals capable of capturing time-dependent signals and make mathematical computation to obtain information that cannot be obtained only with measurements.

This allows the designer to obtain most needed measurements and use them in functions or to calculate equations.

The duty cycle can be accurately measured using the internal 16-bit timer; the gate control of the timer allows a start counting condition with the rising PWM and stop the counting when the PWM falls.

After the count is done, the software function resets the timer to be ready for the next pulse. The timer count is used to compute the duty-cycle value. Figure 10 depicts such an implementation.

Signal measurement timers can be configured to capture not only the duty cycle, but also the period of the same PWM pulse and other signals that the designer may need. In the event that a specific signal is not available, configurable logic cells can be used to generate the necessary composite trigger signal.

Measuring signals that change constantly can be a challenge as ADCs need some time to obtain the correct value. Using two of the internal op amps and the CLC to generate the acquisition pulse and measured timing events, it is easy to obtain a sample and hold measurement system that allows the designer to read the value of a signal at a given moment. An example of this implementation is depicted in Figure 11. Here, the sample and hold configuration is implemented to capture and compute the average inductor current.
Besides the control offered over the SMPS loop, the PIC MCU offers the capability to add communications, functions and libraries to the application. As an example, the PIC MCU can be used in a power harvesting and battery charging system without the need of other ASICs. For this type of application, the power conversion and delivery is controlled by CIPs. The maximum power point tracking and battery charging protocols can be implemented as software functions. The user interface can be implemented with the MCU I/O pins, serial communication and interrupt routines.

*Figure 12* depicts such a system where the PIC MCU absorbs all the needed functions that are usually implemented with multiple ICs and simplifies the overall solution.
FIGURE 11: SAMPLE AND HOLD IMPLEMENTATION FOR AVERAGE INPUT CURRENT MEASUREMENT

- **CCP1**
  - RS
  - COG
  - OUT
  - FS

- **FB**
- **ISENSE**
- **COGA**
- **T1G**

Function to calculate duty cycle %

- **OUT**
- **PRG**
- **IN**
- **FE**

**PIC16F1769**

**OPA**

Function to calculate input current

**ADC**

**DC = 48%**
- **COG1A_OUT**
- **CLC_OUT**

**DC = 46%**

**DC = 44%**

Sample & Hold Signal to ADC

**PRG1_OUT**

**ISENSE**

½ Duty Cycle Value

- **CCP1**
- **ALT**
- **T1**
- **PRG**
- **OUT**
- **COMP**
- **IN**
- **FE**

½ Duty Cycle Value

**CLC**

- **OUT**
- **COMP**
- **IN**
- **FE**

- **FB**
CONCLUSIONS

This application note discusses how the need for configuration capabilities is shifting the way that SMPS controllers are built and how solutions that include such capabilities gain more and more interest. The comparison of ASIC controller solutions that try to offer limited control to designers exposes the problems created by the lack of configuration to the SMPS designs. A list of configuration capabilities that improve analog SMPS control and paves the way for advanced and efficient designs is described in detail. CIP-based designs are part of an 8-bit microcontroller, allowing adjustment of almost any parameter, including topology, while the supply is in operation. This capability opens the possibility for on-the-fly performance evaluation and optimization.

CIPs offer a variety of improvements over a simple ASIC controller-based system, while retaining the familiar analog design methods. Given this greater capability, even designs that may not require communications can still benefit from the inclusion of smart features in their design. This offers a great opportunity to fix many of the limitations of old analog control chips, while also incorporating the flexibility of digital functions for complex designs. For many applications, this provides the best of both worlds and facilitates the implementation of smart systems.
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