INTRODUCTION
In switched-mode power supplies (SMPS), current-mode control has many advantages over voltage-mode control, but has one problem — the current loop can oscillate. This is well known and documented as subharmonic oscillation. The fix to subharmonic oscillation is to add a slope compensating ramp to the current feedback, or subtract the ramp from the error voltage. The PIC16F176X/7X microcontroller (MCU) has a Programmable Ramp Generator (PRG) peripheral able to generate the slope compensation ramp. This application note describes methods to add slope compensation taken by other SMPS controllers and the disadvantages of these solutions. It shows how the ramp generator of the microcontroller overcomes these disadvantages.

THEORY OF OPERATION
Subharmonic oscillation appears when the duty cycle is approaching 50% (can happen even at 45%) and the oscillation appears as a long pulse followed by a short pulse. Figure 1 shows the nature of the current loop oscillation, the clock initiates the on-time of the switch, the control waveform (in orange) terminates the on-time and regulates the peak current at duty cycle >50%. The steady-state current waveform (in violet) shows how it works without perturbation, and the perturbed inductor current (in red) shows how the system oscillates. The perturbation will reach the same peak current (A), but at the next clock cycle the perturbation becomes negative (B) and the amplitude has increased. After another switch cycle, the perturbation is positive again (C) but has increased even more. This will cause the PWM signal to have a long pulse (D) followed by a short pulse (E) and the system will oscillate. The solution to the current loop instability is well known — adding a compensating ramp (Slope Compensation).
CURRENT SOLUTIONS

For the comparison were selected legacy controllers that can be used to control both isolated and non-isolated SMPS and are not dedicated for a specific topology or power range. Legacy solutions as the UC3843a or KA3842B and even updated versions as

the UCC3803 controller, obtain the compensating ramp using the clock signal generated by the RT/CT external components, as depicted in Figure 2.

FIGURE 2: SLOPE COMPENSATION IMPLEMENTATION IN CLASSIC SOLUTIONS

This solution is still used today as many engineers continue to design with the classic parts, but the solution has some issues.

1. The external components used to generate the slope compensation are susceptible to noise due to improper layout. That will influence the ISENSE signal, which is desired to be as clean as possible to have good accuracy and control.

2. The RT/CT line from where the slope compensation is generated is also very susceptible to noise and can create clock period variations by early termination; this will influence the ramp offset and slope.

3. The slope compensation ramp is generated from R/C components, making the ramp nonlinear. The slope compensation ramp is then added to ISENSE, this nonlinearity can create duty cycle jitter.

4. The need for external components to generate the slope compensation adds to the solution BOM, extra layout design effort and total cost.

5. The ramp level can be configured only by changing the values of the external resistances, which limits any modifications or updates.

6. Signal separation is also a problem during debugging. If one of the signals (filtered ISENSE or Slope Compensation signal) is having noise problems, they cannot be analyzed separately to see where the problem is, which prolongs design time.

In newer controllers, such as TLE6389, the slope compensation ramp is generated by a fixed internal current source, depicted in Figure 3A B. In other cases, such as LM5021 or LTC3803, the internal current source can be configured by changing an external resistor value, before it is added to the ISENSE waveform, as depicted in Figure 3A C and A.

These solutions alleviate only some of the issues listed in the previous section.
FIGURE 3A: INTERNAL SLOPE COMPENSATION IN LEGACY CONTROLLERS (LTC3803)

FIGURE 3B: INTERNAL SLOPE COMPENSATION IN LEGACY CONTROLLERS (TLE6389)
These solutions fixed the linearity problem, the noise from the clock, and in the case of the fixed version, the need of external components. The problems that still remain are: no configurability (in the case of the fixed one), need of external components, noise due to layout of the external components, configuration only with external component change and hard debugging because the slope compensation ramp is added internally to the ISENSE without the chance to measure the actual ramp.

While the above mentioned issues do not prevent the SMPS application from working, most designers would prefer a solution that properly addresses them.

CIP Solution

The Microchip microcontrollers with SMPS dedicated peripherals (ex: PIC16F176X/7X) have the capability to implement a current-mode control loop. The parts have internal analog and digital peripherals that work independently of the core and can be internally connected; they are named Core Independent Peripherals (CIPs). CIPs such as op amp, comparators, output generators and slope compensators are analog, asynchronous and can be connected to obtain a complete SMPS controller inside a microcontroller.

For more information on these parts and a better understanding of how to use them for an SMPS application, see TB3140, “Programmable Ramp Generator Technical Brief” (DS90003140), at www.microchip.com/design-centers/8-bit/peripherals/intelligent-analog/slope-comp-program-ramp.

The Programmable Ramp Generator (PRG) peripheral is used to generate the needed slope compensation signal. This CIP can be configured in multiple ways with a vast variety of slope values. It can be connected internally to other CIPs and its output can be brought to an output pin to be measured separately. For current-mode controlled SMPS application the PRG can satisfy the function of slope compensation and for a voltage-mode controlled SMPS the function of sawtooth signal.

The PRG uses internal current sources to generate both rising and falling linear ramps and add them to a signal. In most SMPS controllers the ramp is added to the ISENSE signal, but with this feature the slope compensation ramp can be added to ISENSE as a rising ramp or subtracted from the feedback error signal as a falling ramp, which allows for a separation of the slope compensation waveform from the current waveform. This flexibility with the PRG allows the ramp to be added to other signals, and current limits. It allows for multiple condition ramp starts or stops and even saw tooth signal generation for voltage-mode control.

An example of how to use the PRG as a classic ramp on the ISENSE waveform is depicted in Figure 4.

The rising and falling events can be triggered from a multitude of internal CIPs. In this case the COG output is used to obtain a ramp that starts rising when the pulse gets high and falls in sync with the duty cycle value. In this solution the slope compensation ramp is added to the ISENSE waveform so the ramp cannot be measured separately, but can be added to the error feedback waveform, as depicted in Figure 5, and using an internal op amp as a buffer, the designer can measure the slope compensation separately from the ISENSE signal.
FIGURE 4: SLOPE COMPENSATION IMPLEMENTED IN THE \\ISENSE WAVEFORM

FIGURE 5: SLOPE COMPENSATION IMPLEMENTED IN THE ERROR FEEDBACK WAVEFORM
The possibility to change the ramp value is very important in an SMPS application and its effects can be seen in the current mode loop, as depicted in Figure 6. The bode plot of the circuit that does not implement slope compensation is marked with red color, this behavior depicts an unstable SMPS control. With added ramp an improvement can be seen: the 0.2V ramp ameliorate the situation but the system is still unstable; with 0.9V ramp the system is at the limits of stability and any changes can still cause instability; with 2V ramp the system is stable. Usually, SMPS controllers need an external component to change the ramp value but with the PRG CIP this is done inside the microcontroller.

The slope change of the compensating ramp that the CIPs bring has a great importance during the design and test phase. It may seem that once the slope is set there is no further need for this feature, but this feature comes in handy when the SMPS has a wide output power capability, as the designer can implement a function to adjust the ramp with the output power. This will eliminate the problem of setting too big of a fixed ramp that compensates well on high powers but is too big for low-power delivery. Another use of this feature is in a more complex smart SMPS design that can switch between multiple current-mode control loops or even switch between a current-mode control

**FIGURE 6: CURRENT-MODE LOOP WITH VARYING VALUES OF COMPENSATION RAMP SLOPE**

![Bode plot showing the effect of varying ramp values on gain and phase](image-url)
The linearity of the obtained slope compensation with CIPs compared with external components is also significant and can be seen in Figure 7.

**FIGURE 7: LINEARITY COMPARISON OF SLOPE COMPENSATION IN DIFFERENT SOLUTIONS**
These results show that the slope compensation implemented using the PRG CIP solves all of the issues encountered in other solutions, and provides the designer more flexibility with internal connections to implement smart control loop management.

The use of this peripheral eliminates extra external components, which are usually used in other solutions, and allows for both the classic use of the slope compensation and modifications that can improve specific solutions.

**Example 1:**
An example of a modification that was needed to an SMPS solution is a late start of the ramp.

In this SMPS design, a smaller slope compensation ramp was needed, but the minimum available ramp was too big. A later start of the ramp allowed the minimum to be scaled down to the needed value as depicted in Figure 8, where the slope compensation ramp was added to the error feedback signal as a falling ramp. Since the late start is less than 40% of the switching period, subharmonic oscillations do not happen during the period the ramp is not implemented.

CCP1 sets the Slope Delay (SD), so the user has the liberty to choose at what percentage of the switching period to start using the ramp. In this case, the SD is 30% of the duty cycle. The ramp will be reset as soon as the COG turns off the MOSFET; this eliminates any false triggering due to delays.

**FIGURE 8: PRG CONFIGURED TO IMPLEMENT A LATE SLOPE COMPENSATION START**

Note: SD = Slope Delay
Measured results of this configuration are depicted in figures 9 and 10.

Figure 9 shows the slope compensation waveform on top of the error feedback waveform and current sensed waveform; Results of this ramp provide a very clean entry into current-mode regulation. Figure 10 shows the clean entry into regulation even at 80% duty cycle on a flyback converter.

FIGURE 9: RESULTS OF PRG CONFIGURED FOR LATE SLOPE COMPENSATION START

Note: \( \text{DMAX} = 0.48, \) SC starts at 30\%, resets on the turn-off.

FIGURE 10: RESULTS OF PRG CONFIGURED FOR LATE SLOPE COMPENSATION START

Note: \( \text{DMAX} = 0.8, \) slope compensation start at 30\%, resets on the turn-off.
Example 2:
Another good example of solution improvement with CIPs is an early start of the slope compensation.
In this case, the PRG is also used to generate the slope compensation as a falling ramp added to the feedback error signal, but other internal CIPs are connected to the PRG to generate a custom ramp that provides higher accuracy to the duty cycle control.

**Figure 11** depicts the internal CIP connections that are used to obtain the early starting ramp. This solution allows for better accuracy at the duty cycle limits where other solutions struggle. This is just one example of many implementations that can achieve this result.
When using this solution, a good filter is needed on the ISENSE waveform in order to obtain good, small duty cycle control. Blanking can also be used, but then the minimum duty cycle rises.

Figure 12 depicts the measured results of this solution and shows the duty cycle control is very clean and stable, even when transitioning from open-loop to closed-loop or from closed-loop to pulse skipping where most SMPS controllers encounter high jitter.

**FIGURE 12: RESULTS OF PRG CONFIGURED FOR EARLY SLOPE COMPENSATION START**

![Graph showing results of PRG configured for early slope compensation start]

**Note:** Clean regulation at $D_{\text{MAX}} = 50\%$ and clean regulation at small duty cycles using the early ramp start solution.

Figure 13 depicts the low duty cycle resolution when zooming-in the measurement. In this case, the ISENSE waveform has a good filter and blanking is not used in order to avoid limiting the minimum duty cycle. The solution shows good control at low duty cycles as low as 0.5\% ($\text{SWF} = 125 \text{ kHz}$) and good stability of the system.
CONCLUSIONS

Slope compensation is very important when current-mode control is chosen for a SMPS design, in order to combat the subharmonic oscillation issue that appears when the duty cycle is approaching 50%. But it is good practice to use slope compensation even if the controller has a maximum duty cycle limit at 50%, because subharmonic oscillation can be seen even at the 45% value of the duty cycle.

The solution that legacy controllers have to add slope compensation might work fine in some limited situations but are known to have issues that can cause instability.

The approach using the PRG core independent peripheral eliminates all the mentioned issues, such as: layout noise susceptibility, linearity, need of external components, configuration, clock noise and signal separation; besides adding flexibility and more functions.

Using this solution allows the designer to obtain smarter control loop management, faster design time, easy debugging and measurement, easy layout design, and the ability to add internal control with CIPs and functions. All these build a more stable and smarter SMPS.
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