INTRODUCTION

This technical brief provides examples of functions that utilize the Programmable Ramp Generator (PRG) peripheral as the core of their implementation. This document shows how the PRG is configured to work with other peripherals in order to achieve the expected outcome for each function (see Table A-1). Other peripherals used in the samples include the CMP, FVR, DAC, PWM, TMR, OPA, CLC and COG. For a more detailed discussion on the PRG and its operations, refer to TB3140, “Programmable Ramp Generator Technical Brief” (DS90003140).

PROGRAMMABLE RAMP GENERATOR

The Programmable Ramp Generator provides rising and/or falling voltage ramp signals with no processor overhead. Multiple timing sources can trigger the rise and fall of the ramp signals. The slope rate of the signals is configured from a selection of current settings. A block diagram of the peripheral is provided in Figure 1. Figure 2 shows a sample configuration of the PRG using the MPLAB® Code Configurator (MCC).

FIGURE 1: SIMPLIFIED PRG MODULE BLOCK DIAGRAM

- RTSS<3:0>
- Set_rising Timing Sources
- PRGxR
- PPS
- PRGxRPPS
- Set_falling Timing Sources
- PRGxF
- PPS
- PRGxFPPS

NOTE: SW1 discharged the internal capacitor
SW2 is closed and SW3 is open during rising ramp generator mode
SW3 is closed and SW2 is open during slope compensation mode
SW2 and SW3 alternate switching during alternating rising/falling ramp generator mode
FIGURE 2: MCC – PRG MODULE HARDWARE SETTINGS

The MCC is a user-friendly plug-in tool for MPLAB® X IDE, which generates drivers for controlling and driving peripherals of PIC® microcontrollers. For more information on MCC, refer to the "MPLAB® Code Configurator User’s Guide" (DS40001725) (http://www.microchip.com/mplab/mplab-code-configurator).

Below are the step-by-step procedures for configuring the PRG peripheral. These steps can also be used as a guide for configuring other peripherals needed for the sample functions provided in the next section:

1. Launch MCC by clicking the MCC icon or going to “Tools > Embedded > MPLAB Code Configurator”.
2. In Project Resources, click on the System module and set the desired system clock source, frequency, and Configuration bits.
3. Select PRG::PRG1 under the list of peripherals in the Device Resources area. When selected, the module will appear under Project Resources.
4. In Hardware Settings, select the Ramp Generator mode desired:
   - Alternating Ramp Generator
   - Rising Ramp Generator
   - Slope Compensation (Falling Ramp)
5. Set the voltage input source.
6. Select a slope rate from a range from 0.2-2.5 V/µs. This range applies for a PIC16F176X/7X device (refer to the specific data sheet).
7. Configure the set rising (RS) and falling (FS) timing input sources to be used, as well as their input sensitivity and event polarity. These timing sources indicate when the ramp signal starts to rise or fall. If the function requires specific peripherals as input sources, individually select and configure these peripherals in the same manner as Step 3.
8. Click the Generate button on the top left corner, beside Project Resources, for the MCC to generate individual source and header files for each module. The MCC also generates a main.c source file for the user’s convenience wherein the initialization codes are called and an empty while(1) loop is provided for custom code entry.

These next two steps are needed to ensure the proper operation of the PRG module:

9. Check the status of the PRG module if it is ready to be used by polling the PRG1_IsReady() function.
10. Once Step 9 returns “true”, call the PRG1_StartRampGeneration() function to begin the ramp generation.
SAMPLE FUNCTIONS OF THE PRG

This section contains different functions implemented with the PRG. Each function will be provided with an overview, the significance of using PRG, and setting up the peripherals using the MPLAB® Code Configurator (MCC).

Triangular Wave Generator

A Triangular Wave Generator produces a periodic, non-sinusoidal waveform with a triangular shape of equal rise and fall times. To produce a triangular wave, the PRG must be configured in Alternating Rising/Falling mode.

FIGURE 3: TWG CONFIGURATION

In Figure 3, the PRG determines the output oscillation frequency using two voltage references which triggers the rise and fall of the ramp. These references also determine the minimum and maximum voltage peaks of the triangular wave signal. When the PRG output is below the voltage level set by the Digital-to-Analog Converter (DAC), the RS input of the PRG is triggered and the internal capacitor is charged by the current source. When the PRG output exceeds the Fixed Voltage Reference (FVR), the FS input is triggered and the internal capacitor is charged by the current sink.

Since the PRG does not have a designated output pin, the output of the PRG is buffered through a unity gain configured Operational Amplifier (Op Amp). The configurations for the PRG and other peripherals using MCC are shown in Figure 6. The output frequency can be calculated using Equation 1. Its accuracy however may be affected by different factors such as the parasitic resistance of the capacitor, noise, production variance and temperature.

EQUATION 1: OUTPUT FREQUENCY

\[ f = \frac{1}{2 \left( \frac{V_{FVR} - V_{DAC}}{SR} \right)} \text{Hz} \]
Low-Frequency Operation

The oscillation frequency of the PRG is dependent on the selected current sink/source, the internal capacitance, and the set rising and falling triggers. By placing additional capacitance on the output of the PRG, lower frequency ranges can be achieved.
FIGURE 7: LFO CONFIGURATION

Figure 7 shows Low Frequency Operation based on the TWG configuration, but with added CLC (Configurable Logic Cell) and external capacitor C1. The voltage trip points set by the DAC and the FVR trigger the rising and falling events, respectively. C1 is added at the output of the op amp and effectively in parallel with the PRG’s internal capacitor (see Figure 8). The additional capacitance drags out the time between trigger events, producing a lower frequency for FOUT in Figure 9.

FIGURE 8: SIMPLIFIED PRG BLOCK DIAGRAM – INTERNAL AND EXTERNAL CAPACITORS

Connecting the CLC at the output of the comparators enables the wave generator to produce square waves/pulses. The CLC is configured as an SR Latch (see Figure 10) and the low frequency FOUT is taken from its output. Similar to the PRG, the voltage references trigger the Set and Reset inputs. FOUT is set when the voltage at C1 (OPAOUT) falls below the DAC voltage level. Once OPAOUT rises above the FVR, FOUT is cleared.

FIGURE 9: TIMING DIAGRAMS FOR REGULAR AND LOW FREQUENCY OPERATION

Refer to Figure 6 for similar MCC settings and Figure 10 for the CLC configuration. Reconfigure CMP1’s negative input source with an analog C1INx-pin, CMP2’s positive input with C2INx+, and connect both inputs to OPAOUT.
Voltage-Controlled Oscillator

The Voltage-Controlled Oscillator is an electronic oscillator wherein an input control voltage determines its frequency of oscillation. The instantaneous frequency of the VCO is usually designed to be in linear proportion with the instantaneous voltage. The higher the input voltage, the greater its oscillation frequency. In Figure 11, the PRG’s operation for the VCO implementation is similar with the TWG, except the output frequency is taken from the CLC’s SR Latch and a variable voltage VCNTRL sets the RS input of the PRG.

A higher input for VCNTRL decreases the time needed to retrigger the rising event. Consequently, the switching between current source and sink becomes faster and the oscillation frequency increases. The oscillation frequency can be determined using Equation 2 (similar to Equation 1, with VCNTRL in place of VDAC).

EQUATION 2: OSCILLATION FREQUENCY

$$f = \frac{1}{2 \left( \frac{V_{FVR} - V_{CNTRL}}{SR} \right)} \text{Hz}$$

The relationship between the control voltage and output frequency is presented in Figure 12 with three PRG Slope Rate values. The SR value can be varied for a desired range of frequencies. Lower SR values can produce frequencies ranging from a few Hz to ~500 kHz. Larger SR values, however, can reach up to a MHz range.
Figure 13 shows the behavior of the VCO with two control voltage values and a constant slope rate. A decrease in VCNTRL reduces the VCO frequency out of the CLC.

**FIGURE 13: VCO TIMING DIAGRAM**

For the MCC setup, remove the OPA and DAC modules from Figure 6. Reconfigure CMP1’s positive input source with an analog pin CINx+ connected to VCNTRL. Add a CLC module similar to Figure 10 and have both comparators trigger the R-S Latch to produce a square wave output signal for the VCO.

**Voltage-Controlled Duty Cycle Oscillator**

A standard VCO circuit directly modifies the oscillator frequency. For a Voltage-Controlled Duty Cycle Oscillator, its control voltage modifies the duty cycle of the output pulses.

**FIGURE 14: VCDCO CONFIGURATION**

A similar set-up to the VCO is implemented for the VCDCO, as shown in Figure 14, with the exception that a time base triggers the start of the output pulse. The PWM and TMR modules determine the period/frequency of the oscillator while the PRG (through VCNTRL) determines its Duty Cycle (DC). The rising edge of the PWM triggers the PRG RS input and sets the CLC. When the PRG output exceeds VCNTRL, the FS input is triggered, the PRG capacitor is shorted, and the CLC is reset. The PRG and CLC output will remain low until the next TMR overflow and PWM positive edge. Increasing VCNTRL prolongs the rise of the ramp and the output’s positive pulse width.

The duty cycle is computed as a ratio of VCNTRL to VMAX (see Equation 3-a). To maximize the range of duty cycles, the timer period should be equal to the rise time of the ramp when it reaches VMAX with the given slope rate (see Equation 3-b). Figure 15 shows the linear relationship of the VCO’s Duty Cycle to the input voltage VCNTRL, given that VDD = 5V.

**EQUATION 3: DUTY CYCLE CALCULATION**

\[ DC = \frac{V_{CNTRL}}{V_{MAX}} \]
\[ P = \frac{V_{MAX}}{SR} \]

**FIGURE 15: VCDCO OUTPUT DUTY CYCLE VS. CONTROL VOLTAGE**

**FIGURE 16: VCDCO TIMING DIAGRAMS AT 50% AND 75% DUTY CYCLE**
Figure 16 shows the change of the FOUT duty cycle when two different values of VCNTRL are used. The RS trigger sequence is uniform in both conditions due to the constant period of the timer and PWM. However, an additional delay before the FS trigger is evident in the right half of the diagram due to the constant slope rate and higher VCNTRL.

**FIGURE 17: CONFIGURATION OF PERIPHERALS USING MCC FOR THE VCDCO**

The PRG slope rate and TMR2 period values depend on the required frequency and duty cycle range of the VCDCO. The duty cycle of the PWM is set low enough to trigger the RS input of the PRG. FOUT is still taken from a CLC SR Latch. The PWM and CMP outputs also provide the Set and Reset inputs for the CLC.

**Asynchronous One-Shot**

An Asynchronous One-Shot produces a single output pulse when it is triggered externally. Commonly known as Monostable Multivibrators, the AOS has one stable state. If its stable state is low, an external trigger drives the output high for a specific period. At the end of one period, the AOS returns to its stable state and will wait for the next trigger event.
The Reset state of the CLC is the stable state of the AOS. An external trigger sets the RS input of the PRG and sets the output of the AOS out of the CLC. When the PRG reaches the FVR, the FS input source is triggered, the internal capacitor in the PRG is shorted, and the CLC output is reset. The duration of the Pulse-Width (PW) is dependent on the FVR voltage and PRG slope rate (see Equation 4).

**Equation 4:** Duration of Pulse Width (PW)

\[ PW = \frac{V_{FVR}}{SR} \mu s \]

The settings for CMP1 are similar to the VCDCO, with VCCTRL replaced by the FVR. In Figure 20, an external voltage trigger replaced the PWM/TMR modules to remove the periodic trigger sequence of the PRG RS input and CLC Set sources. The output pulses are taken from the CLC output.

**Voltage-Controlled One-Shot**

This next example is an upgrade of the previous one-shot. One input acts as a trigger, while an additional input determines the one-shot period. One application of the one-shot controls the on-time of a Critical Conduction Mode (CrCM) PFC controller. Figure 21 shows a configuration of the one-shot for the PFC controller but it can also be used in other applications.
The input voltage $V_{\text{CNTRL}}$ determines the one-shot period or “on-time” of the output. A higher value on $V_{\text{CNTRL}}$ produces a longer on-time. When the rising ramp signal of the PRG reaches $V_{\text{CNTRL}}$, the PRG capacitor is shorted and Complementary Output Generator (COG) duty cycle is completed. The output remains low until a signal on $I_{\text{SENSE}}$ retriggers the PRG rising ramp and the beginning of the COG period. In a critical conduction controller, the COG controls the switching of the power MOSFET. The feedback signal from the error amplifier is fed to $V_{\text{CNTRL}}$. A constant feedback signal will result to a fixed on-time. During on and off states, the inductor current ramps up to the input reference voltage, and falls back to zero, respectively. Figure 22 shows the typical behavior of the inductor current for a CrCM controller.

To configure the peripherals with MCC, refer to Figure 17 and replace the PWM/TMR modules with a second CMP. On the list of positive and negative input sources, select a CINx+ pin and the FVR, respectively. In place of the CLC, select a COG module and set the comparators as the rising (RS) and falling (FS) event sources. For a power converter application, the COG peripheral is more suitable as an output driver.
## APPENDIX A: SUMMARY OF PERIPHERALS USED FOR EACH FUNCTION

### TABLE A-1: CHECKLIST OF PERIPHERALS

<table>
<thead>
<tr>
<th>Functions</th>
<th>PRG</th>
<th>CMP</th>
<th>FVR</th>
<th>DAC</th>
<th>PWM</th>
<th>TMR</th>
<th>OPA</th>
<th>CLC</th>
<th>COG</th>
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ISBN: 978-1-5224-0833-8
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