INTRODUCTION

This package application note provides the guidelines for the handling and assembly of Microchip TLA packages during the Printed Circuit Board (PCB) assembly. In addition, it provides general information for the PCB land pattern design and component rework guidelines.

SCOPE

The application note contains generic information for various Microchip TLA packages assembled internally or at external subcontractors. Specific information about each device is not provided. To develop a specific solution, actual experience and development efforts are required to optimize the assembly process and application design per individual device requirements, industry standards (such as IPC and JEDEC), and prevalent practices in the assembly environment. For more details about the specific devices contained in this document, visit www.microchip.com or contact your local Microchip sales office.

PACKAGE DESCRIPTION AND CONSTRUCTION

TLA packages are a plastic encapsulated leadframe based package with low profile (≤1.0 mm). This package type uses perimeter lands/pins on the bottom of the package to provide electrical contacts to the PCB. The perimeter pins are arranged in either single or dual-row configuration, refer to Figure 1 which shows the quarter package. The package can be with or without an exposed center pad (ePAD). In case of ePAD, it is used as a thermal enhancement at the bottom of the package. The ePAD needs to be soldered directly to the PCB for an efficient thermal path from the die to the board (see Figure 1). The center pad also enables stable ground by use of down-bonds and electrical connections through a conductive die attach material. The TLA packages are offered in various pincounts and body sizes, and have the following features:

- Small overall dimensions as compared to leaded packages, which helps maximize board space
- Highest pincount per body size in a leadframe-based package family, due to utilization of the corners
- Thermally enhanced plastic package (when ePAD version is used)
- Very high design flexibility due to the etching process of the leadframe
- Easy accommodation of multi die assemblies, where separated pads are required
- Standard SMT performance characteristics

FIGURE 1: TLA LEADS/PINS CONFIGURATION AND HEAT TRANSFER
A typical multi row TLA package with exposed pad construction (cross-section) is shown in Figure 2. These packages are sawn singulated high-density leadframe strip-assembled with “die up” configuration. A standard wirebond technology with Cu or Au wire is used for the electrical connection between the die and package. The TLA packages are processed in integrated assembly and test lines from die attach through tape and reel.

**FIGURE 2: TLA PACKAGE CONSTRUCTION**

![TLA Package Construction Diagram]

<table>
<thead>
<tr>
<th>#</th>
<th>Description</th>
<th>#</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Copper leadframe – perimeter outer pins</td>
<td>6</td>
<td>Ag or NiPdAu plating – stick bonds</td>
</tr>
<tr>
<td>2</td>
<td>Lead finish material (Ag, Sn, ENIG or NiPdAu)</td>
<td>7</td>
<td>Molding compound</td>
</tr>
<tr>
<td>3</td>
<td>Copper leadframe – center ePad</td>
<td>8</td>
<td>Bonding wire (Au or Cu) to pins</td>
</tr>
<tr>
<td>4</td>
<td>ePad finish material – same as the leads</td>
<td>9</td>
<td>Silicon die</td>
</tr>
<tr>
<td>5</td>
<td>Conductive die attach epoxy</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Various TLA constructions are possible depending on the device and application requirements, as shown in Figure 3.

**FIGURE 3: TLA CONSTRUCTION VARIATIONS**

![TLA Construction Variations Diagram]
TYPICAL TLA CONFIGURATIONS

Microchip offers a range of TLA packages in various sizes with standard pitches of 0.5, 0.6 and 0.8 mm. The actual package outlines are provided on the Microchip website as a separate document. To obtain the complete set of each QFN package dimensions and tolerances, refer to the “Packaging Specification” (DS00000049).

PCB LAND PATTERN GUIDELINES

The TLA is a surface mountable package with bottom termination of its external connections (pins). The land pattern design for all TLA type packages is based on IPC-7093 and IPC-7351. A Non-Solder-Mask Defined (NSMD) pad design is suggested for all perimeter pins, as shown in Figure 4. The solderable area of the center pad, as defined by the solder mask (SMD) or NSMD, should match the size of the ePAD of the component. An array of solid vias should be incorporated in the PCB center pad design in order to achieve maximum thermal and electrical performance of the device.

FIGURE 4: NSMD AND SMD BOARD PAD DEFINITION

The PCB land pattern should match the TLA terminal (pins) and exposed center pad dimensions, as indicated in the Microchip package outline drawings. Nominal values should be used on the PCB land pattern for the dimensions shown in Figure 5. An example of a typical TLA PCB land pattern guideline and dimension is shown in Figure 5.
STENCIL DESIGN GUIDELINES

The optimum reliable solder joints on the perimeter pins should have 75-100 um standoff height. The inner row pin solder joint should be carefully designed in order to not to short pins, and to avoid having insufficient solder volume, and to have a reliable joint.

Microchip recommends that the user follows the guidelines of industry specifications IPC-7525 and IPC-7093 in designing the optimum stencil for a given board.

The thickness of the stencil determines the amount of solder paste deposited onto the printed circuit board land pattern. A 0.127 mm (5 mil) thick stainless steel stencil is recommended. Since the TLA is most likely not the only package on the actual production PCB, the recommended stencil thickness for this package may be thinner than desired. In such a case, a step-down stencil is recommended, where most of the stencil for the PCB has a typical thickness, but the area for the TLA is 5 mils.

REFLOW SOLDERING AND PROFILING

As with all SMT components, it is important that furnace profiles be monitored on all new board designs. Additionally, if there are multiple package types on the board, the thermal profile should be measured at multiple locations. Component temperature may vary because of surrounding components, location of the device on the board, and package densities. To maximize the self-alignment effect of the TLA component, it is recommended that the maximum reflow temperature specified for the solder paste not be exceeded.

Microchip recommends that the user follows the guidelines of industry specifications IPC-7093 and J-STD-020 in developing the optimum reflow profile for the Pb-free TLA components with a given board.
HANDLING

The following information details handling procedures that should be used with product packed in desiccant bags and intended for surface mount applications. Following these handling guidelines will ensure that components maintain their as-shipped, dry state, alleviating package cracking and other moisture-related, stress-induced concerns that may be associated with the surface mount process.

1. Incoming Inspection

Upon receipt, shipments should be inspected for bag integrity. There should not be holes, gouges, tears or punctures of any kind that expose either the contents or the inner layer of the bag.

2. Storage Conditions/Shelf Life

The sealed Moisture Barrier Bag (MBB) and enclosed desiccant have been designed to provide a minimum of 12 months of storage from the seal date in an environment as specified in JEDEC specification J-STD-033.

If the worst-case storage conditions (time, temperature, or relative humidity) are exceeded and there is a need to verify whether inventory has been affected, then a bag can be opened and the Humidity Indicator Card (HIC) can be checked for expiration. If the HIC has not expired (there is no failed dot discoloration), then new desiccant can be added and the bag resealed. If the HIC has expired, then the devices should be either rebaked and used in the SMT, or rebaked and resealed in a new MBB with fresh desiccant as soon as possible. In either case, the remaining allowable ambient exposure time must be reduced by the time the units are out of the MBB or dry storage environment.

3. Opening an MBB

To open a MBB when the containers are ready to be used or inspected, simply cut across the top of the bag, being careful not to damage the enclosed materials. Once the bag has been opened, follow the guidelines for ambient exposure time in the following section to ensure that devices are maintained below the critical moisture level.

4. Manufacturing Conditions/Floor Life

Microchip classifies surface mount components into levels of moisture sensitivity. The labels on the MBB list the moisture sensitivity level and the allowable floor life. Once the MBB has been opened, Microchip recommends that components from the bag be surface mounted and reflowed within the time indicated on the MBB label. This time is based on a manufacturing environment not more extreme than 30°C/60% RH, and a maximum component body temperature during solder reflow of 260°C. If the components cannot be mounted within this timeframe, they should be put into a dry storage environment immediately, or sealed into an MBB with fresh desiccant as soon as possible. In either case, the remaining allowable ambient exposure time must be reduced by the time the units are out of the MBB or dry storage environment.

5. In-Process Storage

Microchip highly recommends having dry storage capability available for units that will not be used within the allowable exposure time. A desiccator with dry nitrogen or air (≤5% RH source) is suggested for such storage.

6. Rebaking

TLA components should be rebaked only if they have been exposed to excessive moisture as indicated by exceeding the recommended ambient exposure time or by expiration of the HIC. Rebaking should be performed (if necessary) prior to the use of the parts in the SMT line, at 125°C for at least 8 hours. Parts should not be rebaked more than twice.

7. Resealing an MBB

If there is a need to reseal an MBB for any reason, Microchip recommends the following guidelines to ensure that the bag seal does not allow moisture into the bag. The seal area must not exhibit any separation when subjected to load and temperature conditions specified in JEDEC J-STD-033 specification. The integrity of the seal is vital to the storage life of the devices.
REWORK

The TLA rework process is similar to BGA/LGA type package rework process. The rework process should follow the major steps below:

- **Part Removal** – The failed part should be removed from the board by applying hot air to the top of the component and bottom heating the PCB. Discard the removed failed part if it is not needed for Failure Analysis (FA) work or reuse.
- **PCB Cleaning** – The PCB land site need to be properly cleaned and dressed for the attachment of the new component. Either a de-soldering system or iron with solder wick method can be used to effectively remove the residual solder without damaging the solder mask material and/or the pads. It should be noted that the applied temperature should not be >245°C; otherwise, the copper pads on the PCB may peel off.
- **Solder Paste Deposition** – A mini stencil with the same thickness and aperture openings as the production stencil should be used to deposit the solder paste. The printed solder paste should be inspected to ensure that a uniform and sufficient volume is deposited before the part placement.
- **Part Placement** – A TLA reworking station with a vacuum nozzle and vision system should be used to pick the new TLA part and accurately align and place it on the corresponding footprint.
- **Rework Reflow** – The replaced TLA component is then soldered to the PCB using a temperature profile similar to the production reflow profile. The TLA reworking station typically has a programmable reflow profile to be selected for a given part.

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